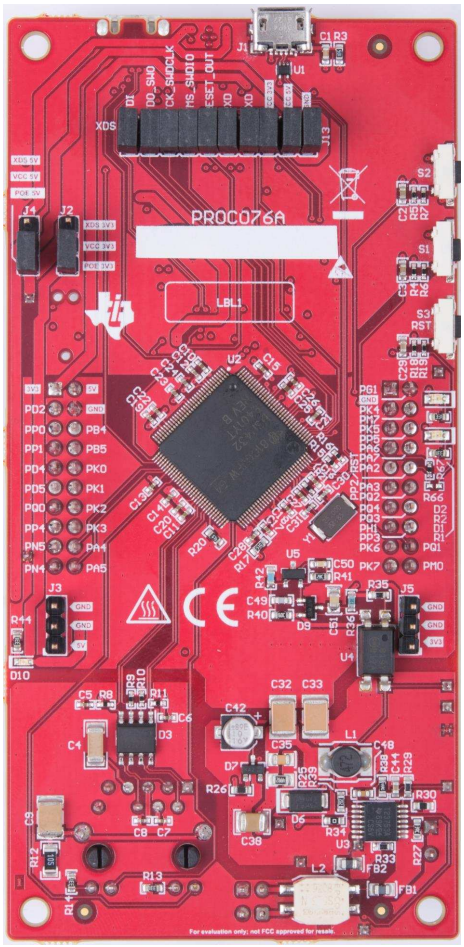
MMWAVEPOEEVM Power Over Ethernet Solution

The MMWAVEPOEEVM integrates TI's Power over Ethernet (PoE) converter solution and the high-performance SimpleLink™ MSP432E4 Ethernet microcontroller (MCU) with Ethernet to enable customers develop applications for mmWave radar applications. The design increases the value of the end application with its ability to derive power over existing network cabling combined with intelligence to gather, process, and exchange data between the cloud and mmWave EVMs.

MMWAVEPOEEVM allows customers to leverage their existing network to not only communicate and control mmWave radar devices securely with the PoE solution but also to deliver power, which reduces the system cost and adds value to their products.

The MMWAVEPOEEVM with the BoosterPack™ plug-in module headers interfaces seamlessly with the mmWave family of products, which includes IWR1443BOOST, IWR1642BOOST and MMWAVEICBOOST.



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1 Key Features

- Small Form Factor Board Measuring 4.55” × 2.15” With MSP432E401Y MCU Featuring Integrated Ethernet PHY and MAC
- Integrated RJ45, Transformer, and Diode Bridge for PoE Power Stage for Cost-Effective BOM
- 7-W Isolated Output From Fly-Back Converter With Provision for Both 5-V and 3.3-V Output Power Rails
- Optional Power Header to Supply External DC Power From UPS in Case of Network Power Failure
- BoosterPack™ plug-in module headers to Prototype End Applications With Wide mmWave radar EVMs and kits.
- Uart and Ethernet data bridge for mmWave applications

2 Kit Contents

- MMWAVEPOEEVM
- Micro USB cable
- Quick start guide

3 Applications

- People Counting
- Home Automation
- Factory Automation
- Robotics
- Gesture control

4 System Overview

4.1 Block Diagram

Figure 1 shows the PoE for connected IoT block diagram.

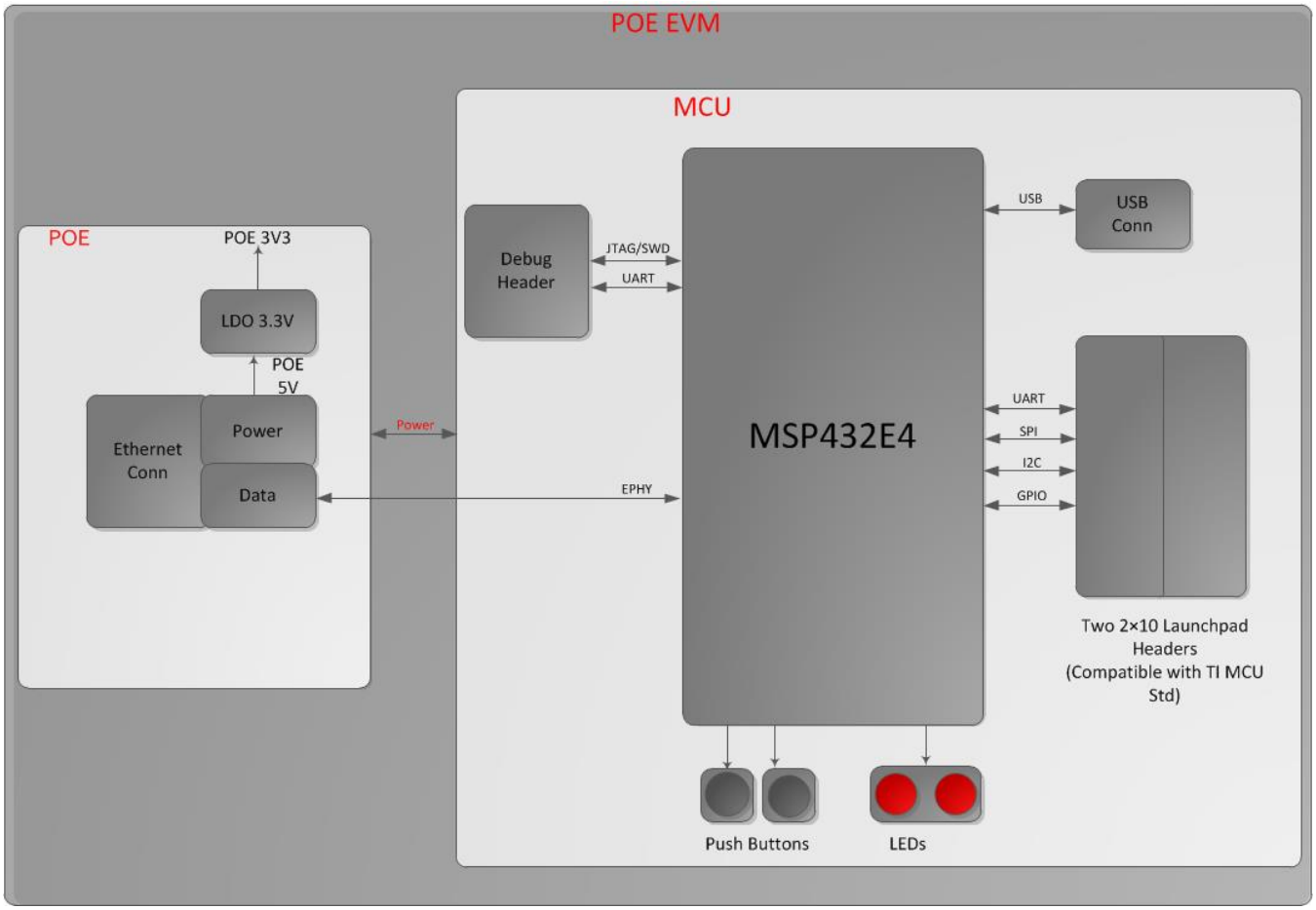

Figure 1. System Block Diagram

4.2 MSP432E401Y

The MSP432E401Y is a 120-MHz, high-performance MCU with 1 MB on-chip flash and 256 KB on-chip SRAM. The MSP432E401Y MCU also features an integrated Ethernet MAC + PHY for connected applications and cryptographic modules of AES, DES, and SHA for encryption, decryption, and authentication. The device has high-bandwidth interfaces such as memory controller and a high-speed, USB2.0 digital interface. With integration of a number of low- to mid-speed serial, up to 4-MSPS, 12-bit analog-to-digital converter (ADC), and motion control peripherals, the device makes a unique design for a variety of intelligent, industrial gateway applications ranging from building automation zone controller and smart grid data concentrators to factory automation and control gateways.

Figure 2 shows the high-level block diagram of the MSP432E401Y MCU.

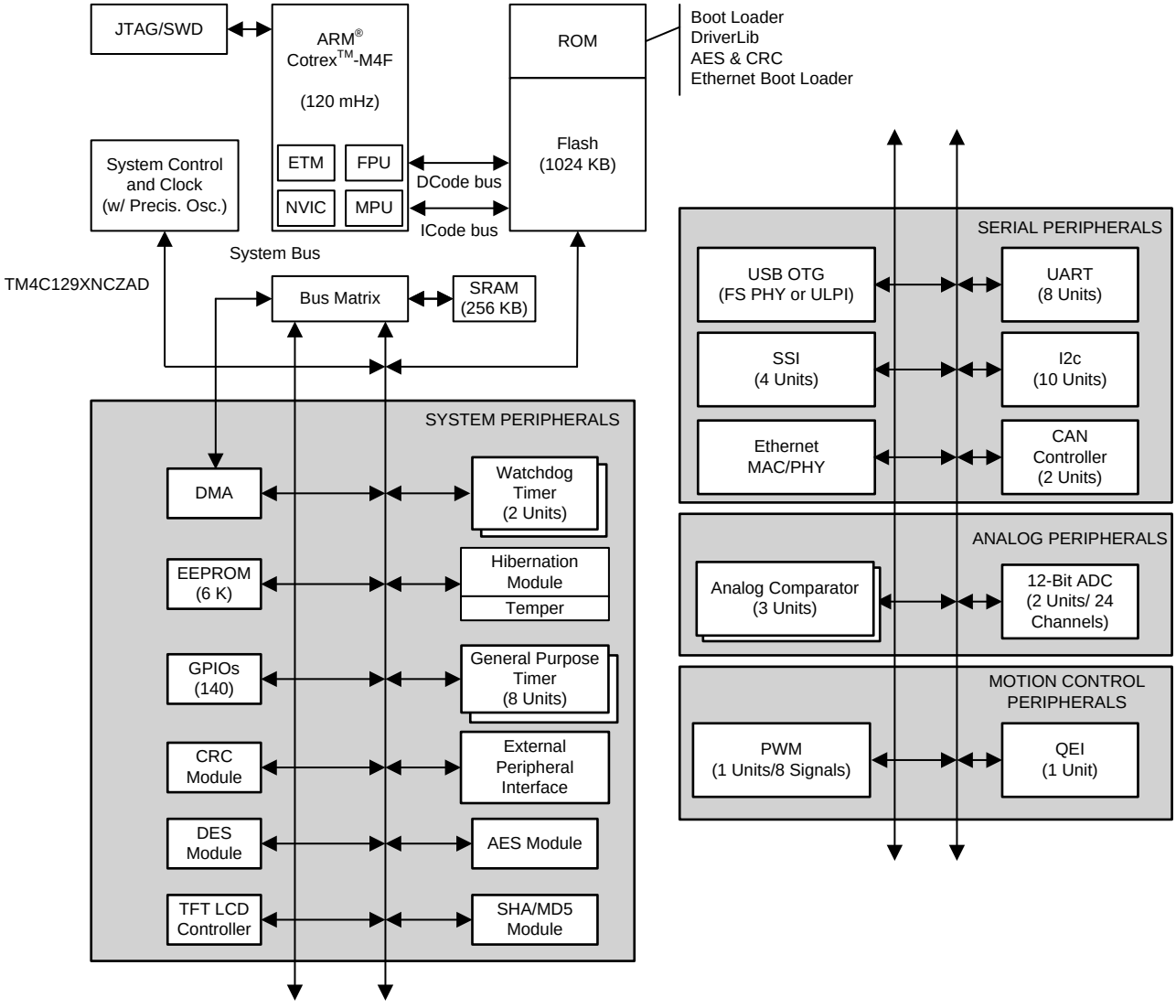

Figure 2. MSP432E401Y MCU High-Level Block Diagram

4.3 TPS23753A

The TPS23753A is a combined PoE powered device (PD) interface and current-mode DC-DC controller optimized specifically for isolated converter designs. The PoE implementation supports the IEEE 802.3at standard as a 13-W, type 1 PD. The requirements for an IEEE 802.3at type 1 device are a superset of IEEE 802.3-2008 (originally IEEE 802.3af).

The TPS23753A supports a number of input-voltage ORing options including highest voltage, external adapter preference, and PoE preference.

The PoE interface features an external detection signature pin that can also be used to disable the internal hotswap MOSFET. This allows the PoE function to be turned off. Classification can be programmed to any of the defined types with a single resistor.

The DC-DC controller features a bootstrap start-up mechanism with an internal, switched current source. This provides the advantages of cycling overload fault protection without the constant power loss of a pullup resistor.

The programmable oscillator may be synchronized to a higher-frequency external timing reference. The TPS23753A features improvements for uninterrupted device operation through an ESD event.

4.4 TPD2E2U06

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and Inter-Integrated Circuit (I2C).

4.5 TLV431A

The TLV431 device is a low-voltage 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between V_{REF} (1.24 V) and 6 V with two external resistors. These devices operate from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt-regulator references.

When used with an optocoupler, the TLV431 device is an ideal voltage reference in isolated feedback circuits for 3-V to 3.3-V switching-mode power supplies. These devices have a typical output impedance of 0.25 Ω. Active output circuitry provides a very sharp turn-on characteristic, making them excellent replacements for low-voltage Zener diodes in many applications, including on-board regulation and adjustable power supplies.

4.6 TPS737

The TPS737xx family of linear low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltage-follower configuration. This topology is relatively insensitive to output capacitor value and ESR, allowing a wide variety of load configurations. Load transient response is excellent, even with a small 1-µF ceramic output capacitor. The NMOS topology also allows very low dropout.

The TPS737xx family uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is less than 20 nA and ideal for portable applications. These devices are protected by thermal shutdown and foldback current limit.

5 Hardware

5.1 Hardware Overview

This design is a plug-and-play system with minimal user intervention required for either supplying or managing any control IOs for power to the device.

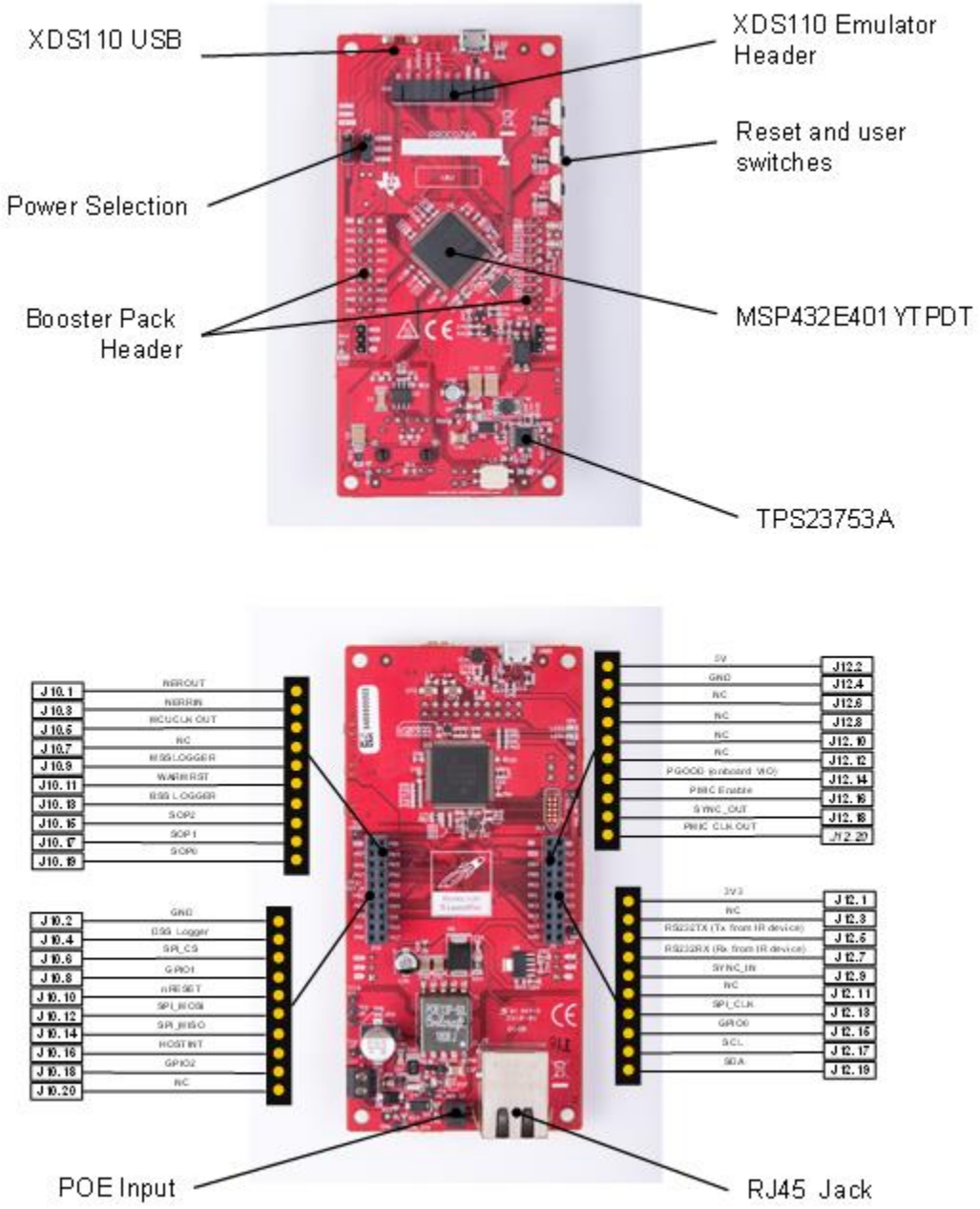

Figure 3. MMWAVEPOEEVM Overview

5.1.1 Test Points, Connectors, Jumpers, Switches, and LEDs

This section provides details about the connectors, test points, and the jumpers that are available on the design for debug, probe, and flexibility of evaluation.

Table 1 lists the test points.

Table 1. Test Points

Designator	Description
TP1	MSP432E401YTPDT 1.2-V core voltage test point
TP2	DC-DC converter bias supply
TP3	Gate driver for the primary-side switching MOSFET
TP4	DC-DC converter output voltage
TP5	Drain terminal of the primary-side switching MOSFET
TP6	Bias voltage regulator
TP7	PoE input, low side
TP8	DC-DC converter return
TP9	DC-DC converter return
TP10	Control loop input to the pulse width modulator (PWM)
TP11	Digital ground

Table 2 lists the connectors and jumpers.

Table 2. Connectors and Jumpers

Designator	Description	Comment
J1	USB connector	MCU USB peripheral port
J2	Vcc 3v3 power source	• Place shunt jumper on XDS 3v3 and Vcc3v3 to power via J14. • Place shunt jumper onPOE 3v3 and Vcc3v3 to power via J8. (1)
J3	5V 3-pin header	-
J4	VCC 5V power source	• Place shunt jumper on XDS 5v and VCC 5V to power via J14. • Place shunt jumper on POE 5V and VCC 5V to power via J8.
J5	3V3 3-pin header	-
J6	PoE input low side from the RJ45 jack	Place shunt jumper for POE (2)
J7	PoE input high side from the RJ45 jack	Place shunt jumper for POE
J8	RJ45 connector	Power over ethernet (POE) data and power port
J9	BoosterPack header	-
J10	BoosterPack header	-
J11	External adapter input connector	Optional for external 12-V DC power supply
J12	XDS110 debugger	-
J13	XDS110 emulator header	• Place shunt jumper on TDI, TDI,TCK,TMS and RESET for JTAG • Place shunt jumper on RXDand TXD for UART • Place shunt jumpers on VCC3v3 and Vcc5V to power booster pack header voltage lines and entire stackup
J14	XDS110 USB connector	-

(1) Ensure J2 and J4 are place to source power from J14 or J8 not both

(2) Ensure shunt jumper is placed on J6 and J7 for POE power

5.1.2 Power-Up

There are five potential sources of power in this design:

- The primary power is through the Ethernet RJ45 (J8). The user must ensure that the switch or hub used is PoE PSE equipment.
- The design can be powered by using the external adapter input connector (11) through a 12-V DC power supply.
- The design can be powered from a 5-V DC power supply by removing the jumper on J4, placing jumper on J2 (POE3v3 and VCC3v3) and applying 5-V input to Pin-2 of J4.

  NOTE: GND from the external power supply must be connected to TP11.

- The design can be powered from a 3.3-V DC power supply by removing the header (J9) and applying 3.3-V input to Pin-1 of J9.

  NOTE: GND from the external power supply must be connected to TP5. In this configuration, the 5 V is not available on the BoosterPack headers.

- Placing shunt jumper J2 and J4 on XDS5V and XDS3V3, respectively, to power through USB port J14

5.1.3 Downloading the Binary

To download an application to the MSP432E401Y MCU connect USB cable to J14 and ensure Universal Asynchronous Receiver/Transmitter (UART) jumpers on J13 are placed. Using unflash program the EXP432E401Y. For more information, see the UniFlash v4 Quick Guide wiki.

5.1.4 Connecting the MMWAVEICBOOST

Mount the MMWAVEICBOOST on the MMWAVPOEEVM as shown in Figure 4 and ensure that MMWAVEPOEEVM is configured to source power through the RJ45 connector (J8).

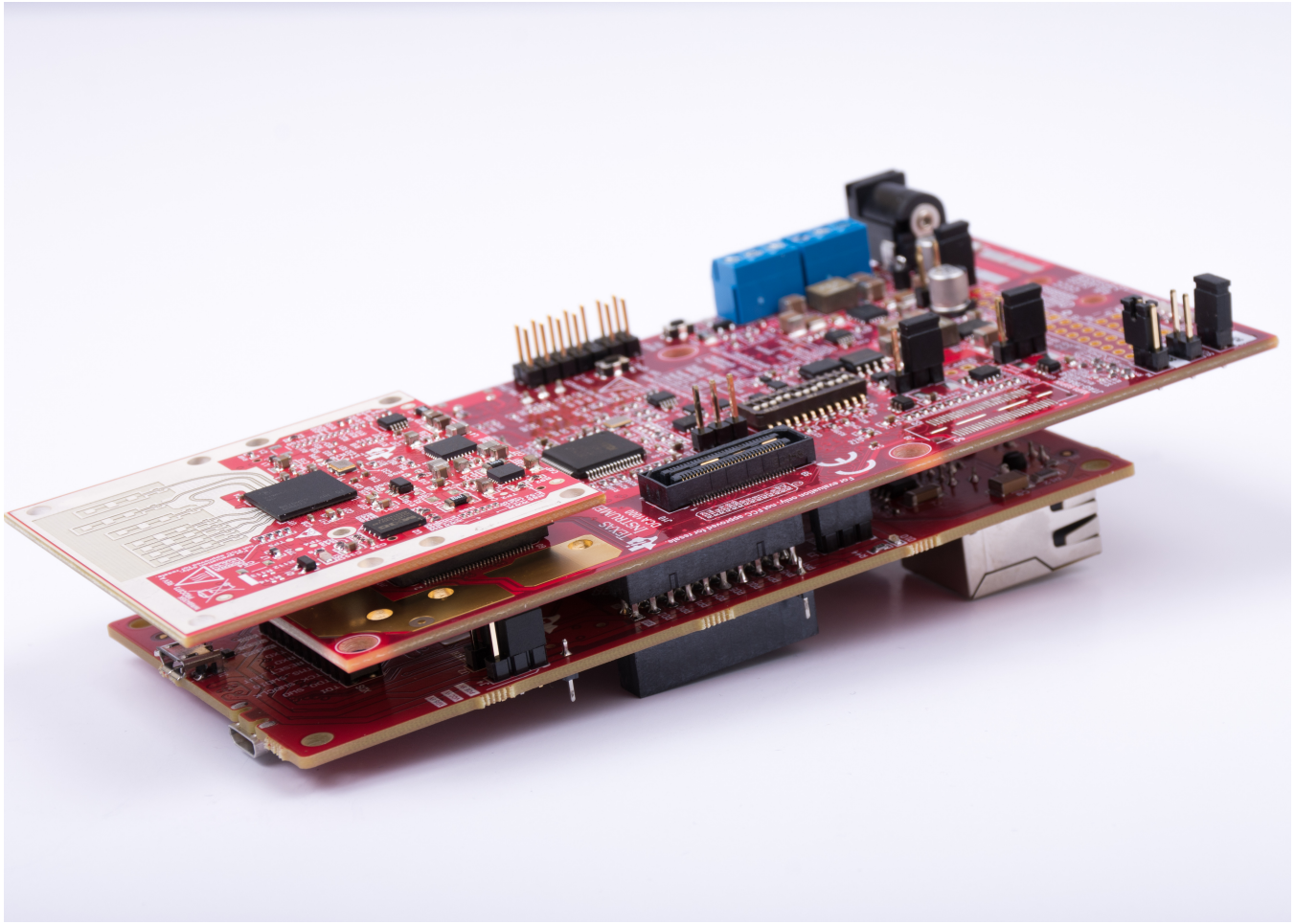

Figure 4. IWR6843ISK, MMWAVEICBOOST and MMWAVPOEEVM Board Stackup

Ensure the mux switches are configured as shown in Table 3.

Table 3. 40-Pin Header mux Switch Position

Description	Switch Position
S1.1	OFF
S1.2	ON
S1.3	OFF
S1.4	ON
S1.5	OFF
S1.6	OFF
S1.7	OFF
S1.8	ON
S1.9	ON
S1.10	OFF
S1.11	OFF
S1.12	ON

Ensure the shunt jumper is placed on the load switch header J28 and shown in Figure 5.

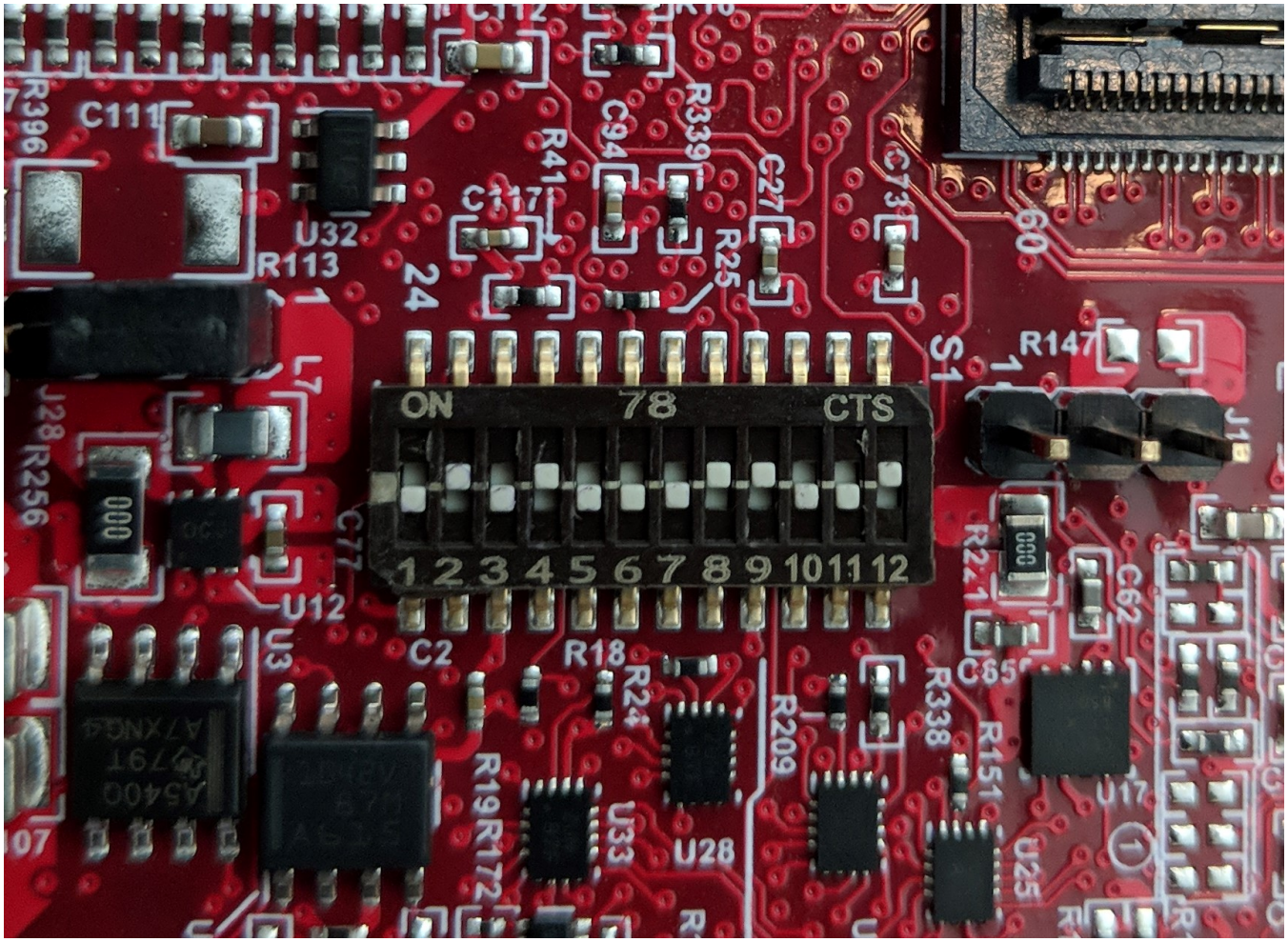

Figure 5. MMWAVEICBOOST Switch S1 Configuration for POE Mode

Connect the power sourcing equipment (PSE) to J8 (RJ45 jack) to power your application.

5.2 Testing and Results

Test results of the power front end (PoE) can be found in the reference design page, TIDM-1018.

6 Design Files and Software Tools

6.1 Software, Development Tools, and Example Codes

To enable quick development of an end application on the R4F core in the IWR1443, TI provides a software development kit (SDK) that includes demo codes, software drivers, an emulation package for debug, and so on. The SDK is available at mmwave-sdk.

6.2 Schematics

To download the schematics, see the design files at SWRC364.

6.3 Bill of Materials

To download the bill of materials (BOM), see the design files at SWRR167.

6.4 PCB Layout Recommendations

An important consideration when doing the layout is the trace width for the Ethernet and USB signals. The Ethernet and USB interfaces have critical differential impedance requirements. Both Ethernet signal pairs must be routed as a 100 Ω ± 10% differential pair on the top layer of the PCB with a ground plane as a reference. The USB signal pair must be routed as a 90 Ω ± 10% differential pair on the top layer of the PCB with a ground plane as a reference.

The optimal solution is if the PCB fab house adjusts the stack up and provides for controlled dielectric. The PCB tools must be used to set the spacing and width of the traces to get close to the target characteristic impedance. The PCB fab house can then adjust the trace space and width to the specific materials and process.

During the PCB layout, if the PCB fab house has a predefined layer stack up for low-cost process, the layer stack up information must be found and used in PCB tools to get the optimum trace width. The design files use a low cost variant with the following PCB stack up for four layer PCB's.

Figure 6 shows the PCB layer stack up for TIDM-1018.

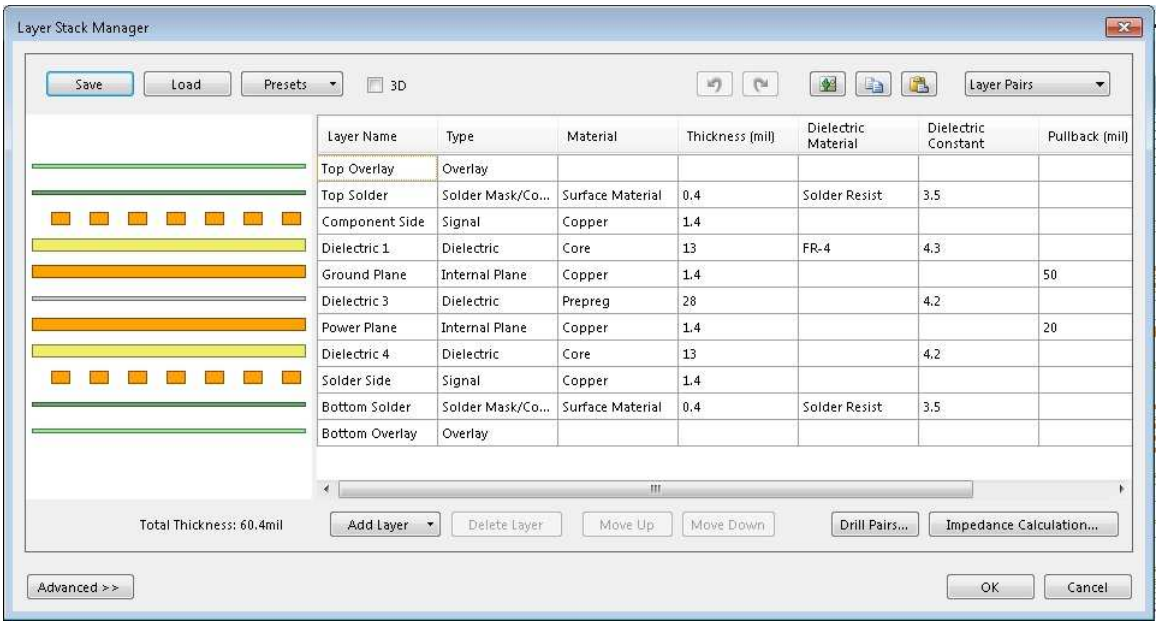

Figure 6. PCB Layer Stack Up for TIDM-1018

When the data shown in Figure 6 is entered into the PCB tool, the trace width and space for Ethernet and USB signals are computed and listed in Table 4. The most important parameter is the Z_{DIFF}, which must be within ±10% tolerance.

Table 4. Differential Signals Trace Information

Trace Width (mil)	Trace Thickness (mil)	Trace Height (mil)	Trace Spacing (mil)	E_R	Z_{DIFF}	Z_O
10	0.4	15.8	5	4.2	109.476	84.766
12.8	0.4	15.8	5	4.2	99.336	76.915

6.5 REACH Compliance

In compliance with the Article 33 provision of the EU REACH regulation, this is to notify you that this EVM includes component(s) containing at least one Substance of Very High Concern (SVHC) above 0.1%. The uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are:

Table 5. Missing Title

Component Manufacturer	Component Part Number	SVHC Substance	SVHC CAS (when available)
Murata	39357-0002	Lead	7439-92-1

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2019) to A Revision	Page
• Update was made in Section 6.1.	10
• Update was made in Section 6.2.	10
• Update was made in Section 6.3.	10

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