Technical Article

Improving Sensor DAQ Performance Using the PRU-ICSS for Grid Protection and Control

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As utility companies shift focus towards improving the quality and efficiency of power systems, they are transitioning from a conventional grid to a smarter grid. This transition entails adding more sensors and communication capabilities to existing primary equipment as well as installing secondary equipment such as protection relays, bay controllers and terminal units for the protection, control and monitoring of primary equipment on the substation switch yard. The secondary equipment are mounted inside the panels placed in the control room of a substation as shown in the below Figure 1.

Figure 1. Control Panel with Protection, Control and Monitoring Equipment

With more sensors connected, data acquisition (DAQ) capabilities are critically important to improving the power system performance. A DAQ system needs to capture multiple analog inputs (current, voltage, temperature), precisely process acquired samples, compute electrical parameters and communicate those processed parameters in real time for analysis at a central location.

AC analog inputs for protection, monitoring and measurement have different input ranges, accuracy and processing requirements. To optimize substation size, improve measurement accuracy, and increase reliability and safety, utilities and large businesses are changing from conventional to non-conventional instrument transformers, which require additional hardware and processing. With more functionality integrated, the number of analog channels required is increasing, algorithms are becoming more complex and so are the processing requirements for computing electrical parameters. Designs are becoming modular and based on the application, designers are adding modules to increase the number of analog input channels to reduce complexity. These added modules are configured for the required functionality within the DAQ system to improve performance and provide expandability.

In an earlier blog post about interfacing multiple analog-to-digital converters (ADCs) to a single processor for grid protection and control, I discussed the interface choices and presented the programmable real-time unit and

industrial communication subsystem (PRU-ICSS) interface as an optimal design. In this post, I will discuss the details, approach and advantages for interfacing multiple ADCs to a single host processor using the PRU-ICSS.

View our PRU-ICSS reference design

Flexible Interface (PRU-ICSS) Reference Design for Simultaneous, Coherent DAQ Using Multiple ADCs.

Using the PRU-ICSS provides flexibility of ADC and processor choice based on the sampling and processing requirements. Figure 2 is a block diagram of a general-purpose core supplemented with real-time coprocessors.

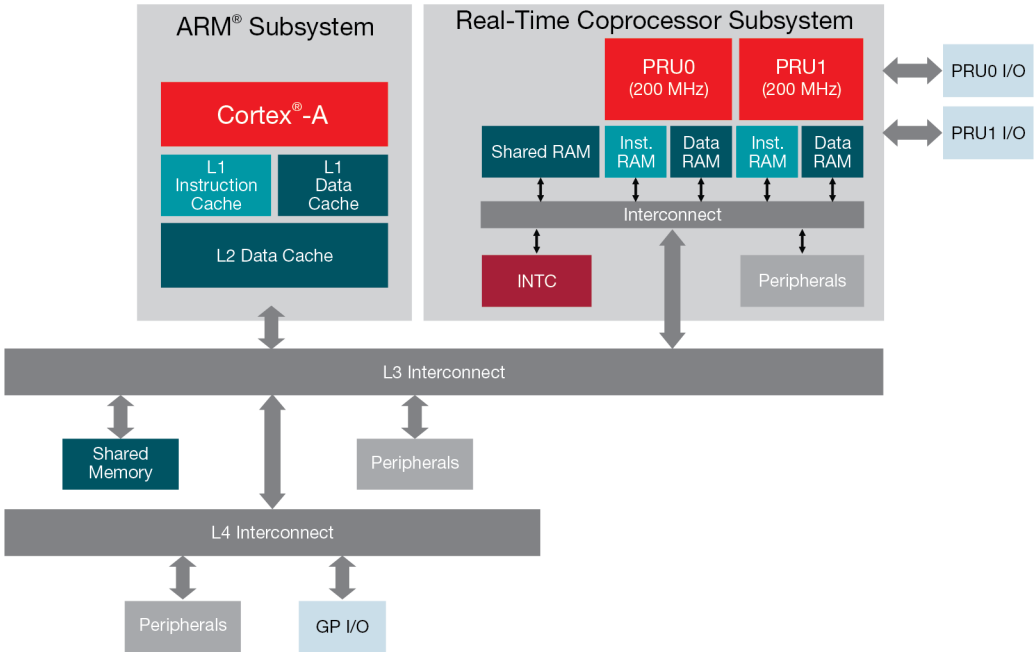

Figure 2. General-purpose Core Supplemented with Real-time Coprocessors (Source: "Ensuring real-time predictability," Page 2)

An ADC with Serial Peripheral Interface (SPI) and host processor with dual-core PRU-ICSS simplify the overall system design and provide a cost-optimized system with improved performance.

The PRU, which is deployed with Arm® cores in Sitara™ AM335x, AM437x and AM5x processors, fulfills the role of a low-latency, deterministic real-time subsystem. Each PRU subsystem comprises two 200MHz real-time cores (or PRUs), each with a 5ns cycle time per instruction. Not equipping the real-time cores with an instruction pipeline ensures single-cycle instruction execution. The PRU's small, deterministic instruction set with multiple bit-manipulation instructions is easy to learn and use. Shared memory, as well as instruction and data memory dedicated to each real-time core, enable flexible program execution among all of the real-time and general-purpose processor Arm cores that might make up the system on chip.

The ADC used is an ADS8688, a 16-bit 8-channel non-simultaneous sampling multiplexed ADC using a single-supply with bipolar input voltages up to ±10.24V with an integrated AFE. It is an optimized solution for cost and performance for low voltage or medium voltage protection, monitoring and control applications, including DTU/FTU. The sampling delay between channels observed when using a multiplexed ADC is compensated in software. ADS8688 has 500ksps or 62.5ksps per channel data throughput that meets protection, monitoring and control sampling requirements, which can vary from 60-512 samples per cycle.

TI's Flexible Interface (PRU-ICSS) Reference Design for Simultaneous, Coherent DAQ Using Multiple ADCs provides the interface between ADS8688 and host processor AM335X, capturing the data and performing coherent sampling. The reference design offers these three key benefits:

- Scalability/flexibility: interfaces with multiple ADS8688 16-bit ADCs (six) and 48 analog input channels with SPI and individually controllable chip select.
- Performance: enables coherent sampling by dynamically adjusting the timing to achieve high AC performance from ADCs.
- Integration: reduced form factor and cost by using a single processor for the DAQ system, industrial Ethernet interface, signal processing and user interface.

The PRU-ICSS implements an enhanced general-purpose input/output (GPIO) module that supports direct input and direct output modes. PRU core register R30 serves as the interface for the general-purpose outputs and register R31 for the inputs. Any value written into register R30 of the PRU core will be output to the PRU's external pins a single cycle later (R30 bit 0 corresponds to pin 0, bit 1 to pin 1, and so on).

Inversely, whenever the PRU core reads register R31, the values on the PRU core's external pins are stored a single cycle later. The value of pin 0 is stored in R31 bit 0, pin 1 in R31 bit 1, and so on. Along with the direct input and output modes, the PRU's determinism makes it a good fit for implementing simultaneous SPI ports for communicating with multiple ADCs.

The GPIO pins from the PRU-ICSS transfer data between all ADCs and the processor. While PRU-1 handles external data communication, PRU-0 performs low-level filtering and zero cross detection. The Arm core running real-time Linux® can handle further processing of data, communication and human machine interface (HMI) control.

To implement DAQ systems using the PRU-ICSS, all ADCs are configured to sample the same channels simultaneously. The reference design highlights the capability of the PRU-ICSS to handle a 1,536KSPS data rate (each sample = 16 bits) by sampling 640 samples per line cycle. For a 50Hz cycle, this corresponds to 32KSPS per channel across six ADCs simultaneously (640 samples/cycle × 50Hz × 6 ADCs × 8 multiplexed channels = 1,536KSPS). The second PRU post-processes the data to achieve coherent sampling.

The PRU-ICSS provides a simplified simultaneous interface to six TI ADS8688 ADCs, with the flexibility to adjust the sampling rate by varying chip-select timing based on the input signal frequency within a specified range. Data can be captured from all the ADCs and processed in real time. Simultaneous SPI data processing occurs in one of the two PRU cores in the PRU-ICSS, freeing up the other PRU core to provide a feedback loop for the incoming signal frequency (adjusting the ADC sampling rate for achieving coherent sampling), as well as performing low-level filtering on incoming ADC data. The use of the PRU-ICSS for analog signal capturing and processing reduces processor overheads and allows implementing external communication protocols and graphic display.

Additional Resources

- Watch the training video, "PRU-ICSS: Interfacing a processor with multiple ADCs."
- Read the blog post, "Analog interfacing for grid infrastructure with Sitara processors."

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