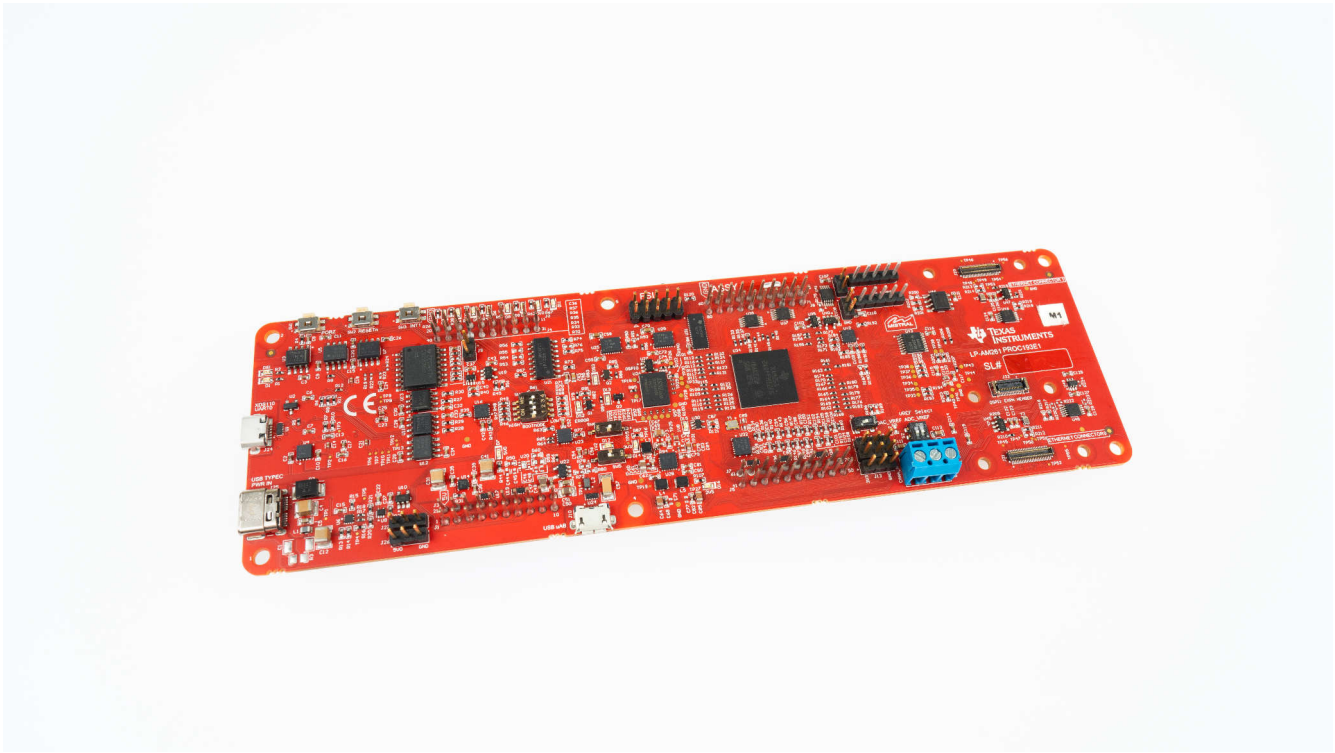
User's Guide

AM261x LaunchPad User Guide

Description

The AM261x LaunchPad™ development kit is a simple and inexpensive hardware evaluation module (EVM) for the Texas Instruments™ Sitara™ AM261x series of microcontrollers (MCUs). This EVM provides an easy way to start developing on the AM261x MCUs with onboard emulation for programming and debugging as well as buttons and LEDs for a simple user interface. The LaunchPad also features two independent BoosterPack XL expansion connectors, two onboard FLASHes and one FLASH expansion connector, two Ethernet PHY add-on board connectors, onboard Controller Area Network (CAN) transceiver, and an onboard XDS110 debug probe.



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Key Features

The AM261x LaunchPad has the following features:

- PCB dimensions: 195.58mm X 58.43mm
- Powered through 5V, 3A USB type-C input
- Two Ethernet PHY add-on board connectors
- Onboard XDS110 debug probe
- Three push buttons:
  - PORz
  - User interrupt
  - RESETz
- LEDs for:
  - Power status
  - User testing
  - I2C driven array
- CAN connectivity with onboard CAN transceiver
- Dedicated FSI connector
- PMIC with three buck converters and one LDO regulator
- Two independent Enhanced Quadrature Encoder Pulse (EQEP) based encoder connectors
- Two independent BoosterPack XL (40 pin) standard connectors
- Onboard memory:
  - 2x 64Mb OSPI Flash
  - 1 Mb I2C Board ID EEPROM

1 LaunchPad Module Overview

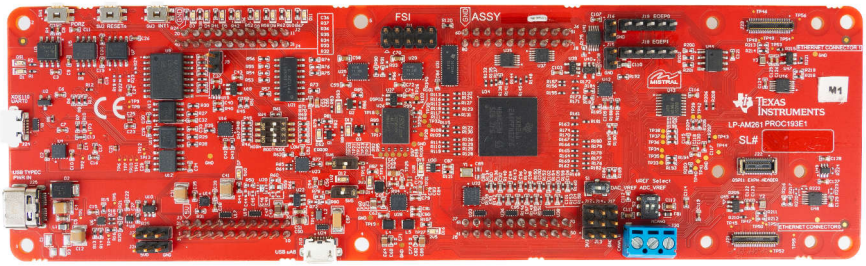

Figure 1-1. AM261x LaunchPad Board

1.1 Introduction

This user's guide details the design of the EVM and how to properly use each interface. The user's guide also details many important aspects of the board including but not limited to power requirements, boot mode selections, and mux/switch signal routing.

1.2 Preface: Read This First

1.2.1 If You Need Assistance

If you have any feedback or questions, support for the Sitara MCUs and the AM261x LaunchPad development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in the Reference Documents.

1.2.2 Important Usage Notes

Note

The AM261x LaunchPad requires a 5V, 3A power supply to function. A 5V, 3A power supply is not included in the kit and must be ordered separately. The *Belkin USB-C Wall Charger* is known to work with the LaunchPad and supplied type-C cable. For more information on power requirements refer to Power Requirements. If there is an insufficient power input then the red LED (DS1) will glow. For more information on power status LEDs refer to Power Status LEDs.

Note

The AM261(U1) SoC on the LaunchPad can reach temperatures of around 54°C during high power consumption use cases as per internal testing. This user guide statement is to alert users to this temperature condition.

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Caution	Caution Hot surface. Contact may cause burns. Do not touch!

Note

External Power Supply or Power Accessory Requirements:

- Nominal output voltage: 5VDC
- Max output current: 3000mA
- Power Delivery

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE,CCC,PSE, etc.

1.3 Kit Contents

The Sitara AM261x Series LaunchPad Development Kit contains the following items:

- AM261x Sitara Series LaunchPad development board
- USB micro-B cable

The kit does not include:

- USB type-C 5V/3A AC/DC supply
- USB type-C cable

1.4 Device Information

1.4.1 System Architecture Overview

The below image shows the overall top level architecture of the AM261x LaunchPad.

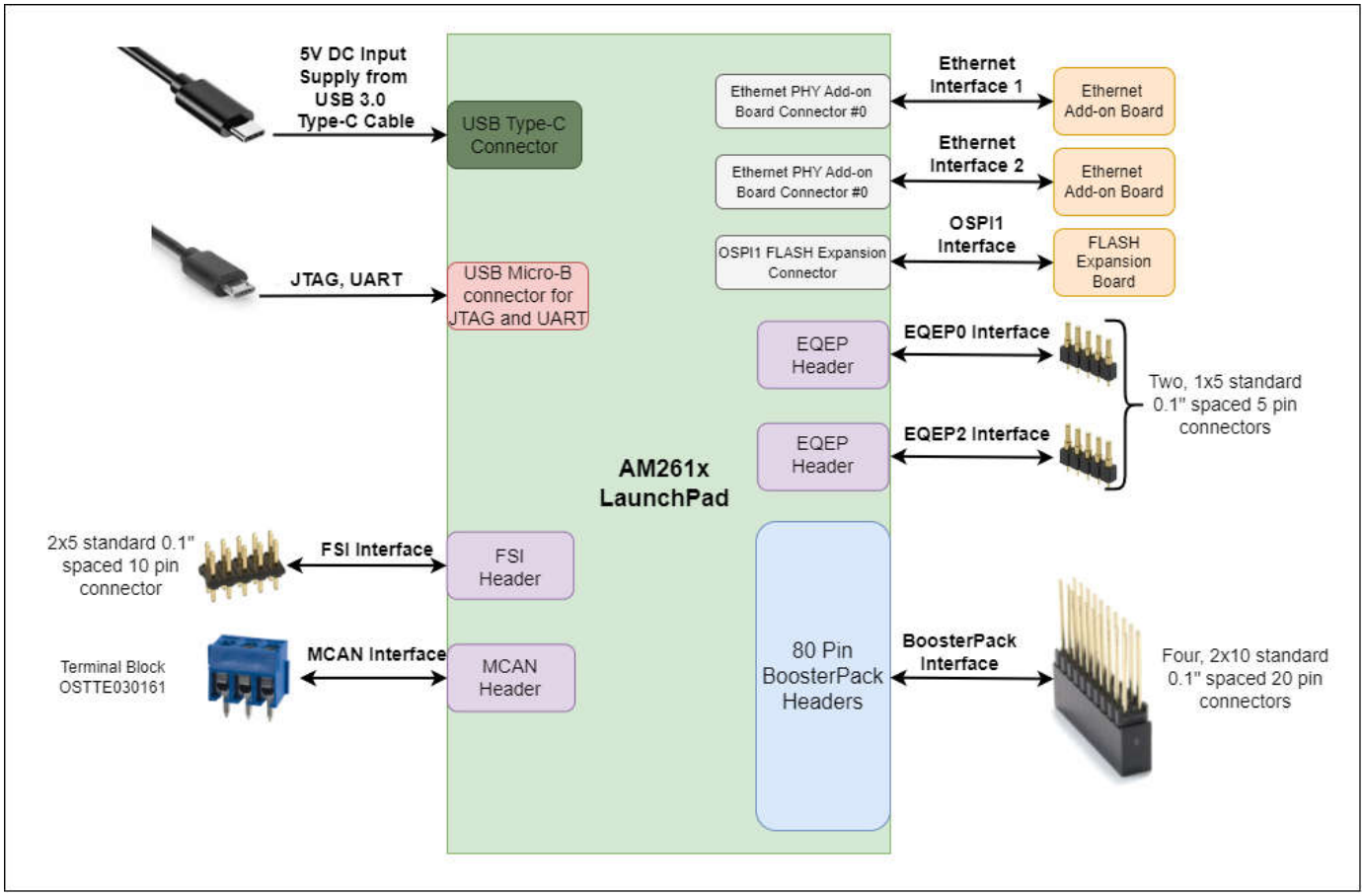

Figure 1-2. System Architecture

1.4.2 Security

The AM261x LaunchPad features a High Security, Field Securable (HS-FS) device. An HS-FS device has the ability to use a one time programming to convert the device from HS-FS to High Security, Security Enforced (HS-SE) device.

The AM261x device leaves the TI factory in an HS-FS state where customer keys are not programmed and has the following attributes:

- Does not enforce the secure boot process
- M4 JTAG port is closed
- R5 JTAG port is open
- Security Subsystem firewalls are closed
- SoC Firewalls are open
- ROM Boot expects a TI signed binary (encryption is optional)
- TIFS-MCU binary is signed by the TI private key

The One Time Programmable (OTP) keywriter converts the secure device from HS-FS to HS-SE. The OTP keywriter programs customer keys into the device efuses to enforce secure boot and establish a root of trust. The secure boot requires an image to be encrypted (optional) and signed using customer keys, which will be verified by the SoC. A secure device in the HS-SE state has the following attributes:

- M4, R5 JTAG ports are both closed
- Security Subsystems and SoC Firewalls are both closed
- TIFS-MCU and SBL need to be signed with active customer key

1.4.3 Compliance

All components selected meet RoHS compliance.

1.4.4 BoosterPacks

The AM261x LaunchPad development kit provides an easy and inexpensive way to develop applications with the AM261x Series microcontroller. BoosterPacks are add-on boards that follow a pin-out standard created by Texas Instruments. The TI and third-party ecosystem of BoosterPacks greatly expands the peripherals and potential applications that you can easily explore with the AM261x LaunchPad. For a detailed diagram on the pin-out of the AM261x LaunchPad, refer to BoosterPack Headers.

You can also build your own BoosterPack by following the design guidelines on TI's website. Texas Instruments even helps you promote your BoosterPack to other members of the community. TI offers a variety of avenues for you to reach potential customers with your solutions.

1.4.5 Component Identification

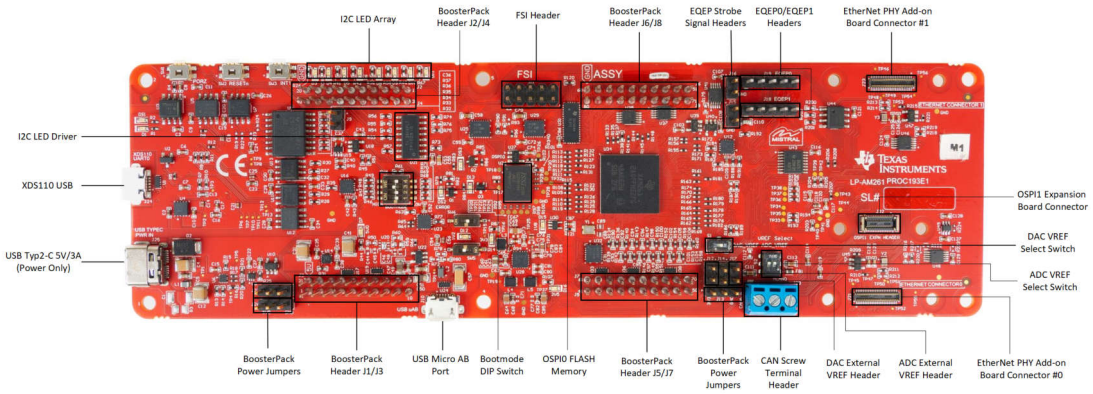

Figure 1-3. AM261x LaunchPad Top Components Identification

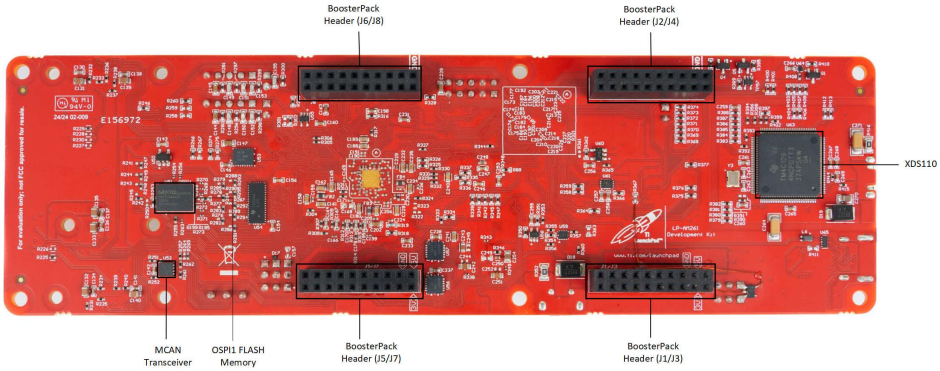

Figure 1-4. AM261x LaunchPad Bottom Components Identification

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2 Hardware Description

2.1 Board Setup

2.1.1 Power Requirements

The AM261x LaunchPad is powered from a 5V, 3A USB type-C input. The following sections describe the power distribution network topology that supply the AM261x LaunchPad, supporting components and the reference voltages.

Power supply solutions that are compatible with the AM261x LaunchPad:

- When using the USB type-C input:
  - 5V, 3A power adapter with USB-C receptacle
  - 5V, 3A power adapter with captive USB-C cable
  - PC USB type-C port that has Power Delivery classification
    - Thunderbolt
    - Battery behind USB logo

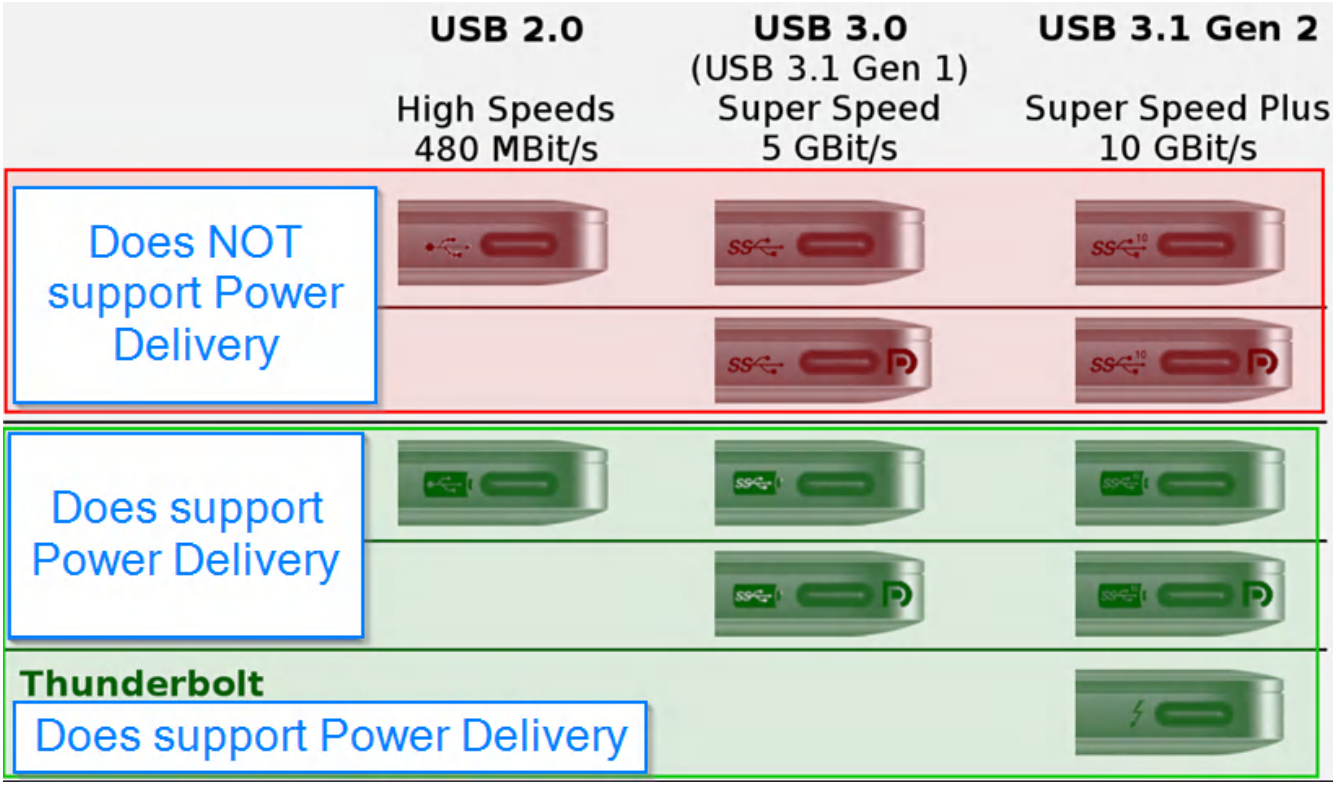

Figure 2-1. USB Type-C Power Delivery Classification

Power supply solutions that are **NOT** compatible with the AM261x LaunchPad:

- When using USB type-C input:
  - Any USB adapter cables such as:
    - Type-A to type-C
    - micro-B to type-C
    - DC barrel jack to type-C
  - 5V, 1.5A power adapter with USB-C captive cable or receptacle
  - PC USB type-C port not capable of 3A

2.1.1.1 Power Input Using USB Type-C Connector

The AM261x LaunchPad is powered through a USB type-C connection. The USB Type-C source should be capable of providing 3A at 5V and should advertise the current sourcing capability through CC1 and CC2 signals. On AM261x LaunchPad, the CC1 and CC2 from USB type-C connector are interfaced to the port controller IC (TUSB320). This device uses the CC pins to determine port attach and detach, cable orientation, role detection, and port control for Type-C current mode. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected.

The Port pin is pulled down to ground with a resistor to configure it as upward facing port (UFP) mode. VBUS detection is implemented to determine a successful attach in UFP mode. The OUT1 and OUT2 pins are connected to a NOR gate. Active low on both the OUT1 and OUT2 pins advertises high current (3A) in the attached state which enables the VUSB_5V0 power switch to provide the VSYS_5V0 supply which powers the PMIC and LDOs.

In UFP mode, the port controller IC constantly presents pull down resistors on both CC pins. The port controller IC also monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The port controller IC de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the port controller device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

The AM261x LaunchPad power requirement is 5V at 3A and if the source is not capable of providing the required power, the output at the NOR gate becomes low that disables the VUSB_5V0 power switch. Therefore, if the power requirement is not met, all power supplies except VCC3V3_TA remains in the off state. The board gets powered on completely only when the source can provide 5V at 3A.

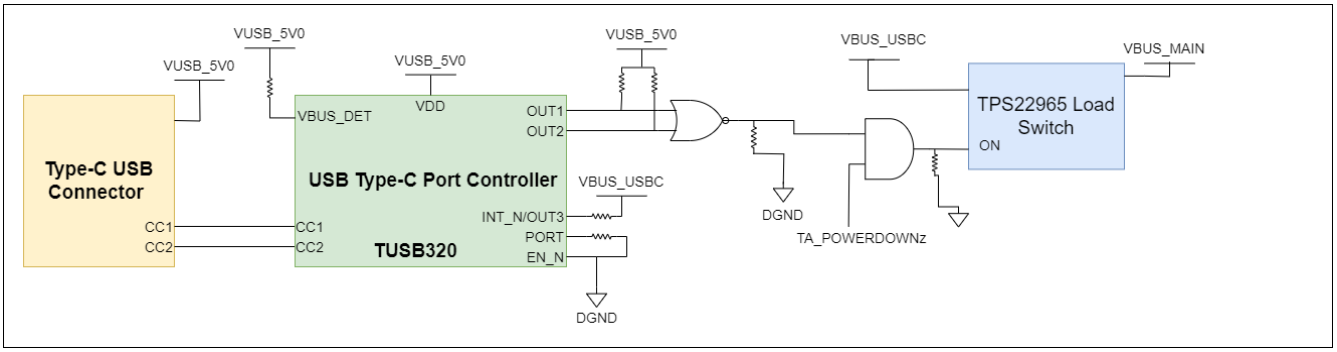

Figure 2-2. Type-C CC Configuration

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Table 2-1. Current Sourcing Capability and State of USB Type-C Cable

OUT1	OUT2	Advertisement
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5A) in attached state
L	L	High current (3.0A) in attached state

The AM261x LaunchPad includes a power solution based on PMIC that comprises three buck converters and one LDO regulator for each of the power rails. During the initial stage of the power supply, 5V supplied by the type-C USB connector is used to generate all of the necessary voltages required by the LaunchPad.

PMIC with three buck converters and one LDO regulator that is used to generate the supplies required for the AM261x system on a chip (SoC) and other peripherals.

Table 2-2. Voltage Rail Generation

Component	Reference Designator	Function	Voltage In	Voltage Out
TPS650360	U28	• Core Digital 1.2V • System 3.3V • System 1.8V • Ethernet Port 2.5V	• Buck_1 VIN - 5.0V • Buck_2 VIN - 5.0V • LDO VIN - 3.3V • Buck_3 VIN - 5.0V	• Buck_1 VOUT - 3.3V • Buck_2 VOUT - 2.5V • LDO VOUT - 1.8V • Buck_3 VOUT - 1.2V

2.1.1.2 Power Status LEDs

Multiple power-indication LEDs are provided onboard to indicate to users the output status of major supplies. The LEDs indicate power across various domains.

Table 2-3. Power Status LEDs

Name	Default Status	Operation	Function
D7	ON	VSYS_5V0	Power indicator for supply 5V voltage
D14	ON	VSYS_3V3	Power indicator for generated 3.3V voltage
D16	ON	VSYS_2V5	Power indicator for generated 2.5V voltage
D12	ON	VDD_1V2	Power indicator for generated 1.2V power-good voltage
D15	ON	VSYS_1V8	Power indicator for generated 1.8V voltage
D13	OFF	WARMRSTN	Power indication for WARMRSTN
DS2	OFF	SAFETY_ERROR	Power error indication for SAFETY_ERROR
D1	OFF	XDS_PROGSTAZ1	LED will glow after micro-B connection is made
DS1	OFF	XDS_PROGSTAZ2	LED will glow to indicate communication over JTAG

Note

DS2 LED that correspond to SAFETY_ERROR is always ON.

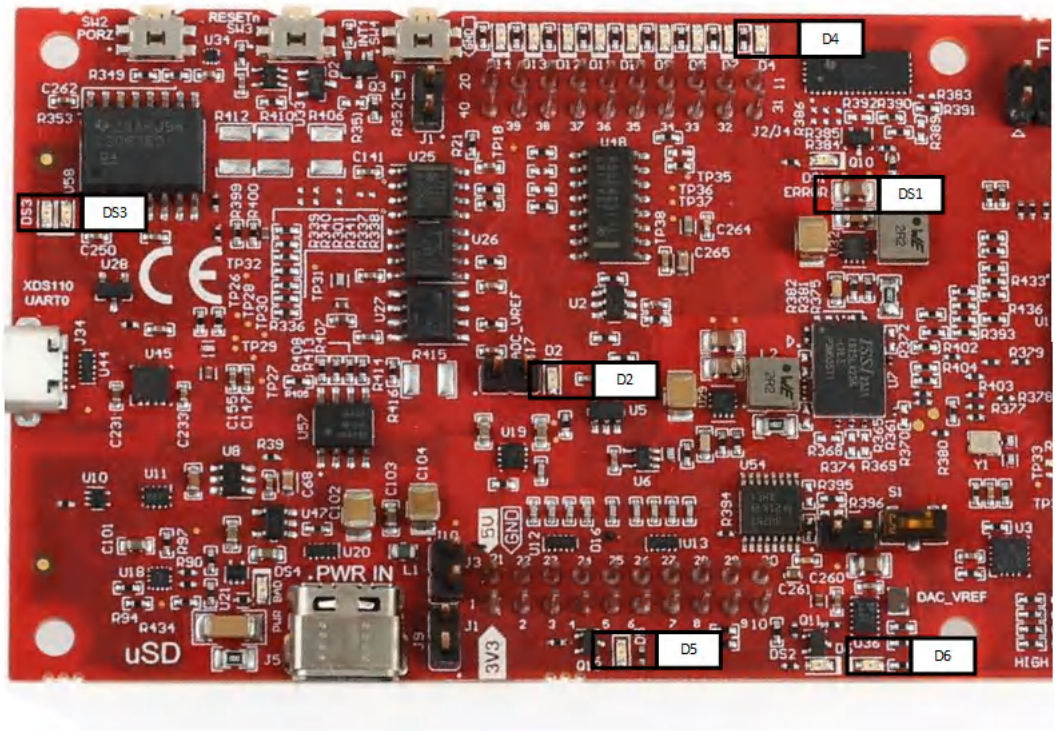

Figure 2-3. Power Status LEDs

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2.1.1.3 Power Tree

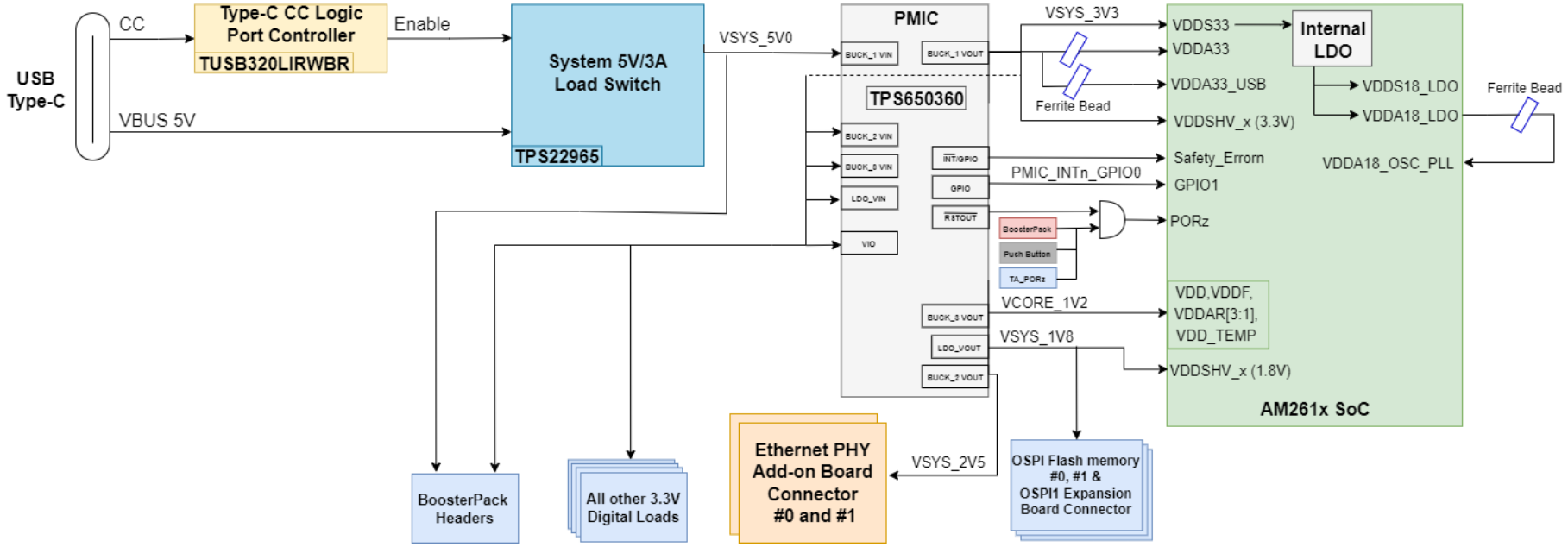

Figure 2-4. Power Tree Diagram of AM261x LaunchPad

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2.1.2 Push Buttons

The LaunchPad supports multiple user push buttons that provide reset inputs and user interrupts to the AM261x SoC.

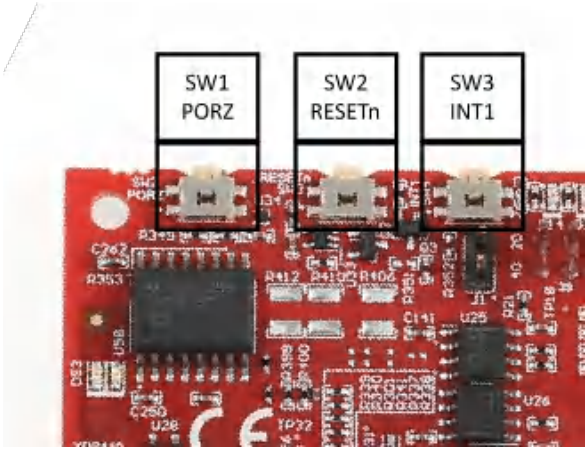

Figure 2-5. Push Buttons

Table 2-4 lists the push buttons that are placed on the top side of the AM261x LaunchPad.

Table 2-4. LaunchPad Push Buttons

Push Button	Signal	Function
SW1	PORz	SoC PORz reset input
SW2	RESETz	SoC warm reset input
SW3	INT1	User Interrupt Signal

2.1.3 Boot mode Selection

The boot mode for the AM261x is selected by a DIP (Dual In-Line Package) switch (SW4) or the test automation header. The test automation header uses an I2C expansion buffer to drive the boot mode when PORz is toggled. The supported boot modes are shown in Table 2-5. The DIP Switch configurations for each boot mode are shown in Table 2-5. As seen in the schematic, enabling a switch pulls the respective pin to GND through a 1kΩ resistor.

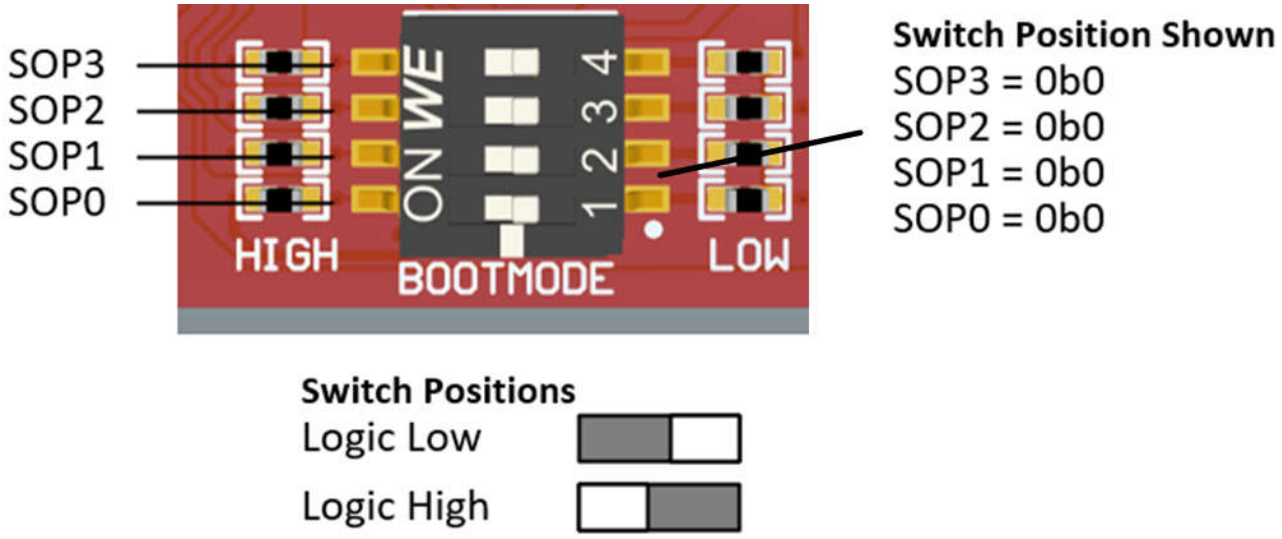

Figure 2-6. Boot mode DIP Switch Positions - LP AM261x E2 SW1 SOP Switches

Table 2-5. Supported Bootmodes and Bootmode Selection

SOP3	SOP2	SOP1	SOP0	Bootmode	ROM Activity	LaunchPad Switch Config
0	0	0	0	OSPI-OSPI (4S), 50MHz, SDR, 0x6B	ROM configures OSPI controller in OSPI 4S mode and downloads image from external flash, supports UART fallback boot mode if any failures	1111
0	0	0	1	UART, XMODEM, 115200bps	ROM configures UART0 with baud rate of 115200 bps and downloads image from external PC terminal using x-modem protocol	1110
0	0	1	0	OSPI-OSPI (1S), 50MHz, SDR, 0x0B	ROM configures OSPI controller in OSPI 1S mode and downloads image from external flash, supports UART fallback boot mode if any failures	1101
0	0	1	1	OSPI (8S), SDR, 33 MHz, 0x8B	ROM configures OSPI controller in 8S mode and downloads image from external flash, supports UART fallback boot mode if any failures	1100
1	0	1	1	DevBoot	To support SBL development, R5-will come up with ROM eclipsed, PLLs are initialized, No L2, TCMA and TCMB PBIST are performed, No L2 and TCM memInit. Supported only on FS devices	0100
1	1	0	0	xSPI (1S->8D), 20 MHz, SFDP	ROM configures OSPI controller in xSPI 8D mode, Reads SFDP table for read command and downloads image from external flash, Flashes with SFDP are of JEDEC standard Rev D only supported. In case of any failure it falls back to UART boot mode	0011
1	1	1	0	USB DFU	ROM configures USB controller to work in device mode and download the image into L2 memory to process. In case of any failure it falls back to UART boot mode. Supports USB 2.0 device mode at High-Speed (HS, 480 Mbps)	0001

Table 2-5. Supported Bootmodes and Bootmode Selection (continued)

SOP3	SOP2	SOP1	SOP0	Bootmode	ROM Activity	LaunchPad Switch Config
1	x	x	x	Unknown Boot mode	Treated as unknown Boot mode, System gets Panic and waits for watchdog to reset	0xxx

2.1.4 IO Expander

AM261x LaunchPad has two TCA6408ARGTR IO Expanders that provide general-purpose I/O expansion and bidirectional voltage translation for processors through I2C communication, an interface consisting of serial clock (SCL), and serial data (SDA) signals.

The TCA6408A consists of one 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high) Register. At power on, the I/Os are configured as inputs. However, the system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output Register. The polarity of the Input Port Register can be inverted with the Polarity Inversion Register. All registers can be read by the system controller. In AM261 SoC, the communication with the IO Expander is done through the I2C0 bus. The signals that are coming out of the IO Expander shown in Figure 2-7. Please refer to TCA6408ARGTR-Datasheet for programming guide of TCA6408ARGTR.

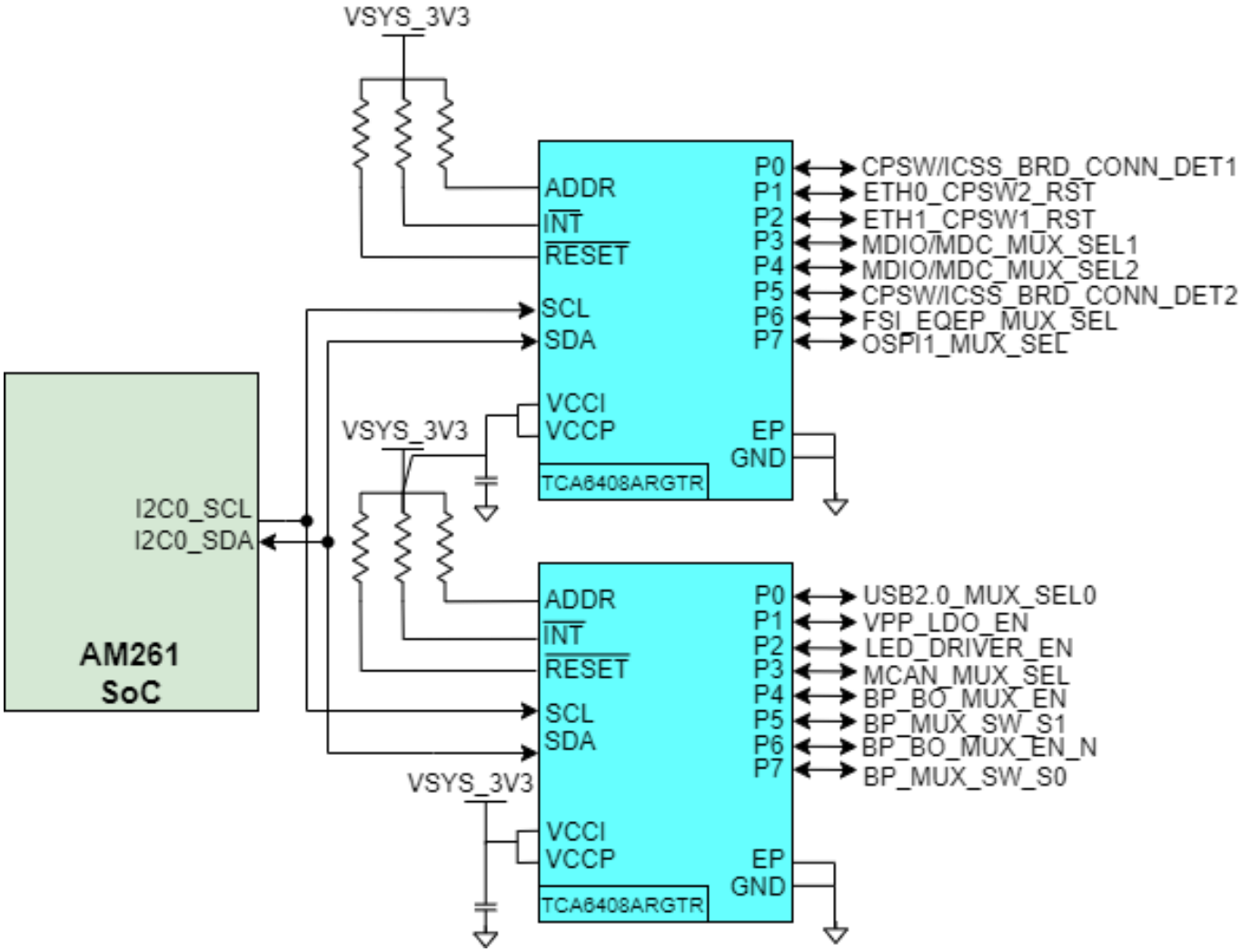

Figure 2-7. IO Expander

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2.2 Functional Block Diagram

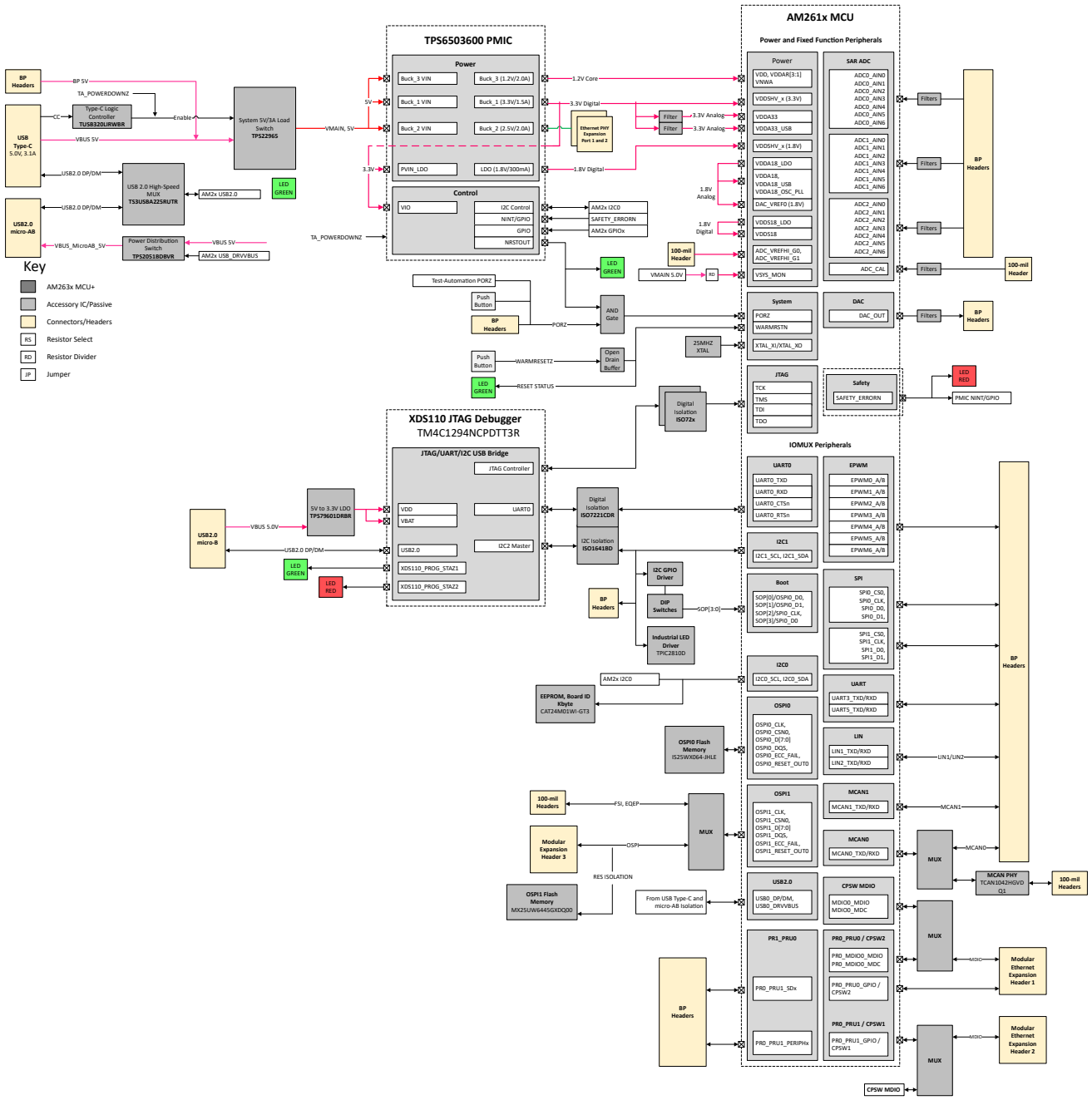

Figure 2-8. AM261x LaunchPad Functional Block Diagram

2.3 GPIO Mapping

Table 2-6. GPIO Mapping Table

GPIO Description	GPIO	Functionality	Net Name	Active Status
GPIO LED	GPIO84	GPIO	AM261_LED_GPIO84	LOW
Interrupt To SoC	GPIO124	Interrupt	AM261_INT_PB_GPIO124	LOW

2.4 Reset

Figure 2-9 shows the reset architecture of the AM261x LaunchPad

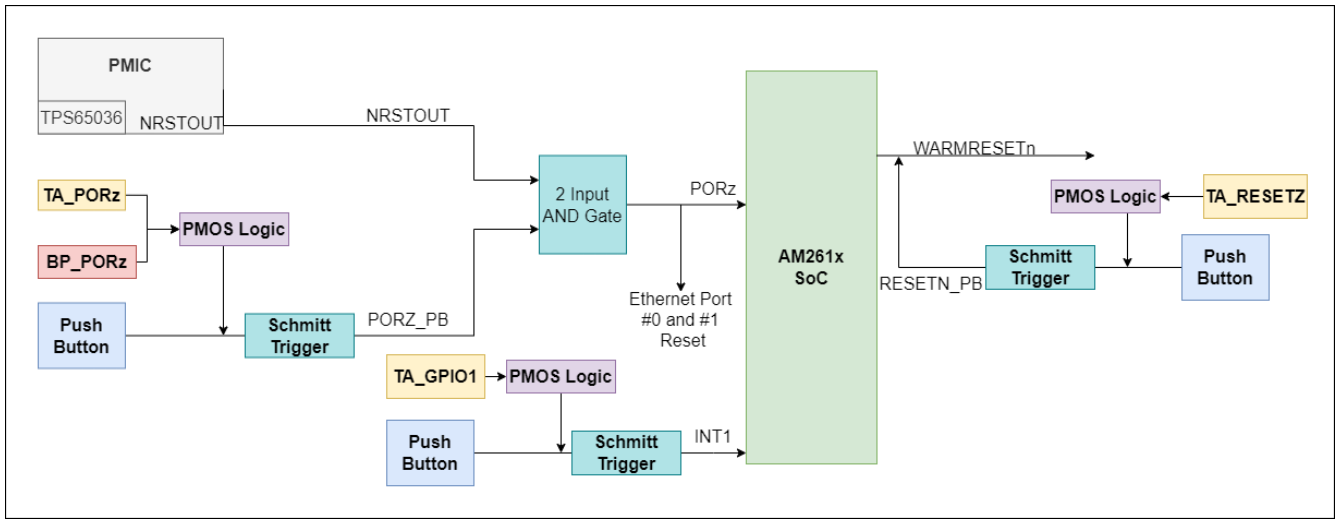

Figure 2-9. Reset Architecture

The AM261x LaunchPad has the following resets:

- PORz is the Power On Reset
- WARMRESETn is the warm reset

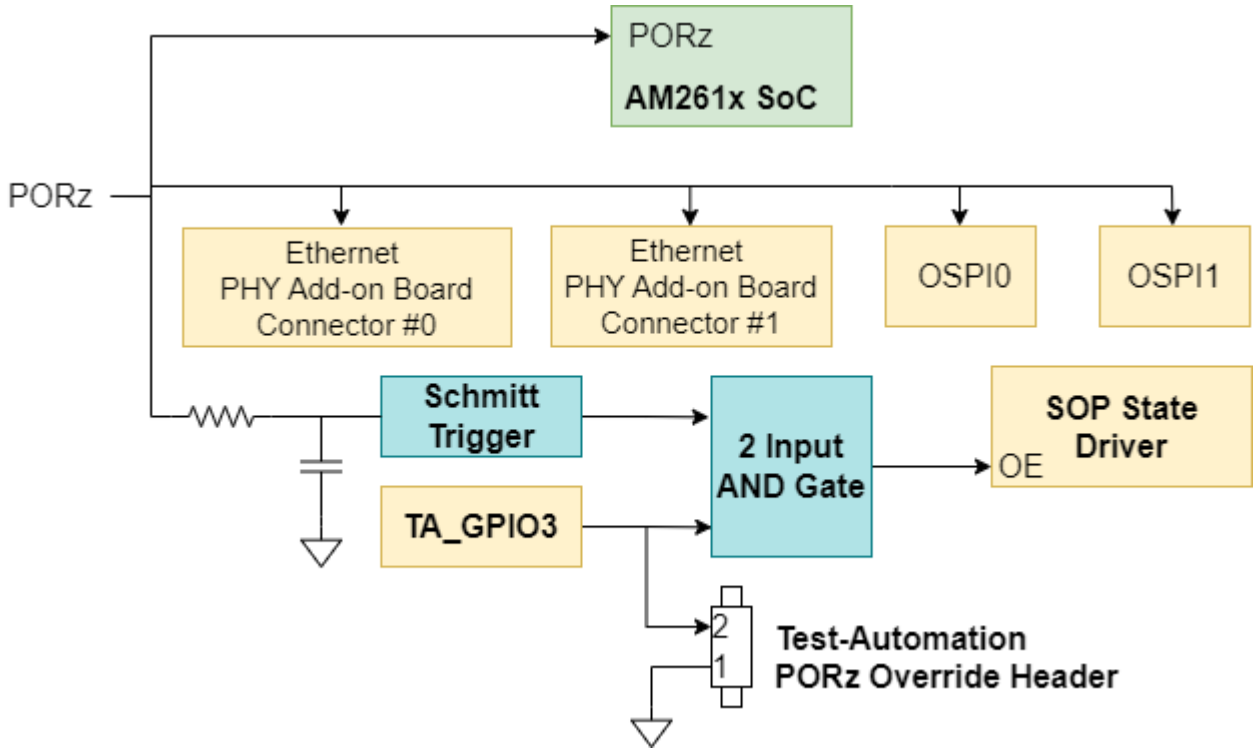

Figure 2-10. PORZ Reset Signal Tree

The PORz signal is driven by a 2-input AND gate that generates a power on reset for the MAIN domain when:

- The PMIC's(TPS650360) NRSTOUT is driven low .
- The user push button (SW1) is pressed.

- A P-Channel MOSFET gate's signal is logic LOW which causes V_{GS} of the PMOS to be less than zero and so the PORz signal connects to the PMOS drain which is tied directly to ground. The signals that can create the logic LOW input to the PMOS gate are:
  - TA_PORZ output from the Test Automation header
  - BP_PORZ output from either of the BoosterPack sites.

The PORz signal is tied to:

- AM261x SoC PORz input
- Both Ethernet port connector's reset input
- Both OSPI FLASH's reset input
- Boot mode State Driver(U61)'s output enable input
  - There is an RC filter to create a 1ms delay from GND to 3.0V such that the SOP State Driver's output enable input is low longer than the required SOP hold time following a PORz de-assertion.

The WARMRESETn signal creates a warm reset to the MAIN domain when:

- The user push button (SW2) is pressed.

The WARMRESETn signal is tied to:

- AM261x SoC WARMRESETN output
- RESETN_PB signal that is created from push button + PMOS logic

The AM261x LaunchPad also has an external interrupt to the SoC , INT1, that occurs when:

- The user push button (SW3) is pressed.

2.5 Clock

The AM261x SoC requires a 25MHz clock input for XTAL_XI. The AM261x LaunchPad uses a 25MHz crystal for the SoC clock source. The LaunchPad also has two 25MHz Crystals onboard for the Ethernet PHY clocking which can be connected to the ethernet port connectors on the board using ethernet add-on boards. The SoC clock signal output CLKOUT1 can be used as a clock source for an Ethernet PHY on an attached Ethernet add-on board. The resistors (R211 & R214) must be removed from the traces connecting the 25MHz Crystals to Ethernet Connector 0 and Ethernet Connector 1. Mount the appropriate resistors (R212 & R213) for CLKOUT1 to be routed to both of the Ethernet add-on board connectors to connect the CLKOUT1 net to the XI pin of the Ethernet PHYs on the add-on boards.

The LaunchPad also has a on board crystal (Y4) of frequency 16MHz which is clock source for the XDS110 for UART-USB JTAG support.

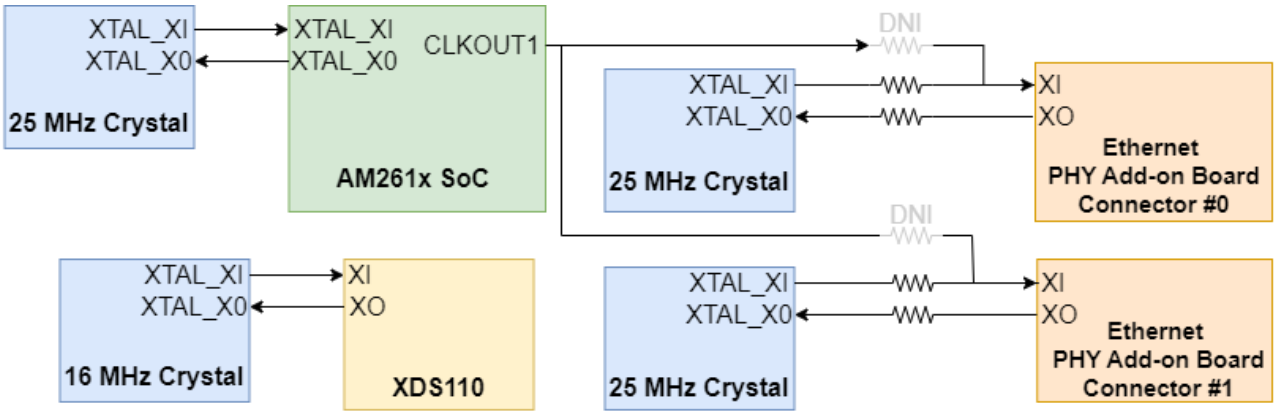

Figure 2-11. AM261x LaunchPad Clock Tree

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2.6 Memory Interfaces

2.6.1 OSPI

The AM261x LaunchPad has two 64Mb OSPI Flash memory devices. IS25LX256-LHLE is connected to the OSPI0 interface. MX25UW6445GXDQ00 IS connected to the OPSI1 interface of the AM261x SoC. The AM261x LaunchPad also has an OSPI Flash expansion connector which is connected to the OSPI1 interface. The OSPI peripheral supports single data rates and double data rates with memory speeds up to 166MHz. The OSPI flash is powered by the 1.8V system supply.

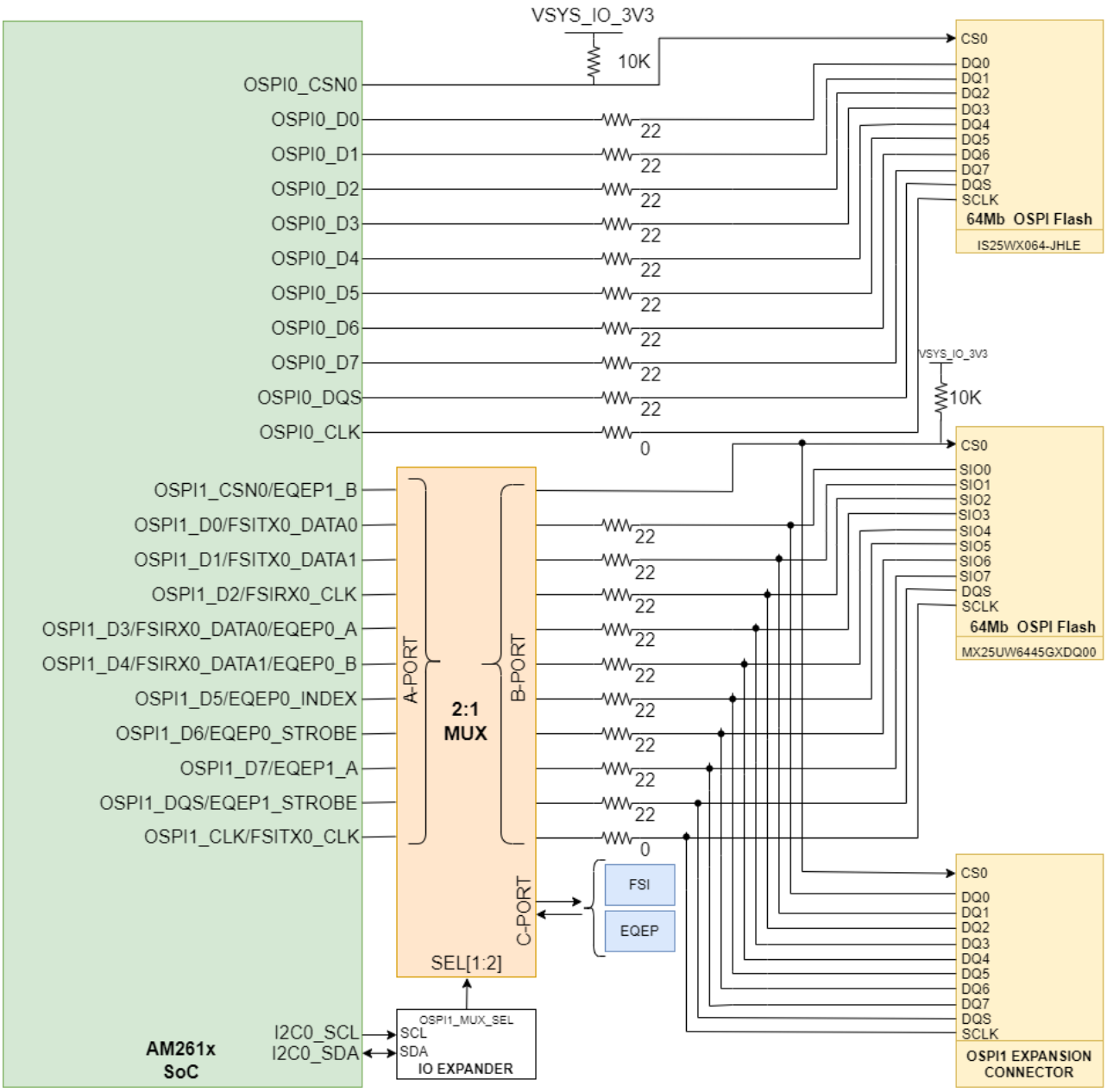

Figure 2-12. OSPI Flash Interface

2.6.2 Board ID EEPROM

The AM261x LaunchPad has a I2C based 1Mbit EEPROM (CAT24M01WI-GT3) to store board configuration details. The Board ID EEPROM is connected to the I2C1 interface of the AM261x SoC. The default I2C address of the EEPROM is set to 0x51 by pulling up the address pin A0 and pulling down the address pins A1 and A2 to ground. The Write Protect pin for the EEPROM is by default pulled down to ground and therefore Write Protect is disabled.

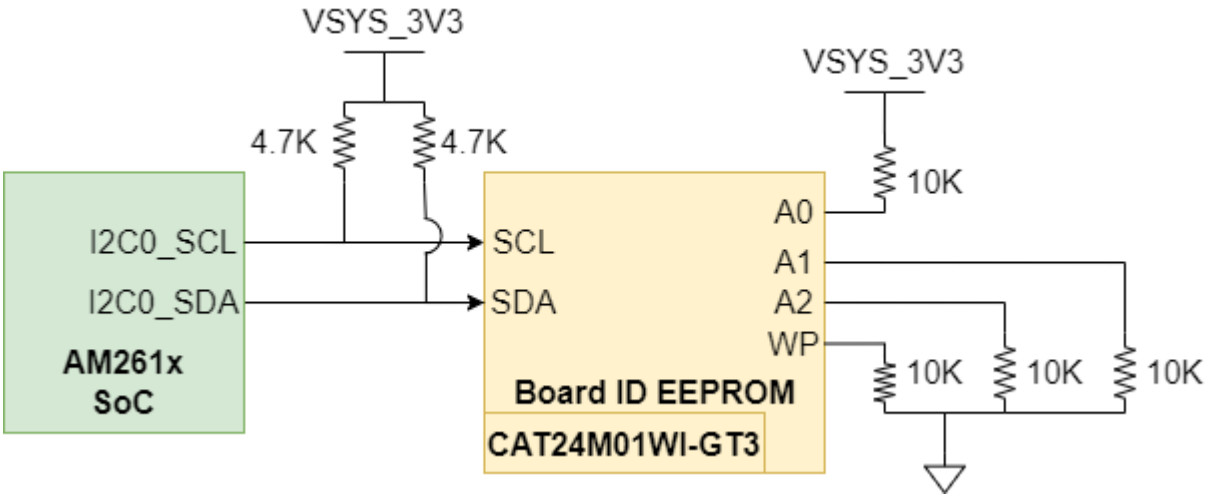

Figure 2-13. Board ID EEPROM

2.7 Ethernet Interface

2.7.1 Ethernet PHY Add-on Board connector #0 - CPSW RGMII/ICSSM

Note

The PRU internal pinmux mapping provided in the TRM is part of the original hardware definition of the PRU. However, due to the flexibility provided by the IP and associated firmware configurations, this is not necessarily a hard requirement. The first PRU implementation for AM65x had the MII TX pins swapped during initial SOC integration and this convention as maintained for subsequent PRU revisions to enable firmware reuse. To make use of the SDK firmware, use the SYSCONFIG generated PRU pin mapping.

The AM261x LaunchPad has a 48-pin Ethernet PHY add-on board connector connected to either CPSW RGMII or one on-die Programmable Real-time Unit and Industrial Communication Sub System (PRU-ICSS). The RGMII CPSW port and ICSSM are internally pinmuxed on the AM261x SoC. For more information on the internal muxing of signals refer to *Pinmux Mapping* . AM261x internal Pinmux is used to select between the RGMII or PRU-ICSS signals. Ethernet port connector can be connected to the Ethernet daughtercard that comprises a PHY device and RJ45 connector.

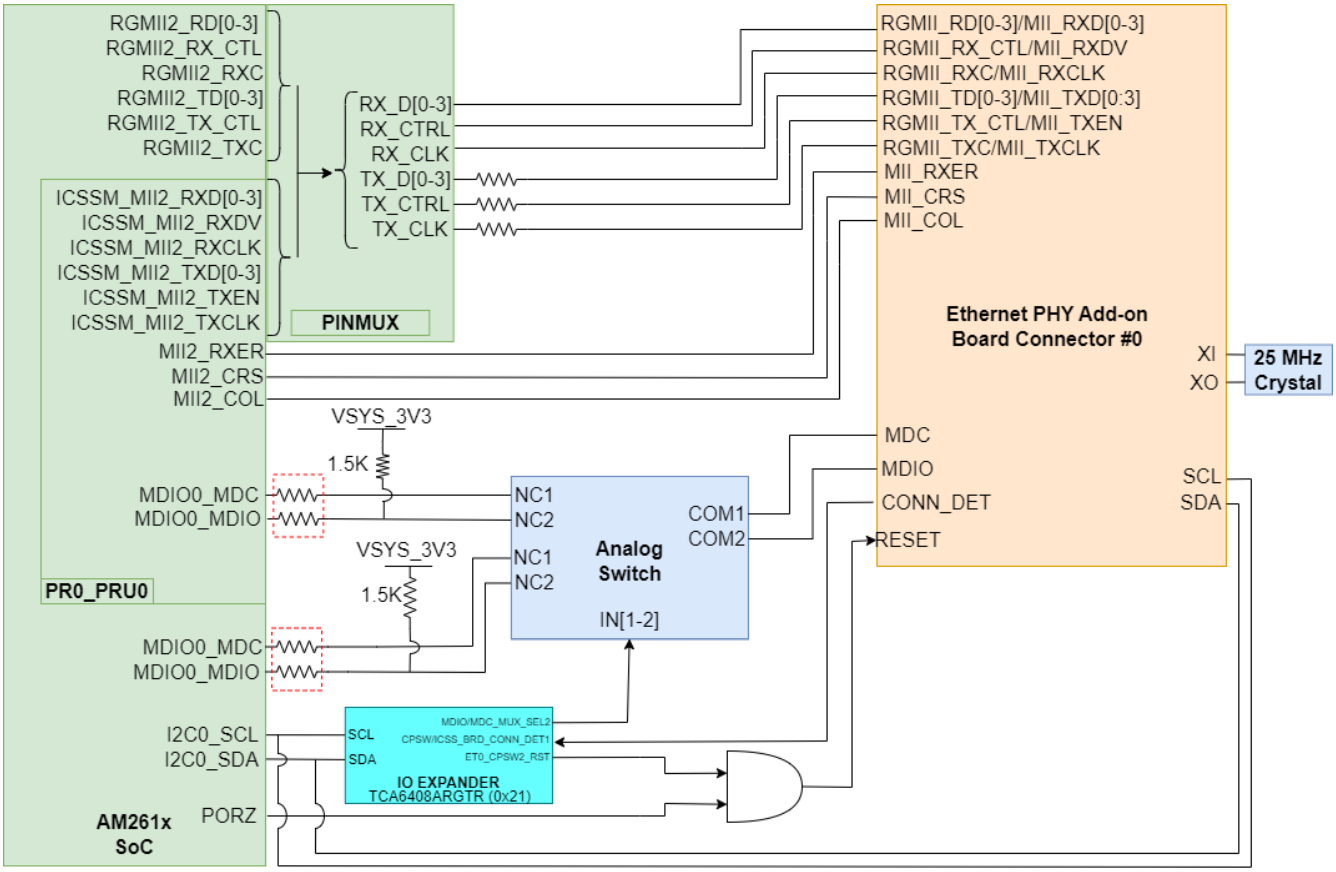

Figure 2-14. Ethernet PHY Add-on Board connector #0

The MDIO signal from the SoC to the ethernet port connector requires 1.5kΩ pullup resistors to the 3.3V system supply voltage for proper operation. There is an analog switch (TS5A23159DGSR) that selects between the CPSW MDIO/MDC and the ICSSM MDIO/MDC signals to be routed to the Ethernet port connector. This analog switch is controlled by an IO expander signal that selects between CPSW MDIO/MDC and ICSSM MDIO/MDC signals.

The reset input for the PHY from Ethernet port connector is controlled by the PORz AM261x SoC output signal.

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2.7.2 Ethernet PHY Add-on Board connector #1 - CPSW RGMII/ICSSM

Note

The PRU internal pinmux mapping provided in the TRM is part of the original hardware definition of the PRU. However, due to the flexibility provided by the IP and associated firmware configurations, this is not necessarily a hard requirement. The first PRU implementation for AM65x had the MII TX pins swapped during initial SOC integration and this convention was maintained for subsequent PRU revisions to enable firmware reuse. To make use of the SDK firmware, use the SYSCONFIG generated PRU pin mapping.

The AM261x LaunchPad has a 48-pin Ethernet PHY Add-on Board connector connected to either CPSW RGMII or one on-die Programmable Real-time Unit and Industrial Communication Sub System (PRU-ICSS). The RGMII CPSW port and ICSSM are internally pinmuxed on the AM261x SoC. For more information on the internal muxing of signals refer to *Pinmux Mapping*. AM261x internal Pinmux is used to select between the RGMII or PRU-ICSS signals. Ethernet port connector can be connected to the Ethernet daughtercard that comprises a PHY device and RJ45 connector.

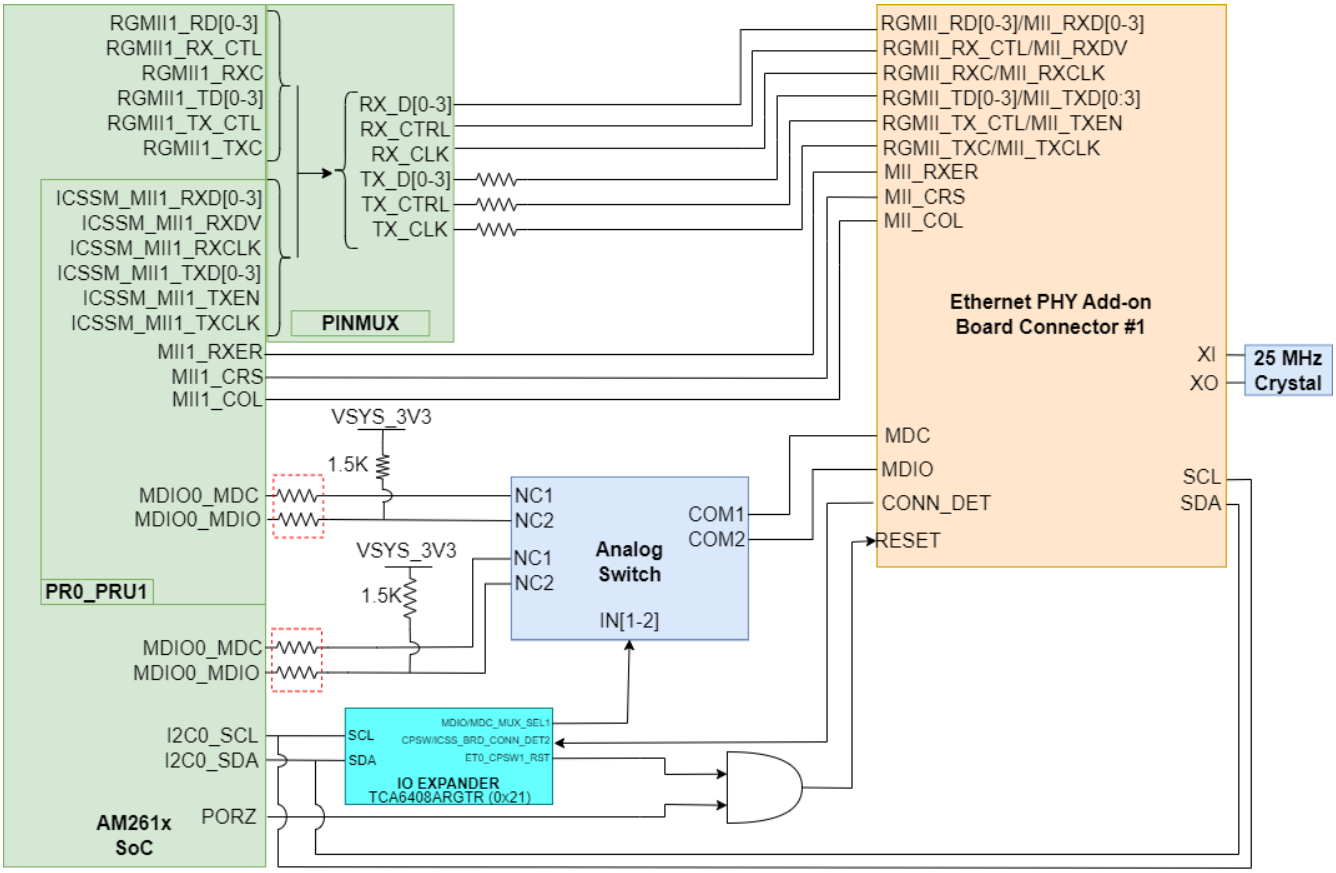

Figure 2-15. Ethernet PHY Add-on Board connector #1

The MDIO signal from the SoC to the ethernet port connector requires 1.5kΩ pullup resistors to the 3.3V system supply voltage for proper operation. There is an analog switch (TS5A23159DGSR) that selects between the CPSW MDIO/MDC and the ICSSM MDIO/MDC signals to be routed to the Ethernet port connector. This analog switch is controlled by an IO expander signal that selects between CPSW MDIO/MDC and ICSSM MDIO/MDC signals.

The reset input for the PHY from Ethernet port connector is controlled by the PORz AM261x SoC output signal.

2.8 I2C

The AM261x LaunchPad uses two AM261x SoC inter-integrated circuit (I2C) ports to operate as a controller for various targets. I2C data and clock lines needs to be pulled up to the 3.3V system voltage supply to enable communication.

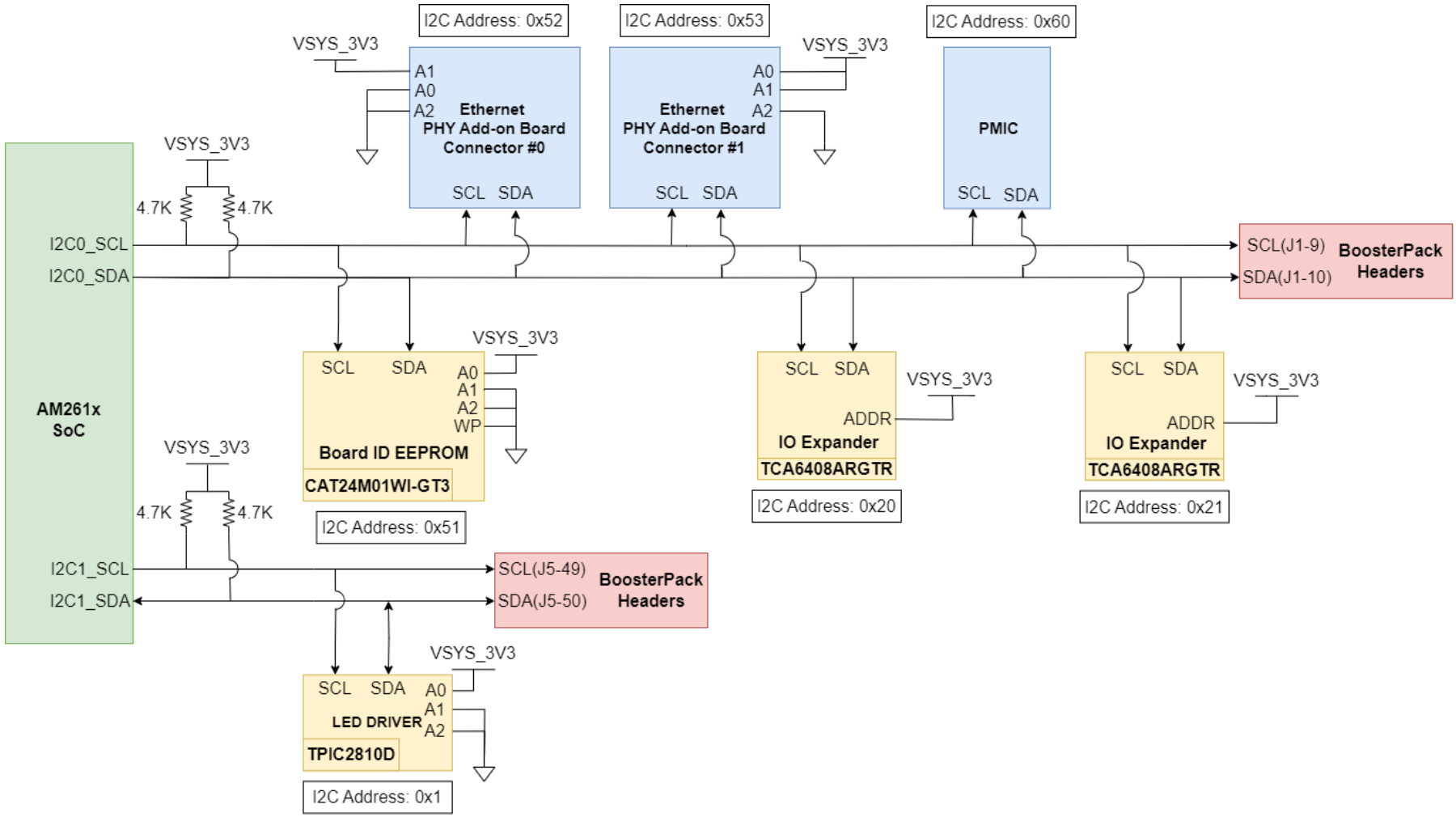

Figure 2-16. I2C Targets

ADVANCE INFORMATION

Table 2-7. I2C Addressing

Target	I2C Instance	I2C Addres Bit Description	Device Addressing	LaunchPad Config.	I2C Address
Board ID EEPROM	I2C0	The first 4 bits of the device address are set to 1010, the next two are set by the A2 and A1 pins, the seventh bit, a16, is the most significant internal address bit	0b10110[A2][A1][a16] A1 and A2 is connected to ground	0b1010001	0x51
LED Driver	I2C1	The first four bits of the target address are 0000, the following three are determined by A2, A1, and A0	0b0000[A2][A1][A0] A2 and A1 are connected to ground A0 is connected to 3.3V supply	0b0000001	0x01
BoosterPack Headers	I2C0, I2C1	Dependent on target			
IO Expander #1	I2C0	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	IO_ADDR pin connected to 3.3V supply	0b0100001	0x21
IO Expander #2	I2C0	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	IO_ADDR pin connected to 3.3V supply	0b0100000	0x20
Ethernet PHY add-on Board Connector #0	I2C0	The first four bits of the target address are 1010, the following three are determined by A2, A1, and A0	0b1010[A2][1][A0] A2 and A0 are connected to ground	0b1010010	0x52
Ethernet PHY add-on Board Connector #1	I2C0	The first four bits of the target address are 1010, the following three are determined by A2, A1, and A0	0b1010[A2][1][A0] A2 are connected to ground and A0 is connected to 3.3V supply	0b1010011	0x53
PMIC	I2C0	7 bit device address for the PMIC is 1100000	0b1100000	0b1100000	0x60

Note

Underlined address bits are fixed based on the device addressing and cannot be configured.

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2.9 Industrial Application LEDs

The AM261x LaunchPad has an LED Driver (TPIC2810D) that is used for Industrial Communication LEDs. The driver is connected to eight green LEDs, and the driver has an I2C address of 0x01.

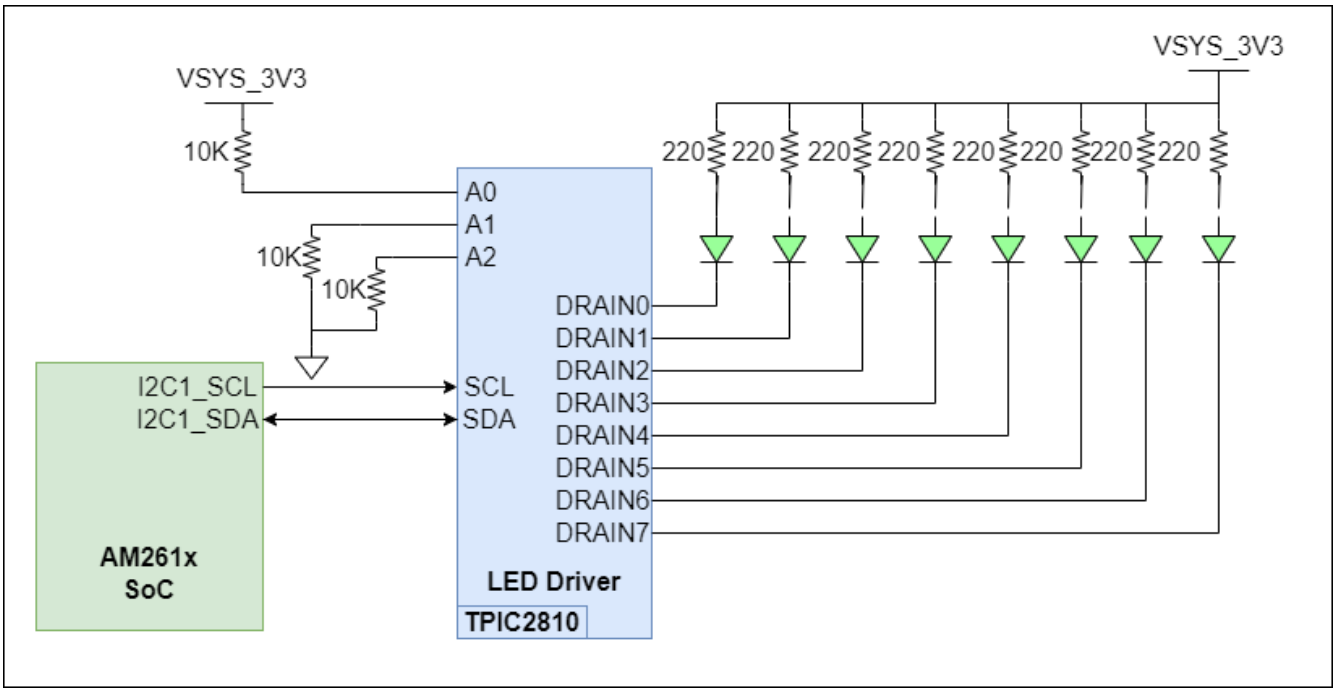

Figure 2-17. Industrial Application I2C LED Array

2.10 SPI

The AM261x LaunchPad maps two SPI instances (SPI0, SPI2) from the AM261x SoC to the BoosterPack Headers. Series termination resistors are placed near the SoC for each SPI clock and SPI D0 signal. There is a 2:1 mux (TS3DDR3812RUAR) that is responsible for selecting SPI0 signals for proper function. The mux is driven by an IO Expander. All SPI2 signals are directly routed to the boosterpack.

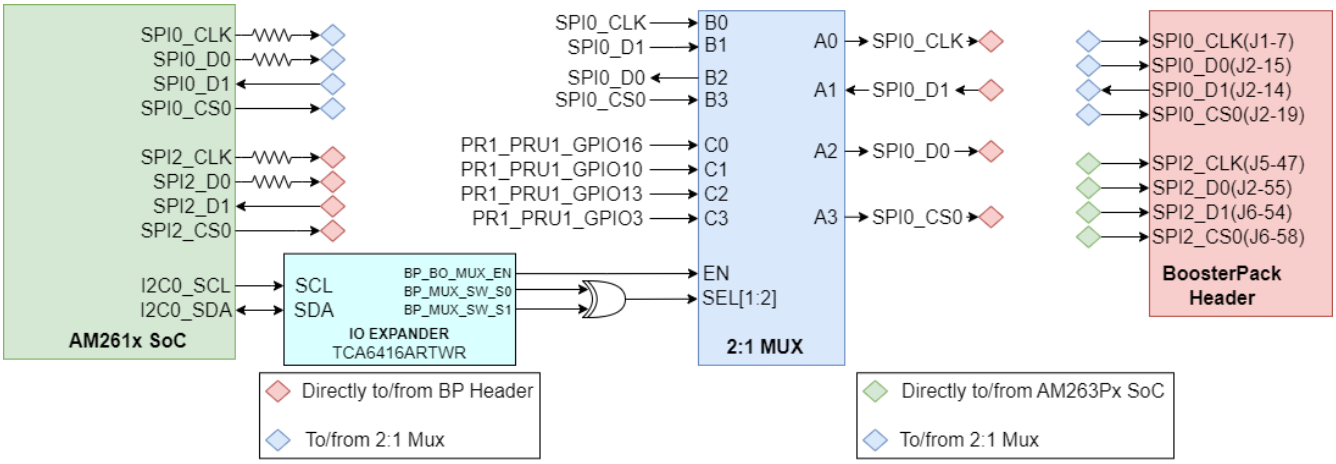

Figure 2-18. SoC SPI to BoosterPack

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2.11 UART

The AM261x LaunchPad uses the XDS110 as a USB2.0 to UART bridge for terminal access. UART0 transmit and receive signals of the AM261x SoC are mapped to the XDS110 with a dual channel isolation buffer (ISO7721DR) for translating from the 3.3V IO voltage supply to the 3.3V XDS supply. The XDS110 is connected to a micro-B USB connector for the USB 2.0 signals. ESD protection is provided to the USB 2.0 signals by a transient voltage suppression device (TPD4E02B04DQAR). The micro-B USB connector's VBUS 5V power is mapped to a low dropout regulator (TPS79601DRBR) to generate the 3.3V XDS110 supply. A separate 3.3V supply for the XDS110 allows for the emulator to maintain a connection when power to the LaunchPad is removed.

UART3 instance is mapped directly to the BoosterPack header.

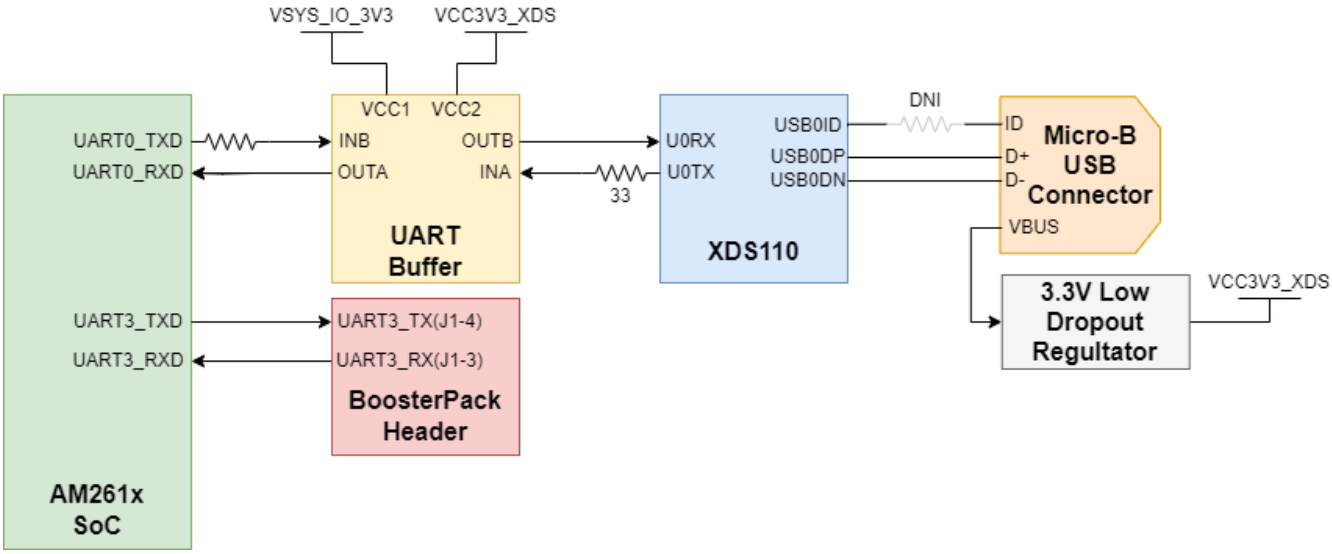

Figure 2-19. UART

ADVANCE INFORMATION

2.12 MCAN

The LaunchPad is equipped with a single MCAN Transceiver (TCAN1044VDRBTQ1) that is connected to the MCAN0 interface of the AM261x SoC. The MCAN Transceiver has two power inputs, VIO is the transceiver 3.3V system level shifting supply voltage and VCC is the transceiver 5V supply voltage. The SoC CAN data transmit data input is mapped to TXD of the transceiver and the CAN receive data output of the transceiver is mapped to the MCAN RX signal of the SoC.

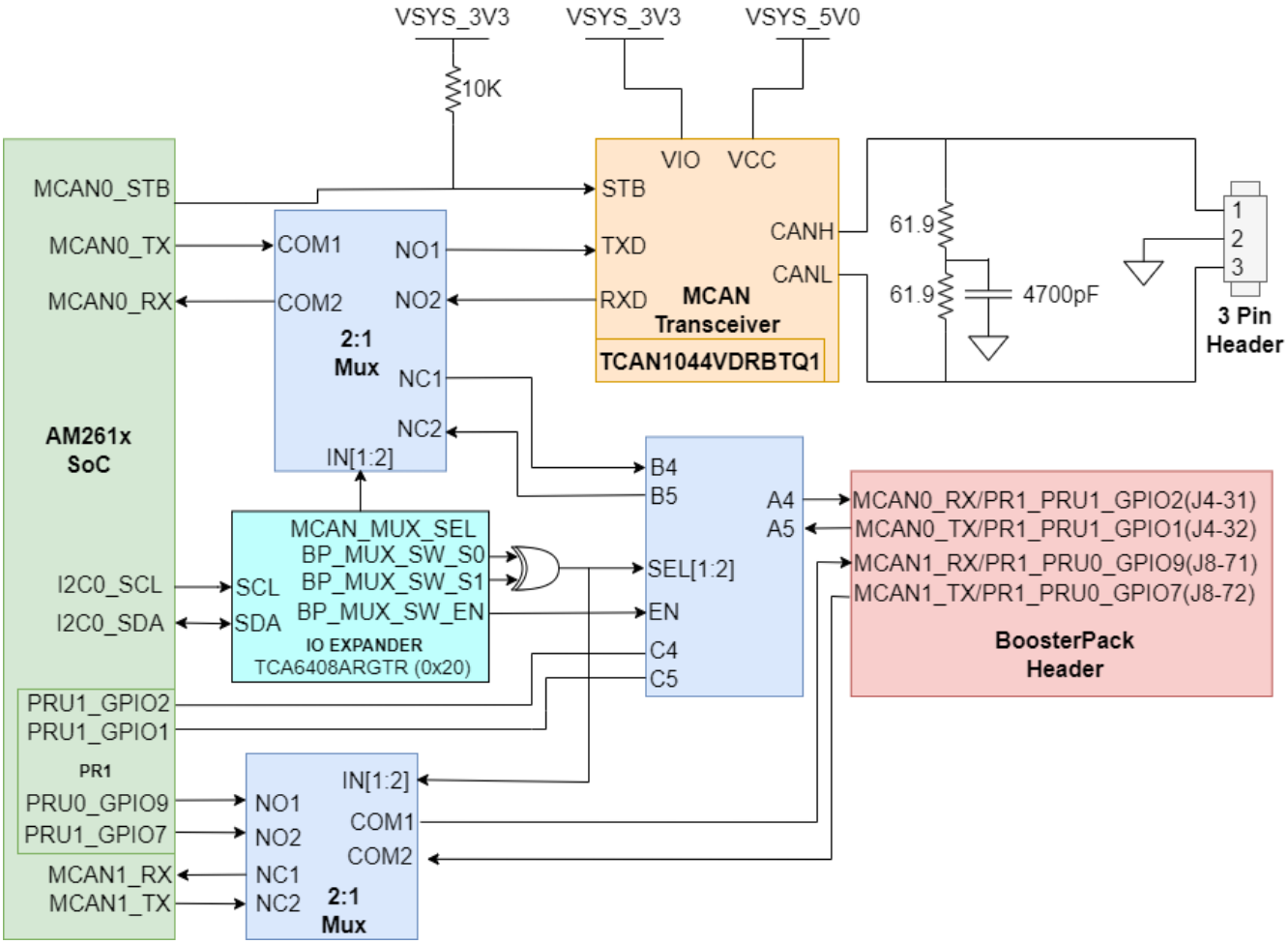

Figure 2-20. CAN Transceiver and BoosterPack Header

The system has a 120Ω split termination on the CANH and CANL signals to improve EMI performance. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The low and high level CAN bus input output lines are terminated to a three pin header.

The standby control signal is an AM261x SoC GPIO signal. The STB control input has a pullup resistor that is used to have the transceiver be in low-power standby mode to prevent excessive system power. Below is a table that shows the operating modes of the MCAN transceiver based on the STB control input logic.

Table 2-8. MCAN Transceiver Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

MCAN1 is routed to the BoosterPack Header via a 2:1 mux. The mux selects whether PR1_PRU0 signals or MCAN signals are mapped to the BoosterPack Header. The Detailed BoosterPack modes are given in BoosterPack Chapter.

Table 2-9. MCAN BoosterPack Mux

BP_MUX_SW_S1	BP_MUX_SW_S0	Condition	Function of Mux
LOW	LOW	MCAN TX/RX Selected	Port A ↔ Port B/COM ↔NC
LOW	HIGH	PRU Signals Selected	Port A ↔ Port C/COM ↔NO
HIGH	LOW	PRU Signals Selected	Port A ↔ Port C/COM ↔NO
HIGH	HIGH	MCAN TX/RX Selected	Port A ↔ Port B/COM ↔NC

2.13 FSI

The AM261x LaunchPad supports a fast serial interface by terminating the SoC signals to a 10-pin header. The interface has two lines of data and a clock line for both the receive and transmit signals. The 10-pin header is connected to the 3.3V System voltage supply. AM261x internal pinmux can be used to select between FSI signals and other functionality of the associated pins. After that there is 2:1 mux that select between FSI signals and OSPI signals, from FSI signals are routed to the 10-pin header.

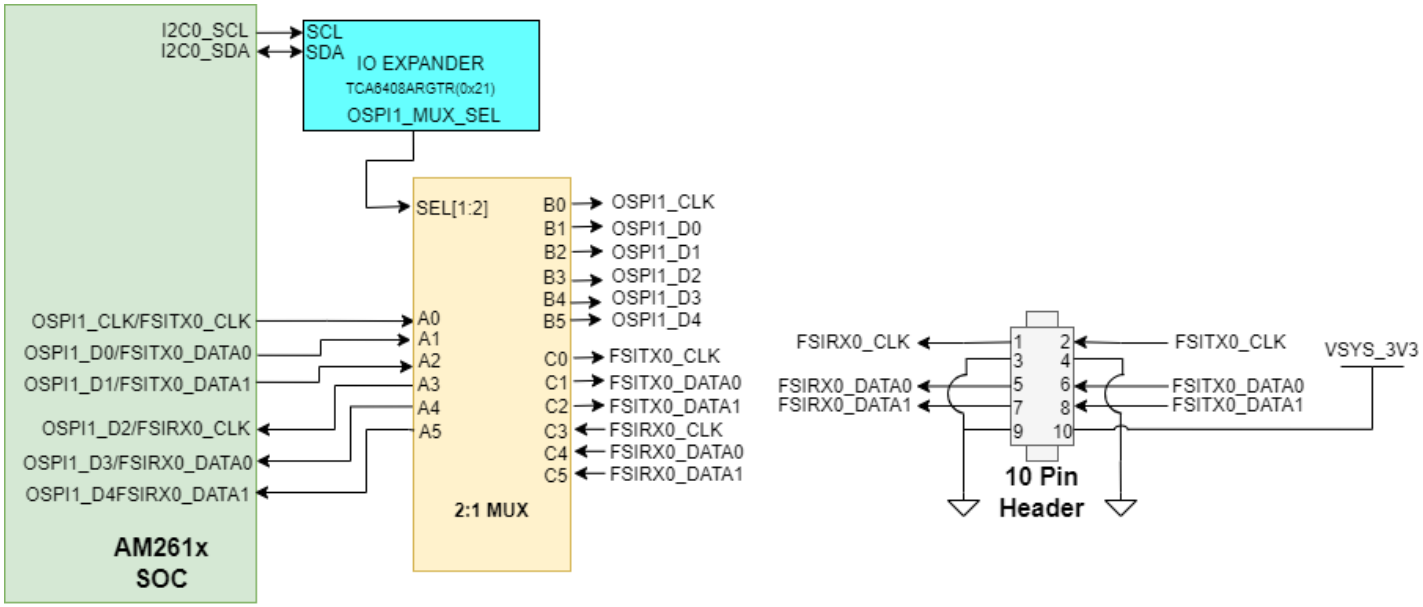

Figure 2-21. FSI 10-Pin Header

2.14 JTAG

The AM261x LaunchPad includes an XDS110 class onboard emulator. The LaunchPad includes all circuitry needed for XDS110 emulation. The emulator uses a USB 2.0 micro-b connector to interface the USB 2.0 signals that are created from the UART-USB bridge. The VBUS power from the connector is used to power the emulator circuit so that the connection to the emulator is not lost when power to the LaunchPad is removed. For more information on the XDS110 and the UART-USB bridge refer to UART

The XDS110 controls two power status LEDs. For more information on the Power Status LEDs refer to Power Status LEDs

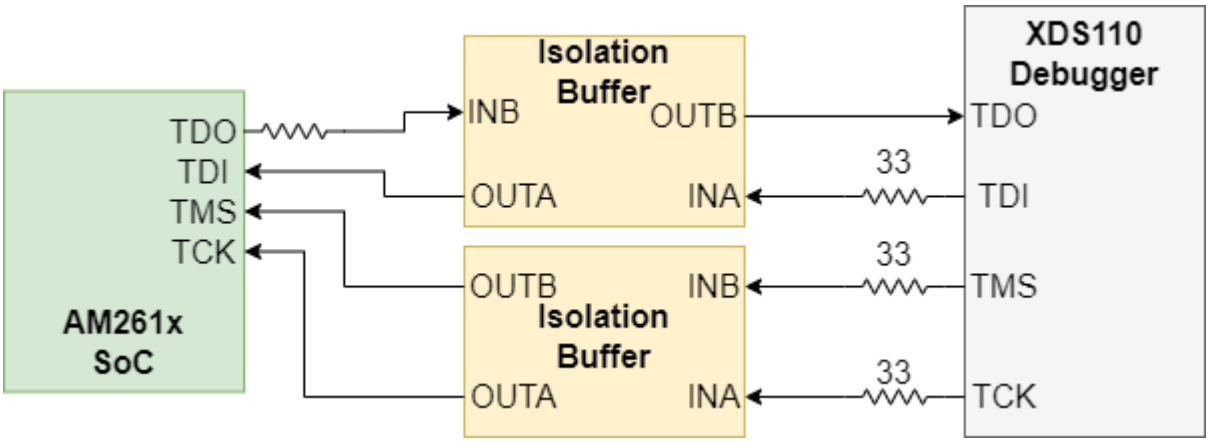

Figure 2-22. JTAG Interface to XDS110

2.15 TIVA and Test Automation Pin Mapping

The following table details the Test Automation mapping.

Table 2-10. Test Automation GPIO and I2C Mapping

Signal Name	Description	Direction
TA_POWERDOWNZ	When logic low, disables the 5V Supply	Output
TA_PORZ	When logic low, connects the PORz signal to ground due to PMOS V_{GS} being less than zero creating a power on reset to the MAIN domain	Output
TA_RESETZ	When logic low, connects the WARM RESETn signal to ground due to PMOS V_{GS} being less than zero creating a warm reset to the MAIN domain	Output
TA_GPIO1	When logic low, connects the INTn signal to ground due to PMOS V_{GS} being less than zero creating an interrupt to SoC	Output
TA_GPIO3	When logic low, disables the boot mode buffer output enable	Output
TA_GPIO4	Reset signal for boot mode IO Expander	Output
TA_I2C_SCL	I2C Clock signal used to communicate with bootmode IO expander to change the boot modes.	Output
TA_I2C_SDA	I2C Data signal used to communicate with bootmode IO expander to change the boot modes.	Output

2.16 LIN

The AM261x LaunchPad supports Local Interconnect Network communication with two LIN instances mapped to the BoosterPack header.

Note

The AM261x does **not** have an onboard LIN Transceiver

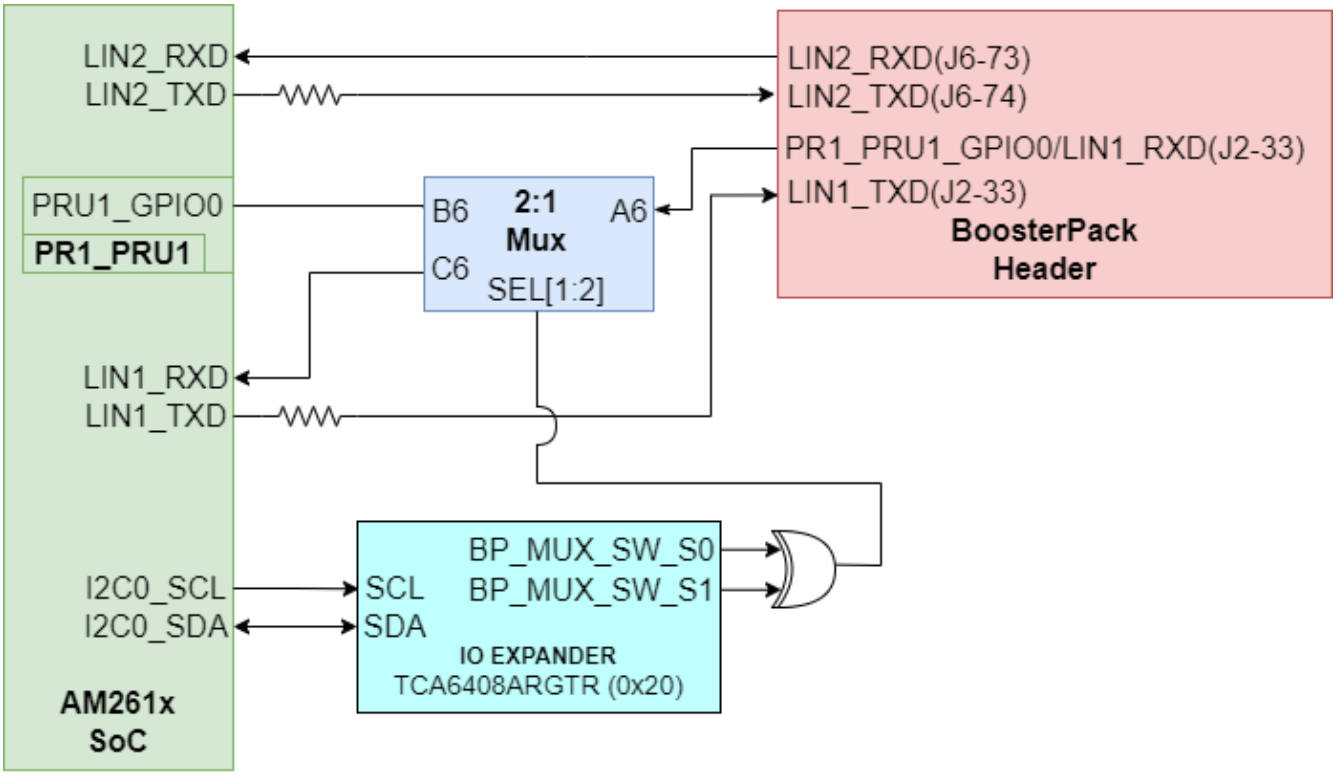

Figure 2-23. LIN Instances to BoosterPack Header

LIN2_TXD, LIN2_RXD and LIN1_RXD signals are directly routed to BoosterPack connectors. LIN1_TXD is going through a 2:1 mux and selection table is given below.

Table 2-11. LIN 2:1 Mux

BP_MUX_SW_S1	BP_MUX_SW_S0	Function of 2:1 Mux	Signals to BP Header
LOW	LOW	Port A ↔ Port C	LIN1_TX
LOW	HIGH	Port A ↔ Port B	PR1_PRU1_GPIO0
HIGH	LOW	Port A ↔ Port B	PR1_PRU1_GPIO0
HIGH	HIGH	Port A ↔ Port C	LIN1_TX

2.17 ADC and DAC

The AM261x LaunchPad maps 20 ADC inputs to the BoosterPack header. All of the ADC inputs that are used in the LaunchPad are ESD protected.

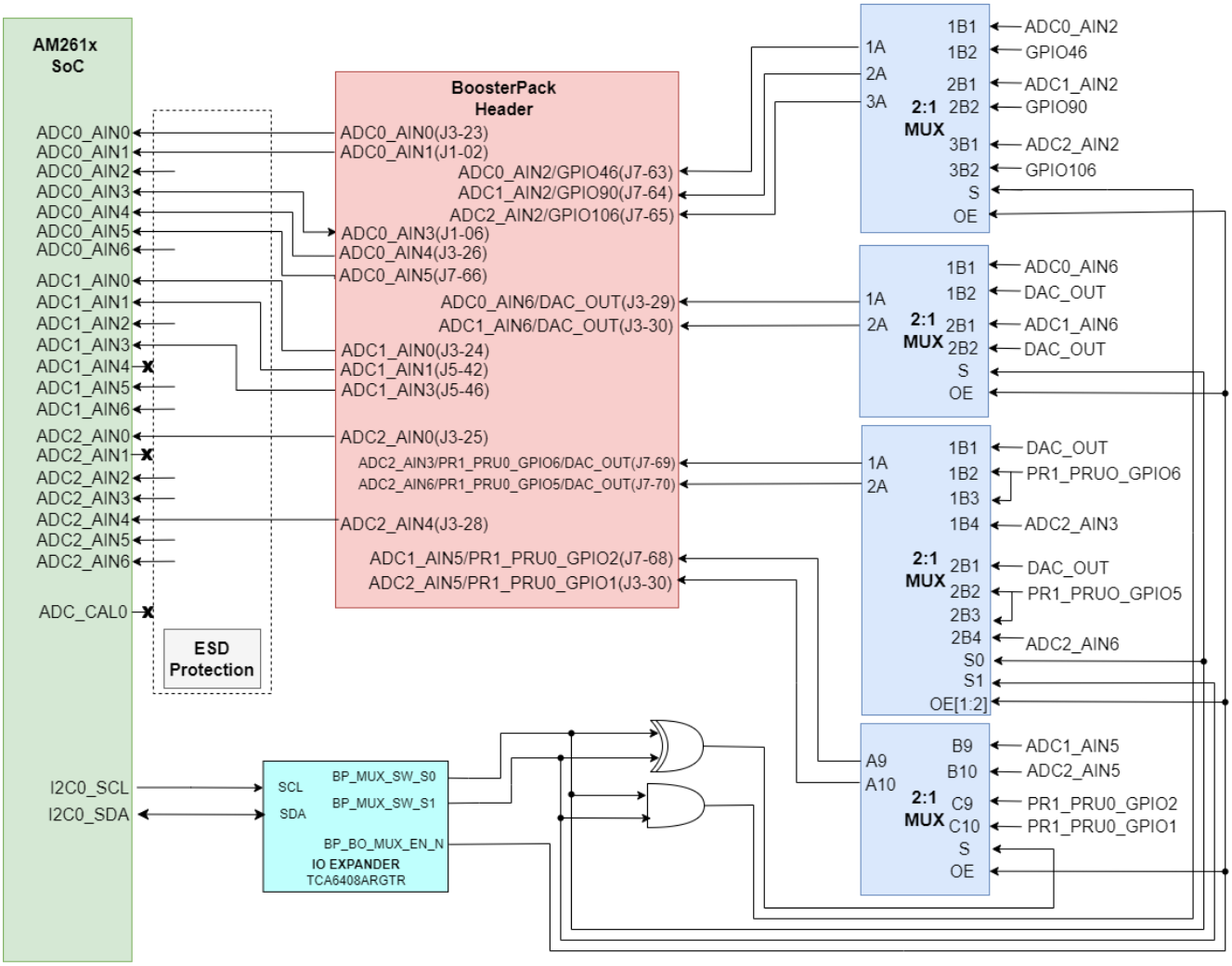

Figure 2-24. ADC/DAC Signal Pathing

Multiple muxes are involved from AM261x Soc to BoosterPack connectors. Detailed table is given in Boosterpack section.

The ADC and DAC require a voltage reference. The AM261x LaunchPad has two switches that allow the user to switch between the DAC and ADC VREF source.

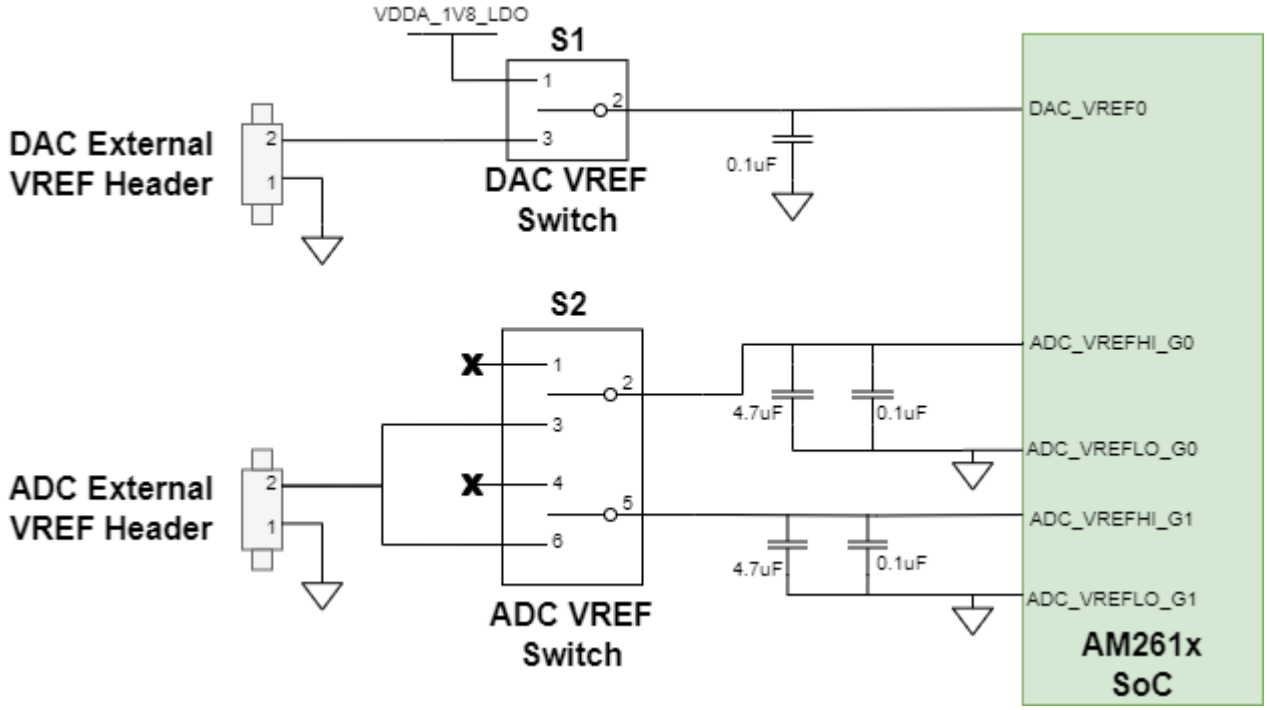

Figure 2-25. ADC and DAC VREF Switches

The DAC VREF Switch (S1) is a single pole double throw switch that controls the input of the ADC VREF inputs of the AM261x SoC.

Table 2-12. DAC VREF Switch

DAC VREF Switch Position	Reference Selection
Pin 1-2	AM261x on-die LDO
Pin 2-3	External DAC VREF Header

The ADC VREF Switch (S2) contains two single pole double throw switches that controls the input of the ADC VREF inputs of the AM261x SoC.

Table 2-13. ADC VREF Switch

ADC VREF Switch Position	Reference Selection
Pin 1-2	OPEN - Allow for reference to be AM261x on-die LDO reference
Pin 2-3	External ADC VREF Header
Pin 4-5	OPEN - Allow for reference to be AM261x on-die LDO reference
Pin 5-6	External ADC VREF Header

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2.18 EQEP and SDFM

The AM261x LaunchPad internally muxes the eQEP, FSI and OSPI1 signals. The eQEP0 instance of the AM261x are terminated to two headers (J19, J16). The eQEP1 instance of the AM261x are terminated to two headers (J18, J15).

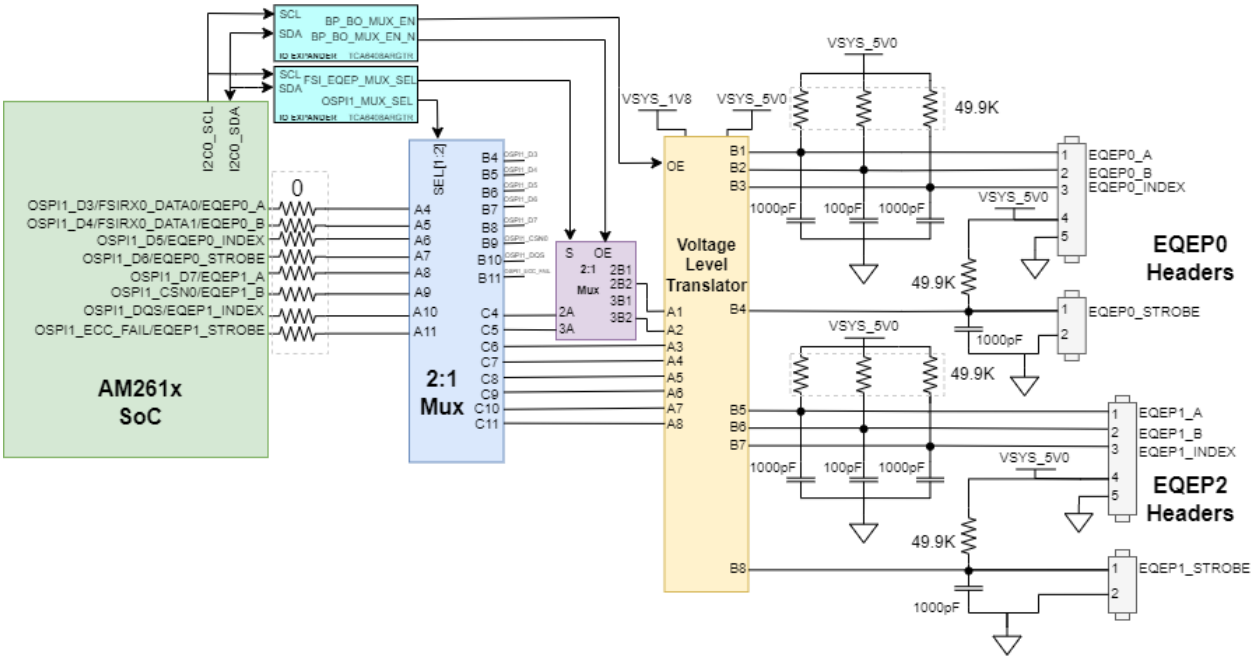

Figure 2-26. EQEP Signal Mapping

All eQEP signals have series termination resistors between the AM261x SoC and the Voltage Level Translator (TXB0108RGYR). The voltage level shifter is responsible for translating the 3.3V to 5V.

2.19 EPWM

The AM261x LaunchPad maps 12 PWM channels (6 PWM_A/B pairs) to the BoosterPack Header. Each EPWM signal has a series termination resistor. For the mapping of each EPWM signal refer to BoosterPack Header.

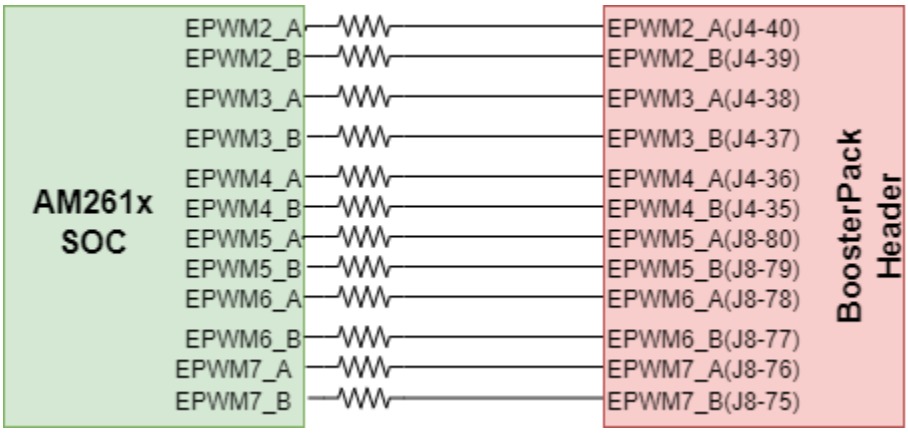

Figure 2-27. EPWM Signal Mapping to BoosterPack Header

2.20 USB

The USB interface of AM261x is routed to the USB2.0 Micro_AB Port and USB Type C port on the AM261x LaunchPad. USB signals from the connector routed to one of the ports of a 2:1 mux and the other port contains signals coming from the Type C power input, an IO expander is used to select between them.

AM261x supports USB DFU Bootmode. Boot mode selection and details are given in Bootmode

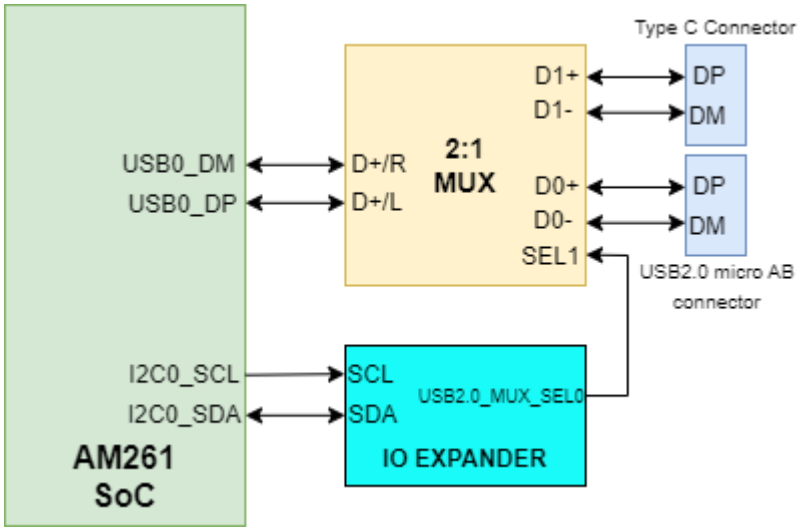

Figure 2-28. USB Connection

2.21 BoosterPack Headers

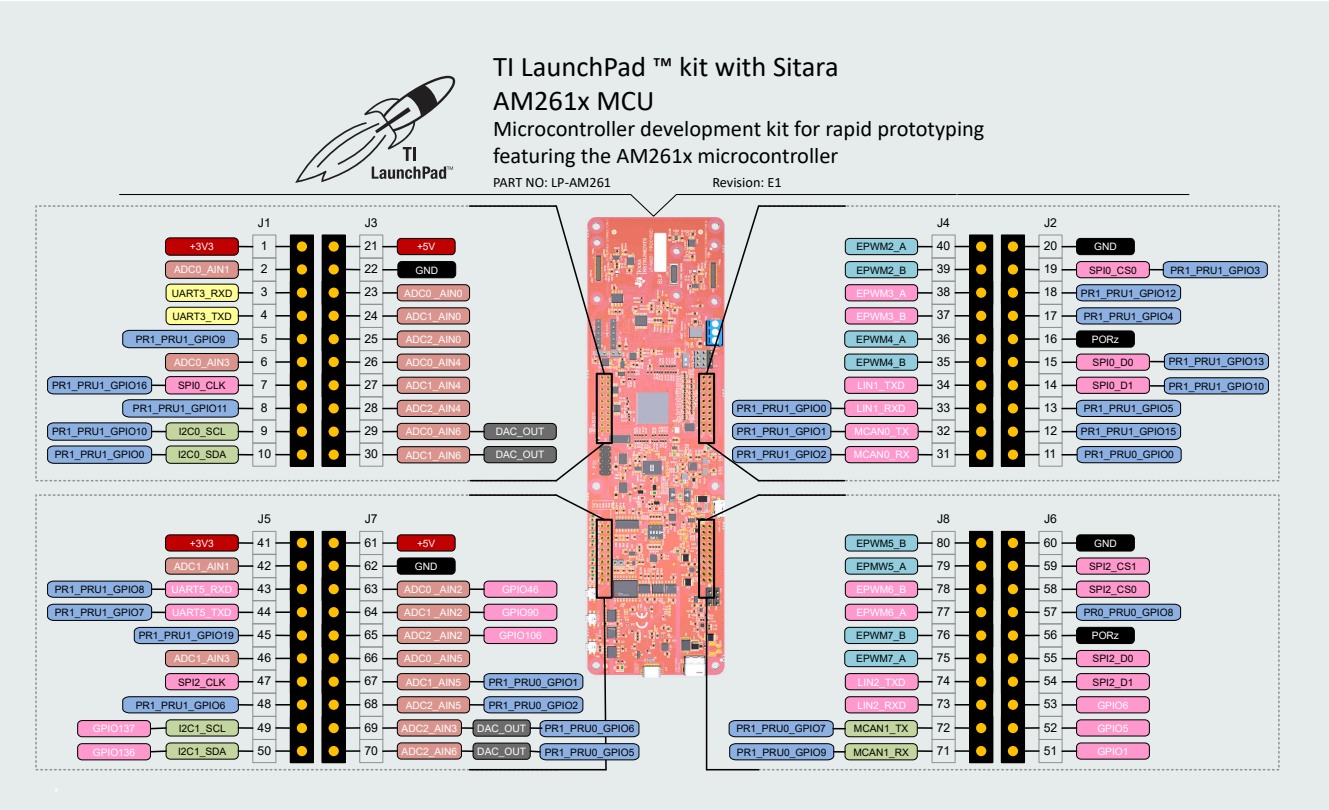

Figure 2-29. AM261x LaunchPad BoosterPack Pinout

Note

This pinout represents the default signals mapped to the BoosterPack Header. Additional signal options for each header are available through *Pinmux Mapping*. Two signals for one pin represents an externally muxed option

The AM261x LaunchPad supports two fully independent BoosterPack XL connectors. BoosterPack site #1 (J1/J3, J2/J4) is located in between the OSPI0 Flash and the micro-B USB Connector. BoosterPack site #2 (J5/J7, J6/J8) is located in between the OSPI0 Flash and the Ethernet port connectors. Each GPIO has multiple functions available through the GPIO mux. The signals connected from the SoC to the BoosterPack headers include:

- Various ADC inputs
- DAC outputs
- UART3 and UART5
- Various GPIO signals
- SPI0 and SPI2
- I2C0 and I2C1
- Various EPWM channels
- LIN1 and LIN2
- MCAN0 and MCAN1

BoosterPack Modes

The AM261x LaunchPad is intended to be compatible with mainly the below 4 Booster Packs, which have different pin out.

- Standard LaunchPad Booster Pack as per https://www.ti.com/lit/ml/slat157/slat157.pdf

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- BP-AM2BLDCSERVO
- BOOSTXL-IOLINKM-8
- Standard C2000 DRVx Booster Packs

Thus the LP-AM261x uses different Muxes to enable selection of different AM261x nets to be brought out on the Booster Pack Headers as per different modes as shown below Table.

The modes of the BoosterPack are controlled using select lines with nets BP_MUX_SW_S1 and BP_MUX_SW_S0 as per the schematic.

When the "Selected Net" is blank, it means that pin has no muxing and the only single net(in the Booster Pack Net Name) is always selected.

- Mode 00 enables Standard LaunchPad BoosterPack Connections and details are captured in below tables

Table 2-14. Mode 00 : Standard LaunchPad BoosterPack (J1/J3)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
VSYS_3V3_BP	VSYS_3V3_BP	1	21	VSYS_5V0_BP_1	VSYS_5V0_BP_1
ADC0_AIN1	ADC0_AIN1	2	22	GND	GND
UART3_RXD	UART3_RXD	3	23	ADC0_AIN0	ADC0_AIN0
UART3_TXD	UART3_TXD	4	24	ADC1_AIN0	ADC1_AIN0
PR1_PRU1_GPIO9	PR1_PRU1_GPIO9	5	25	ADC2_AIN0	ADC2_AIN0
ADC0_AIN3	ADC0_AIN3	6	26	ADC0_AIN4	ADC0_AIN4
SPI0_CLK	SPI0_CLK/PR1_PRU1_GPIO16	7	27	ADC1_AIN4	ADC1_AIN4
PR1_PRU1_GPIO11	PR1_PRU1_GPIO11	8	28	ADC2_AIN4	ADC2_AIN4
I2C0_SCL	I2C0_SCL/PR1_PRU1_GPIO10	9	29	DAC_OUT/ADC0_AIN6	DAC_OUT
I2C0_SDA	I2C0_SDA/PR1_PRU1_GPIO0	10	30	DAC_OUT/ADC1_AIN6	DAC_OUT

Table 2-15. Mode 00 : Standard LaunchPad BoosterPack (J2/J4)

Selected net	BoosterPack Net Name	J2	J4	BoosterPack Net Name	Selected net
EPWM2_A	EPWM2_A	40	20	GND	GND
EPWM2_B	EPWM2_B	39	19	SPI0_CS0/PR1_PRU1_GPIO3	SPI0_CS0
EPWM3_A	EPWM3_A	38	18	PR1_PRU1_GPIO12	PR1_PRU1_GPIO12
EPWM3_B	EPWM3_B	37	17	PR1_PRU1_GPIO4	PR1_PRU1_GPIO4
EPWM4_A	EPWM4_A	36	16	PORZ	PORZ
EPWM4_B	EPWM4_B	35	15	SPI0_D0/PR1_PRU1_GPIO13	SPI0_D0
LIN1_TXD	LIN1_TXD	34	14	SPI0_D1/PR1_PRU1_GPIO10	SPI0_D1
LIN1_RXD	LIN1_RXD/PR1_PRU1_GPIO0	33	13	PR1_PRU1_GPIO5	PR1_PRU1_GPIO5
MCAN0_TX	MCAN0_TX/PR1_PRU1_GPIO1	32	12	PR1_PRU1_GPIO15	PR1_PRU1_GPIO15
MCAN0_RX	MCAN0_RX/PR1_PRU1_GPIO2	31	11	PR1_PRU0_GPIO0	PR1_PRU0_GPIO0

Table 2-16. Mode 00 : Standard LaunchPad BoosterPack (J5/J7)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
VSYS_3V3_BP	VSYS_3V3_BP	41	61	VSYS_5V0_BP_2	VSYS_5V0_BP_2
ADC1_AIN1	ADC1_AIN1	42	62	GND	GND
UART5_RXD	UART5_RXD/PR1_PRU1_GPIO8	43	63	ADC0_AIN2/GPIO46	ADC0_AIN2
PR1_PRU1_GPIO2	UART5_TXD/PR1_PRU1_GPIO7	44	64	ADC1_AIN2/GPIO90	ADC1_AIN2
PR1_PRU1_GPIO19	PR1_PRU1_GPIO19	45	65	ADC2_AIN2/GPIO106	ADC2_AIN2

Table 2-16. Mode 00 : Standard LaunchPad BoosterPack (J5/J7) (continued)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
ADC1_AIN3	ADC1_AIN3	46	66	ADC0_AIN5	ADC0_AIN5
SPI2_CLK	SPI2_CLK	47	67	ADC1_AIN5/PR1_PRU0_GPIO1	ADC1_AIN5
PR1_PRU1_GPIO6	PR1_PRU1_GPIO6	48	68	ADC2_AIN5/PR1_PRU0_GPIO2	ADC2_AIN5
I2C1_SCL	I2C1_SCL/GPIO137	49	69	DAC_OUT/PR1_PRU0_GPIO6/ ADC2_AIN3	DAC_OUT
I2C1_SDA	I2C1_SDA/GPIO136	50	70	DAC_OUT/PR1_PRU1_GPIO5/ ADC2_AIN6	DAC_OUT

Table 2-17. Mode 00 : Standard LaunchPad BoosterPack (J6/J8)

Selected net	BoosterPack Net Name	J6	J8	BoosterPack Net Name	Selected net
EPWM5_A	EPWM5_A	80	60	GND	GND
EPWM5_B	EPWM5_B	79	59	SPI2_CS1	SPI2_CS1
EPWM6_A	EPWM6_A	78	58	SPI2_CS0	SPI2_CS0
EPWM6_B	EPWM6_B	77	57	PR1_PRU0_GPIO8	PR1_PRU0_GPIO8
EPWM7_A	EPWM7_A	76	56	PORZ	PORZ
EPWM7_B	EPWM7_B	75	55	SPI2_D0	SPI2_D0
LIN2_TXD	LIN2_TXD	74	54	SPI2_D1	SPI2_D1
LIN2_RXD	LIN2_RXD	73	53	GPIO6	GPIO6
MCAN1_TX	MCAN1_TX/PR1_PRU0_GPIO7	72	52	GPIO5	GPIO5
MCAN1_RX	MCAN1_RX/PR1_PRU0_GPIO9	71	51	GPIO1	GPIO1

- Mode 01 enables BP-AM2BLDCSERVO BoosterPack Connections and details are captured in below tables.

Table 2-18. Mode 01: BP-AM2BLDCSERVO (J1/J3)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
VSYS_3V3_BP	VSYS_3V3_BP	1	21	VSYS_5V0_BP_1	VSYS_5V0_BP_1
ADC0_AIN1	ADC0_AIN1	2	22	GND	GND
UART3_RXD	UART3_RXD	3	23	ADC0_AIN0	ADC0_AIN0
UART3_TXD	UART3_TXD	4	24	ADC1_AIN0	ADC1_AIN0
PR1_PRU1_GPIO9	PR1_PRU1_GPIO9	5	25	ADC2_AIN0	ADC2_AIN0
ADC0_AIN3	ADC0_AIN3	6	26	ADC0_AIN4	ADC0_AIN4
PR1_PRU1_GPIO16	SPI0_CLK/PR1_PRU1_GPIO16	7	27	ADC1_AIN4	ADC1_AIN4
PR1_PRU1_GPIO11	PR1_PRU1_GPIO11	8	28	ADC2_AIN4	ADC2_AIN4
PR1_PRU1_GPIO10	I2C0_SCL/PR1_PRU1_GPIO10	9	29	DAC_OUT/ADC0_AIN6	ADC0_AIN6
PR1_PRU1_GPIO0	I2C0_SDA/PR1_PRU1_GPIO0	10	30	DAC_OUT/ADC1_AIN6	ADC1_AIN6

Table 2-19. Mode 01 : BP-AM2BLDCSERVO (J2/J4)

Selected net	BoosterPack Net Name	J2	J4	BoosterPack Net Name	Selected net
EPWM2_A	EPWM2_A	40	20	GND	GND
EPWM2_B	EPWM2_B	39	19	SPI0_CS0/PR1_PRU1_GPIO3	PR1_PRU1_GPIO3
EPWM3_A	EPWM3_A	38	18	PR1_PRU1_GPIO12	PR1_PRU1_GPIO12
EPWM3_B	EPWM3_B	37	17	PR1_PRU1_GPIO4	PR1_PRU1_GPIO4

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Table 2-19. Mode 01 : BP-AM2BLDCSERVO (J2/J4) (continued)

Selected net	BoosterPack Net Name	J2	J4	BoosterPack Net Name	Selected net
EPWM4_A	EPWM4_A	36	16	PORZ	PORZ
EPWM4_B	EPWM4_B	35	15	SPI0_D0/PR1_PRU1_GPIO13	PR1_PRU1_GPIO13
LIN1_TXD	LIN1_TXD	34	14	SPI0_D1/PR1_PRU1_GPIO10	PR1_PRU1_GPIO10
PR1_PRU1_GPIO0	LIN1_RXD/PR1_PRU1_GPIO0	33	13	PR1_PRU1_GPIO5	PR1_PRU1_GPIO5
PR1_PRU1_GPIO1	MCAN0_TX/PR1_PRU1_GPIO1	32	12	PR1_PRU1_GPIO15	PR1_PRU1_GPIO15
PR1_PRU1_GPIO2	MCAN0_RX/PR1_PRU1_GPIO2	31	11	PR1_PRU0_GPIO0	PR1_PRU0_GPIO0

Table 2-20. Mode 01 : BP-AM2BLDCSERVO (J5/J7)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
VSYS_3V3_BP	VSYS_3V3_BP	41	61	VSYS_5V0_BP_2	VSYS_5V0_BP_2
ADC1_AIN1	ADC1_AIN1	42	62	GND	GND
LIN1_TXD/ PR1_PRU1_GPIO8	UART5_RXD/PR1_PRU1_GPIO8	43	63	ADC0_AIN2/GPIO46	ADC0_AIN2
PR1_PRU1_GPIO7	UART5_TXD/PR1_PRU1_GPIO7	44	64	ADC1_AIN2/GPIO90	ADC1_AIN2
PR1_PRU1_GPIO19	PR1_PRU1_GPIO19	45	65	ADC2_AIN2/GPIO106	ADC2_AIN2
ADC1_AIN3	ADC1_AIN3	46	66	ADC0_AIN5	ADC0_AIN5
SPI2_CLK	SPI2_CLK	47	67	ADC1_AIN5/PR1_PRU0_GPIO1	PR1_PRU0_GPIO1
PR1_PRU1_GPIO6	PR1_PRU1_GPIO6	48	68	ADC2_AIN5/PR1_PRU0_GPIO2	PR1_PRU0_GPIO2
I2C1_SCL	I2C1_SCL/GPIO137	49	69	DAC_OUT/PR1_PRU0_GPIO6/ ADC2_AIN3	PR1_PRU0_GPIO6
I2C1_SDA	I2C1_SDA/GPIO136	50	70	DAC_OUT/PR1_PRU1_GPIO5/ ADC2_AIN6	PR1_PRU0_GPIO5

Table 2-21. Mode 01 : BP-AM2BLDCSERVO (J6/J8)

Selected net	BoosterPack Net Name	J6	J8	BoosterPack Net Name	Selected net
EPWM5_A	EPWM5_A	80	60	GND	GND
EPWM5_B	EPWM5_B	79	59	SPI2_CS1	SPI2_CS1
EPWM6_A	EPWM6_A	78	58	SPI2_CS0	SPI2_CS0
EPWM6_B	EPWM6_B	77	57	PR1_PRU0_GPIO8	PR1_PRU0_GPIO8
EPWM7_A	EPWM7_A	76	56	PORZ	PORZ
EPWM7_B	EPWM7_B	75	55	SPI2_D0	SPI2_D0
LIN2_TXD	LIN2_TXD	74	54	SPI2_D1	SPI2_D1
LIN2_RXD	LIN2_RXD	73	53	GPIO6	GPIO6
PR1_PRU0_GPIO7	MCAN1_TX/PR1_PRU0_GPIO7	72	52	GPIO5	GPIO5
PR1_PRU0_GPIO9	MCAN1_RX/PR1_PRU0_GPIO9	71	51	GPIO1	GPIO1

- Mode 10 enables BOOSTXL-IOLINKM-8 BoosterPack Connections and details are captured in below tables

Table 2-22. Mode 10: BOOSTXL-IOLINKM-8 (J1/J3)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
VSYS_3V3_BP	VSYS_3V3_BP	1	21	VSYS_5V0_BP_1	VSYS_5V0_BP_1
ADC0_AIN1	ADC0_AIN1	2	22	GND	GND
UART3_RXD	UART3_RXD	3	23	ADC0_AIN0	ADC0_AIN0

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Table 2-22. Mode 10: BOOSTXL-IOLINKM-8 (J1/J3) (continued)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
UART3_TXD	UART3_TXD	4	24	ADC1_AIN0	ADC1_AIN0
PR1_PRU1_GPIO9	PR1_PRU1_GPIO9	5	25	ADC2_AIN0	ADC2_AIN0
ADC0_AIN3	ADC0_AIN3	6	26	ADC0_AIN4	ADC0_AIN4
PR1_PRU1_GPIO16	SPI0_CLK/PR1_PRU1_GPIO16	7	27	ADC1_AIN4	ADC1_AIN4
PR1_PRU1_GPIO11	PR1_PRU1_GPIO11	8	28	ADC2_AIN4	ADC2_AIN4
I2C0_SCL	I2C0_SCL/PR1_PRU1_GPIO10	9	29	DAC_OUT/ADC0_AIN6	DAC_OUT
I2C0_SDA	I2C0_SDA/PR1_PRU1_GPIO0	10	30	DAC_OUT/ADC1_AIN6	DAC_OUT

Table 2-23. Mode 10 : BOOSTXL-IOLINKM-8 (J2/J4)

Selected net	BoosterPack Net Name	J2	J4	BoosterPack Net Name	Selected net
EPWM2_A	EPWM2_A	40	20	GND	GND
EPWM2_B	EPWM2_B	39	19	SPI0_CS0/PR1_PRU1_GPIO3	PR1_PRU1_GPIO3
EPWM3_A	EPWM3_A	38	18	PR1_PRU1_GPIO12	PR1_PRU1_GPIO12
EPWM3_B	EPWM3_B	37	17	PR1_PRU1_GPIO4	PR1_PRU1_GPIO4
EPWM4_A	EPWM4_A	36	16	PORZ	PORZ
EPWM4_B	EPWM4_B	35	15	SPI0_D0/PR1_PRU1_GPIO13	PR1_PRU1_GPIO13
LIN1_TXD	LIN1_TXD	34	14	SPI0_D1/PR1_PRU1_GPIO10	PR1_PRU1_GPIO10
PR1_PRU1_GPIO0	LIN1_RXD/PR1_PRU1_GPIO0	33	13	PR1_PRU1_GPIO5	PR1_PRU1_GPIO5
PR1_PRU1_GPIO1	MCAN0_TX/PR1_PRU1_GPIO1	32	12	PR1_PRU1_GPIO15	PR1_PRU1_GPIO15
PR1_PRU1_GPIO2	MCAN0_RX/PR1_PRU1_GPIO2	31	11	PR1_PRU0_GPIO0	PR1_PRU0_GPIO0

Table 2-24. Mode 10 : BOOSTXL-IOLINKM-8 (J5/J7)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
VSYS_3V3_BP	VSYS_3V3_BP	41	61	VSYS_5V0_BP_2	VSYS_5V0_BP_2
ADC1_AIN1	ADC1_AIN1	42	62	GND	GND
LIN1_TXD/ PR1_PRU1_GPIO8	UART5_RXD/PR1_PRU1_GPIO8	43	63	ADC0_AIN2/GPIO46	GPIO46
PR1_PRU1_GPIO7	UART5_TXD/PR1_PRU1_GPIO7	44	64	ADC1_AIN2/GPIO90	GPIO90
PR1_PRU1_GPIO19	PR1_PRU1_GPIO19	45	65	ADC2_AIN2/GPIO106	GPIO106
ADC1_AIN3	ADC1_AIN3	46	66	ADC0_AIN5	ADC0_AIN5
SPI2_CLK	SPI2_CLK	47	67	ADC1_AIN5/PR1_PRU0_GPIO1	PR1_PRU0_GPIO1
PR1_PRU1_GPIO6	PR1_PRU1_GPIO6	48	68	ADC2_AIN5/PR1_PRU0_GPIO2	PR1_PRU0_GPIO2
GPIO137	I2C1_SCL/GPIO137	49	69	DAC_OUT/PR1_PRU0_GPIO6/ ADC2_AIN3	PR1_PRU0_GPIO6
GPIO136	I2C1_SDA/GPIO136	50	70	DAC_OUT/PR1_PRU1_GPIO5/ ADC2_AIN6	PR1_PRU0_GPIO5

Table 2-25. Mode 10 : BOOSTXL-IOLINKM-8 (J6/J8)

Selected net	BoosterPack Net Name	J6	J8	BoosterPack Net Name	Selected net
EPWM5_A	EPWM5_A	80	60	GND	GND
EPWM5_B	EPWM5_B	79	59	SPI2_CS1	SPI2_CS1
EPWM6_A	EPWM6_A	78	58	SPI2_CS0	SPI2_CS0

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Table 2-25. Mode 10 : BOOSTXL-IOLINKM-8 (J6/J8) (continued)

Selected net	BoosterPack Net Name	J6	J8	BoosterPack Net Name	Selected net
EPWM6_B	EPWM6_B	77	57	PR1_PRU0_GPIO8	PR1_PRU0_GPIO8
EPWM7_A	EPWM7_A	76	56	PORZ	PORZ
EPWM7_B	EPWM7_B	75	55	SPI2_D0	SPI2_D0
LIN2_TXD	LIN2_TXD	74	54	SPI2_D1	SPI2_D1
LIN2_RXD	LIN2_RXD	73	53	GPIO6	GPIO6
PR1_PRU0_GPIO7	MCAN1_TX/PR1_PRU0_GPIO7	72	52	GPIO5	GPIO5
PR1_PRU0_GPIO9	MCAN1_RX/PR1_PRU0_GPIO9	71	51	GPIO1	GPIO1

- Mode 11 enables Standard C2000 DRVx BoosterPack Connections and details are captured in below tables

Table 2-26. Mode 11 : Standard C2000 DRVx Booster Packs (J1/J3)

Selected net	BoosterPack Net Name	J1	J3	BoosterPack Net Name	Selected net
VSYS_3V3_BP	VSYS_3V3_BP	1	21	VSYS_5V0_BP_1	VSYS_5V0_BP_1
ADC0_AIN1	ADC0_AIN1	2	22	GND	GND
UART3_RXD	UART3_RXD	3	23	ADC0_AIN0	ADC0_AIN0
UART3_TXD	UART3_TXD	4	24	ADC1_AIN0	ADC1_AIN0
PR1_PRU1_GPIO9	PR1_PRU1_GPIO9	5	25	ADC2_AIN0	ADC2_AIN0
ADC0_AIN3	ADC0_AIN3	6	26	ADC0_AIN4	ADC0_AIN4
SPI0_CLK	SPI0_CLK/PR1_PRU1_GPIO16	7	27	ADC1_AIN4	ADC1_AIN4
PR1_PRU1_GPIO11	PR1_PRU1_GPIO11	8	28	ADC2_AIN4	ADC2_AIN4
PR1_PRU1_GPIO10	I2C0_SCL/PR1_PRU1_GPIO10	9	29	DAC_OUT/ADC0_AIN6	ADC0_AIN6
PR1_PRU1_GPIO0	I2C0_SDA/PR1_PRU1_GPIO0	10	30	DAC_OUT/ADC1_AIN6	ADC1_AIN6

Table 2-27. Mode 11 : Standard C2000 DRVx Booster Packs (J2/J4)

Selected net	BoosterPack Net Name	J2	J4	BoosterPack Net Name	Selected net
EPWM2_A	EPWM2_A	40	20	GND	GND
EPWM2_B	EPWM2_B	39	19	SPI0_CS0/PR1_PRU1_GPIO3	SPI0_CS0
EPWM3_A	EPWM3_A	38	18	PR1_PRU1_GPIO12	PR1_PRU1_GPIO12
EPWM3_B	EPWM3_B	37	17	PR1_PRU1_GPIO4	PR1_PRU1_GPIO4
EPWM4_A	EPWM4_A	36	16	PORZ	PORZ
EPWM4_B	EPWM4_B	35	15	SPI0_D0/PR1_PRU1_GPIO13	SPI0_D0
LIN1_TXD	LIN1_TXD	34	14	SPI0_D1/PR1_PRU1_GPIO10	SPI0_D1
LIN1_RXD	LIN1_RXD/PR1_PRU1_GPIO0	33	13	PR1_PRU1_GPIO5	PR1_PRU1_GPIO5
MCAN0_TX	MCAN0_TX/PR1_PRU1_GPIO1	32	12	PR1_PRU1_GPIO15	PR1_PRU1_GPIO15
MCAN0_RX	MCAN0_RX/PR1_PRU1_GPIO2	31	11	PR1_PRU0_GPIO0	PR1_PRU0_GPIO0

Table 2-28. Mode 11 : Standard C2000 DRVx Booster Packs (J5/J7)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
VSYS_3V3_BP	VSYS_3V3_BP	41	61	VSYS_5V0_BP_2	VSYS_5V0_BP_2
ADC1_AIN1	ADC1_AIN1	42	62	GND	GND
UART5_RXD	UART5_RXD/PR1_PRU1_GPIO8	43	63	ADC0_AIN2/GPIO46	GPIO46
PR1_PRU1_GPIO2	UART5_TXD/PR1_PRU1_GPIO7	44	64	ADC1_AIN2/GPIO90	GPIO90

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Table 2-28. Mode 11 : Standard C2000 DRVx Booster Packs (J5/J7) (continued)

Selected net	BoosterPack Net Name	J5	J7	BoosterPack Net Name	Selected net
PR1_PRU1_GPIO19	PR1_PRU1_GPIO19	45	65	ADC2_AIN2/GPIO106	GPIO106
ADC1_AIN3	ADC1_AIN3	46	66	ADC0_AIN5	ADC0_AIN5
SPI2_CLK	SPI2_CLK	47	67	ADC1_AIN5/PR1_PRU0_GPIO1	ADC1_AIN5
PR1_PRU1_GPIO6	PR1_PRU1_GPIO6	48	68	ADC2_AIN5/PR1_PRU0_GPIO2	ADC2_AIN5
GPIO137	I2C1_SCL/GPIO137	49	69	DAC_OUT/PR1_PRU0_GPIO6/ ADC2_AIN3	ADC2_AIN3
GPIO136	I2C1_SDA/GPIO136	50	70	DAC_OUT/PR1_PRU1_GPIO5/ ADC2_AIN6	ADC2_AIN6

Table 2-29. Mode 11 : Standard C2000 DRVx Booster Packs (J6/J8)

Selected net	BoosterPack Net Name	J6	J8	BoosterPack Net Name	Selected net
EPWM5_A	EPWM5_A	80	60	GND	GND
EPWM5_B	EPWM5_B	79	59	SPI2_CS1	SPI2_CS1
EPWM6_A	EPWM6_A	78	58	SPI2_CS0	SPI2_CS0
EPWM6_B	EPWM6_B	77	57	PR1_PRU0_GPIO8	PR1_PRU0_GPIO8
EPWM7_A	EPWM7_A	76	56	PORZ	PORZ
EPWM7_B	EPWM7_B	75	55	SPI2_D0	SPI2_D0
LIN2_TXD	LIN2_TXD	74	54	SPI2_D1	SPI2_D1
LIN2_RXD	LIN2_RXD	73	53	GPIO6	GPIO6
MCAN1_TX	MCAN1_TX/PR1_PRU0_GPIO7	72	52	GPIO5	GPIO5
MCAN1_RX	MCAN1_RX/PR1_PRU0_GPIO9	71	51	GPIO1	GPIO1

3 Known Issues and modifications done on LP-AM261 RevE1

The below issues were identified in LP-AM261 RevE1. The details of modifications needed for all these issues are also captured. **All these modifications are already made on all the LP-AM261 RevE1 boards ordered from ti.com**.

3.1 TA_POWERDOWNz pulled up by VSYS_TA_3V3 which is powered by VSYS_3V3

The TA_POWERDOWNz which enables the input power load switch to enable the system VSYS_5V0 power is pulled up using VSYS_3V3. Since VSYS_3V3 is itself derived from VSYS_5V0, the LP-AM261 RevE1 does not power on in default configuration.

Modification: The VSYS_TA_3V3 needs to be powered from power source other than that from PMIC. Hence an LDO is soldered which generates 3.3V from VSYS_5V0 and pulls up TA_POWERDOWNz to 3.3V.

3.2 USB2.0_MUX_SEL0 pulled up by R355

The USB2.0_MUX_SEL0 net is pulled up by R355, which makes the USB signals from AM261x to be routed to USB-C connecter by default, than as intended to USB Micro-AB.

Modification: The resistor R355 is unmounted or made DNI.

3.3 MDIO and MDC of PRU0-ICSS0 needs to be routed to both Ethernet PHYs

The nets AM261_PR0_MDIO0_MDIO and AM261_PR0_MDIO0_MDC need to be connected to both Ethernet PHYs. In the current configuration

- Ethernet Phy 0 has muxed AM261_MDIO0_MDC, AM261_MDIO0_MDIO with AM261_PR**0**_MDIO0_MDC, AM261_PR**0**_MDIO0_MDIO connected.
- Ethernet Phy 1 has muxed AM261_MDIO0_MDC, AM261_MDIO0_MDIO with AM261_PR**1**_MDIO0_MDC, AM261_PR**1**_MDIO0_MDIO connected.

But the needed configuration is

- Both Ethernet Phy 0 and 1 should get muxed AM261_MDIO0_MDC, AM261_MDIO0_MDIO with AM261_PR**0**_MDIO0_MDC, AM261_PR**0**_MDIO0_MDIO nets.

Modification: For the above changes,

- R135 in series with AM261_PR1_MDIO0_MDIO – Unmount(DNP) R135
- R137 in series with AM261_PR1_MDIO0_MDC – Unmount(DNP) R137
- A blue wire from R167 Pin1 to R137 Pin1 should be connected.
- A blue wire from R180 Pin1 to R135 Pin1 should be connected.

3.4 AM261_RGMII1_RXLINK and AM261_RGMII2_RXLINK to be connected to GPIO

The pin 43 of both the Ethernet headers bring out AM261_RGMII1_RXLINK and AM261_RGMII2_RXLINK, which in the current implementation of LP-AM261x RevE1, this is just made a Test point. But these need to be connected to RX_LINK pins of respective PRU of AM261x.

Modification: For the above changes,

- PR0_PRU0_GPIO8(GPIO90) - pr0_mii0_rxlink - should connect to RX_LINK of Ethernet connector 0 (TP52).
- PR0_PRU1_GPIO8(GPIO106) - pr0_mii1_rxlink - should connect to RX_LINK of Ethernet connector 1 (TP46).

4 Additional Information

Trademarks

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4.1 Sitara MCU+ Academy

TI offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

5 References

5.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *Texas Instruments Code Composer Studio*
- *Updating XDS110 Firmware*
  - To find the serial number, only follow steps 1 and 2 of updating XDS110 firmware

5.2 Other TI Components Used in This Design

This LaunchPad uses various other TI components for its functions. A consolidated list of these components with links to their TI data sheets is shown below.

- *TUSB320USB Type-C Configuration Channel Logic and Port Controller*
- *TPD4E02B04 4-Channel ESD Protection Diode for USB Type-C*
- *TPS22965x-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch*
- *TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter*
- *TPS748 1.5-A Low-Dropout Linear Regulator*
- *TCA6408A Low-Voltage 8-Bit I 2C and SMBus I/O Expander*
- *SN74AVC4T245 Dual-Bit Bus Transceiver with Configurable Voltage Translation*
- *TPS22918-Q1, 5.5-V, 2-A, 52-mΩ On-Resistance Load Switch*
- *TPD6E001 Low-Capacitance 6-Channel ESD-Protection for High-Speed Data Interfaces*
- *XDS110 JTAG Debug Probe*
- *TS5A23159 1-Ω 2-Channel SPDT Analog Switch*
- *TCAN1044V-Q1 Automotive Fault-Protected CAN FD Transceiver*
- *DP83869HM High Immunity 10/100/1000 Ethernet Physical Layer Transceiver*
- *TS3DDR3812 12-Channel, 1:2 MUX/DEMUX Switch for DDR3 Applications*
- *TCA9617B Level-Translating I2C Bus Repeater*
- *SN74CB3Q3257 4-Bit 1-of-2 FET Multiplexer/Demultiplexer*
- *TPIC2810 8-Bit LED Driver with I2C Interface*
- *TPS796xx 1-A Low-Dropout Linear Regulators*
- *TXB0108 8-Bit Bidirectional Voltage-Level Translator with Auto-Direction Sensing*
- TCA6408ARGTR 8-bit translating 1.65- to 5.5-V I2C/SMBus I/O expander

5.3 Related Documentation From Texas Instruments

AM261x Documentation

- AM261x Data sheet
- AM261x Errata
- AM261x Technical Reference Manual
- AM261x Register Addendum
- AM261x Flash Selection Guide
- Submit Request for AM261x HSM Addendum here.

AM261x Software

- Sitara MCU+ Academy for AM261x - AM263x URL <---Start Here
- MCU-PLUS-SDK-AM261x - AM263x URL

AM261x Product Folders

- AM2614 Product Folder - AM263x URL
- AM2612 Product Folder - AM263x URL
- AM2611 Product Folder - AM263x URL

AM261x Evaluation Modules

- AM261x System on Module (TBD) - AM263x URL
- AM261x Control Card (TMDSCNCD261) - AM263x URL
- AM261x LaunchPad (LP-AM261)

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

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