EVM User's Guide: TMDSHSECDOCK263

TMDSHSECDOCK-AM263 User's Guide

Description

The AM263x controlCARD Docking Station (TMDSHSECDOCK-AM263) from Texas Instruments (TI) is intended to work primarily with the Sitara™ AM263x controlCARD (TMDSCNCD263), with support for the AM263Px controlCARD (TMDSCNCD263P).

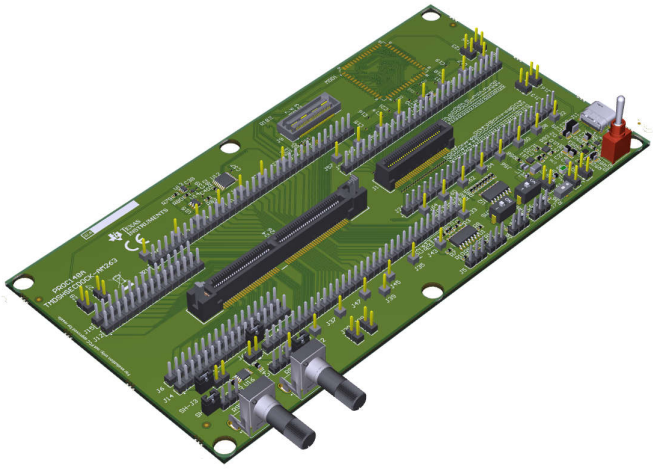
The AM263x controlCARD Docking Station expands on the capabilities of the AM263x/AM263Px controlCARDs by breaking out the controlCARD High Speed Edge Connector (HSEC) Inputs/Outputs (I/O) to user accessible pins, with additional I/O peripheral and PHYs to enhance the user experience of developing on the AM263x series of microcontrollers (MCUs).

The AM263x controlCARD Docking Station features a TI 14-pin JTAG connector, MIPI-60 connector with full JTAG and TRACE support, a two-channel CAN transceiver, a two-channel LIN transceiver, two variable resistors for ADC channel inputs with optional signal conditioning, a 64Mb Pseudo Static RAM (PSRAM) module, and full General Purpose Memory Controller (GPMC) pinout for use with other memory types supported by the AM263x GPMC peripheral (AM263x **only**). This user's guide describes the hardware details of the TMDSHSECDOCK-AM263.

Features

The AM263x controlCARD docking station has the following features:

- PCB dimensions: 7.86 inch (199.61 mm) x 3.76 inch (95.62 mm)
- Powered through 5V, 3A USB type-C input
- LED indicators for:
  - Power status
- 180-pin AM263x controlCARD compatible High Speed Edge Connector (HSEC)
- CAN connectivity with on-board 2-channel CAN transceiver
- LIN connectivity with on-board 2-channel LIN transceiver
- Two variable resistors for ADC channel inputs with optional signal conditioning
- 14-pin TI JTAG connector
- MIPI-60 pin connector with JTAG and full TRACE support
- On-Board Memory:
  - 64Mb PSRAM
  - 56-pin QFN-SMD pinout for AM263x SoC GPMC signals



1 Evaluation Module Overview

1.1 Introduction

The AM263x controlCARD Docking Station was developed to expand on the capabilities of the AM263x controlCARD and AM263Px controlCARD Evaluation Modules (EVM), and enable easy and rapid prototyping of the AM263x/AM263Px and their peripherals. There are several on-board transceivers and PHYs to enable the many interfaces of the AM263x and AM263Px SoC (System on a Chip). This user's guide details the design of the EVM and how to properly use each interface. The user's guide also details many important aspects of the board including but not limited to pin header descriptions, test points, and mux/switch signal routing.

1.1.1 Read This First

1.1.1.1 Sitara MCU+ Academy

Texas Instruments™ offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

1.1.1.2 Important Usage Notes

Note

The AM263x controlCARD Docking Station requires a 5V, 3A power supply to function. A USB type-C cable and 5V, 3A power supply are not included in the kit and must be ordered separately. The *Belkin USB-C Wall Charger* is known to work with the controlCARD and controlCARD Docking Station and USB type-C cable. For more information on power requirements refer to the Sitara MCU EVM and LaunchPad Power Supply Requirements FAQ.

Note

External Power Supply or Power Accessory Requirements:

- Nominal output voltage: 5-VDC
- Max output current: 3000 mA
- Efficiency Level V

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE,CCC,PSE, etc.

1.2 Kit Contents

The Sitara AM263x controlCARD Docking Station contains the following items:

- AM263x controlCARD Docking Station board
- 4 shunt jumpers

Not included:

- AM263x controlCARD (TMDSCNCD263)
- AM263Px controlCARD (TMDSCNCD263P)
- USB Type-C 5V/3A AC/DC supply and cable

2 Hardware Description

2.1 Component Identification

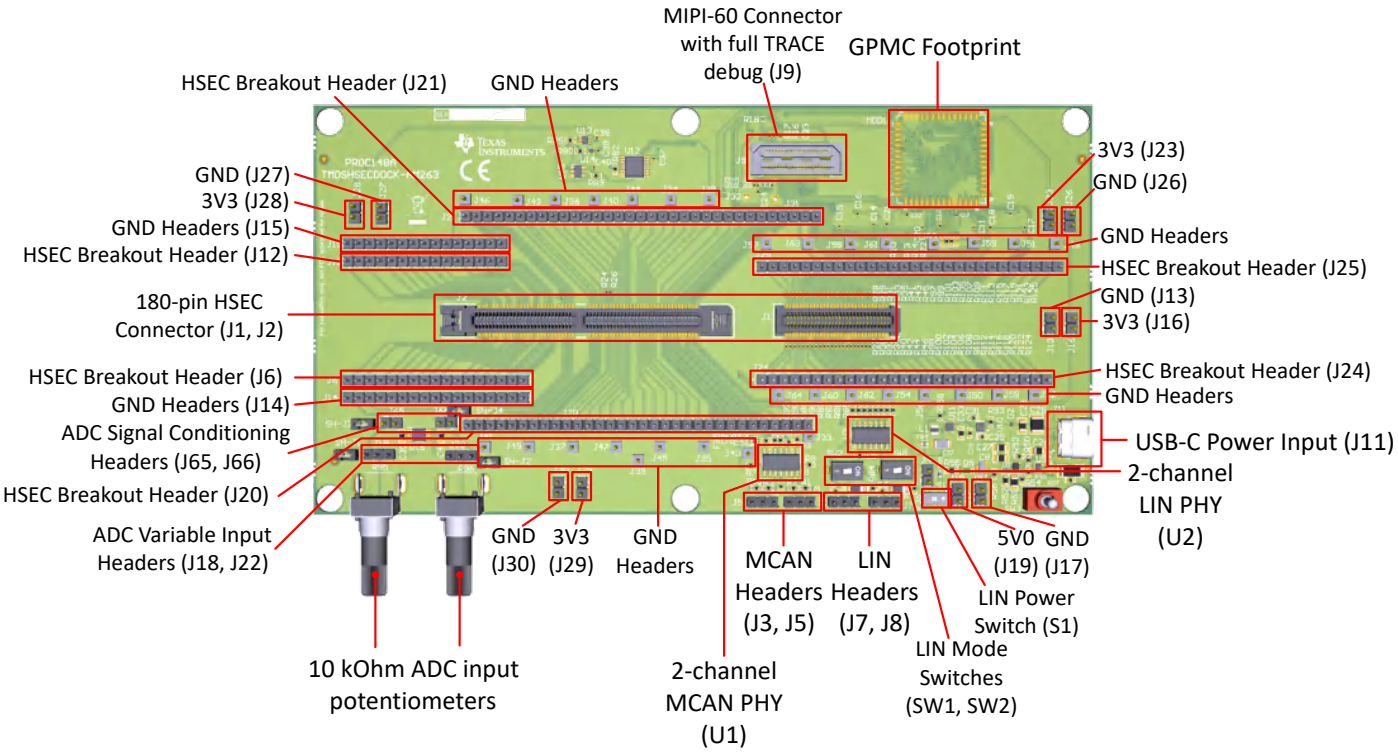


Figure 2-1. AM263x controlCARD Docking Station Top Component Identification

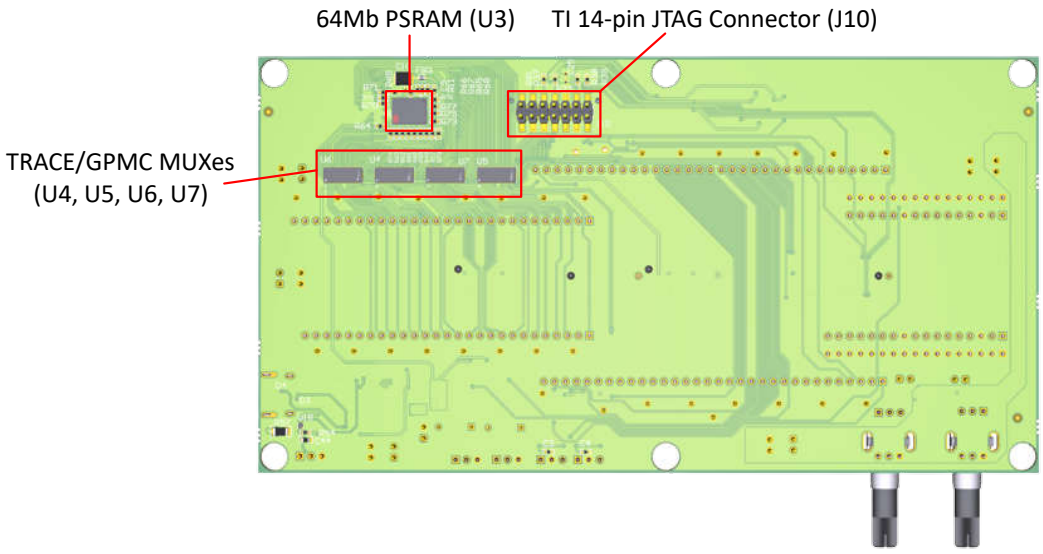


Figure 2-2. AM263x controlCARD Docking Station Bottom Component Identification

2.2 Power Requirements

The AM263x controlCARD Docking Station is powered from a 5 V, 3 A USB type-C input. The following sections describe the power distribution network topology that supply the AM263x controlCARD Docking Station, supporting components and the reference voltages.

Power supply designs that are compatible with the AM263x controlCARD Docking Station:

- When using the USB type-C input:
  - 5 V, 3 A power adapter with USB-C receptacle
  - 5 V, 3 A power adapter with captive USB-C cable
  - PC USB type-C port that has Power Delivery classification
    - Thunderbolt
    - Battery behind USB logo

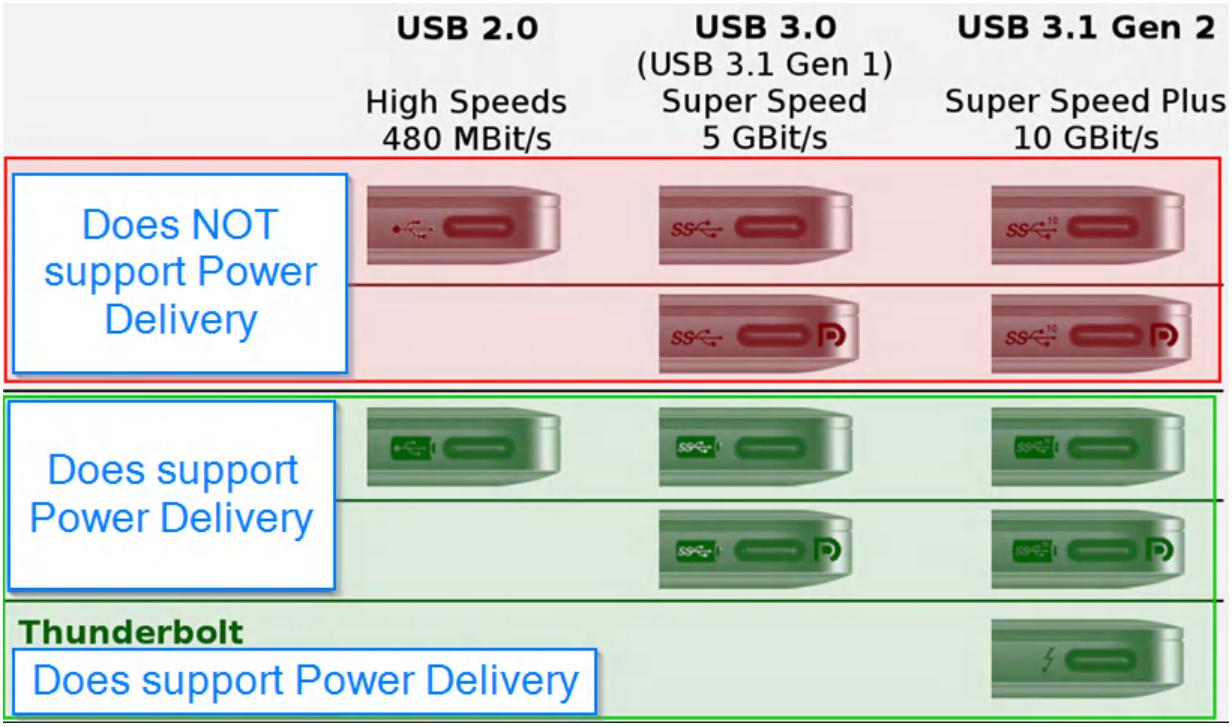


Figure 2-3. USB Type-C Power Delivery Classification

Power supply designs that are **NOT** compatible with the AM263x controlCARD Docking Station:

- When using USB type-C input:
  - Any USB adapter cables such as:
    - Type-A to type-C
    - micro-B to type-C
    - DC barrel jack to type-C
  - 5 V, 1.5 A power adapter with USB-C captive cable or receptacle
  - PC USB type-C port not capable of 3 A

2.2.1 Power Input Using USB Type-C Connector

The AM263x controlCARD Docking Station is powered through a USB Type-C connection. The USB Type-C source is capable of providing 3A at 5V and should advertise the current sourcing capability through the CC1 and CC2 signals. On this EVM, the CC1 and CC2 from the USB Type-C connector are interfaced to the port controller IC (TUSB320IRWBR). This device uses the CC pins to determine port attach/detach, cable orientation, role detection, and port control for Type-C current mode. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected.

The Port pin is pulled down to ground with a resistor to configure the IC in upward facing port (UFP) mode. VBUS detection is implemented to determine a successful attach in UFP mode. The OUT1 and OUT2 pins are connected to a NOR gate. Active low on both the OUT1 and OUT2 pins advertises high current (3A) in the attached state which enables the load switch (TPS22965DSGT) to provide the VBUS_USBC supply which powers other regulators that create the power rails for the device.

In UFP mode, the port controller IC constantly presents pull-down resistors on both CC pins. The port controller IC also monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The port controller IC de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the port controller device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

The AM263x controlCARD Docking Station's power requirement is 5V at 3A and if the source is not capable of providing the required power, the output at the NOR gate becomes low that disables the VBUS_USBC power switch. Therefore, if the power requirement is not met, all power supplies except VCC_3V3_SYS will remain in the off state. The board gets powered on completely only when the source can provide 5V at 3A.

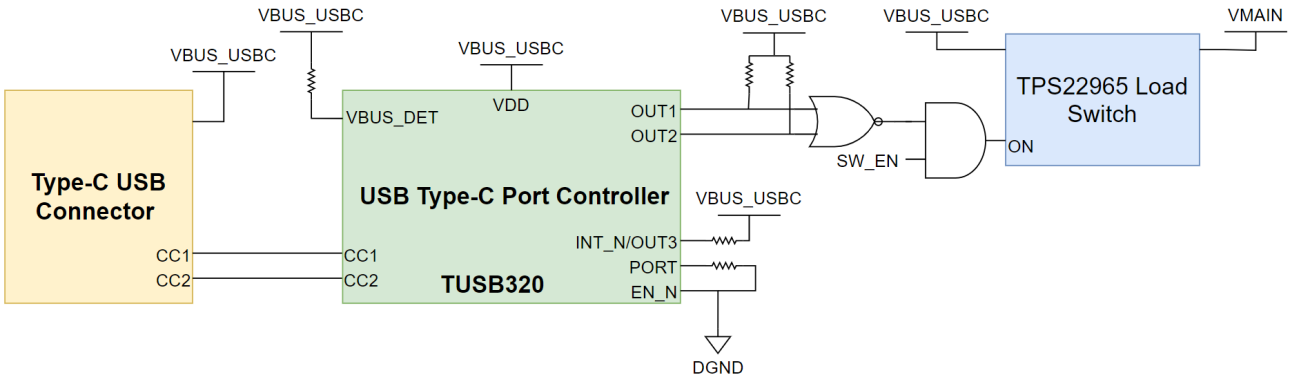


Figure 2-4. Type-C CC Configuration

Table 2-1. Current Sourcing Capability and State of USB Type-C Cable

OUT1	OUT2	Advertisement
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5A) in attached state
L	L	High current (3.0A) in attached state

The AM263x controlCARD Docking Station includes a power solution based on discrete regulators for each of the power rails. During the initial stage of the power supply, 5V supplied by the Type-C USB connector is used to generate all of the necessary voltages required by the controlCARD Docking Station.

Discrete DC-DC buck regulators are used to generate the supplies required for the AM263x system on a chip (SoC) and other peripherals on the Docking Station and connected controlCARD.

One DC-DC buck regulator (TPS62172DSGT) is used to generate the 3.3 V supply from the main 5V supply.

Note

The USB Type-C 5V input supplies both the AM263x controlCARD Docking Station and the docked AM263x/AM263Px controlCARD EVM. A separate supply for the controlCARD EVM is not needed.

2.2.2 Power Status LEDs

A power-indication LED is provided on-board to indicate to users the output status of the major supply. The LED indicates power as shown in the table below.

Table 2-2. Power Status LEDs

Name	Default Status	Operation	Function
D5	ON	VMAIN	Power indicator for VMAIN 5V supply

2.2.3 Power Tree

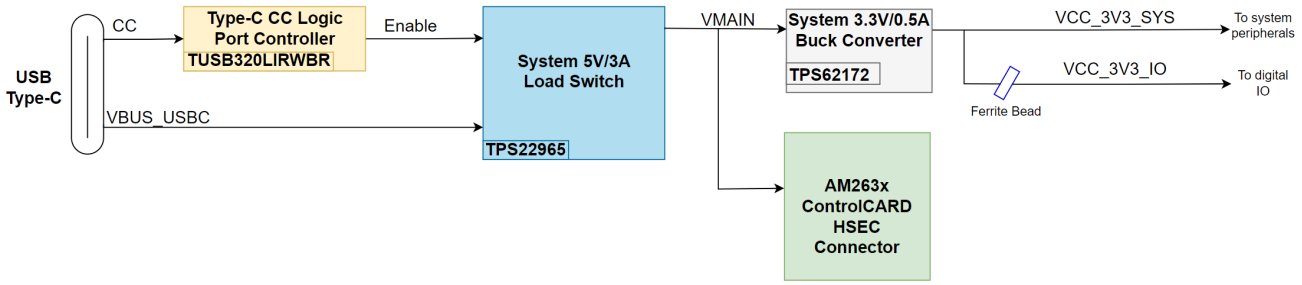


Figure 2-5. Power Tree Diagram of AM263x controlCARD Docking Station

2.3 Functional Block Diagram

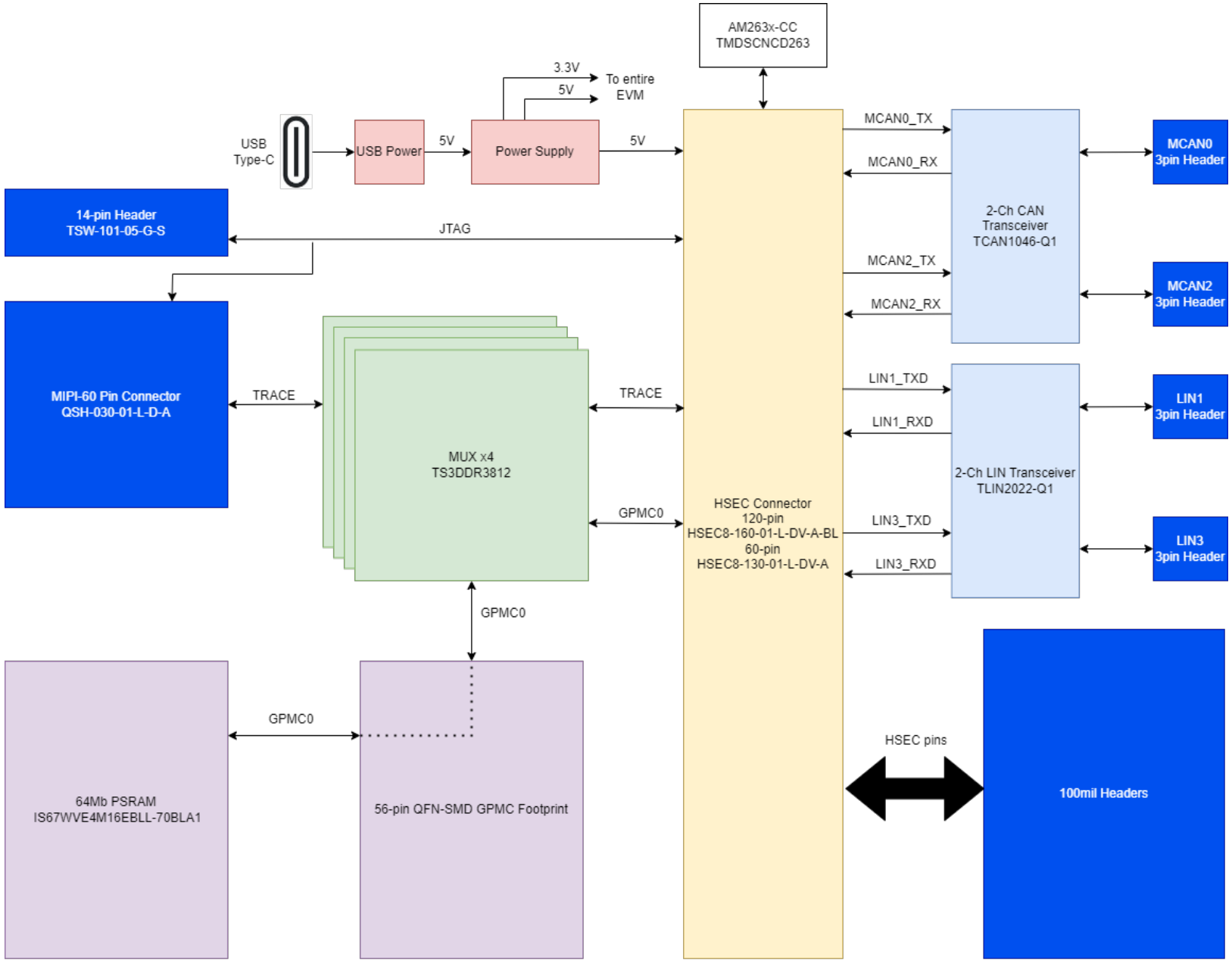


Figure 2-6. AM263x controlCARD Docking Station Functional Block Diagram

2.4 Header Information

This version of the AM263x controlCARD Docking Station has 66 different headers. For the locations of each header, refer to Section 2.1. The signal details for each header pin is detailed below.

- ADC Headers
  - For more information about the ADC interface, refer to Section 2.5.1.

Table 2-3. ADC - Variable Resistor Headers

Designator	Pin 1	Pin 2	Pin 3
J18	ADC0_AIN0	ADC_POT1_OUT	OPAMP1_IN
J22	ADC0_AIN1	ADC_POT2_OUT	OPAMP2_IN

Table 2-4. ADC - Signal Conditioning Headers

Designator	Pin 1	Pin 2
J65	ADC0_AIN0	OPAMP1_OUT
J66	ADC0_AIN1	OPAMP2_OUT

- Power Headers

Table 2-5. Power Supply Header

Designator	Pin 1	Pin 2
J16	3V3	3V3
J19	5V0	5V0
J23	3V3	3V3
J28	3V3	3V3
J29	3V3	3V3

- Ground Headers
  - All pins on the below headers are connected to Ground.

Table 2-6. Ground Headers

Designator	All Pins (# of Pins)
J13	GND (2)
J14	GND (17)
J15	GND (15)
J17	GND (2)
J26	GND (2)
J27	GND (2)
J30	GND (2)
J33, J35, J37, J39, J41, J43, J45, J47, J49	GND
J34, J36, J38, J40, J42, J44, J45	GND
J48, J51, J53, J55, J57, J59, J61, J63	GND
J50, J52, J54, J56, J58, J60, J62, J64	GND

- Breakout Headers
  - Each breakout header is mapped to specific HSEC pins. For more information and complete pinout, see Table 2-18.
- MCAN Header
  - For more information about the MCAN interface, refer to Section 2.5.3.

Table 2-7. MCAN Header

Designator	Pin 1	Pin 2	Pin 3
J3	MCAN0_CAN_P	GND	MCAN0_CAN_N
J5	MCAN2_CAN_P	GND	MCAN2_CAN_N

- LIN Header
  - For more information about the LIN Interface, refer to Section 2.5.2.

Table 2-8. LIN Header

Designator	Pin 1	Pin 2	Pin 3
J4	VBAT_LIN	GND	
J7	VLIN	LIN1_OUT	GND
J8	VLIN	LIN3_OUT	GND

- TRACE Header
  - For more information about TRACE, refer to Section 2.5.7.

Table 2-9. MIPI-60 TRACE Header (J9)

Pin	Signal	Pin	Signal	Pin	Signal
1	VREF_DEBUG	**21**	DATA1	**41**	DATA11
2	TMS	**22**	NC	**42**	NC
3	TCK	**23**	DATA2	**43**	DATA12
4	TDO	**24**	NC	**44**	NC
5	TDI	**25**	DATA3	**45**	DATA13
6	TRST	**26**	NC	**46**	NC
7	RTCK	**27**	DATA4	**47**	DATA14
8	NC	**28**	NC	**48**	NC
9	NC	**29**	DATA5	**49**	DATA15
10	NC	**30**	NC	**50**	NC
11	NC	**31**	DATA6	**51**	NC
12	VREF	**32**	NC	**52**	NC
13	CLK	**33**	DATA7	**53**	NC
14	NC	**34**	NC	**54**	NC
15	DBG_DETECT	**35**	DATA8	**55**	NC
16	GND	**36**	NC	**56**	NC
17	CTL	**37**	DATA9	**57**	GND
18	NC	**38**	NC	**58**	JTAG_MUX_SEL
19	DATA0	**39**	DATA10	**59**	NC
20	NC	**40**	NC	**60**	NC

- JTAG Header
  - For more information about JTAG, refer to Section 2.5.6

Table 2-10. 14-Pin JTAG Header (J10)

Pin	Signal	Pin	Signal
1	TMS	**8**	JTAG_MUX_SEL
2	NC	**9**	TCK
3	TDI	**10**	GND
4	GND	**11**	TCK
5	VREF	**12**	GND

Table 2-10. 14-Pin JTAG Header (J10) (continued)

Pin	Signal	Pin	Signal
6	NC	**13**	NC
7	TDO	**14**	NC

2.5 Interfaces

2.5.1 ADC

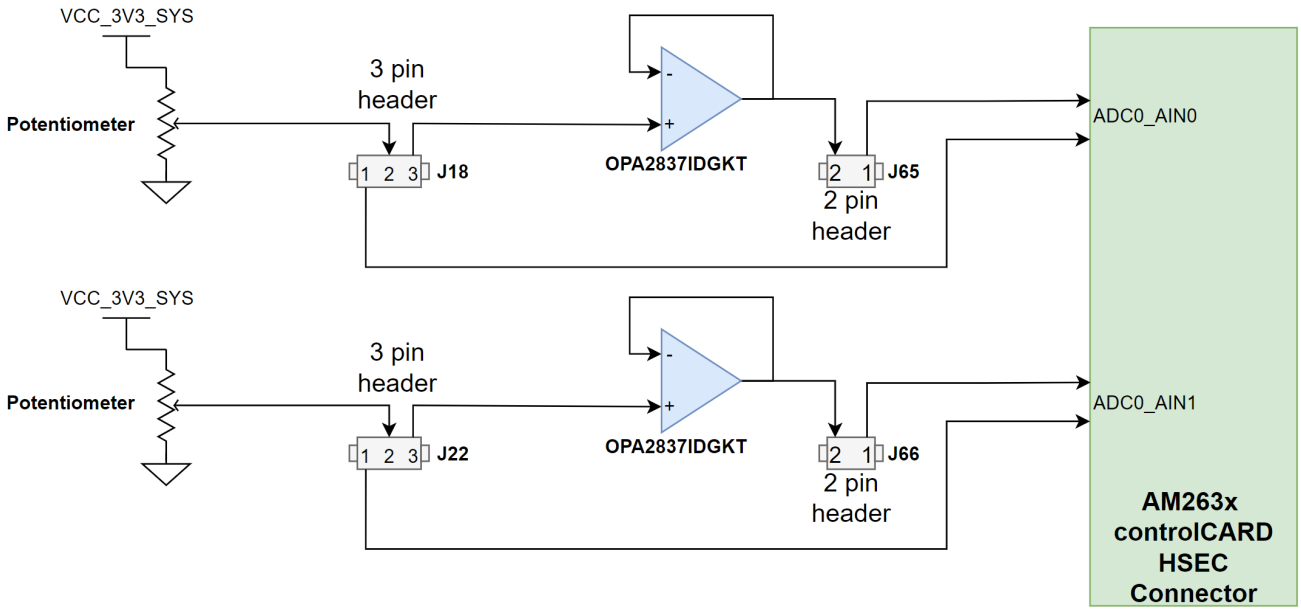


Figure 2-7. Variable ADC Inputs with Signal Conditioning

The AM263x controlCARD Docking Station is equipped with variable resistors to control the input voltage for ADC channels ADC0_AIN0 and ADC0_AIN1 on the AM263x SoC. Each of these channels is also equipped with an OPA2837IDGKT voltage feedback amplifier for signal conditioning along the ADC input lines. The table below shows the configuration options for these ADC input channels.

Table 2-11. ADC Jumper Placement

ADC Channel	Header	Jumper Placement	ADC Input Path
ADC0_AIN0	J18	No jumper	Potentiometer disconnected from ADC input
		Pins 2-3 (default)	Potentiometer connected to OPA2837IDGKT
		Pins 1-2	Potentiometer directly connected to ADC channel input
	J65	No jumper	Op amp disconnected from ADC input
		Pins 1-2	Op amp connected to ADC channel input
ADC0_AIN1	J22	No jumper	Potentiometer disconnected from ADC input
		Pins 2-3 (default)	Potentiometer connected to OPA2837IDGKT
		Pins 1-2	Potentiometer directly connected to ADC channel input
	J66	No jumper	Op amp disconnected from ADC input
		Pins 1-2	Op amp connected to ADC channel input

To use the full potentiometer and op-amp signal conditioning path for ADC0_AIN0, a jumper is placed across pins 2 and 3 on J18, and a jumper is placed on pins 1 and 2 on J65. Likewise, for ADC0_AIN1, a jumper is placed across pins 2 and 3 on J22, and a jumper is placed on pins 1 and 2 on J66.

To connect the potentiometer directly to the ADC channel input, a jumper is placed across pins 1 and 2 on J18 and/or J22.

2.5.2 LIN

The AM263x controlCARD Docking Station supports Local Interconnect Network communication through the use of a Dual LIN transceiver (TLIN2022A-Q1) that outputs the LIN Bus channels LIN1 and LIN3 of the AM263x SoC to the second pin of a pair of 3 pin headers.

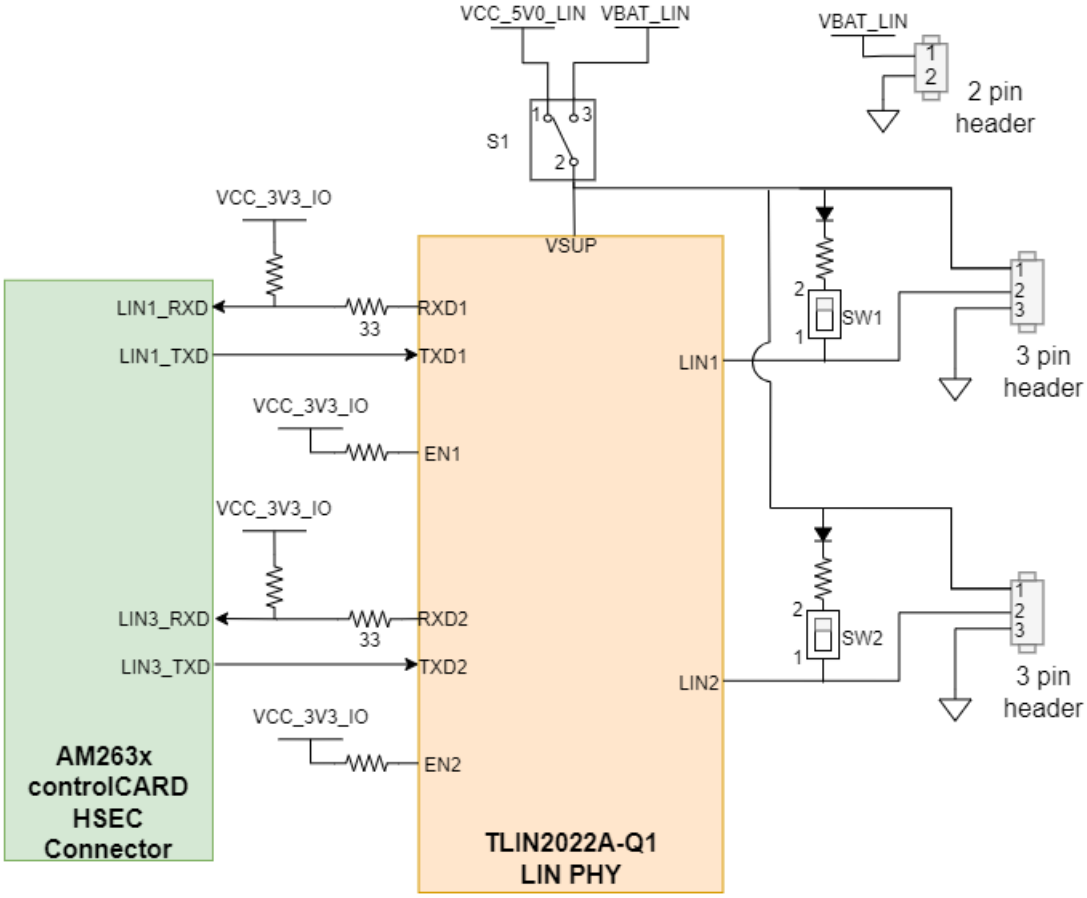


Figure 2-8. LIN Transceiver

The LIN transceiver has power input VSUP, the device supply voltage. The AM263x SoC LIN1 data transmit data input is mapped to TXD1 of the transceiver and the AM263x SoC LIN3 data transmit data input is mapped to TXD2 of the transceiver. The LIN receive data output of the transceiver RXD1 is mapped to the LIN1 RX signal of the AM263x SoC and the data output of the transceiver RXD2 is mapped to the LIN3 RX signal of the AM263x SoC. Both RXD1 and RXD2 nets have a series termination resistor close to the transceiver.

The AM263x SoC does not have an integrated pull up for the LIN RX signal and therefore an external pull up resistor is needed to the I/O supply voltage.

The AM263x controlCARD Docking Station includes a single pole double throw switch (S1) to control the voltage supply for the LIN Transceiver.

Table 2-12. LIN Switch Logic

LIN Voltage Switch Position (S1)	Voltage Supply
Pin 1-2	VMAIN, 5V supply output from the USB-C connection
Pin 2-3	VBAT_LIN, external voltage supply from pin 1 of 2 pin header

There are also two single pole single throw switches (SW1, SW2) that drive the LIN Node application. SW1 controls LIN1, SW2 controls LIN3.

Table 2-13. LIN Node Application Switch

LIN Node Application Switch Position (SW1, SW2)	LIN Node Application
Pin 1	Device node application
Pin 2	Controller node application

The AM263x controlCARD Docking Station pulls up the enable pin of each of the LIN transceiver channels for the transceiver to be in normal operational mode when the I/O Voltage supply is brought up.

2.5.3 MCAN

The AM263x controlCARD Docking Station is equipped with a single dual MCAN transceiver (TCAN1046A-Q1) that is connected to the MCAN0 and MCAN2 interfaces of the AM263x SoC. The MCAN0 and MCAN2 interfaces of the AM263x SoC are mapped directly to the AM263x controlCARD HSEC connector.

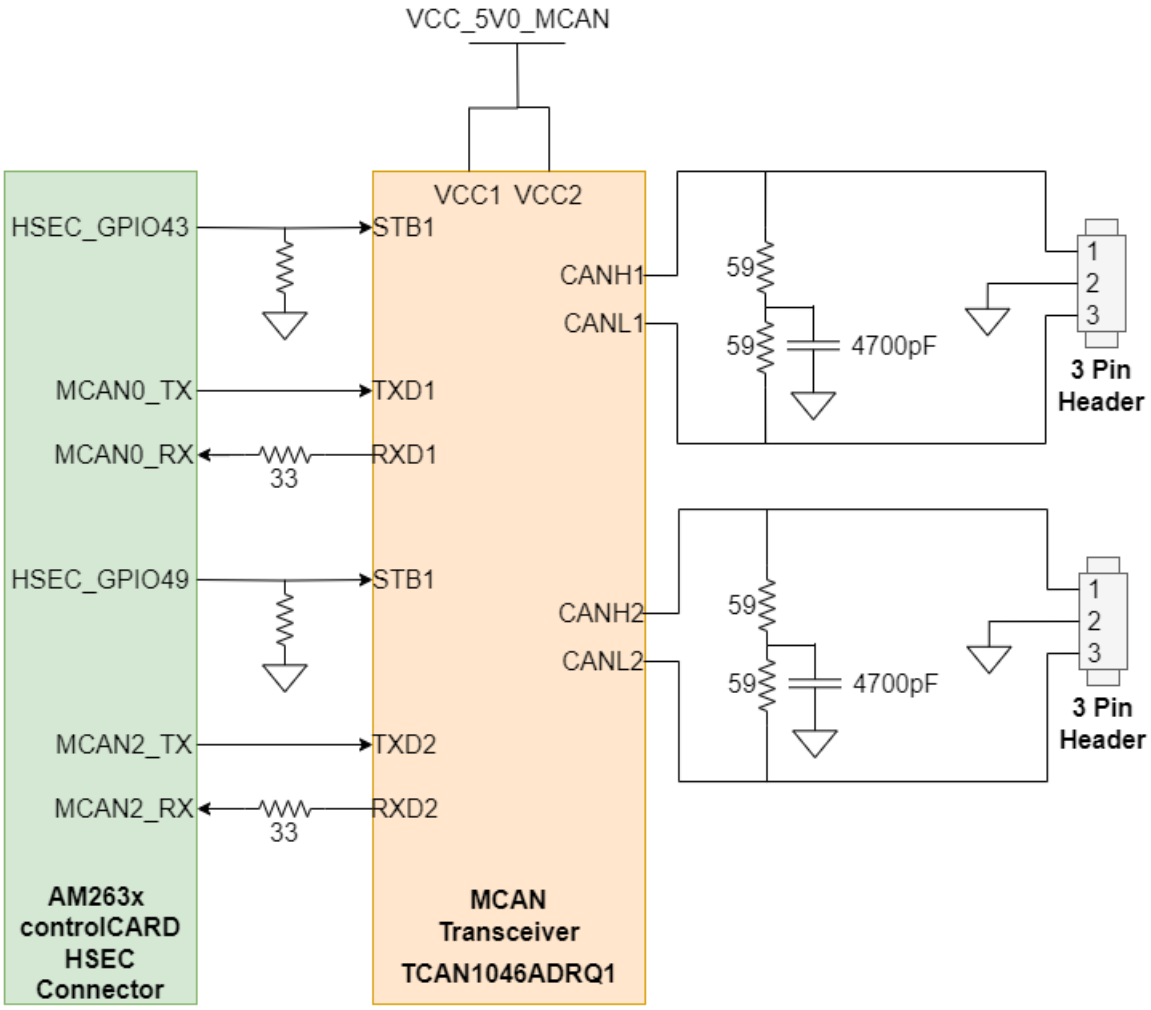


Figure 2-9. MCAN Transceiver

The MCAN transceiver has two power inputs, VCC1 is the 5V supply voltage for channel 1 of the transceiver and VCC2 is the 5V supply voltage for channel 2 of the transceiver. The AM263x SoC MCAN0 data transmit data input is mapped to TXD1 of the transceiver and the SoC MCAN2 data transmit data input is mapped to TXD2 of the transceiver. The CAN receive data output of the transceiver RXD1 is mapped to the MCAN0 RX signal of the AM263x SoC and the data output of the transceiver RXD2 is mapped to the MCAN2 RX signal of the AM263x SoC. Both RXD1 and RXD2 nets have a series termination resistor close to the transceiver.

The standby control signals for each channel are GPIO signals sourced from the AM263x SoC and AM263x controlCARD HSEC connector, GPIO43 for STB1 and GPIO49 for STB2. While the MCAN transceiver's STB inputs have an internal pull-up, the external pull-down resistor defaults the transceiver for normal operation.

The system has a 120Ω split termination on the CANH1/CANH2 and CANL1/CANL2 signals to improve EMI performance. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The low and high level CAN bus I/O lines for each channel are terminated to a three pin header.

2.5.4 TRACE/GPMC Muxing Scheme

On the AM263x SoC, the GPMC signals are pinmuxed with the TRACE data signals. Four TS3DDR3812RUAR 12-channel high speed multiplexers are used to separate the signals and enables both TRACE emulation and GPMC usage on the AM263x controlCARD Docking Station.

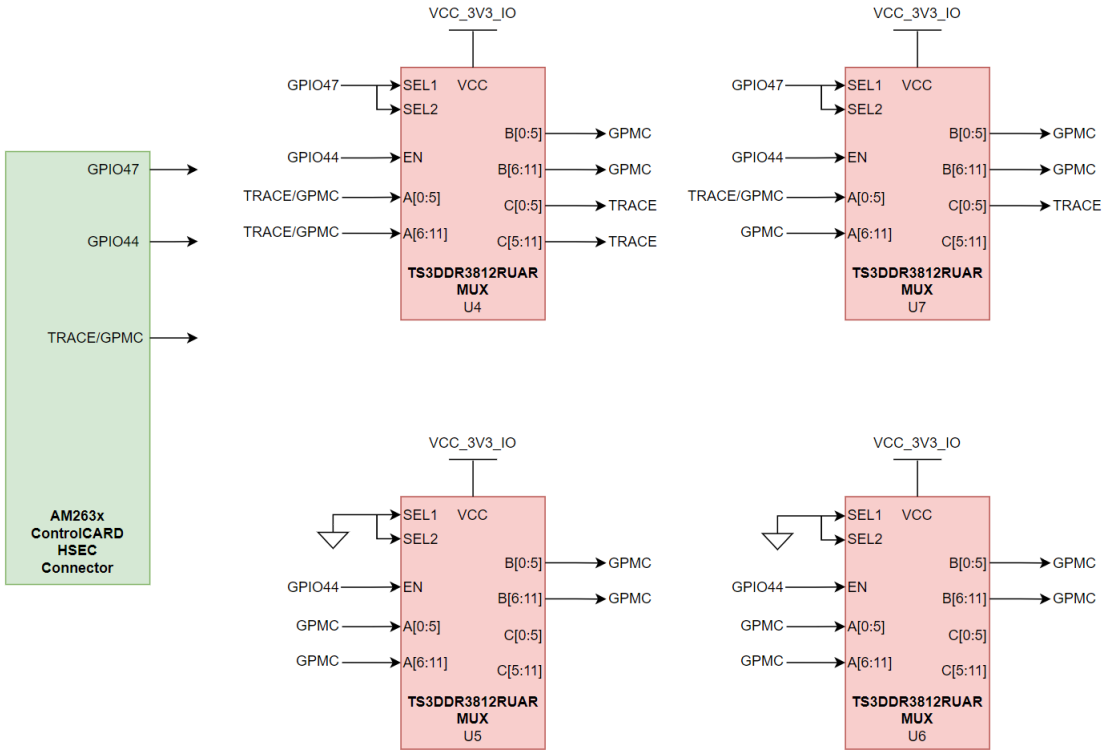


Figure 2-10. TRACE/GPMC Signal Muxing

GPIO44 from the AM263x SoC (HSEC pin 51) is the enable bit on all multiplexers. GPIO47 from the AM263x SoC (HSEC pin 50) is connected to both select bits on U4 and U7. By default, these signals are pulled up to the 3.3V IO rail, with the default signal output being the TRACE signals. The GPMC driver in the AM263x MCU+ SDK pulls GPIO47 low to allow the multiplexers to pass the GPMC signals.

U4 and U7 multiplex both TRACE and GPMC signals, while U5 and U6 do not have configurable select bits and only pass GPMC signals. There are more GPMC signals than TRACE signals, and this keeps timing consistent across all GPMC nets.

Table 2-14. MUX Function Table

EN	SEL1	SEL2	Mux Function	controlCARD Signal Routing
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z	N/A
H	L	L	A0 to A5 = B0 to B5 A6 to A11 = B6 to B11	GPMC Selected
H	L	H	A0 to A5 = B0 to B5 A6 to A11 = C6 to C11	N/A
H	H	L	A0 to A5 = C0 to C5 A6 to A11 = B6 to B11	N/A
H	H	H	A0 to A5 = C0 to C5 A6 to A11 = C6 to C11	TRACE Selected (default)

2.5.5 GPMC Memory Interface

The AM263x controlCARD Docking Station highlights the General Purpose Memory Controller (GPMC) peripheral capabilities of the AM263x SoC. The Docking Station has an on-board 64Mb PSRAM IC and a 56-pin QFN-SMD footprint for custom memory PCB installation. Included in the TMDSHSECDOCK-AM263 design package is a reference design for a NOR FLASH memory PCB that can be installed on the 56-pin footprint.

Note

GPMC is only supported on AM263x SoC. AM263Px SoC does **not** have GPMC.

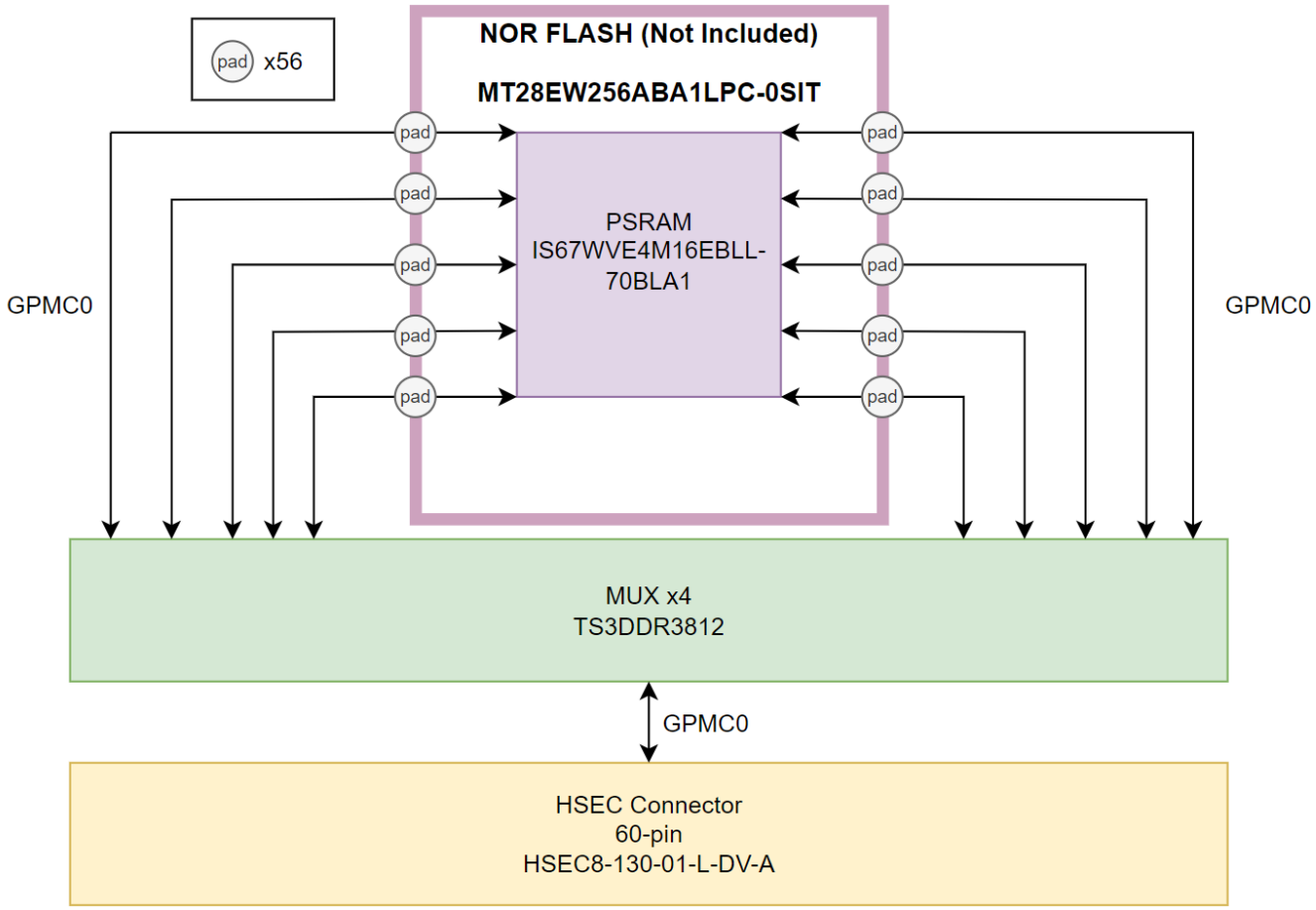


Figure 2-11. AM263x controlCARD Docking Station GPMC Peripheral Functional Block Diagram

2.5.5.1 PSRAM

The AM263x controlCARD Docking Station has a 64Mbit PSRAM memory device (IS67WVEM16EBLL-70BLA1), which is connected to the GPMC0 interface of the AM263x SoC. The PSRAM is powered by the 3.3-V system supply.

Note

There is typically a reset pin for Flash memory. The Reset pin is not present in the TFBGA-48 package that is used on the controlCARD Docking Station.

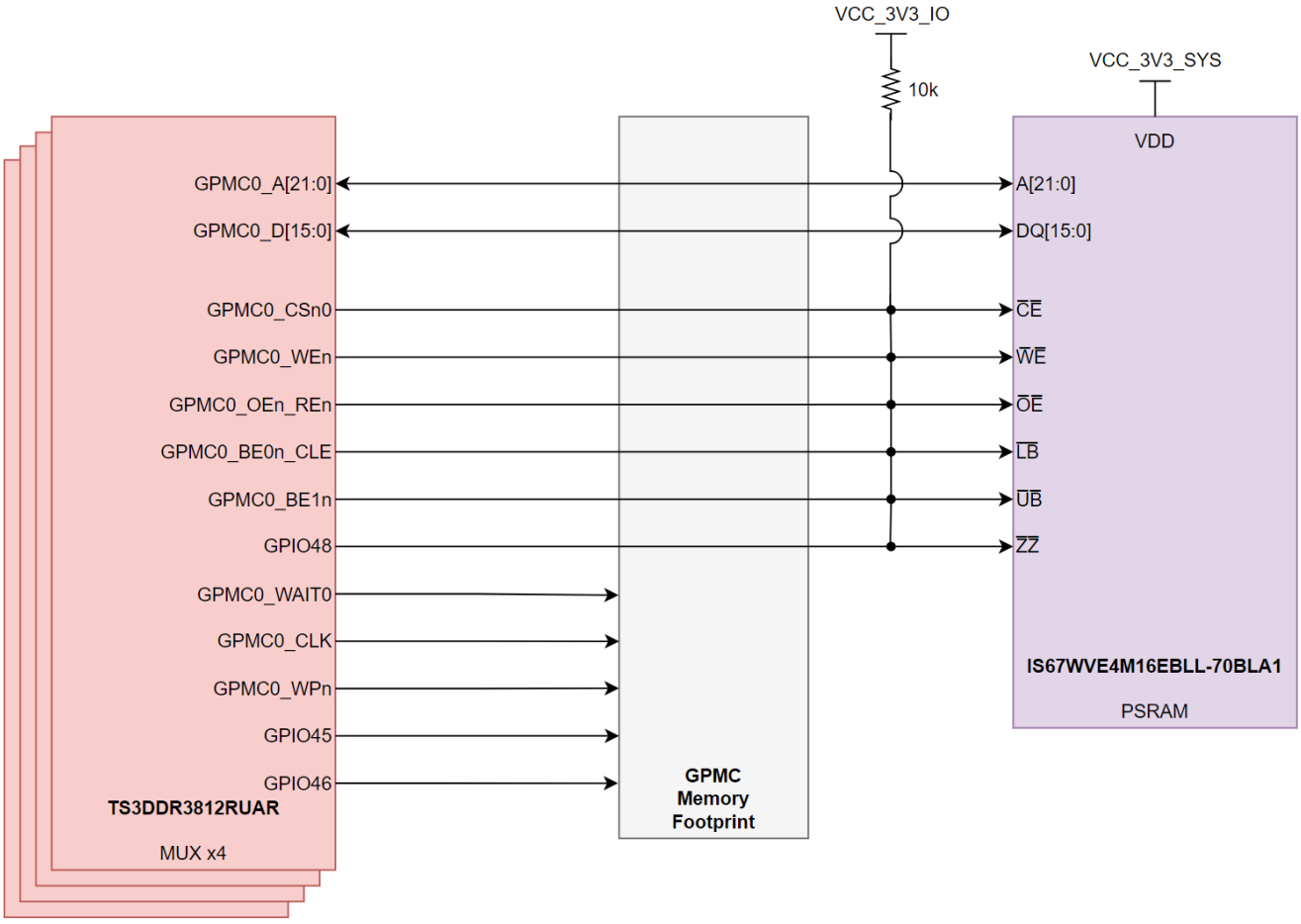


Figure 2-12. GPMC-PSRAM Interface

The GPMC signals originating from the AM263x SoC are passed through the HSEC connector onto the Docking Station. The TRACE/GPMC multiplexing scheme sends the GPMC signals to the installed IS67WVEM16EBLL-70BLA1 64Mb PSRAM module for interfacing with an external memory device. Refer to Table 2-14 for details on the MUX scheme operation.

All select and enable signals are to be pulled high via 10 kΩ resistors to ensure functionality of the active low signals.

Table 2-15. PSRAM Signal Descriptions

AM263x Signal		IS67WVEM16EBLL-70BLA1 64Mb PSRAM Signal	
GPMC0_A[21:0]	GPMC Address Output	A[21:0]	Address Input A[21:0]
GPMC0_AD[15:0]	GPMC Data Input/Output	DQ[15:0]	Data Inputs/Outputs DQ[15:0]
GPMC0_CSn0	GPMC Chip Select 0 (active low)	$\overline{CE}$	Chip Enable/Select
GPMC0_WEn	GPMC Write Enable (active low)	$\overline{WE}$	Write Enable

Table 2-15. PSRAM Signal Descriptions (continued)

AM263x Signal		IS67WVEM16EBLL-70BLA1 64Mb PSRAM Signal	
GPMC0_OEn_REn	GPMC Output Enable (active low) or Read Enable (active low)	$\overline{OE}$	Output Enable
GPMC0_BE0n_CLE	GPMC Lower-Byte Enable (active low) or Command Latch Enable	$\overline{LB}$	Lower Byte Select
GPMC0_BE1n	GPMC Upper-Byte Enable (active low)	$\overline{UB}$	Upper Byte Select
GPMC0_WAIT0	GPMC External Indication of Wait	N/A	N/A
GPMC0_WPn	GPMC Flash Write Protect (active low)	N/A	N/A
GPIO45	General-Purpose IO 45	N/A	N/A
GPIO46	General-Purpose IO 46	N/A	N/A
GPIO48	General-Purpose IO 48	$\overline{ZZ}$	Sleep Enable

2.5.5.2 GPMC Memory Footprint

The AM263x controlCARD Docking Station has a 56-pin QFN-SMD package pinout for the GPMC0 peripheral on the AM263x SoC.

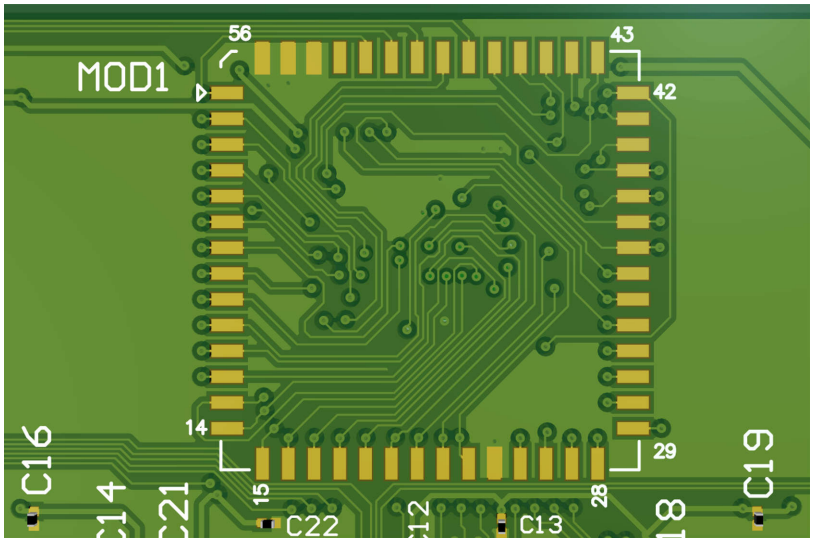


Figure 2-13. GPMC Memory Footprint

Custom PCBs with memory types supported by the AM263x SoC can be soldered to this footprint, giving the user more flexibility in developing with different memory types, and not being restricted to the on-board PSRAM module. A reference design for a NOR FLASH PCB is included with the design package for the AM263x controlCARD Docking Station. Below is the pinout for the memory footprint.

Note

Rev A of the TMDSHSECDOCK-AM263 requires a blue-wire fix to supply the GPMC footprint with 3.3V. Pins 1 and 52 of the footprint are electrically connected together, but not to the 3.3V supply. Blue-wire from nearby header J23 to either of these pins to supply the footprint with 3.3V.

Table 2-16. GPMC Memory Footprint Pinout

Pin	Signal	Description
1	VDD_3V3_SYS	3.3V System Supply
2	GPMC0_A0	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories
3	GPMC0_A1	GPMC Address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode
4	GPMC0_A2	GPMC Address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode
5	GPMC0_A3	GPMC Address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode
6	GPMC0_A4	GPMC Address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode
7	GPMC0_A5	GPMC Address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode
8	GPMC0_A6	GPMC Address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode
9	GPMC0_A7	GPMC Address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode
10	GPMC0_A8	GPMC Address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode
11	GPMC0_A9	GPMC Address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode
12	GPMC0_A10	GPMC Address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode
13	GPMC0_A11	GPMC Address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
14	GPMC0_A12	GPMC Address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
15	GPMC0_A13	GPMC Address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode

Table 2-16. GPMC Memory Footprint Pinout (continued)

Pin	Signal	Description
16	GPMC0_A14	GPMC Address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
17	GPMC0_A15	GPMC Address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
18	GPMC0_A16	GPMC Address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
19	GPMC0_A17	GPMC Address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
20	GPMC0_A18	GPMC Address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
21	GPMC0_A19	GPMC Address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
22	GPMC0_A20	GPMC Address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
23	GPMC0_A21	GPMC Address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode
24	GND	Ground
25	GPMC0_AD0	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode
26	GPMC0_AD1	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode
27	GPMC0_AD2	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode
28	GPMC0_AD3	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode
29	GPMC0_AD4	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode
30	GPMC0_AD5	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode
31	GPMC0_AD6	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode
32	GPMC0_AD7	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode
33	GPMC0_AD8	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode
34	GPMC0_AD9	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode
35	GPMC0_AD10	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode
36	GPMC0_AD11	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode
37	GPMC0_AD12	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode
38	GPMC0_AD13	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode
39	GPMC0_AD14	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode
40	GPMC0_AD15	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode
41	GPMC0_OEN_REN	GPMC Output Enable (active low) or Read Enable (activelow)
42	GPMC0_WEN	GPMC Write Enable (active low)

Table 2-16. GPMC Memory Footprint Pinout (continued)

Pin	Signal	Description
43	GPMC0_BE0N_CLE	GPMC Lower-Byte Enable (active low) or Command Latch Enable
44	GPMC0_BE1	GPMC Upper-Byte Enable (active low)
45	GPMC0_CSN0	GPMC Chip Select 0 (active low)
46	GPMC0_WPN	GPMC Flash Write Protect (active low)
47	GPMC0_WAIT0	GPMC External Indication of Wait
48	GPIO45	General Purpose Input/Output
49	GPIO48	General Purpose Input/Output
50	GPIO46	General Purpose Input/Output
51	GPMC0_CLK	GPMC Clock
52	VDD_3V3_SYS	3.3V System Supply
53	NC	-
54	GND	Ground
55	GND	Ground
56	GND	Ground

2.5.5.3 NOR FLASH

The AM263x controlCARD Docking Station design package includes a design for a custom PCB with a MT28EW256ABA NOR FLASH memory module mounted on it. This enables a user to develop using the GPMC0 interface of the AM263x SoC with a NOR FLASH memory module.

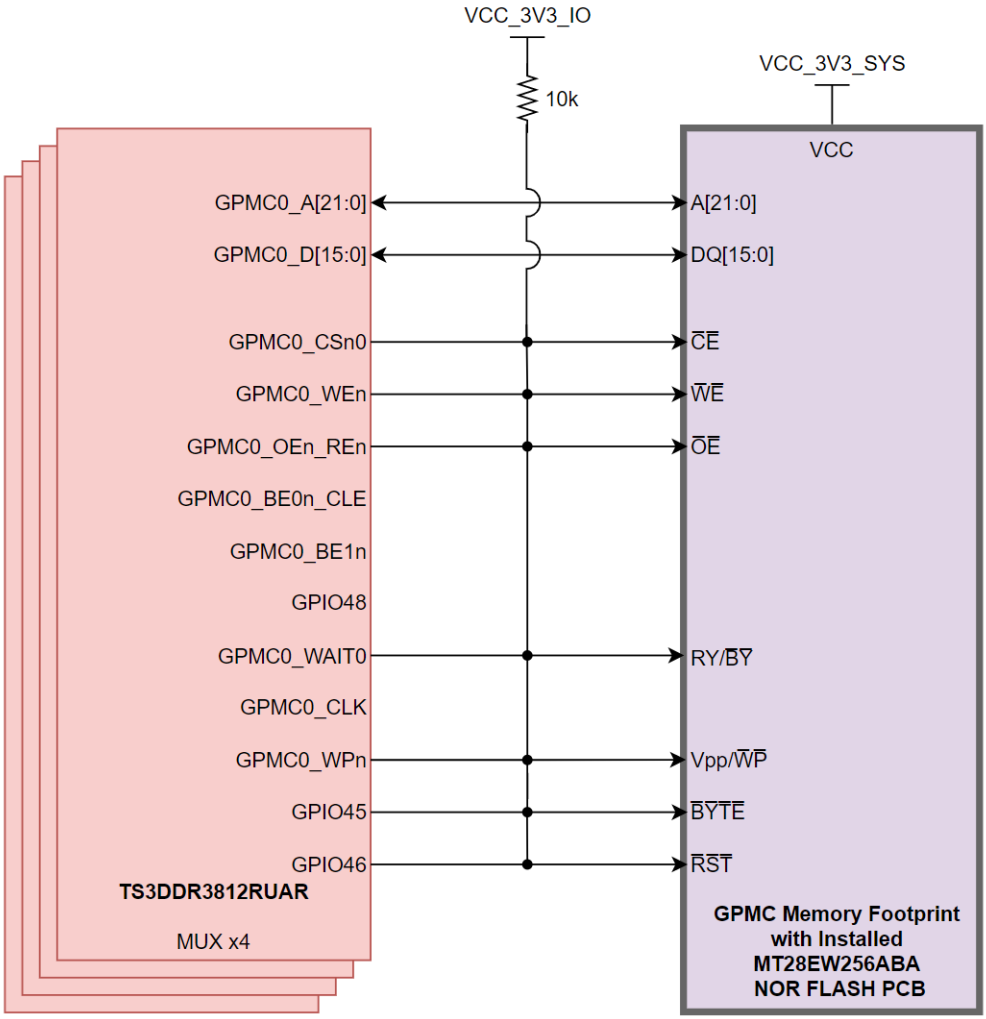


Figure 2-14. GPMC-NOR FLASH Interface

The GPMC signals originating from the AM263x SoC are passed through the HSEC connector onto the Docking Station. The TRACE/GPMC multiplexing scheme sends the GPMC signals to the GPMC memory footprint, and onto the installed custom MT28EW256ABA NOR FLASH PCB. Refer to Table 2-14 for details on the MUX scheme operation.

All select and enable signals are to be pulled high via 10 kΩ resistors to ensure functionality of the active low signals.

Table 2-17. NOR FLASH Signal Descriptions

AM263x Signal		MT28EW256ABA NOR FLASH Signal	
GPMC0_A[21:0]	GPMC Address Output	A[MAX:0]	Address
GPMC0_AD[15:0]	GPMC Data Input/Output	DQ[15:0]	Data I/O
GPMC0_CSn0	GPMC Chip Select 0 (active low)	$\overline{CE}$	Chip Enable
GPMC0_WEn	GPMC Write Enable (active low)	$\overline{WE}$	Write Enable

Table 2-17. NOR FLASH Signal Descriptions (continued)

AM263x Signal		MT28EW256ABA NOR FLASH Signal	
GPMC0_OEn_REn	GPMC Output Enable (active low) or Read Enable (active low)	$\overline{OE}$	Output Enable
GPMC0_BE0n_CLE	GPMC Lower-Byte Enable (active low) or Command Latch Enable	N/A	N/A
GPMC0_BE1n	GPMC Upper-Byte Enable (active low)	N/A	N/A
GPMC0_WAIT0	GPMC External Indication of Wait	RY/$\overline{BY}$	Ready busy
GPMC0_WPn	GPMC Flash Write Protect (active low)	Vpp/$\overline{WP}$	Vpp/Write Protect
GPIO45	General-Purpose IO 45	$\overline{BYTE}$	Byte/word organization select
GPIO46	General-Purpose IO 46	$\overline{RST}$	Reset
GPIO48	General-Purpose IO 48	N/A	N/A

2.5.6 TI 14-Pin Header

The AM263x controlCARD Docking Station includes a 14-pin TI JTAG (J10) connector to support external JTAG emulation. When an external emulator is connected, the signals are routed from the 14-pin connector to the AM263x SoC via the HSEC pins on the AM263x controlCARD.

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

Further information on supported JTAG emulators can be found in the Emulation and Trace Headers Technical Reference Manual.

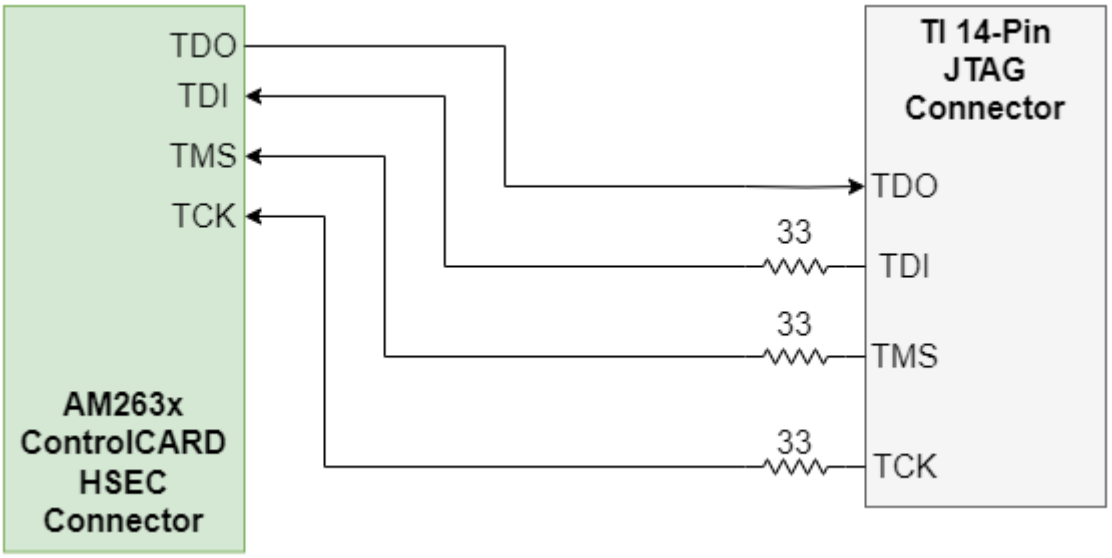


Figure 2-15. TI 14-Pin Header

2.5.7 MIPI-60 Connector

The AM263x controlCARD Dock includes a MIPI-60 (J9) connector to support external JTAG emulation and TRACE capabilities. When an external emulator is connected, the signals are routed from the MIPI60 connector to the AM263x SoC via the HSEC pins on the AM263x controlCARD.

Further information on the emulation and trace header can be found in the Emulation and Trace Headers Technical Reference Manual.

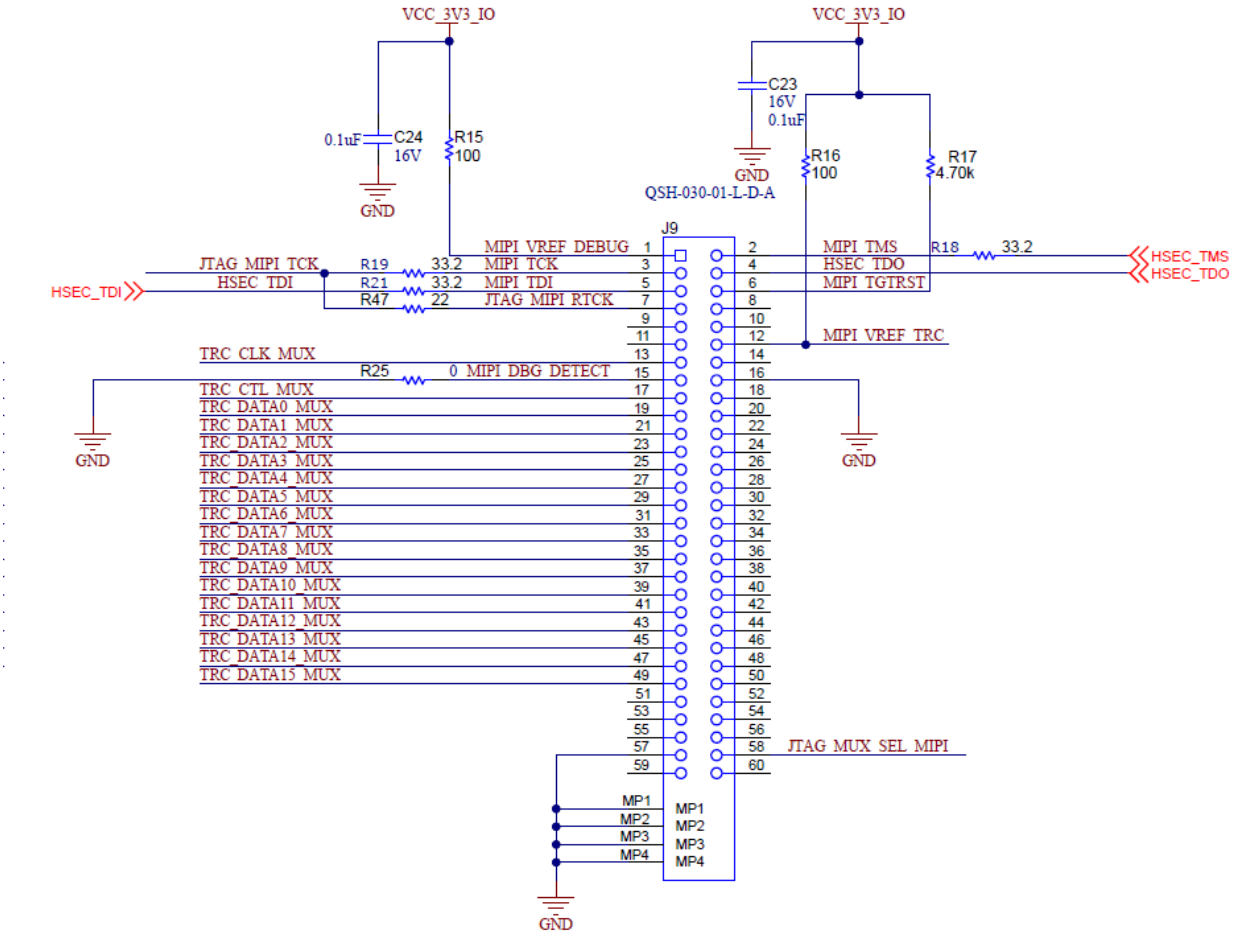


Figure 2-16. MIPI-60 Connector

2.6 HSEC Pinout

Table 2-18 shows the pinout of the 180-pin High Speed Edge Connector (HSEC), the default signal net on the Docking Station, and the associated Breakout Header/Pin connected to the HSEC interface. For all available pinmux mode options on AM263x/AM263Px controlCARD, see the appropriate User's Guide linked in Section 4.1.

Table 2-18. AM263x controlCARD Docking Station HSEC Pinout

Pin#	AM263x controlCARD Docking Station Signal	Breakout Header Reference Designator/Pin		Breakout Header Reference Designator/Pin	AM263x ControlCARD Docking Station Signal	Pin#
1	NC				NC	2
3	TMS				NC	4
5	TCK				TDO	6
7	GND				TDI	8
9	ADC0_AIN0	J6_1			GND	10
11	ADC0_AIN1	J6_2		J12_1	ADC1_AIN0	12
13	GND	J6_3		J12_2	ADC1_AIN1	14
15	ADC0_AIN2	J6_4		J12_3	GND	16
17	ADC0_AIN3	J6_5		J12_4	ADC1_AIN2	18
19	GND			J12_5	ADC1_AIN3	20
21	ADC0_AIN4	J6_6			GND	22
23	ADC0_AIN5	J6_7		J12_6	ADC1_AIN4	24
25	ADC4_AIN0	J6_8		J12_7	ADC1_AIN5	26
27	ADC4_AIN1	J6_9		J12_8	ADC3_AIN0	28
29	GND	J6_10		J12_9	ADC3_AIN1	30
31	ADC2_AIN0	J6_11		J12_10	GND	32
33	ADC2_AIN1	J6_12		J12_11	ADC3_AIN2	34
35	GND			J12_12	ADC3_AIN3	36
37	ADC2_AIN2	J6_13			GND	38
39	ADC2_AIN3	J6_14		J12_13	ADC3_AIN4	40
41	HSEC_41	J6_15		J12_14	ADC3_AIN5	42
43	HSEC_43	J6_16		J12_15	HSEC_44	44
45	HSEC_45	J6_17			GND	46
47	GND				HSEC_5V0	48
49	GPIO43	J20_1		J21_1	GPIO47	50
51	GPIO44	J20_2		J21_2	GPIO48	52
53	GPIO45	J20_3		J21_3	GPIO49	54
55	GPIO46	J20_4		J21_4	EPWM3_B	56
57	EPWM4_A	J20_5		J21_5	EPWM6_A	58
59	EPWM4_B	J20_6		J21_6	EPWM6_B	60
61	EPWM5_A	J20_7		J21_7	EPWM7_A	62
63	EPWM5_B	J20_8		J21_8	EPWM7_B	64
65	GND			J21_9	HSEC_66	66
67	SPI0_D0	J20_9		J21_10	TRC_CLK	68
69	SPI0_D1	J20_10		J21_11	TRC_CTL	70
71	LIN3_TXD	J20_11		J21_12	EQEP1_STROBE	72
73	LIN3_RXD	J20_12		J21_13	EQEP1_INDEX	74
75	SPI1_D0	J20_13		J21_14	LIN1_RXD	76
77	SPI1_D1	J20_14		J21_15	LIN1_TXD	78
79	SPI1_CLK	J20_15		J21_16	MCAN0_RX	80
81	SPI1_CS0	J20_16		J21_17	MCAN0_TX	82
83	GND				HSEC_5V0	84
85	I2C1_SDA	J20_17		J21_18	GPIO65	86
87	I2C1_SCL	J20_18		J21_19	HSEC_88	88
89	EPWM21_A	J20_19		J21_20	EPWM21_B	90
91	SDFM0_D0	J20_20		J21_21	EQEP2_A	92
93	EQEP2_B	J20_21		J21_22	MCAN2_RX	94
95	MCAN2_TX	J20_22		J21_23	HSEC_96	96
97	GND				HSEC_5V0	98

Table 2-18. AM263x controlCARD Docking Station HSEC Pinout (continued)

Pin#	AM263x controlCARD Docking Station Signal	Breakout Header Reference Designator/Pin		Breakout Header Reference Designator/Pin	AM263x ControlCARD Docking Station Signal	Pin#
99	SDFM0_D1	J20_23		J21_24	EQEP0_B	100
101	SDFM0_CLK1	J20_24		J21_25	EQEP0_A	102
103	SDFM0_D2	J20_25		J21_26	EQEP0_STROBE	104
105	SDFM0_CLK2	J20_26		J21_27	EQEP0_INDEX	106
107	SDFM0_D3	J20_27		J21_28	MII0_RXER	108
109	SDFM0_CLK3	J20_28		J21_29	GPMC0_CLK	110
111	GND				HSEC_5V0	112
113	HSEC_113	J20_29		J21_30	HSEC_114	114
115	HSEC_115	J20_30		J21_31	HSEC_116	116
117	HSEC_117	J20_31		J21_32	HSEC_5V0	118
119	HSEC_119	J20_32		J21_33	PORz	120
121	GPMC0_WAIT0	J24_1		J25_1	GPMC0_WPN	122
123	GPIO91	J24_2		J25_2	GPMC0_A0	124
125	ICSS_MII0_RXD0	J24_3		J25_3	GPMC0_A2	126
127	GPMC0_A3	J24_4		J25_4	GPMC0_A4	128
129	GPMC0_A5	J24_5		J25_5	GPMC0_A6	130
131	GPMC0_A7	J24_6		J25_6	GPMC0_A8	132
133	GPMC0_A9	J24_7		J25_7	GPMC0_A10	134
135	GND			J25_8	HSEC_136	136
137	GPMC0_OEN_REN / TRC_DATA0	J24_8		J25_9	GPMC0_BE0N_CLE / TRC_DATA1	138
139	GPMC0_BEN1 / TRC_DATA2	J24_9		J25_10	GPMC0_WEN / TRC_DATA3	140
141	GPMC0_A11 / TRC_DATA4	J24_10		J25_11	GPMC0_A12 / TRC_DATA5	142
143	GPMC0_A13 / TRC_DATA6	J24_11		J25_12	GPMC0_A14 / TRC_DATA7	144
145	GPMC0_A15 / TRC_DATA8	J24_12		J25_13	GPMC0_A16 / TRC_DATA9	146
147	GPMC0_A17 / TRC_DATA10	J24_13		J25_14	GPMC0_A18 / TRC_DATA11	148
149	GPMC0_A19 / TRC_DATA12	J24_14		J25_15	GPMC0_A20 / TRC_DATA13	150
151	GPMC0_A21 / TRC_DATA14	J24_15		J25_16	GPMC0_CSN0 / TRC_DATA15	152
153	GPMC0_AD0	J24_16		J25_17	GPMC0_AD1	154
155	GPMC0_AD2	J24_17		J25_18	GPMC0_AD3	156
157	GND				HSEC_5V0	158
159	GPMC0_AD4	J24_18		J25_19	GPMC0_AD5	160
161	GPMC0_AD6	J24_19		J25_20	GPMC0_AD7	162
163	GPMC0_AD8	J24_20		J25_21	GPMC0_AD9	164
165	GPMC0_AD10	J24_21		J25_22	GPMC0_AD11	166
167	GPMC0_AD12	J24_22		J25_23	GPMC0_AD13	168
169	GPMC0_AD14	J24_23		J25_24	GPMC0_AD15	170
171	HSEC_171	J24_24		J25_25	HSEC_172	172
173	HSEC_173	J24_25		J25_26	HSEC_174	174
175	HSEC_175	J24_26		J25_27	HSEC_176	176
177	HSEC_177	J24_27		J25_28	SAFETY_ERROR	178
179	GND				HSEC_5V0	180

3 Additional Information

3.1 If You Need Assistance

If you have any feedback or questions, support for the Sitara MCUs and the AM263x controlCARD Docking Station kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in the Section 4.1.

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4 References

4.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

AM263x Reference Documents

- *AM263x controlCARD*
- *AM263x controlCARD User's Guide*
- *AM2634 Sitara™ Microcontrollers*
- *AM263x Sitara™ Microcontrollers Data Sheet*
- *AM263x Sitara™ Microcontrollers Technical Reference Manual*

AM263Px Reference Documents

- *AM263Px controlCARD*
- *AM263Px controlCARD User's Guide*
- *AM263P4 Sitara™ Micrcontrollers*
- *AM263Px Sitara™ Microcontrollers Data Sheet*
- *AM263Px Sitara™ Microcontrollers Technical Reference Manual*

General Reference Documents

- *Texas Instruments Code Composer Studio*

4.2 Other TI Components Used in This Design

The AM263x controlCARD Docking Station uses various other TI components for its functions. A consolidated list of these components with links to their TI product pages is shown below.

- *TPD1E05U06-Q1 Automotive 1-Channel Ultra-Low-Capacitance IEC ESD Protection Diode*
- *TPD1E01B04 1-Channel ESD Protection Diode for USB Type-C and Thunderbolt 3*
- *TCAN1046DRQ1 Automotive High Speed Dual CAN Transceiver*
- *TLIN2022DRQ1 Fault Protected Dual Local Interconnect Network (LIN) Transceiver With Dominant State Timeout*
- *TS3DDR3812RUAR 3.3-V, 2:1 (SPDT), 12-channel switch*
- *TUSB320IRWBR USB Type-C configuration channel logic and port control*
- *SN74AHC1G02DRLR Single 2-input, 2-V to 5.5-V NOR gate*
- *TPS22965DSGT 5.7-V, 6-A, 16-mΩ load switch with adj. rise time and optional output discharge*
- *TPS62172DSGT 3–17V 0.5A Step-Down Converter in 2x2 QFN package*
- *SN74CB3Q3257PWR 3.3-V, 2:1 (SPDT), 4-channel general-purpose FET bus switch*
- *SN74LVC1G04 Single 1.65-V to 5.5-V inverter*
- *SN74LVC1G08DSF2 Single 2-input, 1.65-V to 5.5-V AND gate*
- *SN74AHC1G02DBVT Single 2-input, 2-V to 5.5-V NOR gate*
- *OPA2837IDGKT Dual, Low-Power, Precision, Rail-to-Rail Output, 105MHz, Voltage Feedback Amplifier*

5 Revision History

DATE	REVISION	NOTES
December 2023	*	Initial release.

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