User's Guide

Jacinto7 TDA4VE-Q1/TDA4VL-Q1/TDA4AL-Q1 Evaluation Module (EVM)

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1 Introduction

The TDA4VE-Q1/TDA4VL-Q1/TDA4AL-Q1 EVM is a standalone test, development, and evaluation module which gives developers the basic resources to develop software and evaluate performance of the Jacinto7 processor. The J721S2 is a super-set processor/device available in different configurations targeted for different markets and applications (TDA4VE-Q1, TDA4VL-Q1, and TDA4AL-Q1). This user's guide describes the hardware, settings, and interfaces of the EVM.

1.1 Inside the Box

The TDA4VE-Q1/TDA4VL-Q1/TDA4AL-Q1 System on Module is not a stand-alone EVM and must be paired with a base board (such as Jacinto7 Common Processor Board). When paired the two-board system becomes the TDA4VE-Q1/TDA4VL-Q1/TDA4AL-Q1 EVM. This user guide discusses the EVM solution (System on Module + Base Board).

The Jacinto7 TDA4VE-Q1/TDA4VL-Q1/TDA4AL-Q1 System on Module kit includes:

- System on Module mounted with J721S2 Super-set device
- Micro-SD Card
- HEX KEY L SHAPE 4MM 2.68"
- Paper Card with Start-up Link/Support Information

The Jacinto7 Common Processor Board (CPB) kit includes:

- Common Processor Board with mounted Quad Ethernet Adapter
- USB-A to USB micro-B Cable (2x)
- USB-A to USB-C Cable
- Ethernet Cable (2x)
- Display Port Cable
- 2.5mm Power Cable with Wire Leads

The orderable part numbers are provided in table below:

TDA4VE-Q1/TDA4VL-Q1/TDA4AL-Q1	
System On Module	J721S2XSOMG01EVM
Jacinto7 Common Processor Board	J721EXCP01EVM

An EVM power supply is NOT included. For more information on the types of supplies recommended with the EVM, see Section 2.1.

1.2 Key Features

Below are the EVM's key features

- Processor:
  - Texas Instruments Jacinto J721S2 Super-Set Processor
- Optimized Power Management Solution:
  - Dynamic Voltage Scaling
  - Multiple Clock and Power Domains
  - Integrated Power Measurement
- Memory:
  - 16GB LPDDR4 (4266 MT/s), support inline ECC
  - Two 512Mb Non-Volatile NOR Memories, 1x Octal-SPI and 1x Quad-SPI
  - 1Gb Non-Volatile NAND Memory, Octal-SPI
  - 16GB Non-Volatile eMMC Memory, JEDEC/MMC v5.1 compliant
  - MicroSD Card Cage Multimedia Card (MMC)/Secure Digital Card (Micro SD) Cage, UHS-1
  - I2C EEPROM, 1Mbit
- USB

  - USB3.1 (Gen 1) Type C Interface, support DFP, DRP, UFP modes
  - USB2.0 Hub to 2x Type A (Host), 1x Pin Header for PCIe WiFi support
  - Two USB2.0 Micro B (for Dual/Quad UART-over-USB Transceiver)
- Display
  - VESA Display Port (v1.4), supports 4K UHD with MST support
  - VESA Display Port (v1.4), supports 2K QHD
  - Custom CSI2-TX Expansion Interface
- Wired Network
  - Gigabit Ethernet (RJ45 Connector)
  - 5 CAN Interfaces, full CAN-FD support
- Camera Interfaces
  - Two CSI2-RX Camera Interfaces (Custom Interface/Dual-QSH connectors)
  - One CSI2-Tx Interface
- Audio
  - 3.5-mm Stereo Input/Output
- Expansion/Add-on
  - One PCIe/Gen3 4L Card Slot (with 1Lane support)
  - Multiple Pin Headers for ADC, I2C, I3C, and SPI Access
  - Expansion module(s) provide additional Ethernet, CAN, and LIN interface support
- User Control
  - Pushbuttons (Resets, Power Modes, User Defined)
  - LEDs (Power, User Defined, Serial Port)
  - User Configurations (Boot Mode, USB Mode)
  - External or On-board Emulator Support (MIPI-60 w/ adapters to 14-pin or 20-pin CTI
- REACH and RoHS Compliant

1.3 Thermal Compliance

There is elevated heat on the processor/heatsink, use caution particularly at elevated ambient temperatures! Although the processor/heatsink is not a burn hazard, caution should be used when handling the EVM due to increased heat in the area of the heatsink

	Caution	Caution Hot surface. Contact may cause burns. Do not touch!

1.4 Reach Compliance

In compliance with the Article 33 provision of the EU REACH regulation we are notifying you that this EVM includes one or more components containing at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are listed in Table 1-1

Table 1-1. REACH Compliance

Component Manufacturer	Component type	Component part number	SVHC Substance	SVHC CAS (when available)
Tensility	Power Cable	10-02937	Lead	7439-92-1
Rosenberger	FPD Link Connector	D4S20G-400A5-C	Lead	7439-92-1
Littelfuse	Power fuse	0154010.DR	Lead	7439-92-1

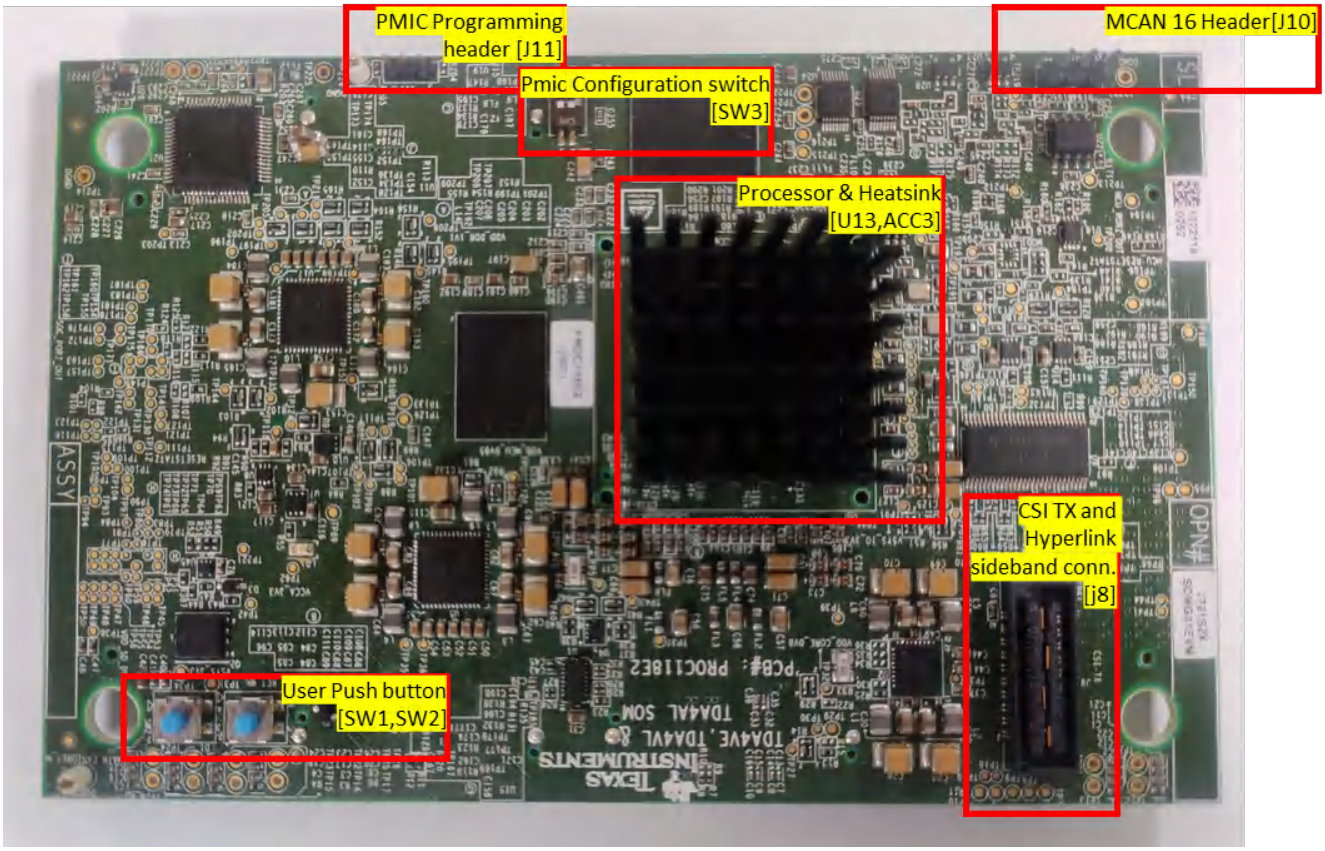
1.5 EMC, EMI, and ESD Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). It is recommended this product be used in an ESD controlled environment. This may include a temperature and/or humidity-controlled environment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is to be used in the basic electromagnetic environment, as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

2 User Interfaces

Figure 2-1 and Figure 2-2 identify the key user interfaces on the EVM (top and bottom view).



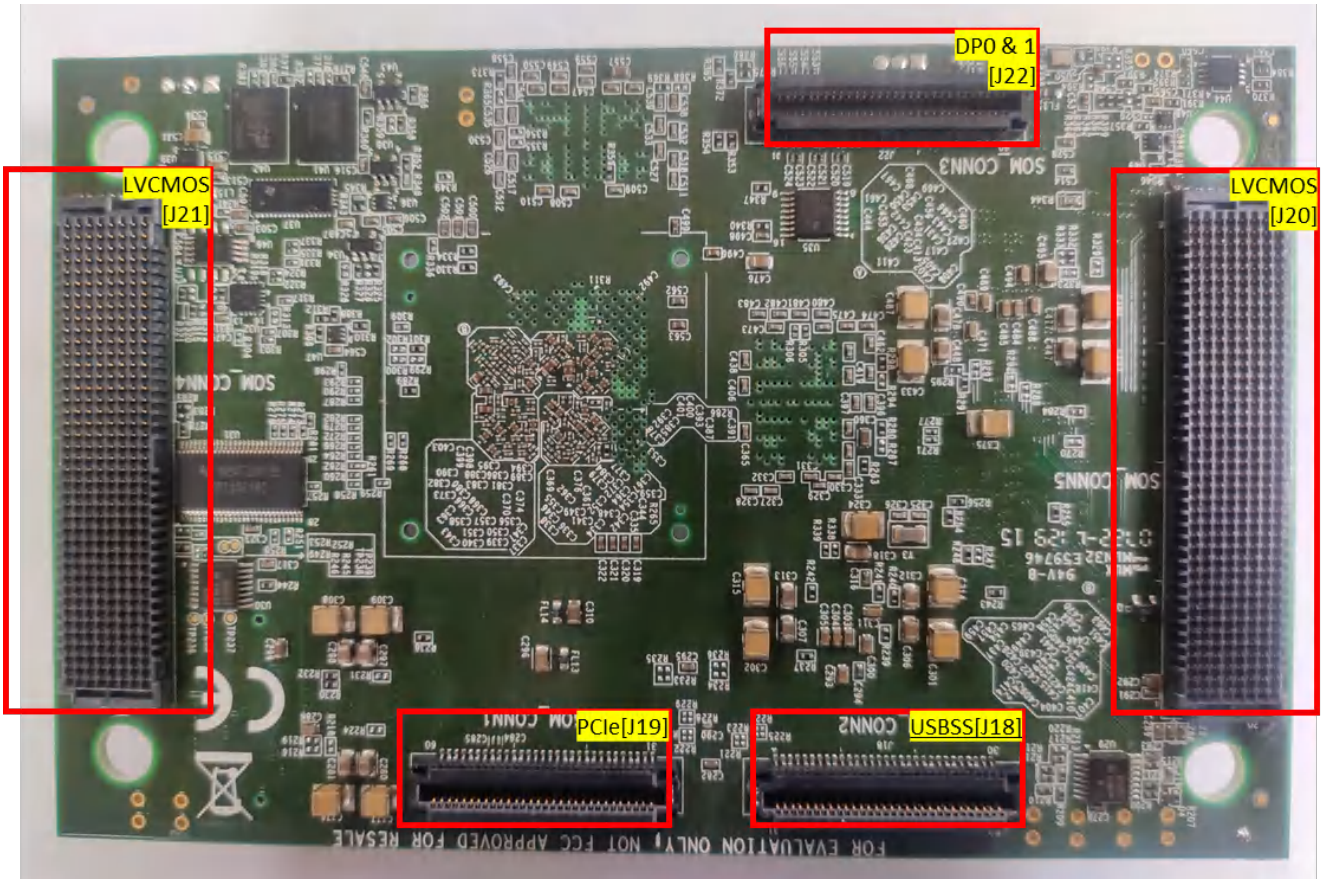
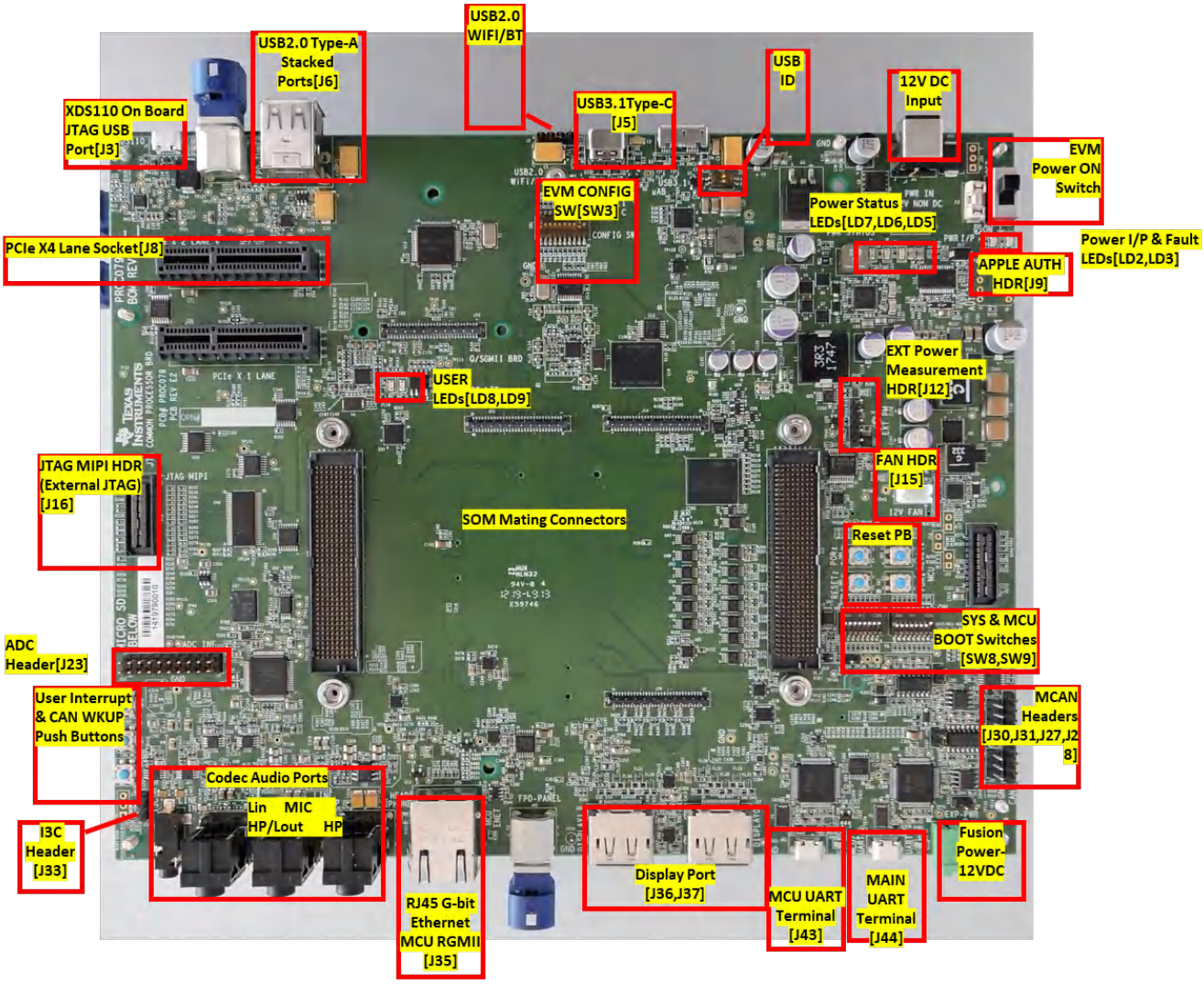


Figure 2-1. TDA4VE-Q1/TDA4VL-Q1/TDA4AL-Q1 System on Module Component Identification



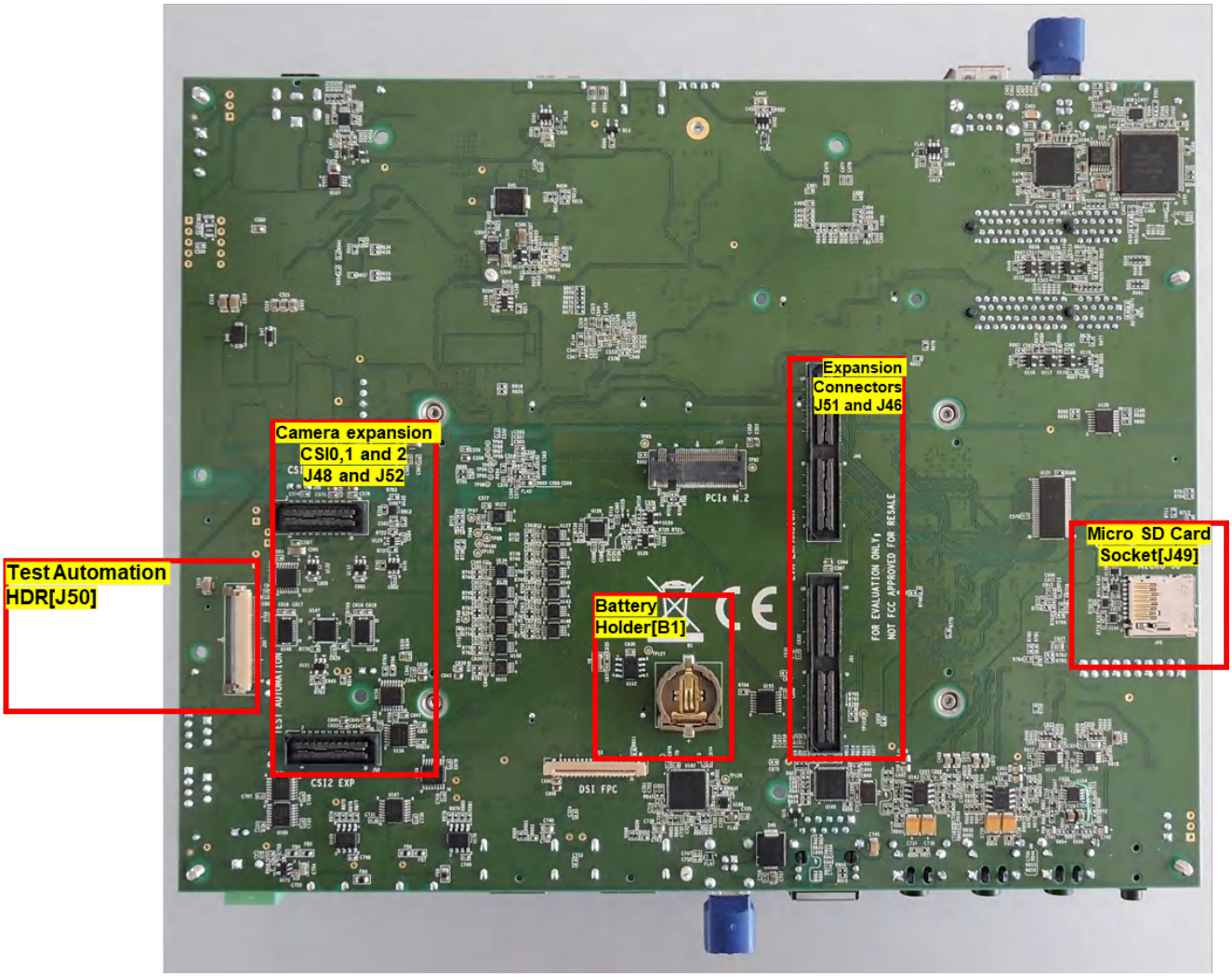


Figure 2-2. Jacinto7 Common Processor Component Identification

Because the Jacinto7 Common Processor board is used with different SOM boards featuring different Jacinto7 processors with different feature sets, some of the board's peripherals/interfaces may not be supported.

2.1 Power Inputs

A power supply is not included with the EVM and must be purchased separately.

External Power Supply or Power Accessory Requirements:

- Output Voltage: 6.5 - 28 VDC
- Output Power Capacity: 100-120 W (depending on use case and connected peripherals)
- Efficiency Level V

Note

TI recommends using an external power supply or power accessory which complies with applicable regional safety standards such as UL, CSA, VDE, CCC, PSE, etc.

2.2 Power Input [J7_CP] with LED for Status [LD2_CP][LD3_CP]

This EVM supports a wide input range of 6.5V to 28V. There is a DC Jack provided for power input. The exact power required for the EVM is largely dependent on the application and connected peripherals. The recommended supplies are listed in Table 2-1. There are many power supply manufacturers and models available in the market, and it is not possible to test the EVM with every combination.

Table 2-1 lists a few recommended supplies that have been tested with the EVM

Table 2-1. Recommended External Power Supply

DigiKey Part#	Manufacturer	Manufacturer Part #
SDI65-12-U-P6-ND	CUI Inc.	SDI65-12-U-P6
SDI65-12-UD-P6-ND	CUI Inc.	SDI65-12-UD-P6

Connector[J7] is a Two pin DC Jack power input connector. This connector mates with the recommend supplies listed in Table 2-1

A green power led [LD2] will be illuminated when a valid power source is connected to either power input. A red power led [LD3] will be illuminated when a power source not within the correct voltage range (less than 6 VDC or greater than 28 VDC).

2.2.1 Power Control [SW2_CP] with LED for Status [LD5_CP] [LD6_CP] [LD7_CP]

The EVM supports a manual switch [SW2] for power control to the EVM. The switch [SW2] is a two-position switch. The OFF position disconnects input power from on-board circuitry. The ON position connects the input power.

Three status LEDs [LD5][LD6][LD7] are used to communicate power status to the user.

Table 2-2. Power Domain Status

LED	'ON' State	'OFF' State
[LD7]	Power switch [SW2] is in the ON position, and input power is being supplied to the EVM.	Power switch [SW2] is in the OFF or there is some other issue causing power to not be supplied.
[LD6]	MCU domain of the EVM is powered	MCU domain of the EVM is not powered/OFF 1
[LD5]	MAIN domain of the EVM is powered	MAIN domain of the EVM is not powered/OFF 1

1. The power management IC (PMIC) includes functions to monitor power domains, including over/under voltage, over current, and residual voltage. If the PMIC detects and error, it may transition to 'safe mode' where it powers down both the MCU and MAIN domains.

2.2.2 Power Budget Considerations

The exact power required for the EVM is largely dependent on the application, usage of the on-board peripherals, and power needs of the add-on devices. Table 2-3 shows the design's power allocations. Again, the input supply must be capable of supplying the power needs of your application.

Table 2-3. Power Allocation

Function	Power	Description
Processor Core	TBD	Processor, DDR Memory
Memory, Non-Volatile	TBD	xSPI NOR, eMMC, Octal NAND etc.
On-Board Peripherals	TBD	Ethernet, Boot Logic, etc.
USB Port(s)	TBD	Type A Port(s), Type C
Expansion Interface(s)	TBD	PCIe, Fusion 2
Camera Port(s)	TBD	RPI Camera(s), Camera Expansion
Display(s)	TBD	DisplayPort, DP transceiver

2.3 User Inputs

The EVM supports several mechanisms for the user to configure, control, and provide input to the system.

2.3.1 Board Configuration Settings [SW3_CP] [SW13_CP] [SW3_SOM]

Dip switches [SW3_CP] [SW13_CP] [SW3_SOM] are used to configure different options available on the EVM.

Table 2-4. Dip Switch [SW3_CP] [SW13_CP] EVM Configuration Settings

[SW2] Position	Default	Function	Description
SW3.1	OFF	Octal-SPI Memory Selection	MUX to select between non-volatile Octal-SPI memory connected to the MCU_OSPI0 interface: ‘0’ (OFF) = xSPI Memory is selected ‘1’ (ON) = Octal-NAND is selected
SW3.2	ON	Debug/Trace Enable	MUX to select between Debug/Trace (connected via MIPI 60 emulation interface) and variety of ‘other’ EVM features (1): ‘0’ (OFF) = ‘Other’ EVM features are selected/enabled ‘1’ (ON) = Debug/Trace is enabled to MIPI-60 emulation interface
SW3.[3:4]	OFF: OFF	USB Type C Mode Selection	Set Mode for USB Type C interface (USB0): '00' (OFF/OFF) = DFP (Downstream Facing Port) ‘01’ (OFF/ON) = DRP (Dual Role Port) ‘1X’ (ON, Don’t Care) = UFP (Upstream Facing Port)
SW3.5	OFF	PCIe0 Mode Selection	Not used with J7AEP SOM
SW3.6	OFF	PCIe1 Mode Selection	Set Mode for PCIe1 (2-Lane) ‘0’ (OFF) = Root Complex ‘1’ (ON) = End Point
SW3.7	ON	IO Voltage for Serial Camera	Configures IO supply for Serial Camera interface. ‘0’ (OFF) = VCC_CSI_IO: 3.3V ‘1’ (ON) = VCC_CSI_IO: 1.8V
SW3.8	ON	Expansion board Selection	Switch is to be used on Expansion board. See specific expansion board User’s Guide for definition. Not used with J7AEP SOM
SW3.9	ON	EVM Configuration EEPROM Write Protection	Sets EVM’s configuration EEPROM Write Protection ‘0’ (OFF) = Configuration EEPROM can be updated ‘1’ (ON) = Configuration EEPROM cannot be updated/protected
SW3.10	ON	User Defined	User Define, maps to IO Expander Input ‘0’ (OFF) = User Defined ‘1’ (ON) = User Defined
SW13.1	OFF	Reserved / Test Mode (Wait Reset)	Reserved, must set to ‘0’ (OFF) for normal EVM operation (only used in Test Mode)
SW13.2	OFF	Reserved / Test Mode (Wait Reset)	Reserved, must set to ‘0’ (OFF) for normal EVM operation (only used in Test Mode)

Table 2-5 shows the J7AEP SOM configuration switches (SW3) to set the various functions on SOM.

Table 2-5. EVM Configuration Switch Function

Switch Name	Default	Function	Operation
SW3.2	ON	Watchdog Disable	Enable/Disable selection for PMIC Watchdog Timer: ‘0’ (OFF) = PMIC watchdog timer is enabled ‘1’ (ON) = PMIC watchdog timer is disabled (Default)
SW3.1	ON	PMIC I2C Selection	MUX to select I2C Interface for PMICs: ‘0’ (OFF) = PMIC I2C to Ext header I2C (test mode only) ‘1’ (ON) = PMIC I2C to SoC WKUP I2C (Default)

2.3.2 Boot Configuration Settings [SW9_CP] [SW8_CP]

Dip switches [SW8] [SW9] are used to configure different boot options available on the processor.

Two common boot mode settings are documented below. For a complete definition and list of all supported modes, see the TDA4VE-Q1/TDA4VL-Q1/TDA4AL-Q1 Technical Reference Manual (TRM).

No Boot: The processor will not attempt to boot any software. This is often selected when downloading software using an emulator.

SW9 [8:1] = 0000 1110

SW8[8:1] = 0001 0001

SD Card Boot: The processor will attempt to boot from image on SD Card.

SW9[8:1] = 0000 0000 (Default)

SW8 [8:1] = 0100 0001 (Default)

The Dip Switch boot tables are formatted to align with how the settings are documented in the TRM.

Table 2-6. Dip Switch [SW9] Configuration for MCU_BOOTMODE

MCU_BOOTMODE Pin Mapping							
0:2 [SW9.1]	3 [SW9.2]	4 [SW9.3]	5 [SW9.4]	6 [SW9.5]	7 [SW9.6]	8 [SW9.7]	9 [SW9.8]
PLL Configuration Must be set to '0' (OFF)	Primary Boot Mode A			MCU Only	Reserved Must be set to '0' (OFF)	POST Config	

Table 2-7. Dip Switch [SW8] Configuration for BOOTMODE

BOOTMODE Pin Mapping							
0 [SW8.1]	1 [SW8.2]	2 [SW8.3]	3 [SW8.4]	4 [SW8.5]	5 [SW8.6]	6 [SW8.7]	7 [SW8.8]
Primary Boot B	Backup Boot Mode			Primary Boot Mode Config			Backup Boot Mode Config

2.3.3 Reset Pushbuttons [SW7_CP] [SW6_CP] [SW5_CP] [SW4_CP]

When pressed, the specific EVM domain is issued a reset, and is held in reset until the button is released.

Table 2-8. Reset Pushbuttons

Push Button	Domain	Function	Description
[SW7]	All	Power-On Reset	Power-On/Cold Reset for EVM, resets both processor domains (MCU, MAIN) and all EVM peripherals.
[SW5]	MCU	MCU Warm Reset	Warm reset for MCU domain
[SW4]	MAIN	Power-On Reset	Power-On/Cold Reset for MAIN domain, MCU domain is unaffected
[SW6]		Warm reset for MAIN domain	Warm reset for MAIN domain

2.3.4 User Pushbuttons [SW2] [SW11] [SW10] [SW1] [SW12] with User LED Indication [LD9] [LD8]

The pushbutton(s) primary function is to be user/application defined. The inputs can be monitored and/or configured to generate an interrupt. Some pushbutton(s) support a secondary function. They can be used to wake the system from a low power mode. Table 2-9 lists a complete definition for each pushbutton.

Table 2-9. User Pushbuttons and LEDs

Push Button	Primary Function	Alternate Function
[SW2_SOM]	User Define (GPIO0_11)	Wake from low power mode (MAIN IO_RET)

Table 2-9. User Pushbuttons and LEDs (continued)

Push Button	Primary Function	Alternate Function
[SW11_CP]	User Define (WKUP_GPIO0_7)	Wake from software-initiated power-down (OFF)
[SW10_CP]	User Define (GPIO0_0)	External Interrupt (EXTINTn)
[SW1_SOM]	User Define (WKUP_GPIO0_70)	Wake from low power mode (MCU IO_RET)
[SW12_CP]	PMIC_GPIO4	Wake from low power mode (any LP_STBY)
LED	**Primary Function**	**Alternate Function**
[LD9_CP]	User Define (IO_EXP 0x22, bit P26)	None
[LD8_CP]	User Define (IO_EXP 0x22, bit P27)	None

Note

The user-defined pushbutton inputs and LED outputs are connected to processor pins. The pins can be accessed via GPIO functions of the pin. The specific pin/GPIO used is identified in the table.

2.4 Standard Interfaces

The EVM provides industry standard interfaces/connectors to connect a wide variety of peripherals. As these interfaces are standard, specific pin information is not provided in this document.

2.4.1 Uart-Over-USB [J43_CP] [J44_CP] with LED for Status [LD10_CP] [LD11_CP]

Five UART ports of the processor are interfaced with the UART-over-USB transceiver(s). When the EVM'sUSB micro-B connectors [J43] and/or [J44] are connected to a Host-PC using supplied USB cable (Type-A to Micro-B), the computer can establish Virtual Com Port(s) to be used with any terminal application. Virtual Com Port drivers for the transceiver(s) can be obtained from:

https://www.ftdichip.com/Products/ICs/FT2232H.html

https://www.ftdichip.com/Products/ICs/FT4232H.html

Once installed, the Host-PC will create the Virtual Com Ports (two ports for FT2232, 4 ports for FT4232). Depending on the other Host-PC resources available, the Com Ports may not be located at COM1-2 and/or COM1-4. However, they will remain in the same numerical order for each transceiver.

The circuit(s) are powered from USB bus power and therefore the COM connection will not be lost when the EVM power is removed. LED(s) [LD11] [LD10] are used to indicate an active COM connection with Host-PC.

Table 2-10. UART to COM Port Mapping [J43] with Status [LD10]

UART Port	Host-PC COM Port
MCU_UART0	COM 1
WKUP_UART0	COM 2

Table 2-11. UART to COM Port Mapping [J44] with Status [LD11]

UART Port	Host-PC COM Port
MAIN_UART8	COM 1
MAIN_UART5	COM 2
MAIN_UART2	COM 3
NA	COM 4

The EEPROM of FTDI bridges are programmed with the CPB serial number, users to identify the connected COM port with board serial number when one or more boards connected to the computer.

Note

The maximum length for the IO cables should not exceed three meters.

2.4.2 Gigabit Ethernet [J35_CP] with Integrated LEDs for Status

A wired Ethernet network is supported via RJ45 cable interface [J8], and is compatible with IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T specifications. The connector includes status indicators for link and activity.

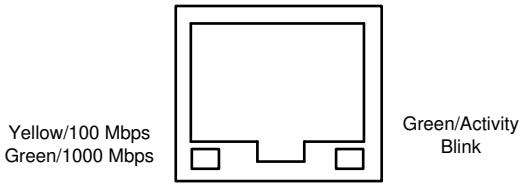


Figure 2-3. RJ45 LED Indicators [J35]

Power-Over-Ethernet (PoE) is not supported.

2.4.3 USB3.1 Gen1 Interface [J5_CP]

The EVM supports one USB3.1 Gen1 Type C interface [J5], which can function as DFP, UFP, or DRP. For details on how to select the USB mode, see Section 2.3.1. The VBUS output for this port is limited to 1.5 A. When operating as UFP, the EVM cannot be powered from this port.

The processor supports a single USB interface. Therefore, the user must configure for either the USB3.1 Type C interface or the USB2.0 Type A interface. Both cannot be operated simultaneously.

2.4.4 USB2.0 Interface [J6_CP]

The EVM supports two USB2.0 Type A interfaces [J6] via an on-board USB hub. These ports can only function as Host. The VBUS output for each port is limited to 0.5 A.

The processor supports a single USB interface. Therefore, the user must configure for either the USB2.0 Type A interface or the USB3.1 Type C interface. Both cannot be operated simultaneously.

Note

The USB2.0 Micro-B connectors [J43] [J44] and [J3] are discussed in the UART-over-USB and/or Emulation sections. While these are USB interfaces, they are dedicated to peripherals and cannot be used for USB development.

2.4.5 PCIe Card Slot [J8_CP]

One lane of PCIe (Gen3) is supported on the EVM. The Common Processor board supports two PCIe slots, however only one PCIe slot [J8] is supported with processor module. The second PCIe connector is unused. The REFCLK is automatically generated (on-board).

2.4.6 Display Port Interfaces [J36_CP] [J37_CP]

The EVM supports two DisplayPort panels via standard DP cables interfaces [J36] [J37]. The processor's native DP [J37] supports resolutions up to 4K UHD (3840x216) including MST (Multi-Stream Transport) for connecting multiple panels. The second DisplayPort [J36] is supported via DP bridge device (SN65DSI86) and supports resolutions up to 1080p. The second DisplayPort (via bridge device) does not support integrated audio.

2.4.7 MicroSD Card Cage [J49_CP]

The EVM supports a micro-SD card cage [J49]. It supports UHS-1 class memory cards, including SDHC and SXDC. The connector is a push-push connector, meaning your push to insert the card and push again to eject/remove the card. A micro-SD card is included with the EVM kit.

2.4.8 Stereo Audio Interface [LINE-IN J38_CP, LINE-OUT J41B_CP, J40B_CP]

The EVM supports dual stereo inputs[J38] and 2x stereo line outputs[J40B & J41B]. Note the Common Processor board supports additional audio input/output channels not used with this system. Audio Port Interface assignment in the Common processor board is shown in the below Figure 2-4. The analog audio is supported via the PCM3168A codec, which supports sampling rates up to 96-KHz ADC/192-KHz DAC.

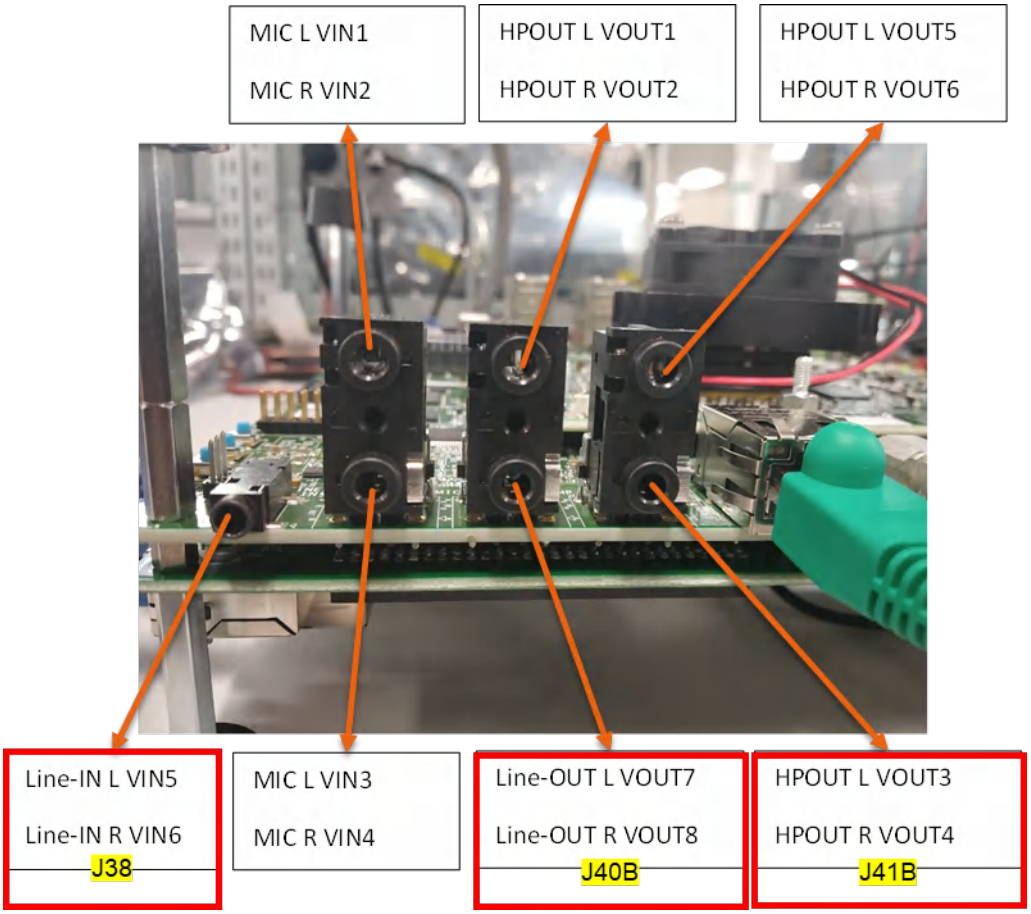


Figure 2-4. Audio Port Interface Assignment [J38,J40B & J41B]

2.5 Expansion Interfaces

The EVM provides several expansion interfaces that have non-standard/custom pinouts. Each of these interfaces are introduced and specific pin information is provided.

Note: that some of the interfaces include 'Direction' information. This is relative to the EVM, so INPUT is input to the EVM/output of the connected device. OUTPUT is output of the EVM/input to the connected device.

2.5.1 Heatsink [ACC3_SOM] with Fan Header [J15_CP]

The heatsink supports cooling of the device at ambient temperatures. If your environment or use case requires additional cooling, a fan can be added to the heatsink. The fan connector is a 3-pin header (440054-3 from TE Connectivity) and supports 12VDC fans. Mating connector is 440129-3 and 1735801-1.

Table 2-12. Fan Header Pin Definition [J15]

Pin #	Pin Name	Description	Direction
1	<open>	Unconnected	n/a
2	12V	12V Supply	Output
3	GND	Ground	

2.5.2 CAN-FD Connectors

The EVM supports up to Six [6] CAN Bus interfaces.

Table 2-13. CAN-FD Interface Assignment

Connector	Process Resource
J30_CP	MCU MCAN0
J31_CP	MCU MCAN1
J27_CP	MAIN_MCAN3
J28_CP	MAIN_MCAN5
J10_SOM	MAIN_MCAN16

Each Controller Area Network (CAN) Bus interface is supported on a 3-pin, 2.54-mm pitch header. The interface meets ISO 11898-2 and ISO 11898-5 physical standards and supports CAN and optimized CAN-FD performance up to 8 Mbps. Each includes CAN Bus end-point termination. If the EVM is included in a network with more than two nodes, the termination my need to be adjusted.

Table 2-14. CAN-FD Header Pin Definition

Pin #	Pin Name	Description	Direction
1	CAN-H	High-Level CAN Bus Line	Bi-Dir
2	GND	Ground	
3	CAN-L	Low-Level CAN Bus Line	Bi-Dir
4	WAKE (J30, J27 only)	Assert PHY Wake Function	Input

2.5.3 Camera Interfaces [J52_CP]

The EVM includes 40-pin (2x20, 0.5-mm pitch) high speed connectors [J52] for connecting with cameras and other image capture devices. This expansion connector can support up to two CSI2 interfaces. The bandwidth of each CSI2 interface is 10Gbps (4 data lanes each up to 2.5Gbps). The expansion connector also includes power and other IO for communicating with the capture devices. All control signals are configurable for 3.3-V or 1.8-V IO voltage levels. See Section 2.3.1 for configuration details.

Table 2-15. High Speed Camera Expansion Pin Definition [J52]

Pin #	Pin Name	Description Processor Resource for [J52]	Dir
1	Power	Power, 12 V	Output
2	I2C_SCL	I2C Bus Clock (I2C5)	Bi-Dir
3	Power	Power, 12 V	Output
4	I2C_SDA	I2C Bus Data (I2C5)	Bi-Dir
5	CSIa_CLK_P	CSI Port 0 / Port 2	Input
6	GPIO0/PWMA	IO Expander 0x20 bit P1 / Open	Output
7	CSIa_CLK_N	CSI Port 0 / Port 2	Input
8	GPIO1/PWMV	IO Expander 0x20 bit P2 / bit P4	Bi-Dir
9	CSIa_D0_P	CSI Port 0 / Port 2	Input
10	REFCLK	25MHz Reference Clock	Output
11	CSIa_D0_N	CSI Port 0 / Port 2	Input
12	GND	Ground	
13	CSIa_D1_P	CSI Port 0 / Port 2	Input
14	RESETz	GPIO, IO Expander 0x20 bit P0	Output
15	CSIa_D1_N	CSI Port 0 / Port 2	Input
16	GND	Ground	
17	CSIa_D2_P	CSI Port 0 / Port 2	Input

Table 2-15. High Speed Camera Expansion Pin Definition [J52] (continued)

Pin #	Pin Name	Description Processor Resource for [J52]	Dir
18	GPIO2	GPIO0_26 / IO Expander 0x20 bit P5	Bi-Dir
19	CSIa_D2_N	CSI Port 0 / Port 2	Input
20	GPIO3	IO Expander 0x20 bit P3 / bit P6	Bi-Dir
21	CSIa_D3_P	CSI Port 0 / Port 2	Input
22	GPIO4	GPIO0_28 / IO Expander 0x20 bit P7	Bi-Dir
23	CSIa_D3_N	CSI Port 0 / Port 2	Input
24	GND	Ground	
25	CSIb_CLK_P	CSI Port 1 / Open	Input
26	CSIb_D3_P	CSI Port 1 / Open	Input
27	CSIb_CLK_N	CSI Port 1 / Open	Input
28	CSIb_D3_N	CSI Port 1 / Open	Input
29	CSIb_D0_P	CSI Port 1 / Open	Input
30	Power	Power, 3.3 V	Output
31	CSIb_D0_N	CSI Port 1 / Open	Input
32	Power	Power, 3.3 V	Output
33	CSIb_D1_P	CSI Port 1 / Open	Input
34	Power	Power, 3.3 V	Output
35	CSIb_D1_N	CSI Port 1 / Open	Input
36	Power	Power, 3.3 V	Output
37	CSIb_D2_P	CSI Port 1 / Open	Input
38	Power	Power, IO Level (1.8 V or 3.3 V)	Output
39	CSIb_D2_N	CSI Port 1 / Open	Input
40	Power	Power, IO Level (1.8 V or 3.3 V)	Output

Note

In the DIR column, output is to the expansion module, input is from the expansion module. Bi-Dir signals can be configured as either input or output.

2.5.4 Automation and Control Connector [J50_CP]

The EVM supports an interface to allow for automated control of the system, including functions like on/off, reset, and boot mode settings.

Table 2-16. Test Automation Interface Pin Definition [J50]

Pin #	Pin Name	Description	Dir
1	Power	Power, 3.3 V	Output
2	Power	Power, 3.3 V	Output
3	Power	Power, 3.3 V	Output
4-6	<open>		
7	GND	Ground	
8-15	<open>		
16	GND	Ground	
17-24	<open>		
25	GND	Ground	
26	POWERDOWNz	EVM Power Down	Input
27	PORz	EVM Power-On/Cold Reset (MCU_PORz)	Input

Table 2-16. Test Automation Interface Pin Definition [J50] (continued)

Pin #	Pin Name	Description	Dir
28	RESETz	EVM Warm Reset (RESETz)	Input
29	<open>		
30	INT1z	EXTINT / GPIO0_0	Input
31	INT2z	WKUP_GPIO0_7	Bi-Dir
32	<open>		
33	BOOTMODE_RSTz	Bootmode Buffer Reset	Input
34	GND	Ground	
35	<open>		

Note

In the DIR, column, output is to the test automation controller, input is from the automation controller. Bi-Dir signals can be configured as either input or output.

Note

The Signal polarity is defined with a trailing 'z' in the Pin Name, which indicates the signal is active LOW. For example, POWERDOWNz is an active low signal, meaning '0' = EVM is Powered Down, '1' = EVM is NOT Powered Down.

2.5.5 ADC [J23_CP]

The EVM supports an interface for connecting external peripherals with ADC inputs. A 20-pin, dual row, 2.54-mm pitch pin header [J23] supports eight (8) input channels to ADC and trigger, and ADC reference signals. See the EVM schematic for pinout details.

2.5.6 CSI-TX [J10_SOM]

The J7AEP SOM Board in the EVM includes a 40-pin (2x20, 0.5-mm pitch) high speed camera transmit interface [J10]. The expansion connector supports a single CSI2-TX (4Lane) interface. The interface is designed for internal testing and may not include all the required power/signals for interfacing with a display. See schematic for connector pinout details.

2.5.7 Accessory Power Connector [J42_CP]

A power output connector [J42] is provided for conditions where an expansion board requires additional power. The 2-pin connector (Phoenix 1757242) supplies a regulated 12-V output, up to 5000 mA. Mating connector is TBD.

Table 2-17. Accessory Power Connector [J42]

Pin #	Pin Name	Description	Dir
1	GND	Ground	
2	Power	Power, 12 V	Output

3 Circuit Details

This sections provides additional details on the EVM design and processor connections.

3.1 Top Level Diagram

Figure 3-1 shows the functional block diagram of the EVM Board.

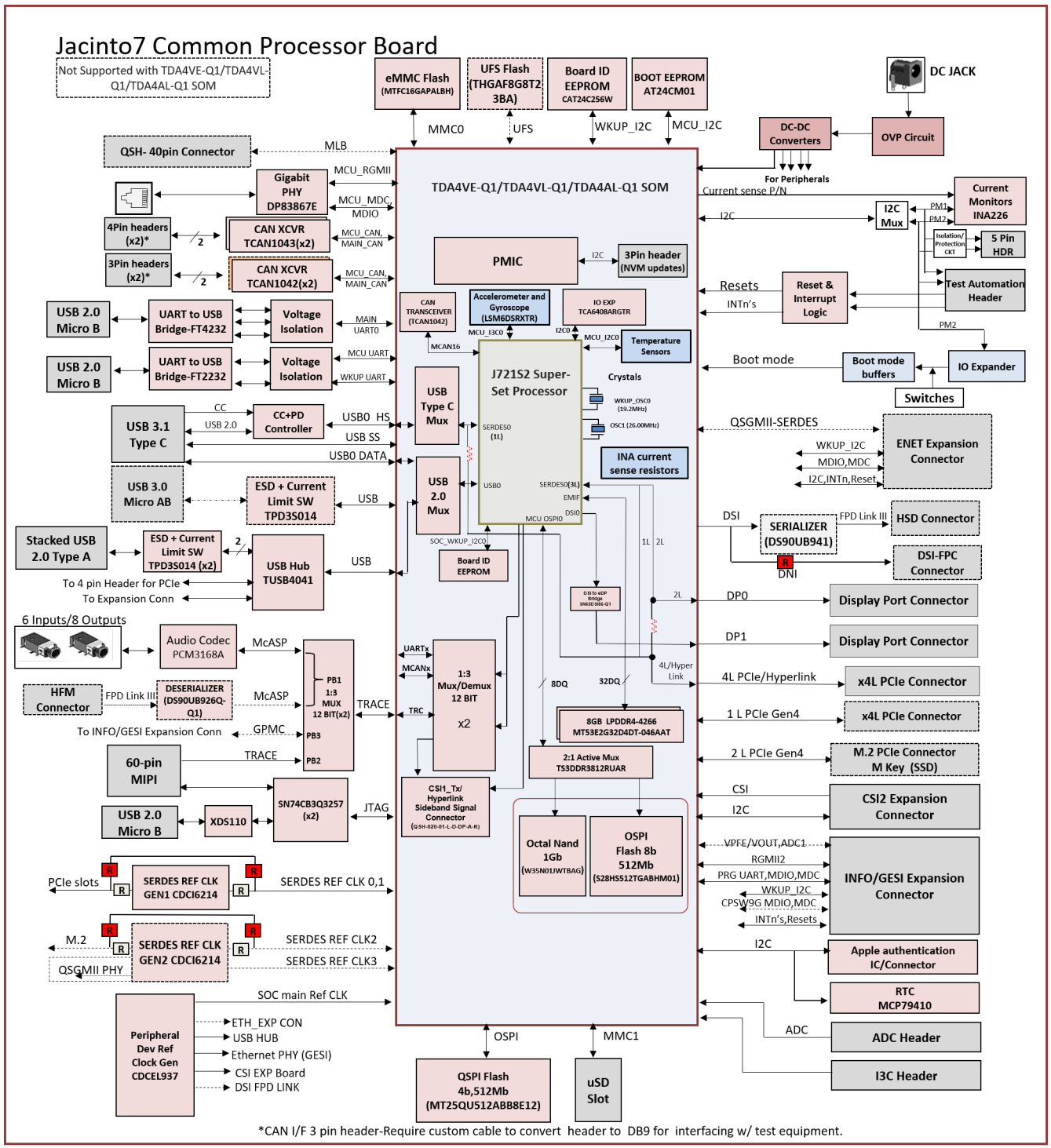


Figure 3-1. EVM Functional Block diagram

3.2 Interface Mapping

The EVM Interface Mapping table is provided in Table 3-1.

Table 3-1. EVM Interface Mapping Table

Connected Peripheral	Processor Resource(s)	Component/Part Numbers
Memory, LPDDR4 DRAM	DDR0, DDR1	Micron, MT53E2G32D4DT-046 AAT: A
Memory, OSPI	MCU_OSPI0(1)	Cypress, S28HS512TGABHM010
Memory, Octal NAND		Winbond, W35N01JWTBAG
Memory, eMMC	MMC0	Micron, MTFC16GAPALBH-AAT ES
Memory, Micro SD Socket	MMC1	
Memory, Board ID EEPROM	WKUP_I2C0	On-Semi, CAV24C256YE-GT3
Memory, Boot EEPROM	MCU_I2C0	Microchip Tech, AT24CM01
Ethernet, RGMII	MCU_RGMII1	Texas Instruments, DP83867ERGZT
Memory, OSPI	MCU_OSPI1	Micron, MT25QU512ABB8E12
USB 3.1 Type C + PD + CC Controller	SERDES0 (TX1/RX1)	Texas Instruments, TUSB321RWBR
USB 2.0 (HUB)	USB0	Texas Instruments, TUSB4041IPAPR
Audio Codec	McASP4	Texas Instruments, PCM3168APAP
PCIe2/Hyperlink, x4 Lane Socket (x1 Lane)	SERDES0 (TX0/RX0)	
UART Terminal (UART-to-USB)	UART 8,5 &2	FTDI, FT4232HL
UART Terminal (UART-to-USB)	WKUP_UART0 & MCU_UART0	FTDI, FT2232HL
CAN (5x)	MCU_MCAN0, MCAN3	Texas Instruments, TCAN1043-Q1
	MCU_MCAN1, MCAN5, MCAN16, MCAN4	Texas Instruments, TCAN1042HGVD
CSI	CSI0, CSI1, CSI_TX	QSH Connector-J52(QSH-020-01-L-D-DP-A-K)
Display Port	DP0	
	DSI1	Texas Instruments, SN65DSI86IPAPQ1
ADC Header	MCU_ADC0, MCU_ADC1	

(1) MCU_OSPI0 is connected to two different flash memories, target memory selected via a mux.

3.3 I2C Address Mapping

Table 3-2 shows the complete I2C address mapping details on the EVM.

Table 3-2. I2C Mapping Table

Connected Peripheral	Processor Resources		J7AEPComponent / Part Number
	I2C Port	Address	
Board ID EEPROM	WKUP_I2C0	0x50, 0x51,	On-Semi, CAT24C256WE-GT3
Power Management IC (PMIC)	WKUP_I2C0	0x48, 0x49, 0x4A & 0x4B	Texas Instruments, TPS659413
Power Management IC (PMIC)	WKUP_I2C0	0x4C, 0x4D, 0x4E & 0x4F	Texas Instruments, TPS659411
Power Management IC (PMIC)	WKUP_I2C0	0x58, 0x59, 0x5A & 0x5B	Texas Instruments, P876411A5RQKRQ1
Temperature Sensors	MCU_I2C0	0x48, 0x49	Texas Instruments, TMP100NA/3K
Boot EEPROM	MCU_I2C0	0x50, 0x51	Texas Instruments, AT24CM01
8-bit I2C GPIO Expander	I2C0	0x21	Texas Instruments, TCA6408ARGTR
SerDes Clock gen #1 Optional	I2C0	Optional	Texas Instruments, CDCI6214
SerDes Clock gen #2	I2C0	0x77,0x76	Texas Instruments, CDCI6214
Peripheral Clock Gen	I2C0	0x6D	Texas Instruments, CDCEL937-Q1

Table 3-2. I2C Mapping Table (continued)

Connected Peripheral	Processor Resources		J7AEPComponent / Part Number
	I2C Port	Address	
16bit I2C GPIO EXPANDER1	I2C0	0x20	Texas Instruments, TCA6416ARTWR
24bit I2C GPIO EXPANDER2	I2C0	0x22	Texas Instruments, TCA6424ARGJR
8-bit I2C GPIO Expander4	I2C4	0x20	Texas Instruments, TCA6408ARGTR
DSI TO eDP BRIDGE	I2C4	0x2C	Texas Instruments, SN65DSI86IPAPQ1
I2C Switch for Automation header	I2C1	0x22	Texas Instruments, TCA6424ARGJR
Current Monitors and Header	I2C1	0x40 to 0x4F	Texas Instruments, INA226AIDGSR
8bit GPIO Expander3	I2C3	0x20	Texas Instruments, TCA6408ARGTR
FPD Link iii Deserializer	I2C3	0x2C	Texas Instruments, DS90UB926Q-Q1
AUDIO IF Codec	I2C3	0x44	Texas Instruments, PCM3168A-Q1
I2C IO Expander	I2C5	0x41	Texas Instruments, PCA9536DGKR
Expansion, Camera	I2C5	Add-On	

3.4 GPIO Mapping

The General Purpose IOs (GPIO) of the EVM are broken into two major groups, IO connected to J7AEP or connected to I2C-based Expander. They are separated into Table 3-3 and Table 3-4.

Table 3-3. GPIO Mapping for Processor IO

GPIO Number	Function	Input/Output	Remarks
WKUP_GPIO0_0	MCU CAN0 Enable	Output	‘0’ – CAN Enable ‘1’ – CAN is disabled (Default)
WKUP_GPIO0_1	Boot EEPROM Write protect	Output	‘0’ – Memory is NOT Write-Protected ‘1’ – Memory is Write-Protected (default)
WKUP_GPIO0_2	MCU CAN1 Standby	Output	‘0’ – Normal Mode ‘1’ – Standby Mode (default)
WKUP_GPIO0_56	MCU_RGMII1_Reset	Output	‘0’ – Resets Ethernet physical Transceiver ‘1’ – Normal mode(default)
WKUP_GPIO0_7	Push-button Interrupt, User Defined/Wake S2R	Input	'0' - Interrupt pending '1' - Normal operation(default)
WKUP_GPIO0_6	Flash Memory Selection	Output	'0' - OSPI0(default) '1' - OCTAL NAND
WKUP_GPIO0_39	Interrupt from PMIC	Input	‘0’ – Active Interrupt Request ‘1’ – No Interrupt Requested (default)
WKUP_GPIO0_30	Interrupt from OSPI Flash	Input	‘0’ – Interrupt from OSPI ‘1’ – No interrupt(default)
WKUP_GPIO0_3	MCU Ethernet Interrupt	Input	'0' - Interrupt pending '1' - Normal operation(default)
WKUP_GPIO0_55	System Power Down	Output	'0' - normal operation(default) '1' - system power down
WKUP_GPIO0_69	MCU CAN0 Standby	Output	‘0’ – Normal Mode ‘1’ – Standby Mode (default)
WKUP_GPIO0_57	Interrupt from I3C Gyroscope sensor	Input	'0' - Interrupt pending '1' - Normal operation(default)
WKUP_GPIO0_70	Push-button wake signal	Input	'0' – wake signal '1' - normal operation(default)
GPIO0_0	Push-button Interrupt, User Defined	Input	'0' - Interrupt pending '1' - Normal operation(default)
GPIO0_11	Push-button wake signal	Input	'0' – wake signal '1' - normal operation(default)
GPIO0_18	IO Expander Interrupt (Bus I2C5)	Input	'0' - interrupt pending '1' - no interrupt(default)
GPIO0_25	IO Expander Interrupt (Bus I2C0)	Input	'0' - interrupt pending '1' - no interrupt
GPIO0_8	SD Card IO Voltage Selection	Output	0’ – SD Card IO Voltage is 1.8V ‘1’ – SD Card IO Voltage is 3.3V (default)
GPIO0_26	CSI2 Expansion Board Specific.	I/O	Camera Expansion Board Specific (Pin 18)

Table 3-3. GPIO Mapping for Processor IO (continued)

GPIO Number	Function	Input/Output	Remarks
GPIO0_28	CSI2 Expansion Board Specific.	I/O	Camera Expansion Board Specific (Pin 22)
GPIO0_51	CP Board - PM I2C Mux selection. GESI - Boosterpack_GPIO1	Output	'0' - SOC_I2C2_SCL/SDA -> PM1_SCL/SDA '1' - SOC_I2C2_SCL/SDA -> PM2_SCL/SDA

Note

GPIO functions sometimes share pins with other functions. The default state of these IO is set by the MCU_BOOTMODE and/or BOOTMODE pins. For the EVM, these pins are set via dip switches.

Table 3-4. GPIO Mapping for Expansion IO

I2C0/TCA6416 Addr: 0x21	Function	Input/Output	Remarks
P00	USB2.0 Mux Select line	Output	'0' – USBC path selected
			'1' - USB Hub path is selected
P01	Select line for MAIN MUX Control #1	Output	Refer schematic for the details of TRC/CAN UART/ Hyperlink sideband signals mux selection
P02	Select line for MAIN MUX Control #2	Output	
P03	Select line for MAIN MUX Control #3	Output	
P04	GESI Expansion Board Specific, RST# to RGMII PHY	Output	'0' – RGMII Phy is Reset (default) '1' –RGMII Phy is enabled/active
P05	Enable to DSI to eDP Bridge	Output	0' – DisplayPort Transmitter is disabled (default) '1' – DisplayPort Transmitter is enabled
P06	Expansion Board Specific	Bi-Dir	'0' – LIN Bus PHY is Disabled (default)
			'1' – LIN Bus PHY is Enabled
P07	Standby signals for CAN Transceivers	Output	'0' – Normal Mode
			'1' – Standby Mode (default)
I2C5/TCA6408 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P00	Camera Expansion Reset (#1 and #2)	Output	0' – Camera Expansion is disabled/Reset (default) '1' – Camera Expansion is enabled/active
P01	Camera Expansion #1 GPIO #0	Bi-Dir	Camera Expansion Board Specific (Pin 6)
P02	Camera Expansion #1 GPIO #1	Bi-Dir	Camera Expansion Board Specific (Pin 8)
P03	Camera Expansion #1 GPIO #3	Bi-Dir	Camera Expansion Board Specific (Pin 20)
P04	Camera Expansion #2 GPIO #1	Bi-Dir	Camera Expansion Board Specific (Pin 8) (Reserved)
P05	Camera Expansion #2 GPIO #2	Bi-Dir	Camera Expansion Board Specific (Pin 18) (Reserved)
P06	Camera Expansion #2 GPIO #3	Bi-Dir	Camera Expansion Board Specific (Pin 20) (Reserved)
P07	Camera Expansion #2 GPIO #4	Bi-Dir	Camera Expansion Board Specific (Pin 22) (Reserved)
I2C0/TCA6416 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**

Table 3-4. GPIO Mapping for Expansion IO (continued)

I2C0/TCA6416 Addr: 0x21	Function	Input/Output	Remarks
P00	PCIe1 mode selection	Input	0' – Processor/PCIe1 is Root Complex '1' – Processor/PCIe1 is End Point (Note Default is set via dip switch)
P01	PCIe1 PERSTz status	Input	0' – PCIe1 Reset is asserted '1' – PCIe1 Reset is NOT asserted
P02	PCIe1 PERSTz Output (Root Complex Mode)	Output	'0' – PCIe1 Reset is asserted '1' – PCIe1 Reset is NOT asserted
P03	PCIe1 PERSTz to PORz (End Point Mode)	Output	0' – PCIe1 PERSTz is separate from PORz '1' – PCIe1 PERSTz can control PORz
P04	PCIe0 mode selection	Input	0' – Processor/PCIe0 is Root Complex '1' – Processor/PCIe0 is End Point (Note Default is set via dip switch) (Reserved)
P05	PCIe0 PERSTz status	Input	0' – PCIe0 Reset is asserted '1' – PCIe0 Reset is NOT asserted (Reserved)
P06	PCIe0 PERSTz Output (Root Complex Mode)	Output	'0' – PCIe0 Reset is asserted '1' – PCIe0 Reset is NOT asserted (Reserved)
P07	PCIe0 PERSTz to PORz (End Point Mode)	Output	0' – PCIe0 PERSTz is separate from PORz '1' – PCIe0 PERSTz can control PORz(Reserved)
P10	PCIe1 Card Presence Detection	Input	'0' – Card detected for PCIe1 '1' – Card NOT detected for PCIe1 (default)
P11	PCIe0 Card Presence Detection	Input	0' – Card detected for PCIe0 '1' – Card NOT detected for PCIe0 (default)(Reserved)
P12	External Clock enabled for PCIe0	Output	0' – External Clock is NOT enabled for PCIe0 '1' – External Clock is enabled for PCIe0 (default)(Reserved)
P13	External Clock enabled for PCIe1	Output	0' – External Clock is NOT enabled for PCIe1 '1' – External Clock is enabled for PCIe1 (default)

Table 3-4. GPIO Mapping for Expansion IO (continued)

I2C0/TCA6416 Addr: 0x21	Function	Input/Output	Remarks
P14	GESI Expansion Mux Control	Output	Refer GESI expansion board user guide for more detail.
P15	GESI Expansion Mux Control	Output	
P16	GESI Expansion Mux Control	Output	
P17	GESI Expansion Ethernet Reset	Output	
I2C0/TCA6424 Addr: 0x22	**Function**	**DIR/Level**	**Remarks**
P00	Reset to apple authentication header	Output	'0' – Device is in reset '1' – Device normal operation (Reserved)
P01	MLB interface specific	Output	Reserved (MLB interface is not supported)
P02	SD Card Power Enable/Reset	Output	'0' – SD Card Power is disabled/ Reset '1' – SD Card Power is enabled/ active (default)
P03	USB Type C Power Enable	Output	'0' – USB Type C Power is disabled '1' – USB Type C Power is enabled (default)
P04	USB Type C Mode Selection #1	Input	'00' = DFP (Downstream Facing Port) '01' = DRP (Dual Role Port) 1x' = UFP (Upstream Facing Port) (Note Default is set via dip switch [SW3 bits 3:4])
P05	USB Type C Mode Selection #2	Input	
P06	ENABLE signal to MCAN3 Phy	Output	MCAN3 PHY Enable '0' - device disabled '1' normal operation
P07	Standby signals for MCAN3 Transceivers	Output	MCAN3 PHY Standby '0' - device standby '1' - normal operation)
P10	Power Measurement Bus Enable	Output	0' – Enabled access to INA from processor (I2C1) (default) '1' – Disables access to INA from processor
P11	TRACE MUX Control Select line #1 on CP	Output	Signal Mux Control, DIP switch allow default to either Trace or GPMC. · TRACE with MIPI-60 Interface (set to '1 / 1') · Expansion for GPMC Support (set to '1 / 0') -P12 Audio Codec/Tuner Support (set to '0 / 1')
P12	TRACE MUX Control Select line #2 on CP	Output	
P13	MLB Mux selection	Output	Reserved (MLB interface is not supported)
P14	MCAN Interface mux selection	Output	'0' - MCAN5 '1' - Expansion/EQEP
P15	MDIO Mux selection	Output	Expansion board specific (Not supported)

Table 3-4. GPIO Mapping for Expansion IO (continued)

I2C0/TCA6416 Addr: 0x21	Function	Input/Output	Remarks
P16	PCIe Clk req Mux selection	Output	'0' - PCIe Clk req Path is selected '1' - UB926 GPIO path is selected
P17	External Clock Generator Reset	Output	0' – Expansion board is RESET '1' – Expansion board is NOT reset (default)
P20	ENET Expansion power down	Output	Reserved(ENET expansion is not supported)
P21	ENET expansion reset	Output	Reserved(ENET expansion is not supported)
P22	ENET expansion I2C Mux sel	Output	Reserved(ENET expansion is not supported)
P23	ENET Expansion spare GPIO	Bi-Dir	Reserved(ENET expansion is not supported)
P24	Reset to M.2 PCIe	Output	Reserved(ENET expansion is not supported)
P25	User Dip Switch Input [SW3]	Input	0' – Dip Switch SW2 position 10 set to OFF '1' – Dip Switch SW2 position 10 set to ON (Note Default is set via dip switch SW3.10)
P26	User LED [LD9]	Output	'0' – LED [LD9] is ON '1' – LED [LD9] is OFF (default)
P27	User LED [LD8]	Output	'0' – LED [LD8] is ON '1' – LED [LD8] is OFF (default)
I2C3/TCA6408 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P00	Audio Codec Enable/Reset	Output	'0' – Audio Codec is disabled/ Reset (default) '1' – Audio Codec is enabled/ active
P01	Reserved / Unused	Bi-Dir	Reserved / Unused
P02	RESET to UB926	Output	Reserved (UB926 is not supported)
P03	UB926 PLL lock status	Input	Reserved (UB926 is not supported)
P04	Power enable to UB926	Output	Reserved (UB926 is not supported)
P05	Tuner reset to UB926	Output	Reserved (UB926 is not supported)
P06	Spare GPIO to UB926	Bi-Dir	Reserved (UB926 is not supported)
P07	Unused	NA	NA
I2C4/TCA6408 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P00	DisplayPort #0 Power Enable	Output	'0' – DisplayPort Power is disabled (default) '1' – DisplayPort Power is enabled
P01	DisplayPort #1 Power Enable	Output	'0' – DisplayPort Power is disabled (default) '1' – DisplayPort Power is enabled

Table 3-4. GPIO Mapping for Expansion IO (continued)

I2C0/TCA6416 Addr: 0x21	Function	Input/Output	Remarks
P02	Power-Down to UB981	Output	Reserved (UB981 is not supported)
P03	GPIO to UB981 #1	Bi-Dir	Reserved (UB981 is not supported)
P04	GPIO to UB981 #2	Bi-Dir	Reserved (UB981 is not supported)
P05	GPIO to UB981 #3	Bi-Dir	Reserved (UB981 is not supported)
P06	GPIO to UB981 #4	Bi-Dir	Reserved (UB981 is not supported)
P07	Power enable to UB981	Output	Reserved (UB981 is not supported)

3.4.1 Power Monitoring

The EVM includes power monitoring/measurement of 32 discrete power rails. The on-board analog-to-digital converters (INA226) are accessed via I2C. The processor can access using I2C1. The test automation [J50_CP] can access the I2C bus, or it can be access externally via 5-pin header [J12_CP]. Due to the number of rails, the ADCs are split across two I2C buses. Selection of the buses is done via mux setting.

Table 3-5. Power management IC's

Bus #1 Address	Power Rail	Nom V	Shunt Value	Bus #2 Address	Power Rail	Nom V	Shunt Value
0x40	Processor MCU VDD (VDD_MCU_0V85)	0.85	10m-ohm	0x40	Processor IO at 1.8V (VDD_IO_1V8)	1.8	10m-ohm
0x41	Processor MCU VDD (VDD_MCU_RAM_0V85)	0.85	10m-ohm	0x41	Processor IO at 3.3V (VDD_IO_3V3)	3.3	10m-ohm
0x42	(VDA_MCU_1V8)	1.8	10m-ohm	0x42	Processor Dual Voltage IO (VDD_SD_DV)	3.3/1.8	10m-ohm
0x43	Processor MCU IO at 3.3V (VDD_MCUIO_3V3)	3.3	10m-ohm	0x43	LPDDR4 Memory (VDD1) (VDD1_DDR_1V8)	1.8	10m-ohm
0x44	Processor MCU IO at 1.8V (VDD_MCUIO_1V8)	1.8	10m-ohm	0x44	(VDD2Q_DDR_1V1)	1.1	10m-ohm
0x45	(VDD_CORE_0V8)	0.8	5m-ohm	0x45	(VDD_MCUWK_0V8)	0.8	10m-ohm
0x46	(VDD_RAM_0V85)	0.85	10m-ohm	0x46	MCU Peripherals at 1.8V (VSYS_MCUIO_1V8)	1.8	10m-ohm
0x47	(VDD_WK_0V8)	0.8	10m-ohm	0x47	MCU Peripherals at 3.3V (VSYS_MCUIO_3V3)	3.3	10m-ohm
0x48	(VDD_CPU_AVS)	0.8	5m-ohm	0x48	(VSYS_IO_1V8)	1.8	10m-ohm
0x49	(VDD_MCU_GPIORET_3V3)	3.3	10m-ohm	0x49	(VSYS_IO_3V3)	3.3	10m-ohm

Table 3-5. Power management IC's (continued)

Bus #1 Address	Power Rail	Nom V	Shunt Value	Bus #2 Address	Power Rail	Nom V	Shunt Value
0x4A	Processor LPDDR IO (VDD_DDR_1V1)	1.1	10m-ohm	0x4A	(VCC_12V0)	12	10m-ohm
0x4B	(VDD_PHYCORE_0V8)	0.8	10m-ohm	0x4B	(VSYS_5V0)	5	10m-ohm
0x4C	(VDA_PLL_1V8)	1.8	10m-ohm	0x4C	(VSYS_3V3)	3.3	5m-ohm
0x4D	(VDD_PHY_1V8)	1.8	10m-ohm	0x4D	(VSYS_3V3)	3.3	1m-ohm
0x4E	(VDA_USB_3V3)	3.3	10m-ohm	0x4E	(VDA_DLL_0V8)	0.8	10m-ohm
0x4F	(VDD_GPIORET_3V3)	3.3	10m-ohm	0x4F	(EXP_3V3)	3.3	10m-ohm

3.4.2 Shared Interfaces / Signal Muxing

Due to the number of features available on the EVM, there are some limitations for which features can be used simultaneously. Many of the conflicts revolve around the emulation/trace functionality. When trace is selected/ enabled, the following features are not accessible: Audio, Power Measurement (access from processor), reduce CAN-FD availability as well as few other items. See schematic for a complete definition of interfaces which share resources.

3.4.3 Power Delivery Network (PDN)

Refer to separate document.

3.4.4 Identification EEPROM

The EVM board identity and revision information are stored in an on-board EEPROM. The first 259 bytes of the memory are pre-programmed with EVM identification information. The format of the data is provided in Table 3-6. The remaining bytes are available to user defined storage.

Table 3-6. Board ID Information

Field Name	Offset /Size	Value	Comments
MAGIC	0000 / 4B (Hex)	0xEE3355AA	Header Identifier
M_TYPE	0004 / 1B (Hex)	0x01	Fixed length and variable position board
			ID header
M_LENGTH	0005 / 2B (Hex)	0x3C	Size of payload
B_TYPE	0007 / 1B (Hex)	0x10	Payload type
B_LENGTH	0008 / 2B (Hex)	0x2E	Offset to next header
B_NAME	000A / 16B (CHAR)	J721S2X-PM1-SOM	Name of the board
DESGIN_REV	001A / 2B (CHAR)	E4	Revision number of the design
PROC_NBR	001C / 4B (CHAR)	118	PROC number
VARIANT	0020 / 2B (CHAR)	01	Design variant number
PCB_REV	0022 / 2B (CHAR)	E4	Revision number of the PCB
SCHBOM_REV	0024 / 2B (CHAR)	E4	Revision number of the schematic
SWR_REV	0026 / 2B (CHAR)	01	first software release number
VENDORID	0028 / 2B (CHAR)	01	0x1: Manufactured by Mistral
BUILD_WK	002A / 2B (CHAR)	40	week of the year of production
BUILD_YR	002C / 2B (CHAR)	22	year of production
BOARDID	002E / 6B (CHAR)	0	
SERIAL_NBR	0034 / 4B (CHAR)	xxxx	incrementing board number

Table 3-6. Board ID Information (continued)

Field Name	Offset /Size	Value	Comments
DDR_TYPE	0038 / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	0039 / 2B (Hex)	0x2	offset to next header
DDR_CONTROL	003B / 2B (Hex)	0xC560	DDR Control Word Bit 1:0 = ‘00’ First DDR Bit 3:2 = ‘00’ No SPD Bit 5:4 = ‘10’ LPDDR4 Bit 7:6 = ‘01’ 32 bits Bit 9:8 = ‘01’ 32 bits Bit 10 = ‘1’ dual rank Bit 13:11 = ‘000’ Density 64 Gb (bit 0 to 3) Bit 14 = ‘1’ ECC bits present (inline, not separate bits) Bit 15 = ‘1’ Density 64 Gb (bit 4)
DDR_TYPE	003D / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	003E / 2B (Hex)	0x2	offset to next header
DDR_CONTROL	0040 / 2B (Hex)	0xC560	DDR Control Word
DDR_TYPE	0042 / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	0043 / 2B (Hex)	0x2	offset to next header
DDR_CONTROL	0045 / 2B (Hex)	0xC560	DDR Control Word
DDR_TYPE	0047 / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	0048 / 2B (Hex)	0x2	offset to next header
DDR_CONTROL	004A / 2B (Hex)	0xC560	DDR Control Word
END_LIST	0111 / 1B (Hex)	0xFE	End Marker

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2022	*	Initial Release

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