DM388 Base Board

User's Guide

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About This Manual

Developed with Mistral Solutions, the DM388 base evaluation module (EVM) enables developers to start immediate evaluation of DM388 processors and begin building on different video applications.

This document describes the board level operations of the DM388 base EVM. The EVM is based on the Texas Instruments DM388 Applications Processor.

National Conventions

The DM388 base EVM will sometimes be referred to as the DM814x EVM or the base EVM.

Information About Cautions

This Document may contain cautions.

This is an Example of a Caution Statement

A caution statement describes a situation that could potentially damage your software, hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes, and User Guides

Information regarding the DM388 processor can be found at http://www.ti.com.

Table 0-1. Document History

Version Number	Description of Changes
0.1	Draft version

Table 0-2. Board History

PCB Revision	History
Revision A	Created
Revision B	HDDAC and GMPC sections changed

Acronyms

Table 0-3 lists the acronyms used in this document.

Table 0-3. Acronyms

Acronym	Definition
BGA	Ball grid array
CCS	Code Composer Studio
DDR	Double data rate
EEPROM	Electrically erasable programmable read-only memory
ESD	Electrostatic discharge
EVM	Evaluation module
GPIO	General purpose Input/Output
GPMC	General purpose memory controller
I^2C	Inter-integrated circuit
JTAG	Joint test action group
LCD	Liquid crystal display
LED	Light emitting diode
MAC	Media access controller
McBSP	Multichannel buffered serial port
OTG	On-the-go
PCB	Printed circuit board
PHY	Physical transceiver
SD/MMC	Secure digital and multimedia card
SDRC	SDRAM controller
SDRAM	Synchronous dynamic random access memory
SPI	Serial peripheral interface
SPDT	Single pole double throw
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus

Introduction to DM388 Base EVM

This chapter provides a functional overview of the DM388 processor, key features, and a high-level block diagram of the DM388 base EVM design. This chapter also provides information about memory and I/O mapping, GPIO mapping, and inter-integrated circuit (I^2C) mapping of devices on the DM388 base EVM.

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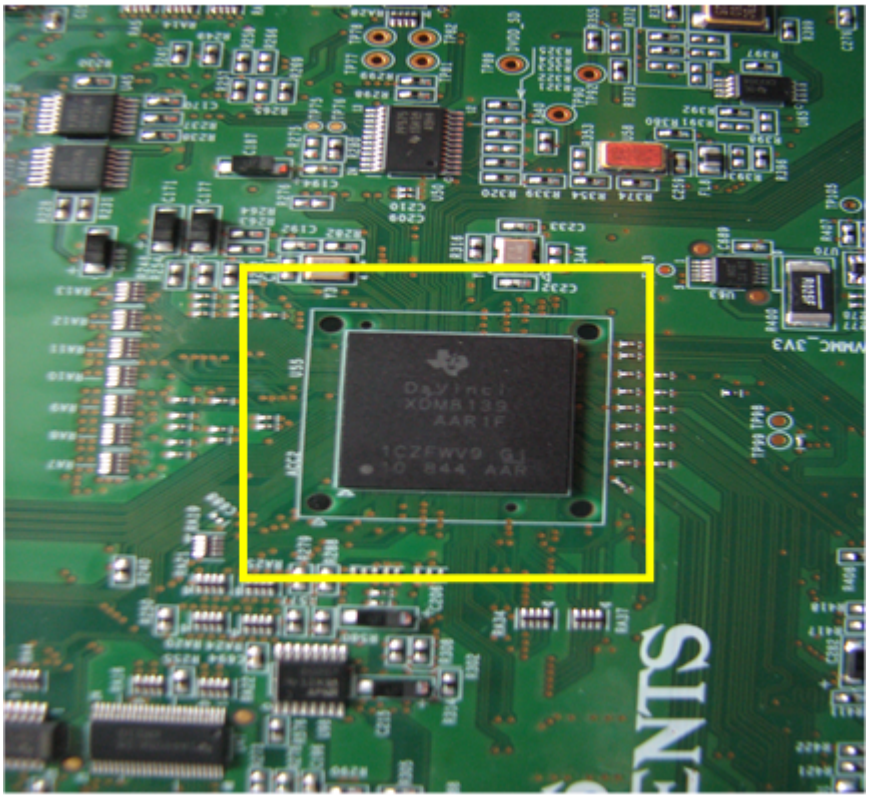
1.1 DM388 Processor

The DM388 processor mainly consists of ARM® Cortex®-A8 RISC CPU with NEON™ technology extension, TI C674x VLIW floating-point DSP core, and high-definition video and imaging coprocessors.

Figure 1-1. DM388 Processor



The DM388 processor is a highly integrated, programmable platform that leverages DaVinci™ technology from TI to meet the processing needs of the following applications:

- IP-netcam
- Digital video server (DVS)
- High-definition webcam
- High-definition embedded video communication modules
- Remote media display (RMD) and interactive digital signage

In addition to these markets, this user's guide also addresses:

- 3G gesture control (HDI)
- Video doorbell
- Telemedicine
- Test and Measurement
- Analytics
- Instrumentation
- Inspection and machine vision
- Avionics
- Skype™ endpoint applications

An ARM Cortex-A8 RISC CPU with a NEON extension, a TI C674x VLIW floating-point DSP core, and high-definition video and imaging coprocessors provide the programmability.

The ARM Cortex-A8 32-bit RISC microprocessor with NEON floating-point extension includes:

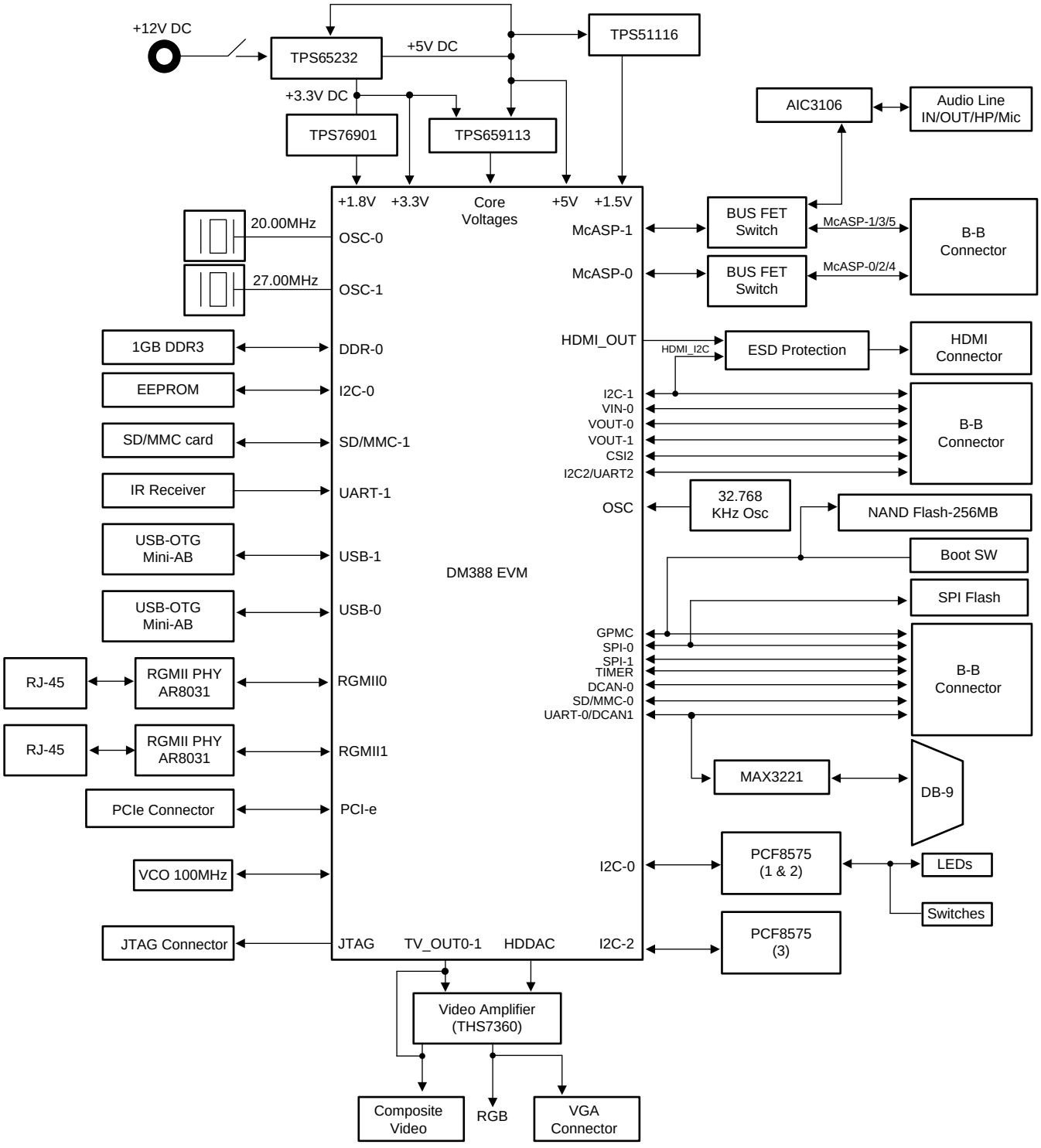
- 32KB of instruction cache
- 32KB of data cache
- 256KB of L2 cache
- 176KB of on-chip boot ROM (128KB of secure ROM and 48 KB of public ROM)
- 64KB of RAM

The DM388 processor is a 609-pin, Pb-Free BGA Package that has a 0.5-mm ball pitch with Via Channel technology to reduce the printed-circuit board (PCB) cost. The core of the ARM Cortex-A8 CPU operates at a speed of up to 1 GHz.

1.2 Block Diagram

Figure 1-2 shows the block diagram of the DM388 processor.

Figure 1-2. DM388 EVM Block Diagram



1.3 Key Features

The DM388 processor includes the following key features:

- High-performance digital media System-on-Chip (SoC)
- Memory
  - 32-bit DDR3 SDRAM interface (DDR0)
  - 1GB (256MB x4 chip) of memory from Micron is used on the DDR3 interface of the DM388 EVM
  - 256MB of NAND flash memory from Micron with socket for placing the NAND is used on the DM388 base EVM
- Power for the processor is derived from integrated power-management IC TPS659113.
- Analog video-out interface – Composite SD video from the TV OUT interface of the processor is available on the yellow RCA jack of the board.
- Component video out (RGB) from the HD digital-to-analog converter (DAC) interface of the processor is available on the board of the VGA connector.
- Digital video-out interface – Supported by an on-chip high-definition multimedia interface (HDMI) transmitter with a resolution and frame rate of 1080p60.
- USB interface – Dual high- and full-speed USB OTG 2.0 port with integrated PHYs
- Ethernet interface – Two RGMII ports interfaced to the MAC have a speed of 10/100/1000 Mbps.
- Stereo audio interface – Audio Line IN, Mic IN, Speaker OUT and Headset OUT
- Serial Interfaces – SD/MMC connector in 4-bit SD mode Supporting up to 48 MHz
- A 32-MB serial peripheral interface (SPI) flash memory is available on the DM388 EVM for SPI booting.
- Ultra-low-power MSP430™ microcontroller (MCU) to monitor the current flow of the DM388 device with INA226
- Dip switch to select different boot mode configurations
- Standard 20-pin JTAG debug interface
- Video, GPMC, and MCASP expansion board-to-board connectors are available to connect different application boards of the DM814x and AM387x (such as video camera, video conference, video security, and catalog application).
- PCI Express® 2.0 port with integrated PHY and one lane supports up to 5.0 GT/s
- RoHS compliant

1.4 Functional Overview

The DM388 EVM is based on the DM388 application processor from TI. The Micron memory MT41J256M8HX-125 is connected to the DM388 processor through the SSTL_15 interface. The DDR memory on the board consists of four chips (MT41J256M8HX-125) of micron memory that each have a capacity of 2Gb (256MB), and the memory has an excellent on-chip ODT for better signal quality. NAND flash memory is connected to the processor through the GPMC interface. The chip enable pin of the NAND device is connected to GPMC_nCS0 of the DM388 processor.

Analog video outputs of the EVM support composite TV outputs on the main board. The composite video outputs are available on the respective connector by default.

The DM388 base EVM supports multiple video input options from the application board through VIN0, VIN1, and the camera port. Any of the following interfaces can be active at a given point of time when the catalog application board is connected through the expansion board to the board connectors.

- S-video input digitized through video decoder (TVP5147)
- Composite video input digitized through video decoder (TVP5147)
- RGB video input digitized through video decoder (TVP7002)
- VGA input digitized through video decoder (TVP7002)
- Camera input from parallel camera interface

The EVM has a SD/MMC slot connected by using an SD/MMC1 4-bit interface on the main board. The SD/MMC2 interface is routed to the expansion connector for WLAN module on application board. The EVM has two RGMII Ethernet ports (RGMII0, RGMnII1) using two external AR8031 Gigabit PHY devices that are interfaced to the processor through the RGMII interface. It has a PCIe2.0 ×4 connector with integrated PHY on the DM814x processor that can be configured as Root complex or Endpoint.

The EVM supports two UART interfaces (DM388 UART, MSP430 UART) through two serial ports (DB9 connector) on the main board. The board has two USB mini-AB connectors to support a high-speed USB OTG2.0 interface. One Stereo Line IN, MIC IN, Speaker OUT, and Stereo Headset OUT audio interface is supported through the audio codec TLV320AIC3106IRGZT on the EVM. The audio codec on the EVM is controlled by the I2C0 and MCASP1 interface.

The EVM has five DIP switches for various purposes such as selecting different boot modes, GPIO toggling, video-out enable, NAND and SPI flash selection, and resetting the GPIO. The EVM also includes three reset push-button switches, one SYS_WAKE push-button switch, and three slide switches for power flow. The EVM has a standard 20-pin JTAG header (10 × 2 1.27-mm pitch) for debug interface. This JTAG port can be accessed through Code Composer Studio™ development version 4.0 and higher. The EVM is powered by a 12-V, 5-A external power supply, and a TPS659113 power-management device provides the required CPU core voltages and I/O voltages for the DM388 processor.

1.5 Memory and I/O Mapping

Table 1-1 provides the memory and I/O mapping for the DM388 EVM.

Table 1-1. Memory and I/O Map

Device	Start Address	End Address	Size	Description
GPMC	0x0000_0000	0x1FFF_FFFF	512MB	GPMC
On-chip ROM	0x4000_0000	0x4001_FFFF	128KB	Secure ROM
	0x4002_0000	0x4002_BFFF	48KB	ROM
On-chip RAM	0x402F_0000	0x402F_FFFF	64KB	Secure RAM
	0x4030_0000	0x4031_FFFF	128KB	OCMC SRAM
PCIe	0x2000_0000	0x2FFF_FFFF	256MB	PCIe
DDR	0x8000_0000	0xFFFF_FFFF	2GB	DDR
I2C0	0x4802_8000	0x4802_8FFF	4KB	I2C0 peripheral registers
I2C1	0x4802_A000	0x4802_AFFF	4KB	I2C1 peripheral registers
I2C2	0x4819_C000	0x4819_CFFF	4KB	I2C2 peripheral registers
SPI0	0x4803_0000	0x4803_0FFF	4KB	SPI0 peripheral registers
SPI1	0x481A_0000	0x481A_0FFF	4KB	SPI1 peripheral registers
MMC	0x481D_8000	0x481E_7FFF	64KB	MMC/SD/SDIO1 peripheral registers

1.6 GPIO Mapping

Table 1-2 lists some of the GPIOs that are used in the DM388 base EVM.

Table 1-2. GPIO Mapping

Number	GPIO Name	Source	Purpose
1	ENET_WoL_INT	GP0[12]	WoL interrupt
2	HDMI_CT_HPD	PCF8575 DEVICE-3	Enabling load switch
3	HDMI_LS_OE	PCF8575 DEVICE-3	Enabling level shifter
4	DISABLE_SD	PCF8575 DEVICE-3	SD and SF channel control of video amplifier
5	DISABLE_SF	PCF8575 DEVICE-3	
6	BYPASS_SD	PCF8575 DEVICE-3	To bypass LPF of SD and SF in VA
7	BYPASS_SF	PCF8575 DEVICE-3	
8	FILTER1	PCF8575 DEVICE-3	Selectable filter for SF channels
9	FILTER1	PCF8575 DEVICE-3	
10	IO_EXP2_GP1	PCF8575 DEVICE-2	GPIO used in CATALOG board
11	IO_EXP2_GP2	PCF8575 DEVICE-2	GPIO used in CATALOG
12	MCA0_DEC_A	PCF8575 DEVICE-2	MCASP0 decoder select
	MCA0_DEC_B		Lines
13	MCA1_MUX_SEL	PCF8575 DEVICE-2	MCASP1 MUX select lines
14	MCA0/1/3_RSEL_A MCA0/1/3_RSEL_B	PCF8575 DEVICE-2	MCASP0/1/3_R decoder select lines
15	PCF8575_INT_IO2	GP0[13]	Interrupt
16	MCA0_AXR9	PCF8575 DEVICE-2	GPIO used in VC board
17	IO_EXP2_GP3	PCF8575 DEVICE-2	GPIO used in VC board
18	MCA5_MUX_OE	PCF8575 DEVICE-2	To select B/T GPIO N MCA5_AHCLKX
19	VOUT_FLD_SEL1	PCF8575 DEVICE-3	To provide the pin muxing option for the VOUT0_FLD and VOUT1_FLD pins
20	VOUT_FLD_SEL2	PCF8575 DEVICE-3	
21	GPIO_VC_1	PCF8575 DEVICE-2	GPIO used on the application board
22	GPIO_VC_2	PCF8575 DEVICE-2	
23	MCA1_MUX2_nOE	PCF8575 DEVICE-2	MCASP1 muxing selection
24	ENET_INT	GP1[10]	Interrupt from EMAC PHY ICs
25	PCF8575_INT_IO1	GP1[4]	Interrupt from PCF8575 (U39)
26	EN_BCK2_LS	TPS659113-GPIO 7	Enabling load switch
27	EN_BCK3_TPS65232	TPS659113-GPIO 2	Enabling PCI_3V3
28	EN_TPS51116	TPS659113-GPIO 0	Enabling DDR supply
29	MSP430_INT	PCF8575 DEVICE- 1	Interrupt from MSP430
30	TPS_INT1	TPS659113-INT 1	Interrupt from PMIC
31	TPS_SLEEP	PCF8575 DEVICE-1	Sleep for TPS659113
32	PCI_SW_RESETn	PCF8575 DEVICE-1	PCIe reset
33	IR_REMOTE_OFF	PCF8575 DEVICE 1	To control IR sensor
34	UART0_OFF	PCF8575 DEVICE-1	UART0 controlling
35	EXP_ETH_RESET	PCF8575 DEVICE-1	Ethernet reset
36	GPMC_ADD_SELn	PCF8575 DEVICE-1	To select either GPMC or HDMI lines
37	SW_VOUT_EN	TDA04H0SK1 device	Video software enable
38	GPMC_nWP	TDA04H0SK1 device	GPMC write-protect
39	RESET_GPIO	TDA04H0SK1 device	Enabling PCI POR buffer

1.7 I²C Address Mapping

Table 1-3 provides the address mapping for the I²C interface on the DM388 base EVM.

Table 1-3. I²C Address Mapping

I²C Used	Device	Address
I2C0	Audio codec	0x18
I2C0	EEPROM	0x50
I2C0	TPS659113	0x2D
I2C0	I/O Expander-PCF8575	0x20
I2C0	PCF8575-2	0x23
I2C2	PCF8575-3	0x20
I2C1	HDMI	
I2C0 and I2C2	Application board devices	
I2C0	MSP430	0x25

Interfaces and Power Section of DM388 Base EVM

This chapter provides information about the interfaces and power section of the DM388 EVM.

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2.1 EVM Interfaces

The main interfaces of the DM388 base EVM are:

- DDR
- NAND flash
- SD/MMC
- Audio
- Ethernet
- EEPROM
- HDMI
- Composite video
- Component video
- VGA
- USB
- SPI flash
- UART
- JTAG
- PCI Express

2.1.1 DDR Interface

The DM388 supports single 32-bit mDDR/DDR2/DDR3 SDRAM interface (DDR0). The DDR3 device on the DM388 base EVM is the MT41J256M8HX-125 with configuration of 256MB x 8. Four 8-bit, 256-MB DDR3 devices are interfaced to 32-bit memory mDDR/DDR2/DDR3 SDRAM interface (DDR0). Hence a total of 1GB of DDR3 memory is interfaced DM814x/AM387x.

The DDR3 supply voltage (1.5 V) and termination voltage (0.75 V) for the DDR3 chips is generated by the synchronous buck converter (TPS51116). The reference voltage (0.75 V) is generated by a voltage divider. For the DQ and DQS lines, series termination is 0E; 22E series termination is provided for DM lines. All of the address and control lines have a resistor (51E) and a 0.1-µF capacitor parallel termination.

DM0 and DQS0 are the references for write and read to the first DDR chip DDRx_0 (in each DDR interface). DM1 and DQS1 are the references for the second DDR chip (DDRx_1), DM2 and DQS2 are the references for the third DDR chip (DDRx_2), and DM3 and DQS3 are the references for the fourth DDR chip (DDRx_3).The address lines A[0:14], bank address lines BA[0:2], and the control signals are connected to each of the DDR3 chips.

2.1.2 NAND Interface

The MT29F2G16ABAEAWP:E is the NAND flash device used on the DM388 EVM. The memory configuration is 2Gb with a 16-bit databus. The NAND flash is interfaced to the GPMC port of the DM388. NAND flash has 16 multiplexed I/O lines for data and address. The address lines are selected by enabling the GPMC_ADVN_ALE (address latch enable) to high. The chip select of NAND flash is connected to GPMC_nCS0 of the GPMC controller. A DIP switch (SW5) is provided on the DM388 base EVM to select between onboard NAND booting or NOR booting on an application board (video security). For onboard NAND booting, SW5.1 should be on. NAND IC is placed inside the 48-pin socket on the EVM.

The NAND and SPI interface selection table is silkscreened on the board for user convenience.

2.1.3 SD/MMC Interface

The SD/MMC card connector (MHC-W21-601-LF) interfaces to the SD1/MMC1 port of the DM388. The load switch (MIC94062YC6) controls the power supply to the MMC card (VMMC). VMMC is derived from the EVM_3V3 supply. The enable pin of the load switch (U70) is connected to GP1[2]. The load switch is enabled by default (resistor R266 connecting the GP1[2] pin to the EN pin of the load switch is not mounted in the default configuration).

The card detect pin of the SD/MMC connector is connected directly to the SD1_SDCD (ball G28) of the DM388. The write-protect pin of the SD/MMC connector is not connected directly to the E29 pin of the DM388; a resistor option is available if the write-protect feature is required. Write-protect is multiplexed (muxed) with {UART0_DSRn/SPI[0]_SCS[2]n/I2C[2]_SDA/SD1_SDWP/GP1[3]}. By default, the SD/MMC card is not write-protected (resistor R265 connects the pin to E29 as described in this paragraph). The E29 pin is used for I2C2 data on the application boards as well as on the base board.

2.1.4 Audio Interface

The audio codec used in the DM388 base EVM is a TLV320AIC3106 device. The device is a low-power stereo audio codec with a stereo headphone amplifier with single-ended or fully-differential configurations. The stereo audio DAC supports sampling rates from 8 kHz to 96 kHz and includes programmable digital filtering in the DAC path for 3D, bass, treble, midrange effects, speaker equalization, and de-emphasis for 32-kHz, 44.1-kHz, and 48-kHz rates.

The stereo audio analog-to-digital converter (ADC) supports sampling rates from 8 kHz to 96 kHz and is preceded by programmable gain amplifiers or AGC that can provide up to 59.5-dB analog gain for low-level microphone inputs. A highly programmable PLL is included for flexible clock generation and support for all standard audio rates from a wide range of available MCLKs, varying from 512 kHz to 50 MHz. The audio codec operates at an analog supply of 3.3 V, a digital core supply of 1.8 V, and a digital I/O supply of 3.3 V. A 24.576-MHZ clock is used as a master clock for the audio codec in the EVM.

The TLV320AIC3106 is controlled by I2C0 and McASP1 interfaces. McASP1 selection involves muxing logic because only two McASP instances are available on the DM388 device. Mux logic supports all of the legacy expansion boards of DM814x, which has six instances of McASP.

McASP1 is mapped to the onboard codec, McASP1, McASP3, and McASP5. McASP1 signals MCA1_ACLKX, MCA1_AFSX, MCA1_AXR[0], and MCA1_AXR[1] are mapped to other interfaces using two ICs of Quad x [2:1] MUX SN74CB3Q3257PWR (U36 and U49). Two GPIOs from I/O expander PCF8575PWR (U50) are used to select the required interfaces (onboard codec, McASP1, McASP3, and McASP5) from McASP1 lines using MUX logic.

GPIO MCA1_MUX2_nOE from I/O expander U50 is used to enable any multiplexer IC. GPIO MCA1_MUX_SEL is used to select a particular channel (or particular interface) from the MUX that is enabled.

Table 2-1 lists the McASP1 mapping.

Table 2-1. McASP1 Mapping

MCA1_MUX2_nOE	MCA1_MUX_SEL	MUX Selected	McASP1 is mapped to
0	0	MUX2 (CH 1)	McASP5
0	1	MUX2 (CH 2)	McASP3
1	0	MUX1 (CH 1)	McASP1 on expansion connector
1	1	MUX1 (CH 2)	Onboard codec

The default state of GPIOs from the I/O expander is high (logic 1). By default, McASP1 is mapped to the onboard codec.

NOTE: Interfaces that use McASP1, McASP3, and McASP5 cannot be tested simultaneously. Whenever McASP1 must be routed to expansion connectors to test the interfaces on the application boards, the onboard codec will be automatically disabled.

2.1.5 EMAC Interface

The EMAC software controls the flow of packet data between the device and two external Ethernet PHYs, with hardware flow control and quality-of-service (QOS) support. The EMAC software contains a 3-port gigabit switch, where one port is internally connected and the other two ports are brought out externally. Each external EMAC port supports 10Base-T (10 Mbps) and 100BaseTX (100 Mbps) in half- or full-duplex mode, or 1000BaseT (1000 Mbps) in full-duplex mode.

The EVM has two RGMII Ethernet ports (RGMII0, RGMII1) that use two external PHY AR8031 devices that are interfaced to the processor through the RGMII interface. A single MDIO interface (MDIO clock and MDIO data) is connected out to control the PHY configuration and status monitoring of RGMII0 and RGMII1. Multiple external PHYs can be controlled by the MDIO interface. The EMAC software I/Os operate at 3.3 V and are compatible with 2.5-V I/O signaling. Therefore, Ethernet PHYs with a 2.5-V I/O interface can be used.

The AR8031 requires a single, 3.3-V power supply with an I/O level of 2.5 V. On-chip regulators provide all other required voltages. The AR8031 embeds cable diagnostics test (CDT) technology on chip; this allows measuring the cable length, detecting the cable status, and identifying remote and local PHY malfunctions, bad or marginal patch cord segments, or connectors. Some of the problems that can be detected include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and a bad transformer. The AR8031 also supports Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up. The AR8031 integrates the termination R/C circuitry and the serial resistors for the line side and no external parallel termination required between PHY and magnetics on the board.

The EVM uses two external 25-MHz crystals (Y2 and Y7) to generate local clock for RGMII0 and RGMII1. The PHY uses three clock signals (RX_CLK, MDIO_CLK, and GTX_CLK) and four transmit and receive data lines. Signal RX_CLK comes from PHY to MAC, and signal GTX_CLK comes from MAC to PHY.

2.1.6 EEPROM Interfaces

The EVM uses a 256-Kb I^2C CMOS Serial EEPROM CAT24C256WI-GT3 to store the board ID information. EEPROM is interfaced to the DM388 processor by using I2C0. The CAT24C256 device is a 256-Kb Serial CMOS EEPROM, internally organized as 512 pages of 64 bytes each. The device features a 64-byte page write buffer and supports the standard (100 kHz) and fast (400 kHz) I^2C protocol.

The write-protect pin (WP) of EEPROM has been pulled low internally by default. If the EEPROM memory must be write-protected, pins 7 and 8 of J19 must be shorted by using a jumper.

Table 2-2 lists the board ID information that is stored. This information is read-only data and should be used to get complete details of the board.

Table 2-2. Board Information

Field Name	Size (in Bytes)	Field Contents
Header	4	0xAA 0x55 0x33 0xEE
Board name	8	813X_EVM
Version	4	B001 (Alphabet) = Beta.001 PCB Version B – Rev B Board 001 : Batch No
BOM version	2	XX (Number)
ECN version	2	XX (Number)
Test package version	2	XX (Number)
Batch code	4	WW YY (2 digits for week and 2 digits for year)
Board serial number	4	XXXX (4-digit number)
Configuration option	18	None
Processor mount option	1	0x01: Socketed 0x02: Soldered
Reserved	32719	None

2.1.7 HDMI

The DM388 processor includes an HDMI transmitter for digital video and audio data to display devices. The HDMI interface consists of a digital HDMI transmitter (HDMI 1.3a-compliant transmitter) core with a TMDS encoder, a core wrapper with interface logic and control registers, and a transmit PHY. An HDMI connector is connected to the processor through ESD protection device (TPD12S016PWR [U4]). The HDMI is controlled by the I2C1 interface of the DM388. The HDMI has three differential pairs of data lines and one differential pair of clock lines.

The HDMI has the following features:

- Hot-plug detection
- Supports up to a 165-MHz pixel clock
  - 1920 × 1080p at 75 Hz with 8-bit per component color depth
  - 1600 × 1200 at 60 Hz with 8-bit per component color depth
- Support for deep-color mode:
  - 10-bit per component color depth up to 1080p at 60 Hz (maximum pixel clock = 148.5 MHz)
  - 12-bit per component color depth up to 720p and 1080i at 60 Hz (maximum pixel clock = 123.75 MHz)
- The TMDS clock to the HDMI-PHY is up to 185.625 MHz.

NOTE: The GPMC_A22 signal is internally muxed with CE_REMOTE_IN on pin N2, and the GPMC_A23 signal is muxed with HDMI_HP_IN on R8 of the DM814x processor. GPMC lines or HDMI lines are selected through switch IC U98 (SN74CB3Q3257PWR) using a GPIO signal (GPMC_ADD_SELn) from U39 (PCF8575PWR). By default, HDMI lines are selected and used in the board.

2.1.8 Video DAC Interface

The DM388 processor supports one SD DAC module (AVDAC1BGTVV4) from the OMAP4430 and a GS70 3-channel HD DAC. The SD DAC module supports composite video standard with sampling rates up to 60 MSPS. The composite video signal (TV_OUT0) is connected directly from the processor to RCA jack J8. An option is available to pass the TV_OUT0 signal through video amplifier THS7360IPW (U5).

The HD DAC consists of three channels of 10-bit current-steering DACs. The output of the DAC can drive the composite video signal to 37.5-Ω load directly. The HD DAC also contains an internal band gap to provide a low-noise reference voltage to the video DAC. The HD DAC supports sampling rates up to 150 MSPS.

HD DAC signals HDDAC_A, HDDAC_B, and HDDAC_C from the processor are connected to component video connectors J7 (Green), J9 (Blue), and J6 (Red) through video amplifier THS7360IPW (U5). HD DAC signals from U5 are also routed to VGA connector P1. The VGA control signals and the sync signals are routed to P1 through an ESD protection device TPD7S019-15DBQR (U7).The control signals required for U5 are taken from I/O expander PCF8575PWR (U14) by using I2C2 lines.

2.1.9 High-Speed USB Interface

The USB controller provides a low-cost connectivity solution for numerous consumer portable devices by providing a mechanism for data transfer between USB devices with a line and bus speed of up to 480 Mbps. The USB subsystem of the DM388 device has two independent USB 2.0 modules (USB0 and USB1) built around two OTG controllers; the OTG supplement feature (support for a dynamic role change) is also supported. Each port can support a dual-role feature allowing for additional versatility that enables operation capability as a host or a peripheral. Both ports have identical capabilities and operate independently.

Each USB controller is built around the Mentor® USB OTG controller and the TI GS70 PHY. Each USB controller has a user-configurable 32KB of endpoint FIFO, and has the support for 15 transmit endpoints and 15 receive endpoints in addition to endpoint 0. The USB uses the CPPI 4.1 DMA to accelerate data movement through dedicated DMA hardware. The two USB modules share the CPPI DMA controller and accompanying queue manager, interrupt pacer, power-management module, and PHY and UTMI clock. The PHY does not have a built-in charge pump and requires an external power source to source the 5-V VBUS power. The PHY has a built-in charge detection for device mode and a control capability for host applications for implementing an external charge detection capability.

For an OTG controller, the procedure of the controller to assume the role of a host or a device is governed by the state of the ID pin. Also, the procedure is controlled by the USB cable connector type. The DM388 device bonds out these ID pins and allows the control to be handled directly from the connector (for example, the USB controller assumes the role based on the cable end inserted into the mini A/B connector [J3 and J4] on the EVM). A jumper option is available on the EVM to ground the USB_ID pin for USB0 (J12) and USB1 (J13). This jumper option enables the EVM to be used in Host Only mode.

2.1.10 SPI Flash Interface

The SPI flash interface is a high-speed synchronous serial I/O port that allows a serial bit stream (4 to 32 bits) to be shifted in and out of the device at the programmed bit-transfer rate. The DM388 processor supports four SPIs. The SPI0 signal from DM388 controls SPI flash memory device. A 32-Mb SPI flash memory (W25X32VSFIG) on the EVM provides SPI booting. For SPI booting, SW5.2 must be on and SW5.1 must be off.

2.1.11 UART Interface

The UART performs serial-to-parallel conversions on data received from a peripheral device, and performs parallel-to-serial conversions on data received from the CPU. There are three UART interfaces (UART0, UART1, and UART2) available for the DM388. One UART interface is available for the MSP430 on the EVM. UART0 on the base EVM is selected by enabling the UART0_OFF signal to low. UART0 is also routed to application boards through board-to-board connectors on the EVM. The UART interface (UART0) can be used on the base EVM or the application boards. UART0 supports a baud rrate of up to 3.6 Mbps. UART1 is connected to the IR receiver on the EVM. The IR receiver is selected by enabling the IR_REMOTE_OFF signal to LOW.

2.1.12 I²C Interface

The device includes three I2C modules that provide an interface to other devices that are compliant with version 2.1 of the Philips Semiconductors Inter-IC bus (I2C-bus) specification. External components attached to this 2-wire serial bus can transmit and receive 8-bit data to and from the device through the I2C module.

The I²C port supports the following features in the DM388:

- Standard and fast modes from 10 to 400 kbps
- Noise filter to remove noise 50 ns or less
- Seven- and 10-bit device addressing modes
- Multimaster transmitter and slave receiver mode
- Multimaster receiver and slave transmitter mode
- Combined master transmit and receive and receive and transmit modes
- Two DMA channels, one interrupt line
- Built-in FIFO (32 byte) for buffered read or write

I2C0 of DM388 is being shared across devices like the audio codec, I/O expanders, MSP430 MCU, TPS659113, and EEPROM. I2C2 is shared across the I/O expander and VGA connector. Also, I2C0 and I2C2 are routed to the board-to-board expansion connector to support the interfaces on the application board. The HDMI interface uses I2C1 signals.

2.1.13 Debug Interface

The EVM supports two JTAG debug interfaces: DM388-JTAG and MSP430-JTAG. Debug connectors are used to test, debug, execute, trace, and download the program to the target unit. The following two JTAG connectors are on the board:

- 14-pin MSP430-JTAG header
- 20-pin DM388-JTAG Header

2.1.14 PCI Express Interface

PCIe is a serial-based technology that uses low-voltage differential signaling (LVDS) to reduce the number of data-signal lines and high-frequency clock signals in a point-to-point interconnect arrangement between two devices. PCIe also eliminates multiple host presences on the same bus.

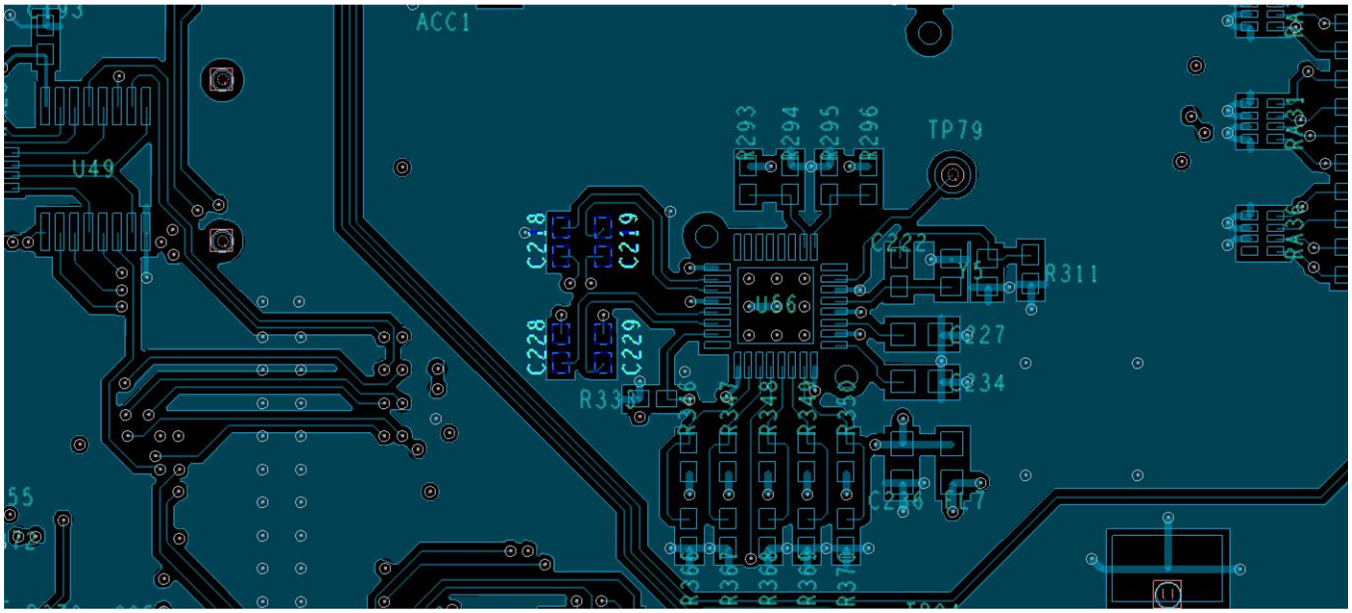
The PCIe subsystem contains the DesignWare® core (DWC), PCIe dual-mode (DM) core, and SerDes PHY. The DM core operates in endpoint (EP) mode or root-complex (RC) port mode. The core supports a single in-port and a single out-port. The operating mode of the PCIe core is set to EP or RC based on: the value sampled from the BOOTMODE[4:0] pins, use as a secondary boot loader, or application software by configuring the PCIE_CFG [PCIE_DEVTYPE] register. The DM core can be switched between modes at run time by applying a power-on reset.

PCIe supports high-speed data transfer at rates of up to 5.0 Gbps per lane per direction. PCIe on the EVM uses PCI_3V3 and IP_EVM_12V as the supply voltages. The clock required for clocking data and PHY functional clocks are generated by the PHY through the supplied external input 100-MHz differential clock from the device (U56 [CDCM61002RHBR]) on the EVM.

Use the following instructions to enable the PCIe to be compatible with the spread spectrum clock of a PC.

1. Remove the PCIe clock AC-decoupling capacitors on C218, C219, C228, and C229 (see Figure 2-1).
2. Place a 0805 size 270-pF or 0.1-µF capacitor across the pads of C218 and C228 for negative reference clock and across the pads of C219 and C229 for positive reference clock that are in proximity.
3. Configure the DM388 board as EP and configure the computer as RC.

Figure 2-1. PCIe Clock AC-Decoupling Capacitors – Host Clocking Enabled



2.1.15 MSP430™ Interface

All of the power supplies on the base EVM and application boards are provided with power measurement capability by using the ultra-low-power MSP430 MCU.

Use the MSP430-based controller in combination with a current and power monitor and the I^2C interface (INA226) for power monitoring. In the DM388 base EVM, 11 INA current monitors are available for monitoring the currents of the following supplies:

- PLL_1V8
- HDMI_CSI_1V8
- CVDD_ARM
- VDDQ_DM_1V5
- DVDD
- VDDA_1V8
- DVDD_GPMC
- DVDD_C
- CORE_VDD
- CVDD_DSP
- VMMC

Table 2-3 shows the I²C addresses if the power monitors.

Table 2-3. I²C Power-Monitor Addresses

Supply Number	Supply Name	Address
1	PLL_1V8	1000000
2	HDMI_CSI_1V8	1000001
3	CVDD_ARM	1000010
4	VDDQ_DM_1V5	1000011
5	DVDD	1000100
6	VDDA_1V8	1000101
7	DVDD_GPMC	1000110
8	DVDD_C	1000111
9	CORE_VDD	1001000
10	CVDD_DSP	1001001
11	VMMC	1001010

2.2 Clock

The EVM has the following clocks:

- Y1 – Provides 32.768-kHz real-time clock (RTC) to the power-management IC (TPS659113).
- Y2 – Provides 25-MHz clock for Ethernet PHY (RGMII0).
- Y3 – Provides 20-MHz device (DEV) clock that generates the majority of the internal reference clocks for the DM388.
- Y4 – Provides 32.768-kHz auxiliary clock to the MSP430 MCU.
- Y5 – Provides 25-MHz clock to generate differential clock for the PCI and SerDes CLK.
- Y6 – Provides 27-MHz auxiliary (AUX) clock that can be used as a source for the audio, video PLLs, or both.
- Y7 – Provides 25-MHz clock for Ethernet PHY (RGMII1).
- U58 – Provides 32768-Hz clock input that is provided at the CLKIN32 pin to serve as a reference clock in place of the RTCDIVIDER clock for the following modules:
  - RTC
  - GPIO0, GPIO1, GPIO2, and GPIO3
  - TIMER1, TIMER2, TIMER3, TIMER4, TIMER5, TIMER6, and TIMER7
  - SYNCTIMER

2.3 Power

The main power input for the EVM system is provided by using an external 12-V universal adapter. The other voltages required for the main board are derived by using onboard regulators on the main board. Four major switching regulators are used to derive power for the DM388 EVM.

- TPS65232 (U16) – Gives TPS_EVM_5V0, BCK2_3V3, PCI_3V3
- TPS659113 (U25) – Gives power to DM388
- TPS51116 (U46) – DDR power supply

Figure 2-2 shows the 12-V supply circuitry.

Figure 2-2. IP_EVM_12V

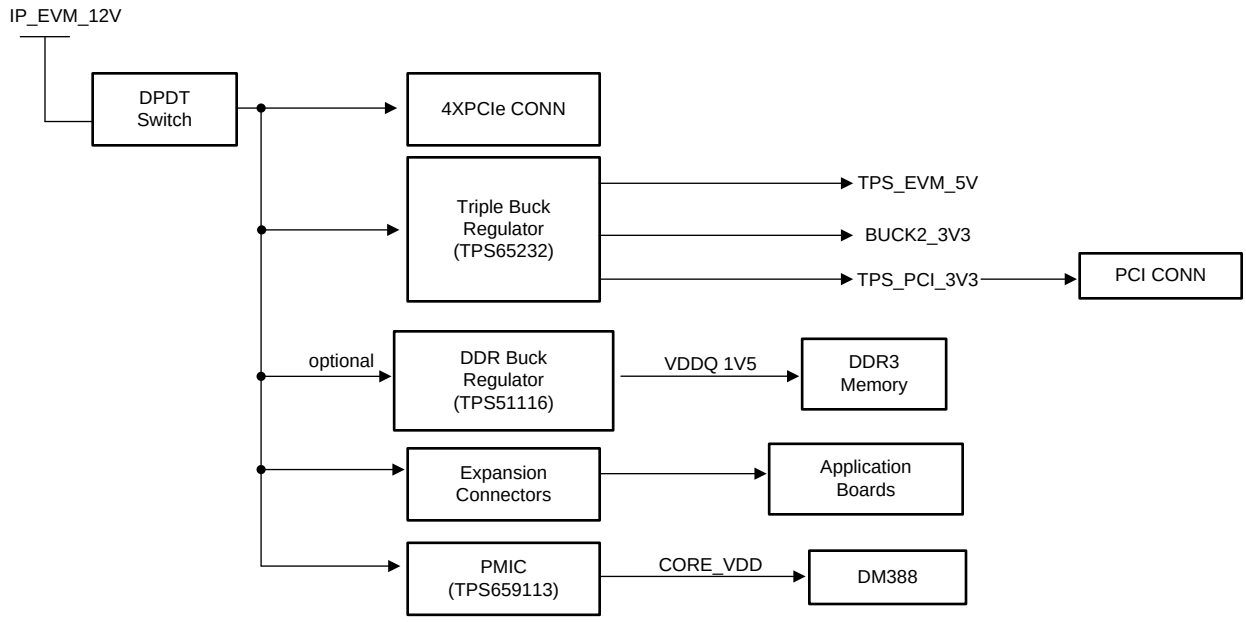


Figure 2-3- shows the TPS_EVM_5V0 supply circuitry.

Figure 2-3. TPS_EVM_5V0

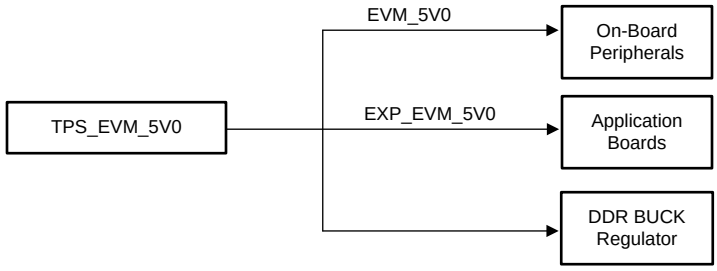


Figure 2-4 shows the BCK2_3V3 supply circuitry.

Figure 2-4. BCK2_3V3

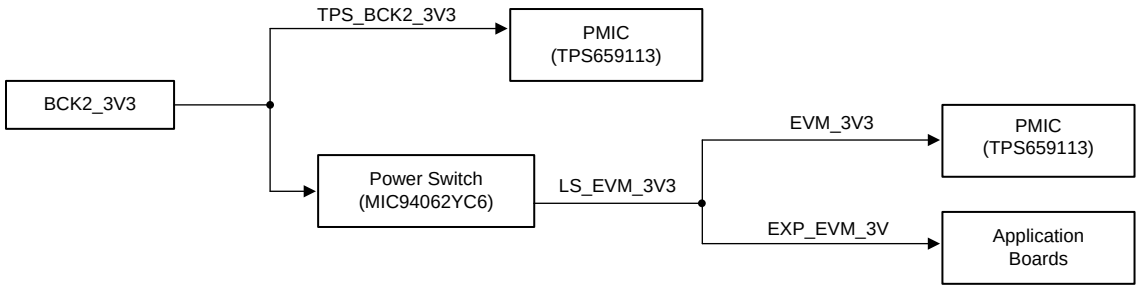


Figure 2-5 shows the EVM_5V0 supply circuitry.

Figure 2-5. EVM_5V0

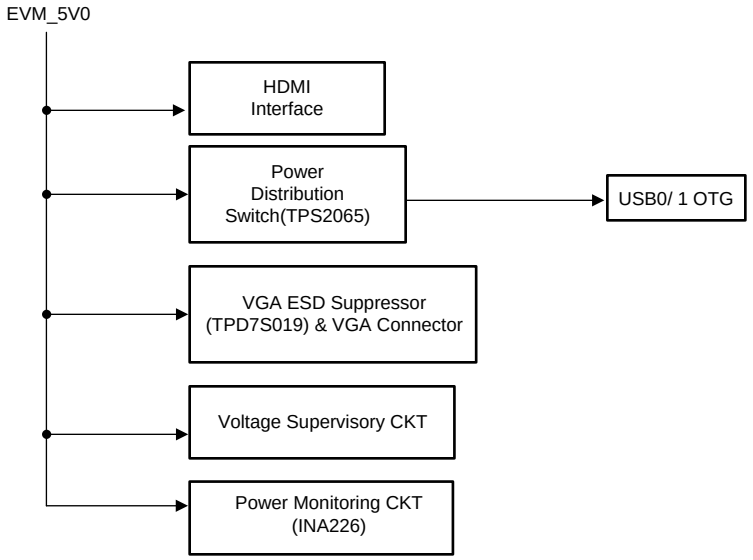
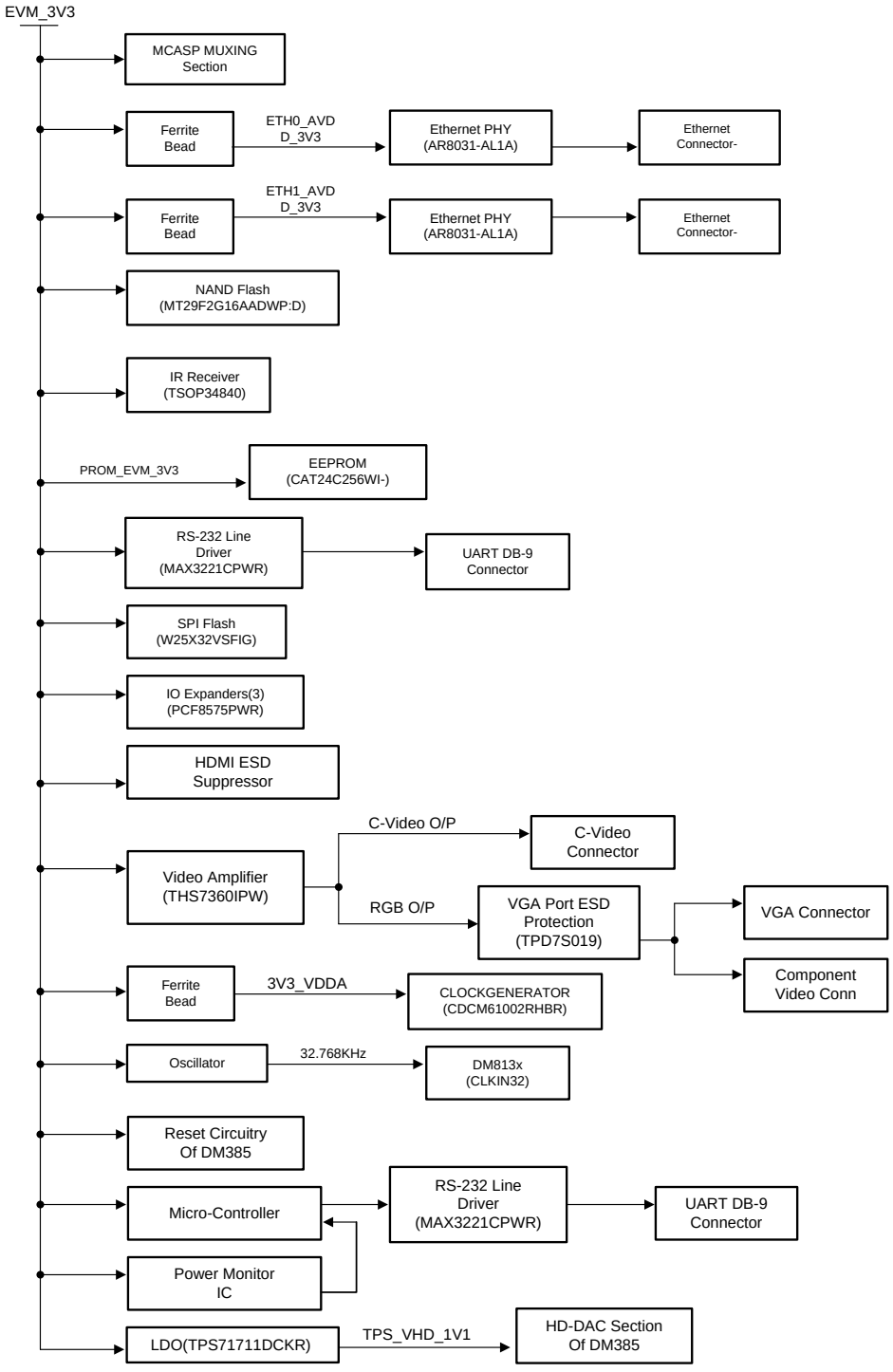


Figure 2-6 shows the EVM_3V3 supply circuitry.

Figure 2-6. EVM_3V3



2.3.1 DM388 Power From PMIC

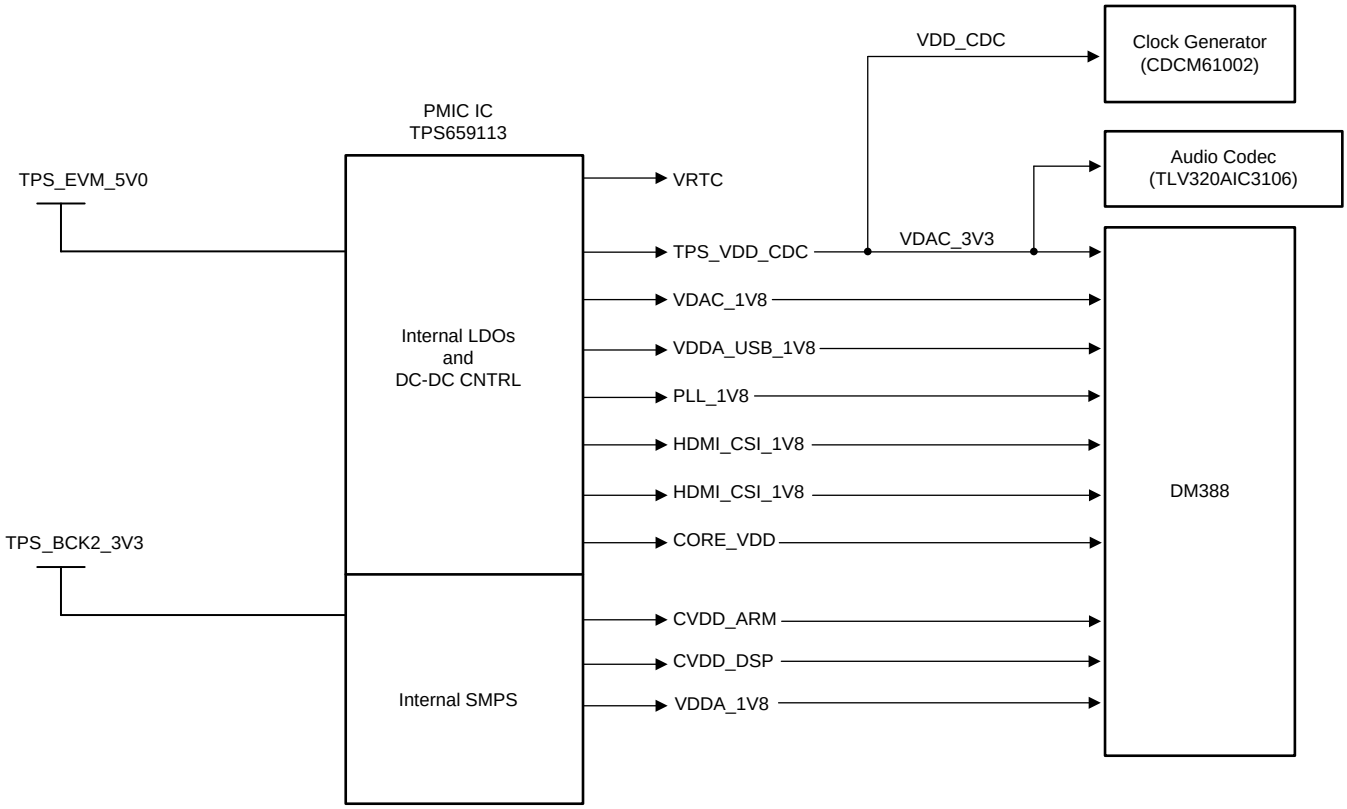
The following list provides the power requirements of the DM388 processor that the power-management IC (TPS659113 [U25]) generates and distributes.

- DM388 I/O supply: TPS_VDDA_1V8-1.8V
- DM388 core supply
  - VDD1(CVDD_ARM)-1.2V
  - VDD2 (CVDD_DSP)-1.2V
  - CORE_VDD-1.2V
- DM388 auxiliary supplies
  - DVDD_GPMC-3.3V
  - DVDD-3.3V
  - DVDD_C-3.3V
  - DVDD_SD-3.3V
  - VDDA_1V8-1.8V
  - HDMI_CSI_1V8-1.8V
  - VDDA_USB_1V8-1.8V
  - VDDQ_1V5-1.5V
- DM388 VDAC supply
  - VDAC_3V3-3.3V
  - VDAC_1V8-1.8V
- PLL supply PLL_1V8-1.8V

The input supply to the power manager is from the TPS_EVM_5V0 and TPS_BCK2_3V3 to generate different voltage rails. The TPS659113 is controlled by the I2C0 interface of the DM388 processor and the address is 0X2D.

Figure 2-7 shows the PMIC circuitry.

Figure 2-7. PMIC Circuitry



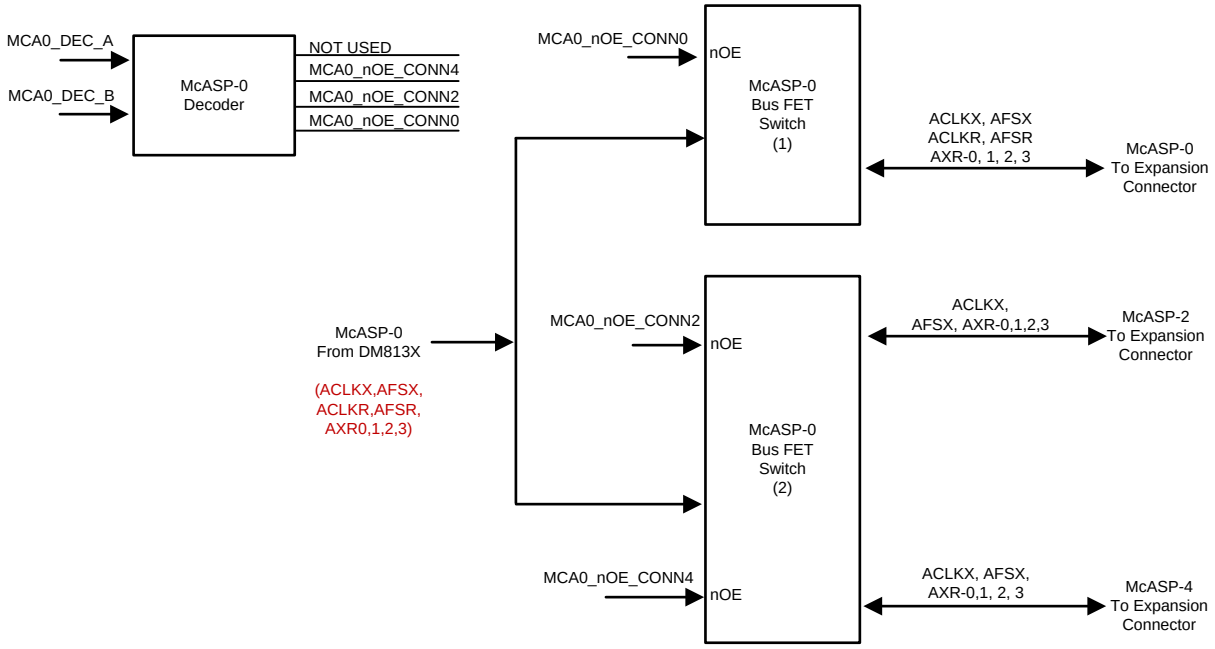
2.4 DM388 EVM Muxing Options

On the DM388 base Board EVM, McASP muxing has been implemented because of the shortage of McASP interfaces compared to Centaurus. In Centaurus, six McASP (McASP[0:5]) interfaces are available, and in the DM388 only two McASP (McASP[0:1]) interfaces are available. Because the DM388 EVM supports four other application boards that use the McASP[0:5], the muxing option is given for the available McASPs on the DM388 EVM.

2.4.1 McASP0 Muxing

Figure 2-8 shows the muxing of McASP0.

Figure 2-8. McASP0 Muxing



The McASP0 signals MCA0_ACLKX, MCA0_AFSX, and MCA0_AXR[0:3] are mapped using MUXs, and MCA0_AFSR and MCA0_CLKR are directly connected to expansion connector.

To map McASP0 exclusively to one of the McASPs (McASP0, McASP2, McASP4), a decoder has been used with the controlling inputs taken from the I/O expander GPIOs (MCA0_DEC_A and MCA0_DEC_B). By configuring these two GPIOs , McASP0 mapping is achieved (see Table 2-4).

The default state of GPIOs from the I/O expander is high (logic 1). By default, McASP0 is mapped to McASP0.

Table 2-4 shows the McASP0 mapping.

Table 2-4. McASP0 Mapping

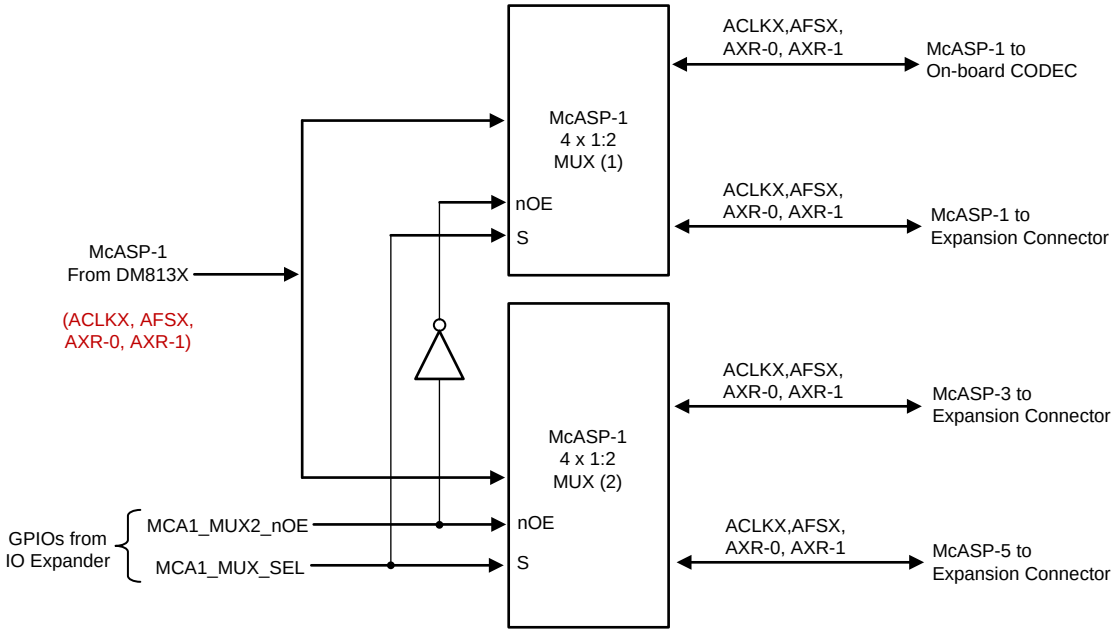
MCA0_DEC_B	MCA0_DEC_A	Output From Decoder	Mux Selected	McASP0 is Mapped to
0	0	Not used	—	—
0	1	MCA0_nOE_CONN4 is LOW	BUS FET SWITCH-2 (CH 2)	McASP4
1	0	MCA0_nOE_CONN2 is LOW	BUS FET SWITCH-2 (CH 1)	McASP2
1	1	MCA0_nOE_CONN0 is LOW	BUS FET SWITCH-1	McASP0

NOTE: Interfaces on the application boards that use McASP0, McASP2, or McASP4 cannot be tested at the same time.

2.4.2 McASP1 Muxing

Figure 2-9 shows the McASP1 muxing.

Figure 2-9. McASP1 Muxing



McASP1 is mapped to the onboard codec, McASP1, McASP3, McASP5. McASP1 signals MCA1_ACLKX, MCA1_AFSX, MCA1_AXR[0], and MCA1_AXR[1] are mapped to other interfaces using two 4 × [2:1] MUXs. Two GPIOs from the I/O expander are used to select the required interfaces (codec, McASP1, McASP3, McASP5) from McASP1 lines using a MUX.

GPIO MCA1_MUX2_nOE from the I/O expander is used to enable any multiplexer IC, and GPIO MCA1_MUX_SEL is used to select a particular channel (or particular interface) from the MUX that is enabled.

Table 2-5 provides the McASP1 muxing.

Table 2-5. McASP1 Muxing

MCA1_MUX2_nOE	MCA1_MUX_SEL	MUX Selected	McASP1 is Mapped to
0	0	MUX2 (CH 1)	McASP5
0	1	MUX2 (CH 2)	McASP3
1	0	MUX1 (CH 1)	McASP1 on expansion connector
1	1	MUX1 (CH 2)	Onboard codec

The default state of GPIOs from the I/O expander is high (logic 1). By default, McASP1 is mapped to the onboard codec.

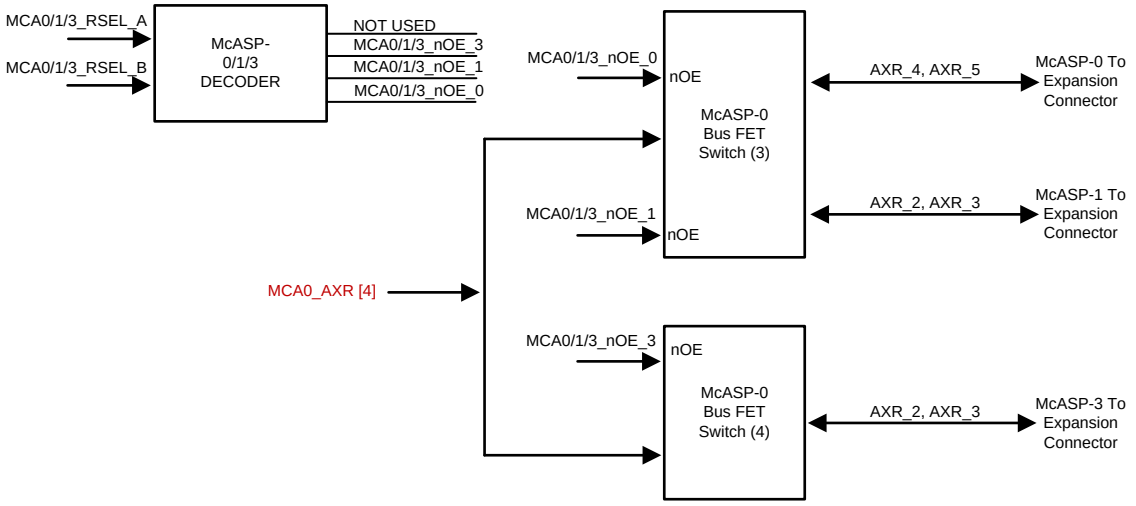
NOTE: Interfaces that use McASP1, McASP3, McASP5 cannot be tested at the same time. When McASP1 must be routed to expansion connectors to test the interfaces on the application boards, the onboard codec must be disabled.

2.4.3 McASP0_AXR [4:5] Lines Muxing

In Centaurus, McASP0 has five data channels (MCA0_AXR[0:9]), McASP1 has two data channels (MCA1_AXR[0:3]), and McASP3 also has two data channels (MCA3_AXR[0:3]). In the DM388, McASP0 has three data channels (MCA0_AXR[0:5]) and McASP1 has one data channel (MCA1_AXR[0:1]). Because McASP3 is muxed with McASP1 signals and MCA0_AXR[4:5], MCA1_AXR[2:3], and MCA3_AXR[2:3] are used on the application boards, hence the EVM provides one more muxing option to select between MCA0_AXR[4:5], MCA1_AXR[2:3], and MCA3_AXR[2:3].

Figure 2-10 shows the McASP0 muxing.

Figure 2-10. McASP0 Muxing



MCA0_AXR[4:5] is used as an input to MUXs, and a decoder is used to select one interface at a time. Input to the decoder is taken from the I/O expander. The following GPIOs are HIGH by default and map the inputs to McASP0_AXR[4:5] that are connected to expansion connector.

- MCA0_RSEL_A
- MCA1_RSEL_A
- MCA2_RSEL_A
- MCA0_RSEL_B

- MCA1_RSEL_B
- MCA3_RSEL_B

Table 2-6 lists the selections.

Table 2-6. McASP0_AXR Muxing

MCA0/1/3_ RSEL_B	MCA0/1/3_ RSEL_A	Output from decoder	MUX selected	MCA0_AXR[4:5] is Mapped to
0	0	Not used	—	—
0	1	MCA0/1/3_nOE_3	BUS FET SWITCH-4	MCA3_AXR[2:3]
1	0	MCA0/1/3_nOE_1	BUS FET SWITCH-3 (CH 2)	MCA1_AXR[2:3]
1	1	MCA0/1/3_nOE_0	BUS FET SWITCH-3 (CH 1)	MCA0_AXR[4:5]

NOTE: McASP0 and McASP1 muxing must be considered before selecting the MCA0_AXR[4:5] lines. Ensure that McASP0 lines are selected by using other muxing schemes before opting for MCA0_AXR[4:5] lines to McASP0. Similarly, before opting MCA0_AXR[4:5] lines that are mapped to MCA1_AXR[2:3] and MCA3_AXR[2:3], ensure that McASP1 and McASP3 are selected using other muxing schemes.

2.4.4 McASP5 and GPIO Selection for VC Board

The McASP5 signals (MCA5_AFSX and MCA5_AXR0) are used as GPIOs on the video conference board. McASP5 signals are mapped from McASP1 on the DM388 EVM, and McASP1 lines on the DM388 cannot be configured as GPIOs. As a result, DM388 EVM provides a muxing option of McASP5 lines (MCA5_AFSX and MCA5_AXR0) that are mapped from McASP1 and two GPIOs (GPIO_VC_1 and GPIO_VC_2) from the I/O expander. The output (MCA5_AFSX_EXP and MCA5_AFSX_EXP) from the MUX stage is routed to the expansion connector.

When the VCONF board is plugged in, signals on the expansion connectors are used as GPIOs. These signals can be used as McASP5 lines when other application boards are plugged in.

Figure 2-11 shows the selection of either MCA5 lines or GPIOs from the I/O expander by using a GPIO (MCA5_MUX_OE) from the same I/O expander.

Figure 2-11. MCA5 and GPIO Selection

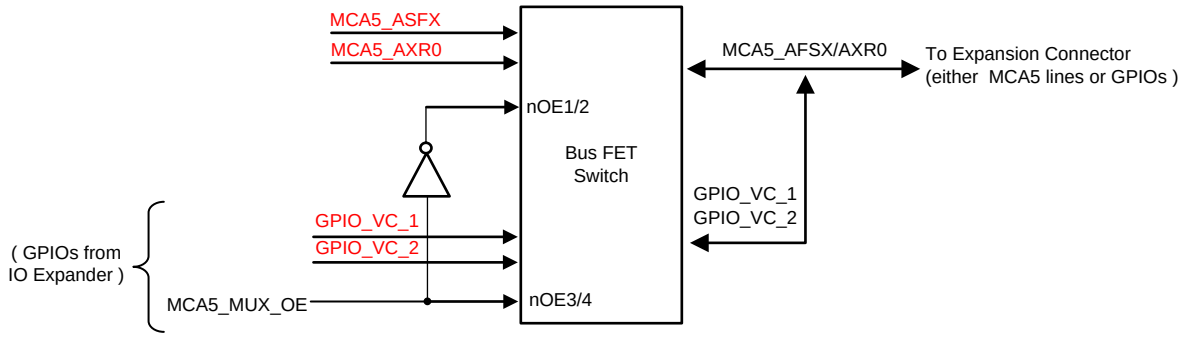


Table 2-7 shows the selection.

Table 2-7. Channel Selection

MCA5_MUX_OE	Channel Selected	Signals on Expansion Connector
1	CH 1	MCA5_AFSX and MCA5_AXR0
0	CH 2	GPIO_VC_1 and GPIO_VC_2

By default, MCA5_AFSX and MCA5_AXR0 are available on the expansion connector if McASP5 is enabled in the McASP1 muxing scheme.

2.4.5 MCA1_AHCLKX Muxing

MCA1_AHCLKX is used in the Centaurus EVM to provide an option to get MCLK for the onboard codec or it will be routed to the expansion connector. In the DM388, ensure that MCA1_AHCLKX provides the same option as it does in the Centaurus EVM.

GPIO MCA1_MUX_SEL from the I/O expander is used to select the required output (see Figure 2-12).

Figure 2-12. Required Output Selection

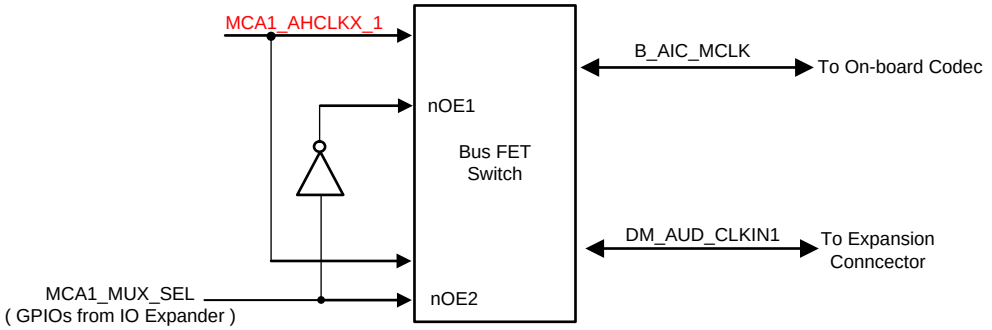


Table 2-8 lists the channel selection and output.

Table 2-8. Channel Selection and Output

MCA1_SEL_OE	Channel Selected	OUTPUT
1	CH 1	B_AIC_MCLK (codec)
0	CH 2	DM_AUD_CLKIN1 (expansion)

By default, MCA1_AHCLKX is connected to the onboard codec (B_AIC_MCLK) because the GPIO from the I/O expander is high.

2.5 UART2, I2C2, and VOUT Muxing

In Centaurus, UART3 (TX and RX) and I2C2 (SCL and SDA) are pin multiplexed. These signals are connected to the expansion connector and are used on the application boards as UART3 or as I2C2 signals. However, the UART3 interface is not available on the DM388. Instead of UART3, UART2 signals are used on the DM388 device. Because the I2C2 signals are not pin multiplexed with UART2 signals, the DM388 EVM provides an option to select UART2 (TX and RX) or I2C2 (SCL and SDA) and route the selected signals to the expansion connector.

The UART3 (RTS and CTS) signals are pin multiplexed with UART0 (RIN and DTRn) in Centaurus.UART2 is used instead of UART3 on the DM388, and UART2 (RTS and CTS) lines are pin multiplexed with VOUT0 and VOUT1 lines.

The UART2_RTS signal is pin muxed with VOUT0_FLD and CAM_PCLK, and the UART2_CTS signal is pin muxed with VOUT1_FLD. The EVM provides a logic using a MUX, a buffer, and a decoder to get UART3 or I2C2 and VOUT0 and VOUT1 (see Figure 2-13).

Figure 2-13. UART2, I2C2, and VOUT Muxing

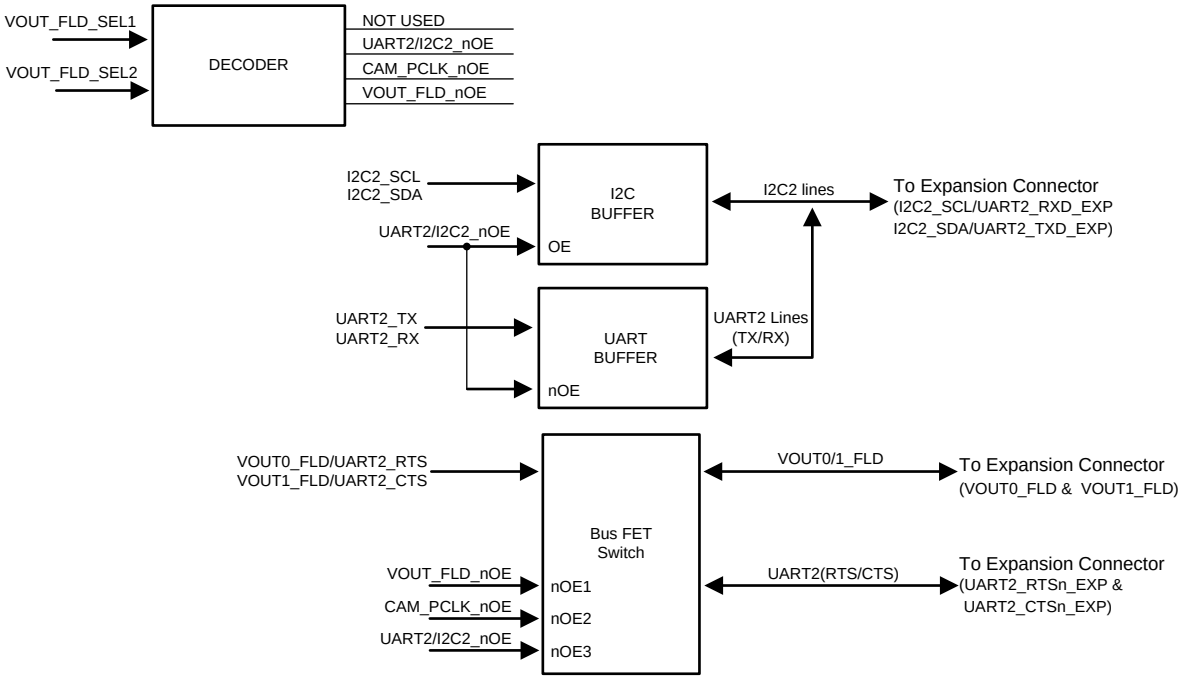


Table 2-9 lists the I/O expander GPIOs (VOUT_FLD_SEL1 and VOUT_FLD_SEL2) that are used as input-to-decoder.

By default, inputs to the decoder are high, so VOUT_FLD_nOE = LOW is selected and VOUT0_FLD and VOUT1_FLD signals are routed to the expansion connector. Because all other outputs from the decoder are high, when UART2 and I2C2_nOE are high, the I2C2 buffer is enabled. So, I2C2, VOUT0_FLD, and VOUT1_FLD lines will be enabled by default.

When UART2 and I2C2_nOE are LOW, the UART2 signals (TX, RX, RTS, and CTS) are available on the expansion connectors. I2C2 and VOUT lines are not available whenever UART2 signals are selected.

Table 2-9. I/O Expander GPIOs

VOUT_FLD_SEL2	VOUT_FLD_SEL1	Output From Decoder	Device Selected	OUTPUT
0	0	Not used	—	—
0	1	UART2/I2C2_nOE	Bus FET switch (CH 3)	UART2 signals. I2C2 buffer is disabled.
1	0	CAM_PCLK_nOE	I^2C buffer and VOUT bus FET switch (CH 2)	VOUT0_FLD as i/p (CAM_PCLK). I2C2 buffer is enabled.
1	1	VOUT_FLD_nOE	I^2C buffer and VOUT bus FET switch (CH 1)	VOUT0_FLD and VOUT1_FLD. I2C2 buffer is enabled.

Physical Description

This chapter provides information about the physical characteristics of the board.

Topic **Page**

3.1 DM388 EVM Layout

The DM388 base EVM has the following dimensions:

- 317.5 mm × 187.96 mm
- 10-layer PCB
- 2-cm height (completed PCB)

Figure 3-1 shows the top view of the DM388.

Figure 3-1. TMDXEVM388 Base EVM (Top View)

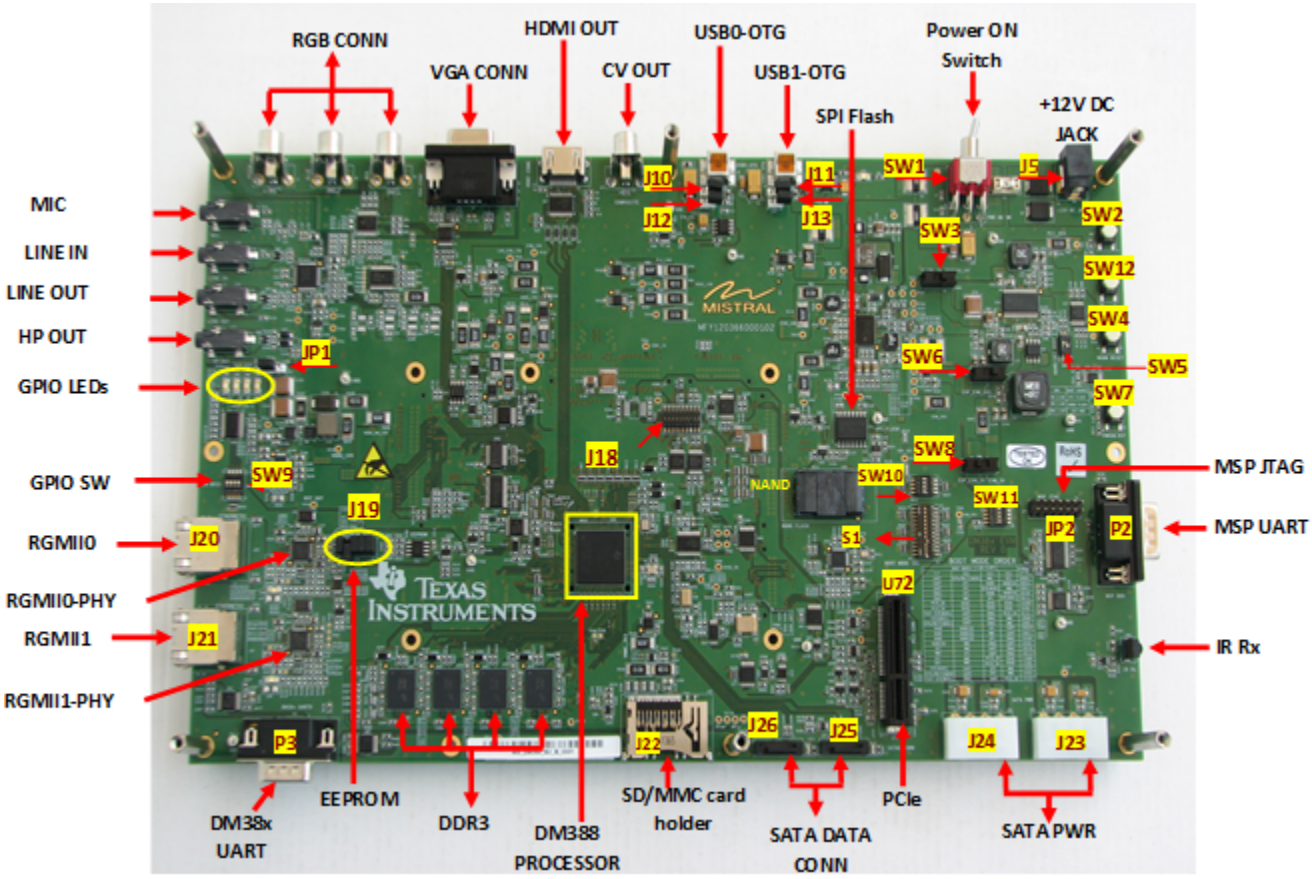
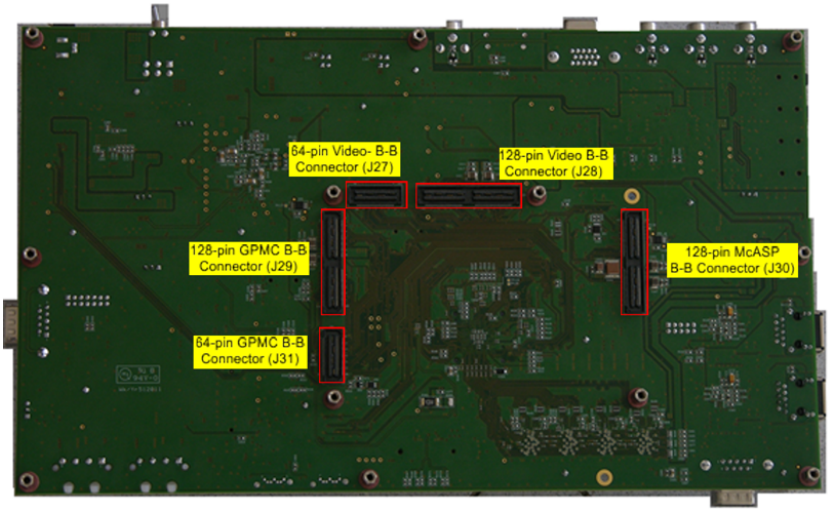


Figure 3-2 shows the bottom view of the DM388.

Figure 3-2. TMDXEVM388 Base EVM (Bottom View)



3.2 Connectors, Switches, Headers, and Jumpers

The DM388 base EVM has several connectors, switches, headers, and jumpers that serve various purposes. These components are detailed in the subsections that follow.

3.2.1 SD/MMC Card Holder

The SD/MMC card holder is a 28-pin connector that is on the top side of the board; the card holder provides an interface to a SD/MMC card. Figure 3-3 shows the location of SD/MMC connector on the base EVM.

Figure 3-3. SD/MMC Card Holder

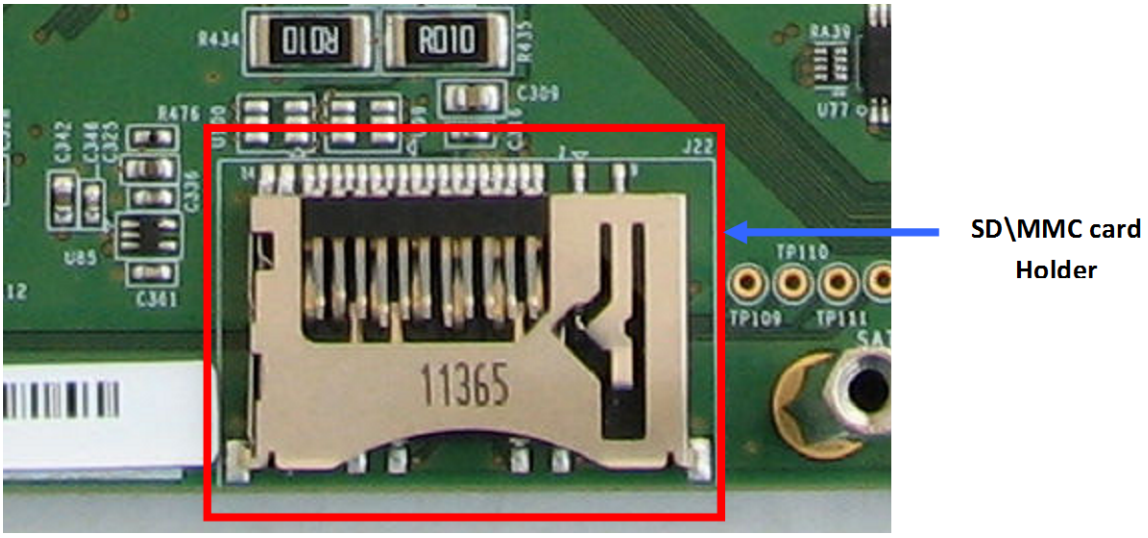


Table 3-1 provides the pinout details of the SD/MMC card holder (J22).

Table 3-1. Pinout of SD/MMC Card Holder

Pin Number	Signal Name	Pin Number	Signal Name
1	MMC1_DAT3	15	MMC1_SD_CD
2	MMC1_CMD	16	NC
3	GND	17	NC
4	VMMC	18	GND
5	MMC1_CLK	19	NC
6	GND	20	NC
7	MMC1_DAT0	21	GND
8	MMC1_DAT1	22	NC
9	MMC1_DAT2	23	NC
10	NC	24	NC
11	NC	25	NC
12	NC	26	NC
13	NC	27	GND
14	MMC1_SD_WP	28	GND

3.2.2 JTAG Header

A JTAG emulator can be used for advanced debugging by connecting it to the JTAG header on the top side of the EVM. The JTAG header has 20 pins (10 × 2, 1.27-mm pitch). If the user has a 14-pin JTAG version, then users must contact their emulator supplier for the appropriate adapter. All JTAG signal levels are 3.3 V.

Figure 3-4 shows the location of the JTAG header.

Figure 3-4. JTAG Header

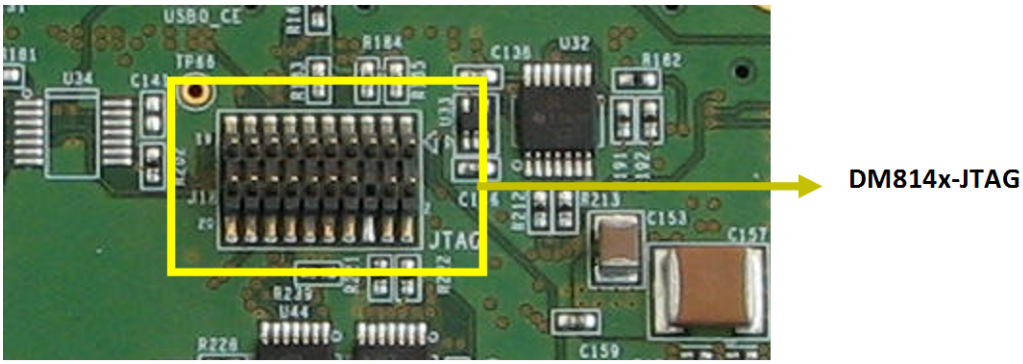


Table 3-2 provides the pinout details of the JTAG header (J18).

Table 3-2. Pinout of JTAG Header

Pin Number	Signal Name
1	TMS
2	TRSTN
3	TDI
4	TDIS
5	TVD
6	KEY
7	TDO
8	GND1
9	TCKRTN
10	GND2
11	TCLK
12	GND3
13	EMU0
14	EMU1
15	SRST
16	GND4
17	EMU2
18	EMU3
19	EMU4
20	GND5

3.2.3 Component Video Out

A T.V. or monitor that supports HD DAC inputs can be connected to the component video connectors (RGB connectors) of the base EVM board by using a component video cable. HD DAC signals from the DM388 processor are connected to the RGB connectors through video-amplifier U5. Component video connectors J7 (green), J9 (blue), and J6 (red) are 4-pin connectors (see Figure 3-5).

Figure 3-5. Component Video Connectors

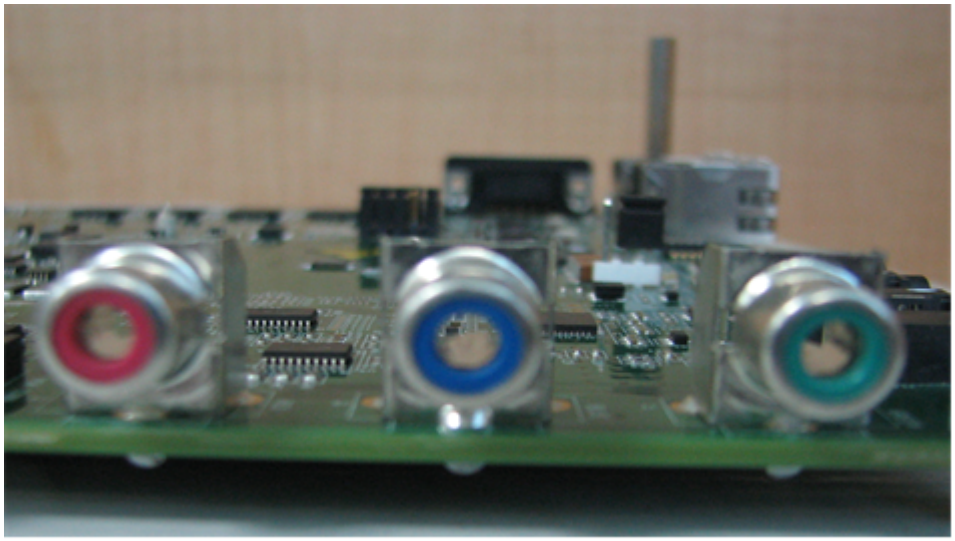


Table 3-3 provides the pinout details of the RGB connectors.

Table 3-3. Pinout of RGB Connector

Pin Number	Signal
1	VIDEO OUT
2	GND
3	GND
4	GND

Figure 3-6 shows an example of a component video cable.

Figure 3-6. Component Video Cable

3.2.4 VGA Connector

A VGA cable can be used to connect a T.V. or monitor to the DM388 EVM through the VGA connector (P1) provided on the board. HD DAC signals from the video-amplifier (U5) are shared with VGA connector P1. VGA connector P1 is a 15-pin female connector.

Signals from U5 are passed through ESD protection IC TPD7S019-15DBQR and then go to the VGA connector.

Figure 3-7 shows a top view and side view of the VGA connector.

Figure 3-7. VGA Connector

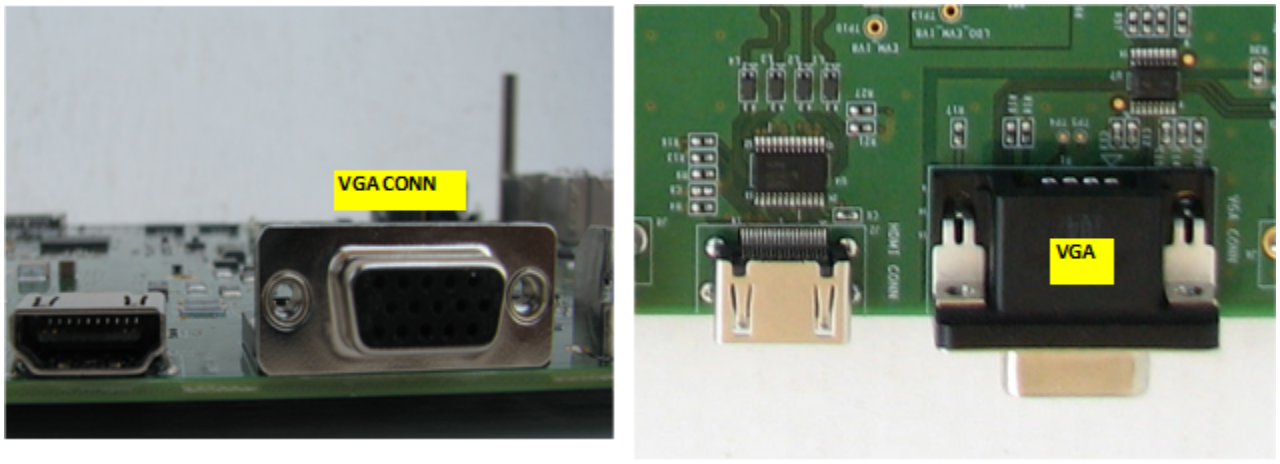


Table 3-4 provides the pinout details of the VGA connector.

Table 3-4. Pinout of VGA Connector

Pin Number	Signal Name
1	Red video
2	Green video
3	Blue video
4	NC
5	GND
6	GND
7	GND
8	GND
9	EVM_5V0
10	GND
11	NC
12	I2C2_SDA_BUF
13	VGA_HSYNC
14	VGA_VSYNC
15	I2C2_SCL_BUF

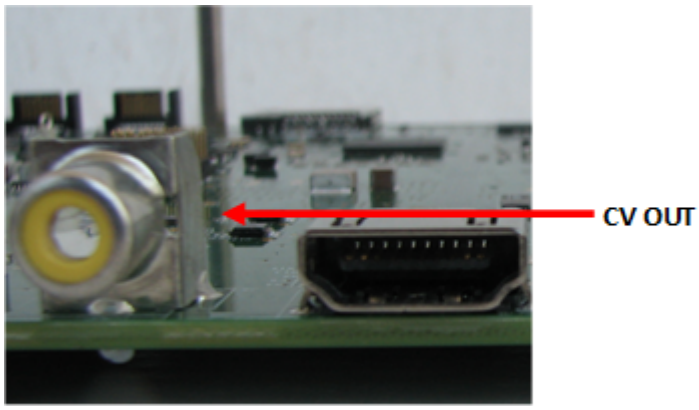
Figure 3-8 shows an example of a VGA male-to-male cable.

Figure 3-8. VGA Male-to-Male Cable

3.2.5 Composite Video Connector

A composite video (CV) cable is used to connect a T.V. or monitor to the base board through the RCA jack (J8) provided on the board. Figure 3-9 shows J8 as viewed from the card edge.

Figure 3-9. Composite Video Out Connector



Composite video connector J8 is a 4-pin RCA connector. Do not plug the cable into connector J8 while the board is powered on.

Table 3-5 provides the pinout details of the CV OUT on the RCA connector.

Table 3-5. CV OUT

Pin Number	Signal
1	VIDEO OUT
2	GND
3	GND
4	GND

Figure 3-10. Composite Video Cable

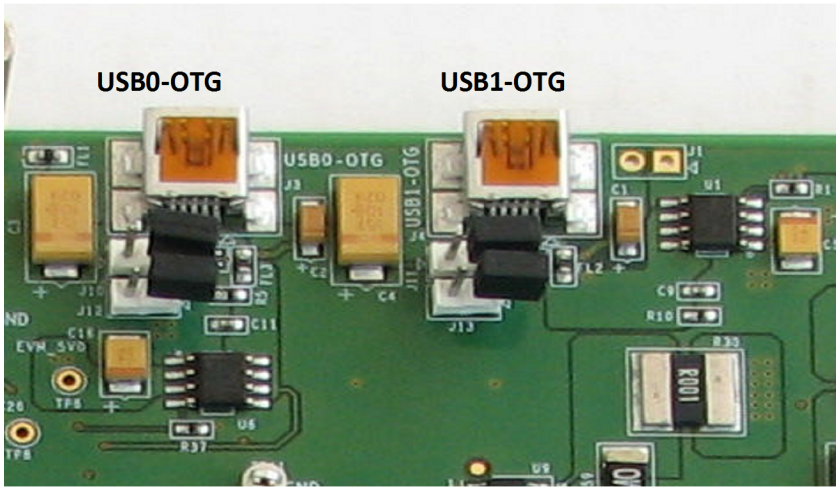
3.2.6 USB-OTG Connector

The DM388 EVM is equipped with two USB-OTG connectors (J3 and J4). Both USB interfaces are capable of dynamic role change; they can act as a host or as a device. TPD2E001DRLR ESD protection devices U2 and U3 are used for USB0 and USB1, respectively.

While configuring the OTGs in host-only mode, the header must be placed on J10 and J12 for USB0, and on J11 and J13 for USB1. Type A to mini-AB adapter is used to connect a memory stick, mouse, or other USB slave devices. The USBBx_DRV_VBUS signal from the processor is given to TPS2065DR (U6 and U1). This signal is driven high, enabling the TPS2065 IC to provide USBx_VBUS voltage to a connected slave device.

Figure 3-11 shows the connectors on the side of the board.

Figure 3-11. USB-OTG Connectors



The USB-OTG connector is a 9-pin, mini-AB connector. Table 3-6 provides the pinout details of the USB-OTG connector (J3 and J4).

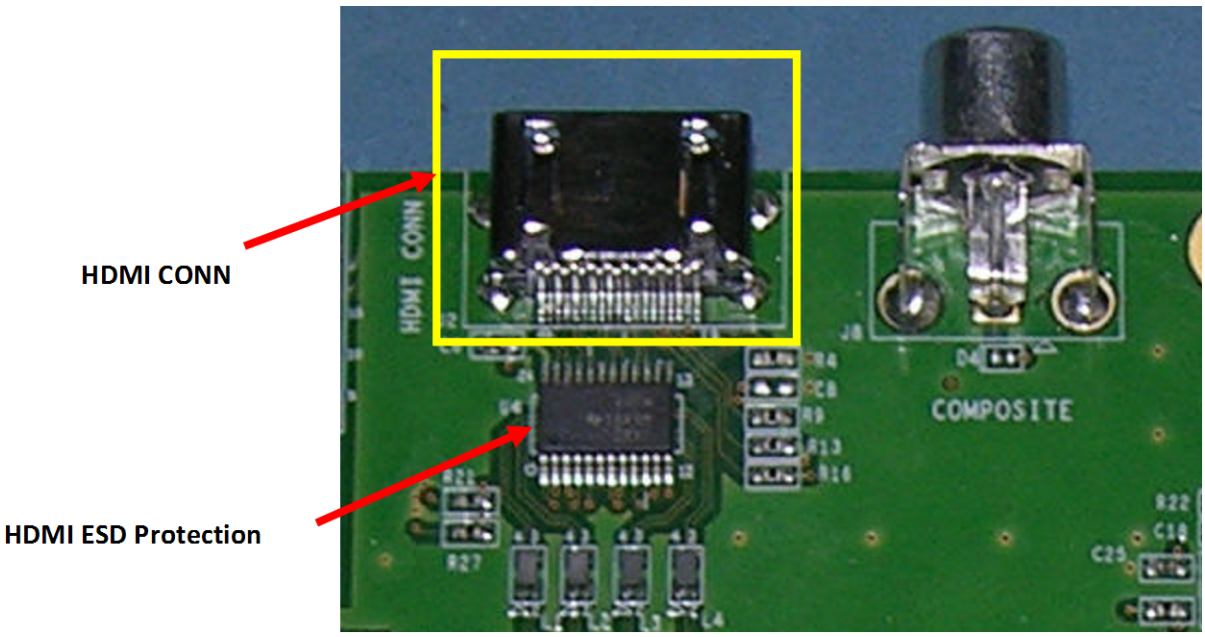
Table 3-6. Pinout of USB-OTG Connector

Pin Number	Pin Name	Pin Number	Pin Name
1	VCC	6	SH1
2	D+	7	SH2
3	D–	8	SH3
4	ID	9	SH4
5	GND		

3.2.7 HDMI OUT Connector

Any T.V. or monitor with an HDMI connection can be connected to the DM388 EVM through the HDMI connector. This connector is on the top side of the EVM. The HDMI signals from the processor are routed to the HDMI connector (J2) through an ESD protection device (TPD12S016PWR [U4]). Figure 3-12 shows the HDMI connector.

Figure 3-12. HDMI Connector



The HDMI connector is a 23-pin, type-A receptacle connector. Table 3-7 provides the pinout details of HDMI OUT J2.

Table 3-7. Pinout of HDMI OUT

Pin Number	Signal Name	Pin Number	Signal Name
1	HDMI_D2+	2	GND
3	HDMI_D2–	4	HDMI_D1+
5	GND	6	HDMI_D1–
7	HDMI_DO+	8	GND
9	HDMI_DO–	10	HDMI_CLK+
11	GND	12	HDMI_CLK–
13	CE_REMOTE_OUT	14	NC
15	DDC_CLK	16	DDC_DAT
17	GND	18	5V_OUT_HDMI
19	HDMI_HP_OUT	20	GND
21	GND	22	GND
21	GND	—	—

Figure 3-13 shows an example of an HDMI cable.

Figure 3-13. HDMI Cable

3.2.8 Ethernet Connector

The DM388 EVM has two RJ-45 connectors with magnetics for RGMII0 and RGMII1 interfaces. Both connectors are connected to the respective Ethernet PHY transceivers (AR8031-AL1A) through parallel termination. The AR8031-AL1A supports WoL interrupt to detect the magic packet and notify the sleeping system to wake up. The ENETx_WoL signal from U52 or U66 is given to GP0[12] of the DM388 processor through an OR gate (U53).

Figure 3-14 shows the Ethernet connectors.

Figure 3-14. Ethernet Connectors

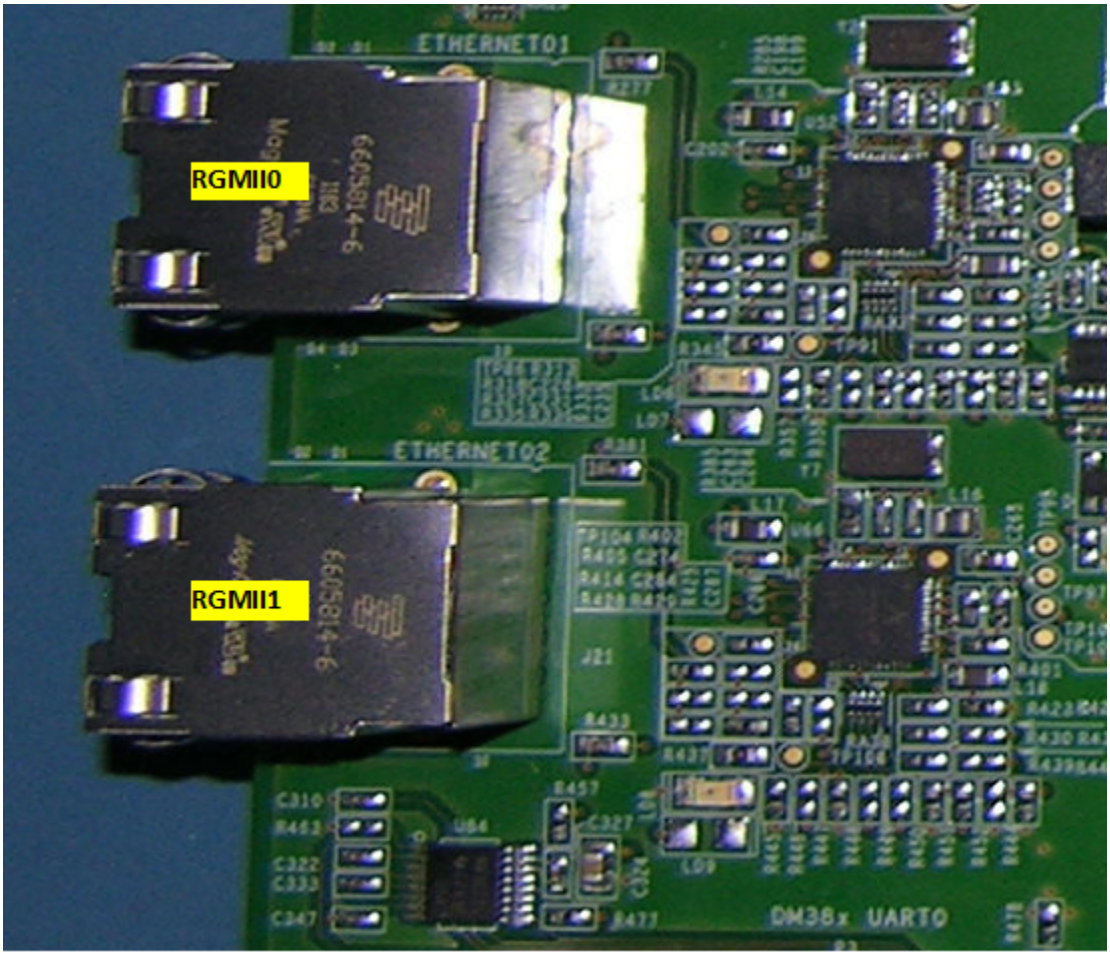


Table 3-8 provides the pinout details of the Ethernet connectors.

Table 3-8. Pinout of Ethernet Connectors

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	PHY_VDD_2V5
3	TRD[3]P	4	TRD[2]N
5	TRD[2]P	6	TRD[2]N
7	TRD[1]P	8	TRD[1[N
9	TRD[0]P	10	TRD[0]N
D1	ENET_LED_LINK	D2	GND
D3	ENET_LED_RX	D4	EVM_3V3
SH1	GND	SH2	GND

3.2.9 PCI Express Connector

The EVM has four PCIe 2.0 connectors with integrated PHY on the DM388 device. The dual mode (DM) core operates in endpoint (EP) mode or root complex (RC) port mode. The core supports one in port and one out port. The operating mode of the device, the role that the PCIe core assumes, is set to EP or RC based on the value that is sampled from the BOOTMODE[4:0] pins. Figure 3-15 shows the PCIe connector.

Figure 3-15. PCIe Connector

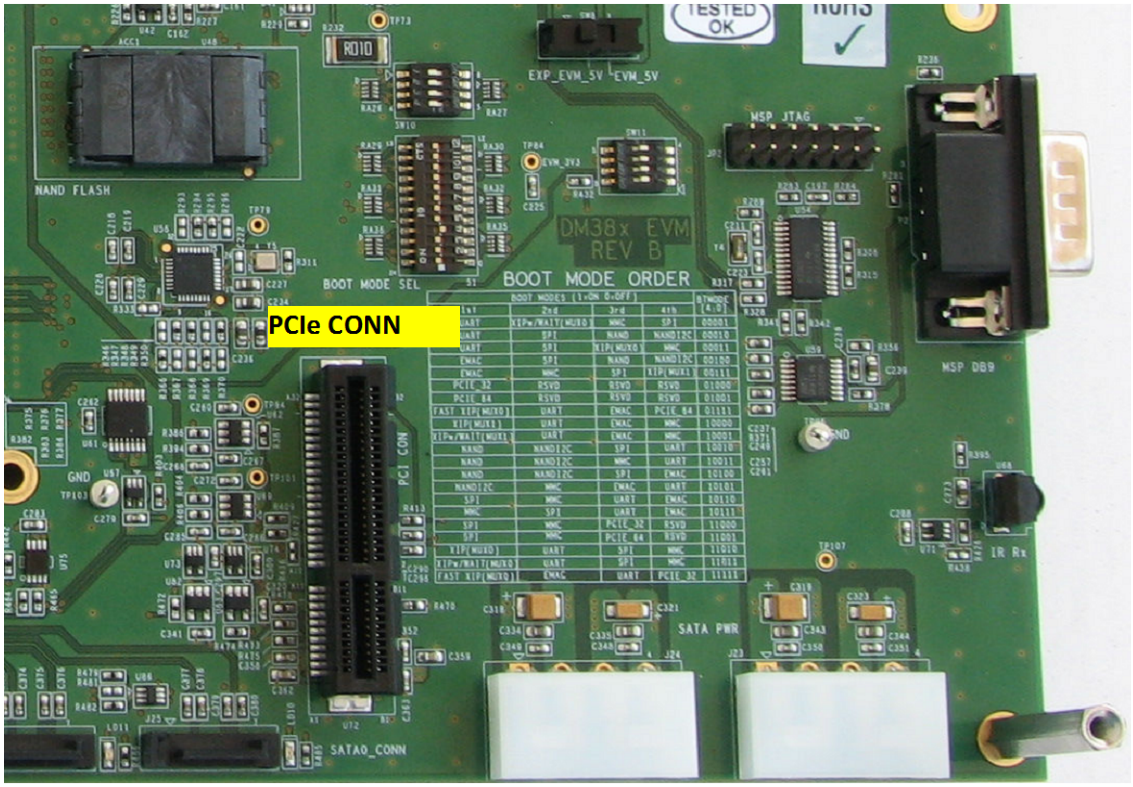


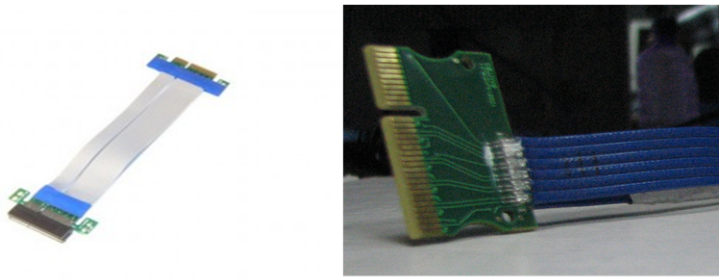
Table 3-9 provides the pinout details of the PCIe connector.

Table 3-9. Pinout of PCIe Connector

Pin Number	Pin Description	Pin Number	Pin Description
B1	IP_EVM_12V	A1	PRSNT#
B2	IP_EVM_12V	A2	IP_EVM_12V
B3	IP_EVM_12V	A3	IP_EVM_12V
B4	GND	A4	GND
B5	NC	A5	TCK
B6	NC	A6	TDI
B7	GND	A7	NC
B8	PCI_3V3	A8	TMS
B9	TRSTn	A9	PCI_3V3
B10	NC	A10	PCI_3V3
B11	NC	A11	PCI_CON_PORz
B12	NC	A12	GND
B13	GND	A13	REFCLKp
B14	CON.PCIE_TXP0	A14	REFCLKn
B15	CON.PCIE_TXN0	A15	GND
B16	GND	A16	CON.PCIE_RXP0
B17	PRSNT#	A17	CON.PCIE_RXN0
B18	GND	A18	GND
B19	NC	A19	NC
B20	NC	A20	GND
B21	GND	A21	NC
B22	GND	A22	NC
B23	NC	A23	GND
B24	NC	A24	GND
B25	GND	A25	NC
B26	GND	A26	NC
B27	NC	A27	GND
B28	NC	A28	GND
B29	GND	A29	NC
B30	NC	A30	NC
B31	PRSNT#	A31	GND
B32	GND	A32	NC

Figure 3-16 shows an example of a PCIe cable.

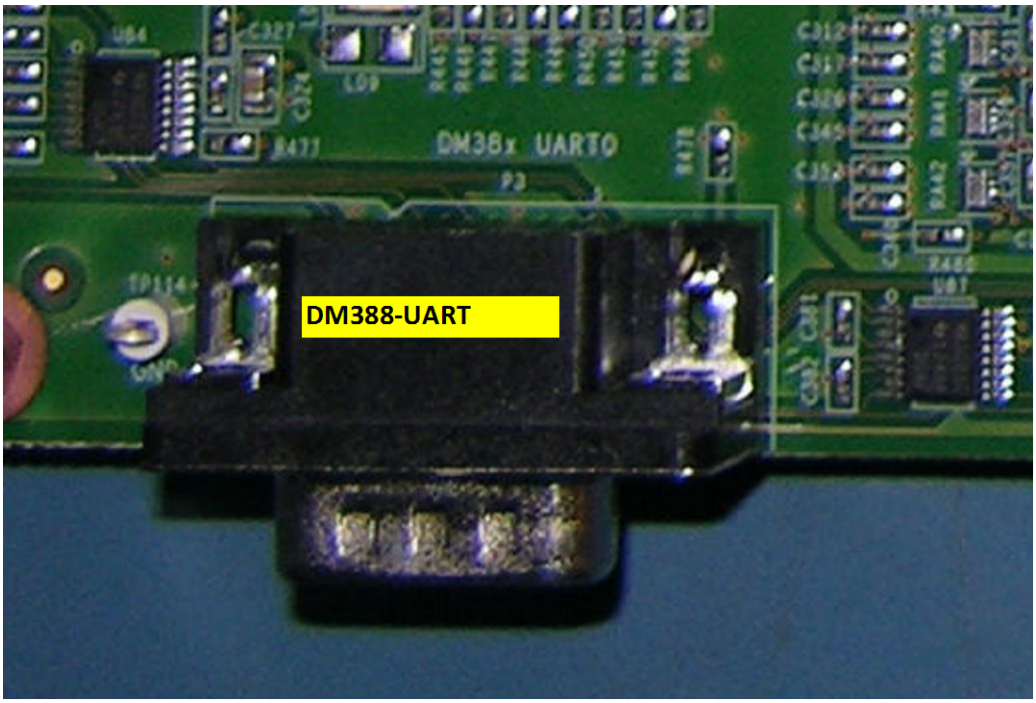
Figure 3-16. PCIe Cable



3.2.10 UART Connector

The EVM has two UART DB-9 connectors. One UART connector (P3) is connected to the DM388 through the RS-232 transceiver. The other UART connector (P2) is connected to the MSP430 MCU through the RS-232 transceiver. Figure 3-17 shows the UART connector of the DM388 device.

Figure 3-17. UART Connector



The voltage- and current-monitoring results calibrated by the MSP430 MCU can be viewed on the console through MSP430 UART connector.

Figure 3-18 shows the UART connector of the MSP430.

Figure 3-18. MSP430 UART Connector

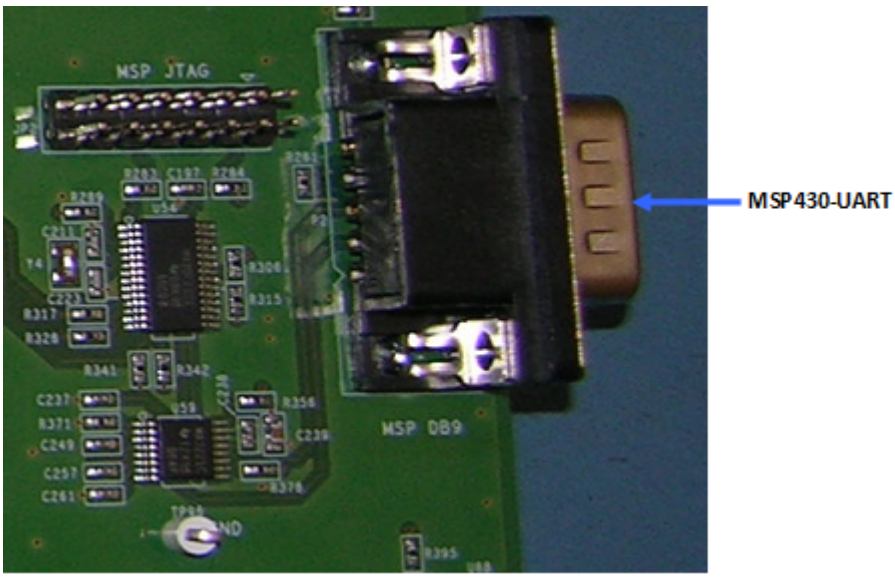


Table 3-10 provides the pinout details of the UART connectors.

Table 3-10. Pinout of UART Connectors

Pin Number	Description	Pin Number	Description
1	NC	7	RTS
2	RXD	8	CTS
3	TXD	9	NC
4	NC	10	UART_GND
5	GND	11	UART_GND
6	NC	—	—

Figure 3-19 shows a UART F-F serial cable.

Figure 3-19. UART F-F Serial Cable

3.2.11 EEPROM Header

The DM388 EVM has five 2-pin EEPROM headers on the board. A jumper should be put on the header as shown in Figure 3-20. To get the default connection from the DM388, place the jumper between pins 1 and 2 , 3 and 4, 5 and 6, and 9 and 10. Do not place a jumper between pins 7 and 8. Pins 7 and 8 must be shorted for the write-protect function of EEPROM.

Figure 3-20. EEPROM Header

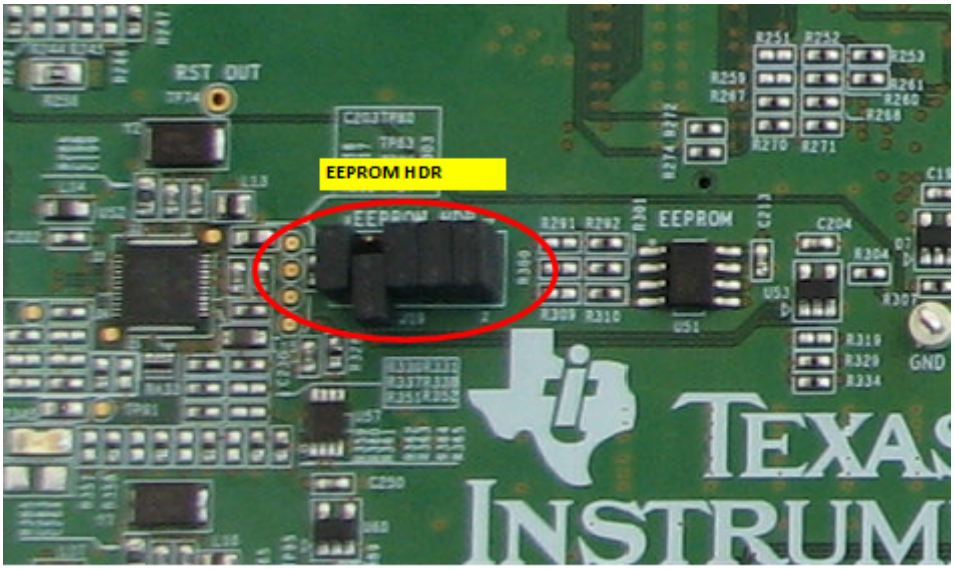


Table 3-11 provides the pinout details of the EEPROM header.

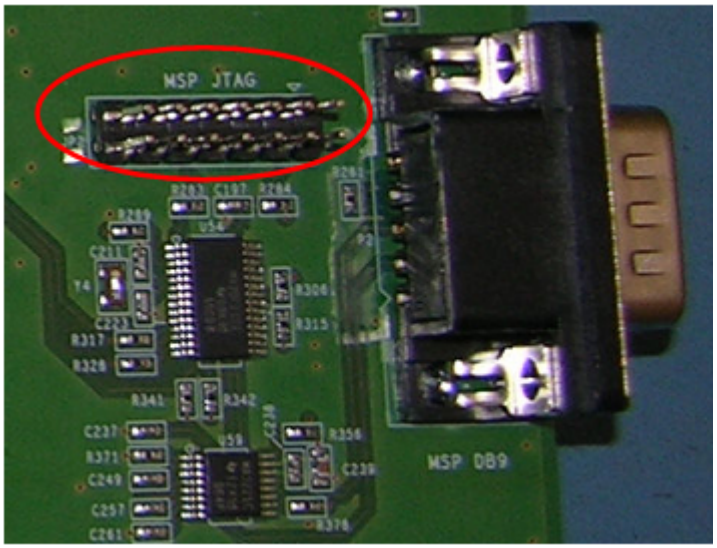
Table 3-11. Pinout of EEPROM Header

Pin Number	Description	Pin Number	Description
1	EVM_3V3	2	PROM_EVM_3V3
3	I2C0_SCL	4	PROM_I2C0_SCL
5	I2C0_SDA	6	PROM_I2C0_SDA
7	EVM_3V3	8	PROM_WP
9	GND	10	GND

3.2.12 MSP JTAG Header

The MSP430 MCU is used to monitor the voltage and current ratings on the chosen power rails that are connected to INA226 devices. INA226 devices are controlled through I2C0 lines. The MSP430 MCU must be programmed through the MSP430 emulator that is connected to the MSP JTAG header (JP2). The calibrated results can be observed on the console through the MSP-DB9 connector. Figure 3-21 shows the MSP JTAG header.

Figure 3-21. MSP JTAG Header



The DM388 EVM has a 14-pin (2 × 7), 2.54-mm pitch JTAG header to access the MSP430 MCU. Table 3-12 provides the pinout details of the MSP JTAG header.

Table 3-12. Pinout of MSP JTAG Header

Pin Number	Signal Name	Pin Number	Signal Name
1	MSP430_TDO/TDI	8	NC
2	NC	9	NC
3	NC	10	NC
4	EVM_3V3	11	NC
5	NC	12	NC
6	NC	13	NC
7	MSP430_TCK	14	NC

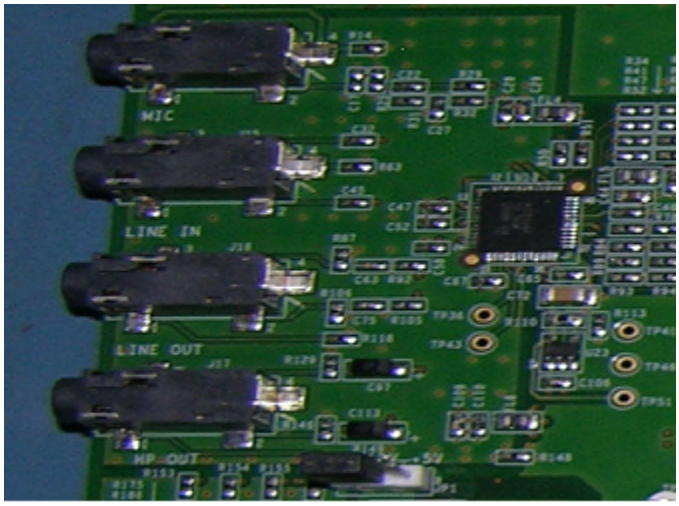
3.2.13 Audio Connectors

The DM81x and AM38x EVM includes an audio codec (TLV320AIC3106IRGZT) that is controlled through MCASP1 and I2C0 lines. The EVM has four audio connectors for different functions, such as:

- Headphone OUT (J17)
- Speaker OUT (J16)
- Audio LINE IN (J15)
- Microphone input (J14)

Figure 3-22 shows the audio codec connectors.

Figure 3-22. Audio Codec Connectors



Each connector is a 3.5-mm, 4-pin, female stereo jack that is connected to the audio codec through a coupling capacitor. Table 3-13 provides the pinout details of the audio LINE OUT connector.

Table 3-13. Pinout of Audio LINE OUT

Pin Number	Signal Name
1	GND
2	LEFT_OUT
3	RIGHT_OUT
4	NC

Table 3-14 provides the pinout details of the audio LINE IN connector.

Table 3-14. Pinout of Audio LINE IN

Pin Number	Signal Name
1	GND
2	LEFT_IN
3	RIGHT_IN
4	GND

Table 3-15 provides the pinout details of the audio MIC IN connector.

Table 3-15. Pinout of Audio MIC IN

Pin Number	Signal Name
1	GND
2	LEFT_IN
3	Shorted to pin 2
4	GND

Figure 3-23 shows examples of HP-out, mic-in, and line-in cables.

Figure 3-23. HP-Out, Mic-in, and Line-in Cables

3.2.14 Power Switches

The DM388 EVM has one DPDT switch (SW1) for main power (12-V supply) and three SPST, 3-pin slide switches for various purposes.

- SW3 (TOS65232 SW) – Connected to IP_EVM_12V when the switch position is toward the arrow mark, and off when it is away from the arrow mark.
- SW6 (EXP_EVM_3V3 SW) – Connected to EXP_EVM_3V3 when the switch position is away from the arrow mark, providing EVM_3V3 to the application board if required.
- SW8 (EXP_EVM_5V0 SW) – Connected to EXP_EVM_5V0 when the switch position is away from the arrow mark, providing EVM_5V0 to the application board if required.

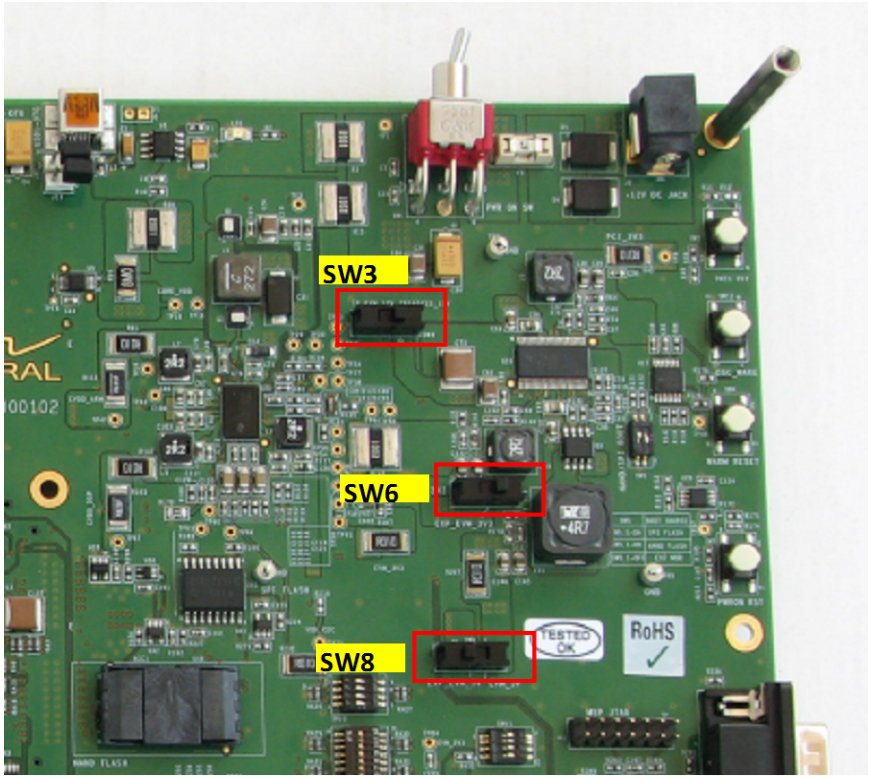
3.2.14.1 Default Switch Settings of EVM

Ensure the switches are positioned as follows when the EVM is powered on:

- SW3 – toward the arrow mark (right side)
- SW6 – toward the arrow mark (right side)
- SW8 – toward the arrow mark (left side)

Figure 3-24 shows the arrangement of the switches.

Figure 3-24. EVM Switch Arrangement



3.2.15 Boot Mode Switches

Switch positions 1 to 5 of S1 determine the order of boot modes. The first boot mode listed for each S1 [5:1] configuration is the primary boot mode. If the primary boot mode fails, the second, third, and fourth boot modes are executed in that order until a successful boot is completed.

The other positions of S1 [6:12] and SW10 [1:4] are reserved and are to be pulled down (off). The boot mode order table is silk screened on the EVM board for user convenience.

Figure 3-25 shows the boot mode switches.

Figure 3-25. Boot Mode Switches

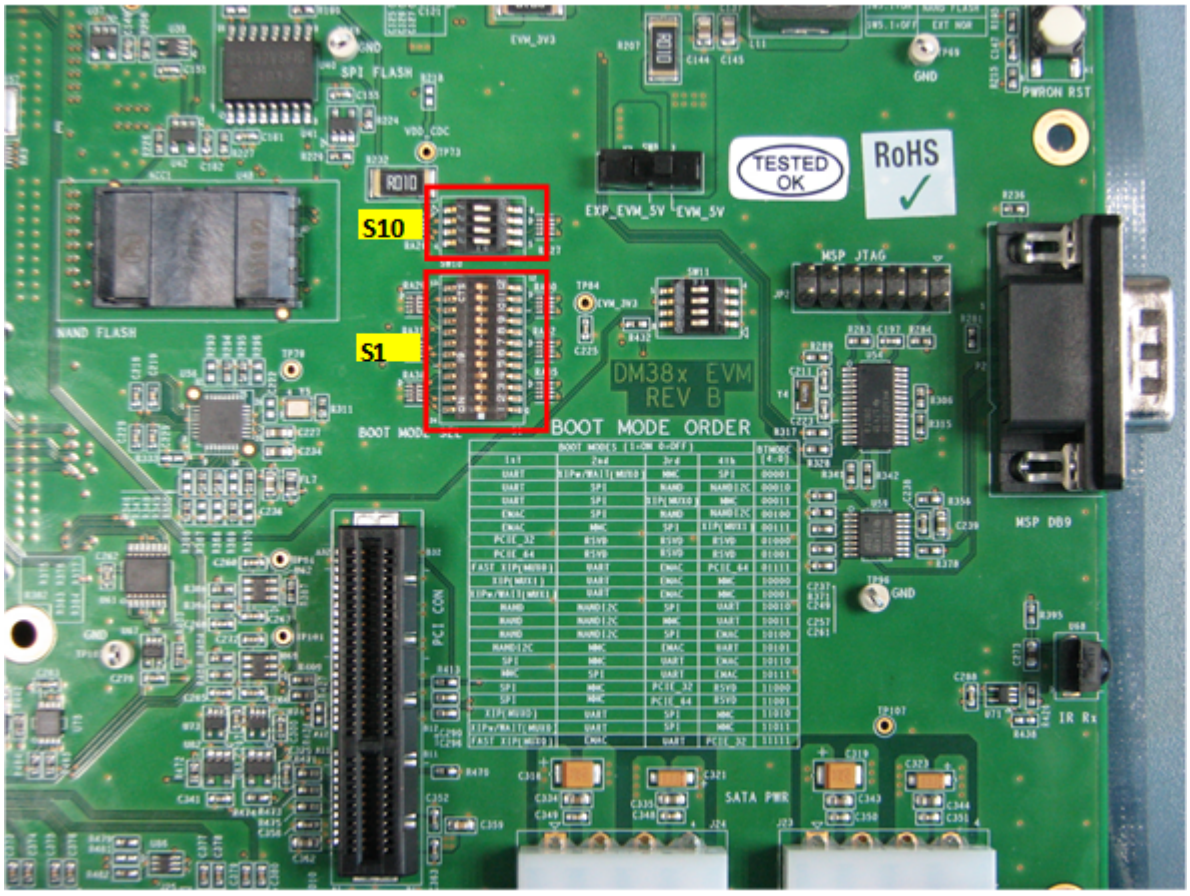


Table 3-16 provides the boot mode combinations.

Table 3-16. Boot Mode Combinations

S1.1	S1.2	S1.3	S1.4	S1.5	Boot Mode Order
0	1	0	0	1	NAND- NANDI2C- SPI- UART
1	0	0	0	0	UART-XIP/WAIT(MUX0)(1)-MMC-SPI
1	1	1	0	1	MMC-SPI –UART-EMAC
0	0	1	0	0	EMAC-SPI-NAND-NANDI2C

3.2.16 Reset Switch SW4

This switch generates a warm reset to the processor to reset all modules in the device except for the test and emulation logic and the EMAC switch. Table 3-17 provides the two settings and results of the warm-reset push-button.

Table 3-17. Warm Reset Push-Button

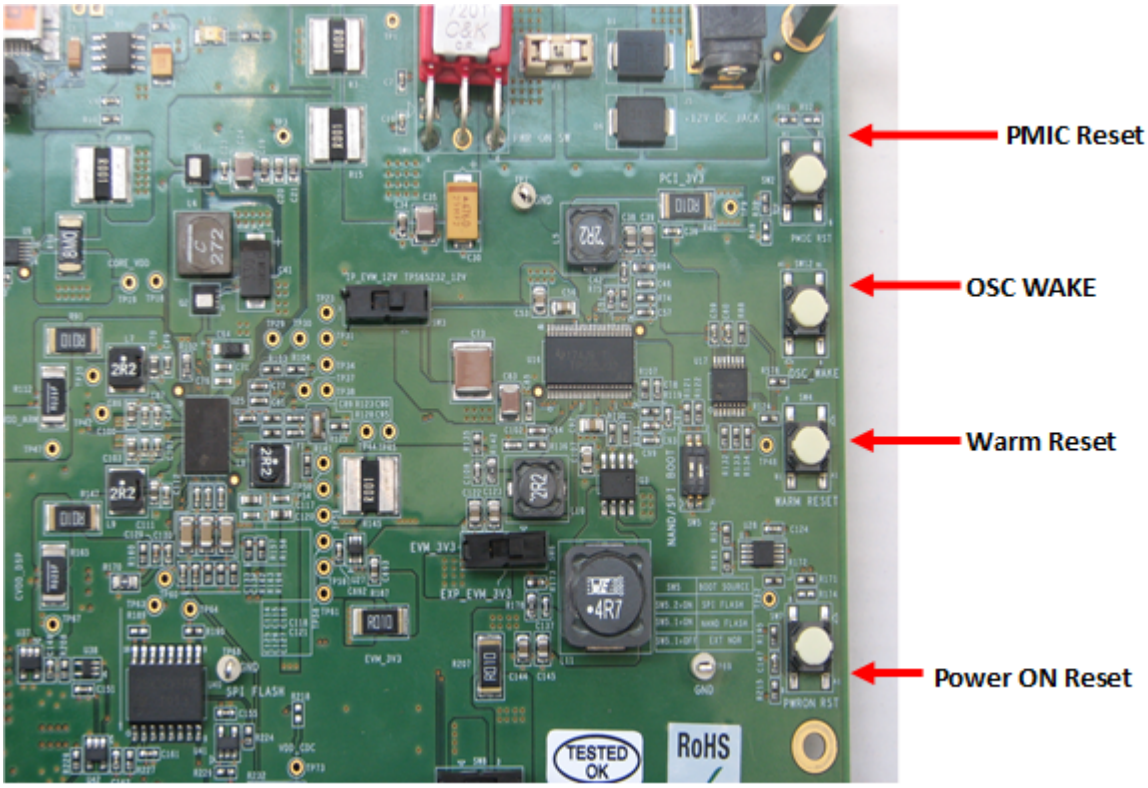
Setting	Result
Open	Normal operating condition. Open = logical 1 state
Push button closed	Active low reset signal. Closed = logical 0 state

The following sequence must be followed during a warm reset:

1. Ensure that the power supplies and input clock sources are stable.
2. Ensure that the RESET pin is asserted (low) for a minimum of 30 DEV clock cycles. The following things occur within the low period of the RESET pin:
   - All pins (except for the test and emulation pins) enter a Hi-Z mode and the associated pulls are enabled.
   - The PRCM asserts reset to all modules within the device, except for the test and emulation logic, EMAC switch, PLL, and clock configuration.
3. Deassert (drive high) the RESET pin. The following things occur when the RESET pin is deasserted:
   - All pins, except test and emulation pins, enter a Hi-Z mode and the associated pulls are enabled.
   - Reset to the ARM Cortex-A8 processor and modules without a local processor is deasserted except for the test and emulation logic, EMAC switch, PLL, and clock configuration.
   - If BTMODE[11] was latched as 0, then RSTOUT_WD_OUT is asserted for TBD DEV clock cycles.
   - The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
   - The ARM Cortex-A8 processor begins executing from the boot ROM.

Figure 3-26 shows the reset switches.

Figure 3-26. Reset Switches



3.2.17 Power-On Reset Switch SW7

Switch SW7 can be used to reset the entire chip (including the test and emulation logic and the EMAC switch). PORn is also referred to as a cold reset because it must be asserted when the device goes through a power-up cycle. Table 3-18 provides the two settings and results of the cold-reset push button.

Table 3-18. Cold-Reset Push-Button

Setting	Result
Open	Normal operating condition. Open = logical 1 state
Push button closed	Active low power-on reset. Closed = logical 0 state

The following sequence must be followed during a power-on reset (POR):

1. Wait for the power supplies to reach normal operating conditions while keeping the POR pin asserted (low).
2. Wait for input clock sources DEV_CLKIN, AUX_CLKIN, and SERDES_CLKN/P to be stable (if used by the system) while keeping the POR pin asserted.

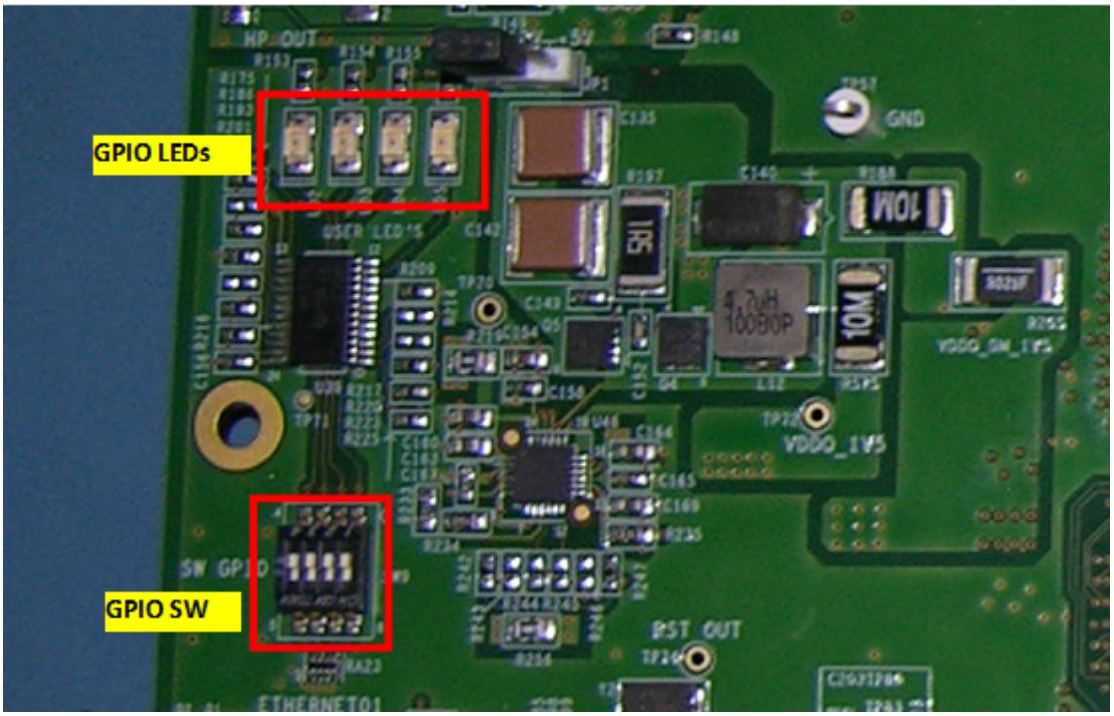
   When the power supplies and the input clock sources are stable, go to Step 3.
3. Ensure that the POR pin remains asserted for a minimum of two DEV clock cycles. The following things occur within the low period of the POR pin:
   - All pins (except the emulation pins) enter a Hi-Z mode and the associated pulls are enabled.
   - The PRCM asserts reset to all modules within the device.
   - The PRCM begins propagating these clocks to the chip with the PLLs in BYPASS mode.
4. Deassert (drive high) the POR pin. The followings things occur when the POR pin is deasserted:

- The BTMODE[15:0] pins are latched.
- Reset to the ARM Cortex-A8 processor and modules without a local processor is deasserted.
- If BTMODE[11] was latched as 0, then RSTOUT_WD_OUT is briefly asserted.
- The clock, reset, and power-down state of each peripheral is determined by the default settings of the PRCM.
- The ARM Cortex-A8 processor begins executing from the boot ROM.

3.2.18 GPIO Switches and LEDs

The DM388 EVM includes four LEDs and a GPIO switch (SW9) controlled by an I/O expander (PCF8575PWR [U39]) through an I2C0 interface. Figure 3-27 shows the GPIO switch and LEDs.

Figure 3-27. GPIO Switch and LEDs



3.2.19 Fuses

The DM388 EVM has a fuse (F1) near switch SW1. One end of F1 is connected to a Schottky barrier rectifier and transient voltage suppressors. The other end of F1 is connected to switch SW1.The current rating of F1 is 4 A and the voltage rating is 125 VDC.

3.3 Test Points

The DM388 EVM has many test points. All test points are available on the top side of the board. Figure 3-28 shows the position of each major test point.

Figure 3-28. Major Test Points

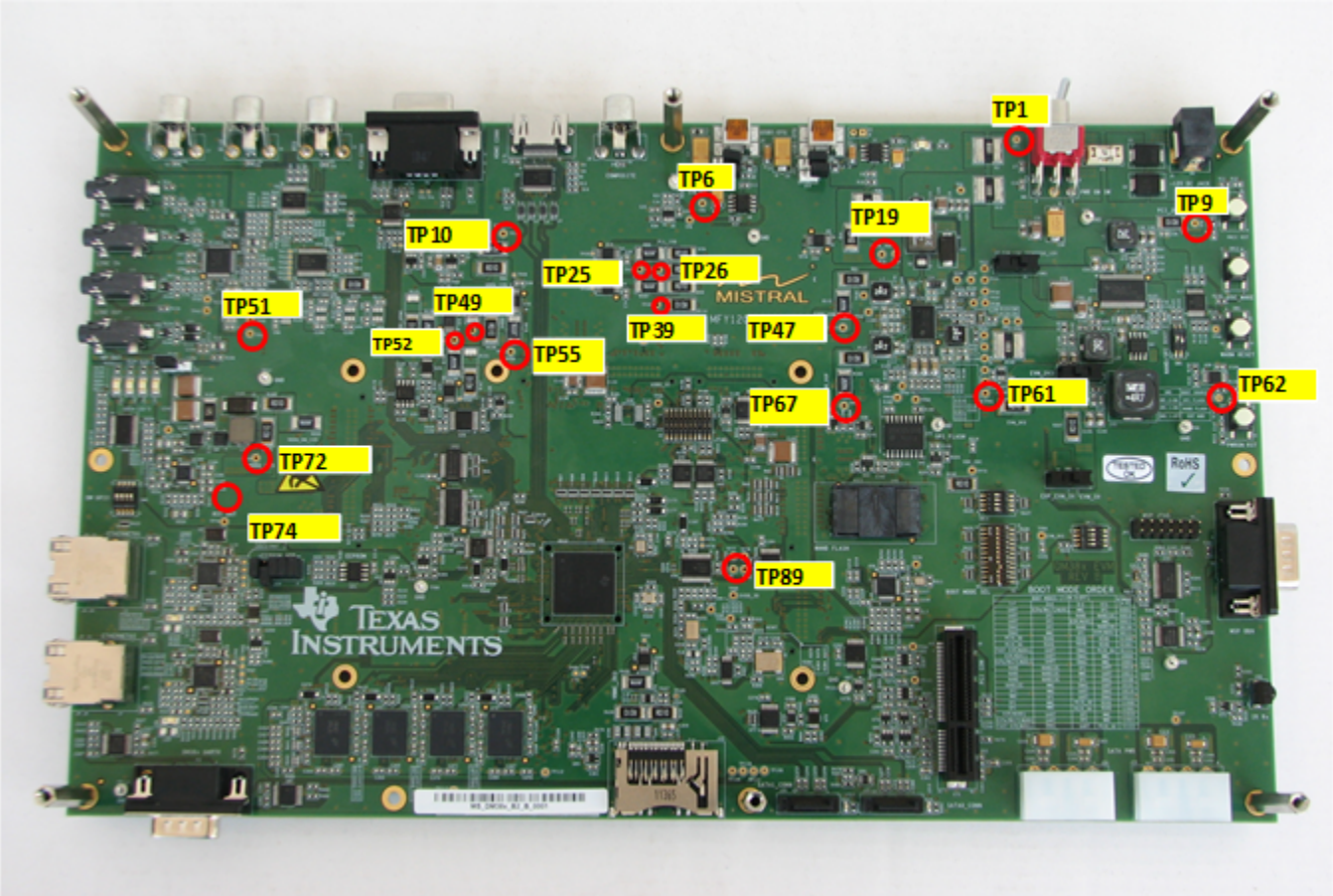


Table 3-19 lists each test point signal.

Table 3-19. Test Point Signals

Signal Number	Supply	Reference
1	IP_EVM_12V	TP1
2	EVM_5V0	TP6
3	LS_EVM_3V3	TP61
4	PCI_3V3	TP9
5	VDDQ_1V5	TP72
6	CORE_VDD	TP19
7	CVDD_ARM	TP47
8	CVDD_DSP	TP67
9	VDDA_1V8	TP49
10	PLL_1V8	TP25
11	VDDA_USB_1V8	TP39
12	VDAC_1V8	TP26
13	DVDD	TP55
14	DVDD_GPMC	TP52
15	DVDD_SD	TP89
16	EVM_1V8	TP10
17	VAIC_1V8	TP51
18	RSTOUTn	TP74
19	PORz	TP62

3.4 Expansion Connector

Table 3-20 provides the pinout details of the 64-pin, board-to-board video expansion connector (J27) of the EVM.

Table 3-20. 64-Pin Video Expansion Connector (J27)

Pin Number	Pin Description	Pin Number	Pin Description
1	VIN0_DE0	2	NC
3	GND	4	GND
5	VIN0_HSYNC	6	NC
7	NC	8	NC
9	GND	10	GND
11	VIN0_VSYNC	12	NC
13	NC	14	VIN0_DE1
15	GND	16	GND
17	NC	18	NC
19	NC	20	VIN0_FLD0
21	GND	22	GND
23	NC	24	CS12_DX4
25	NC	26	CS12_DY4
27	GND	28	GND
29	NC	30	CS12_DX3
31	NC	32	CS12_DY3
33	GND	34	GND
35	SPI1_SCLK	36	CS12_DX2
37	SPI1_MISO	38	CS12_DY2
39	GND	40	GND
41	SPI1_MOSI	42	CS12_DY1
43	SPI1_nCS0	44	CS12_DX1
45	GND	46	GND
47	NC	48	CS12_DY0
49	NC	50	CS12_DX0
51	GND	52	GND
53	NC	54	NC
55	NC	56	NC
57	GND	58	GND
59	NC	60	NC
61	GND	62	GND
63	GND	64	GND

Table 3-21 provides the pinout details of the 128-pin, board-to-board video expansion connector (J28) of the EVM.

Table 3-21. 128-Pin Video Expansion Connector (J28)

Pin Number	Pin Description	Pin Number	Pin Description
1	VIN0_DE0	2	VIN0_D0
3	GND	4	GND
5	VIN0_FLD0	6	VIN0_D2
7	VIN0_CLK1	8	VIN0_D9
9	GND	10	GND
11	VIN0_D1	12	VOUT0_G_Y_YC2
13	VIN0_D4	14	VOUT0_G_Y_YC6
15	GND	16	GND
17	VIN0_D11	18	VOUT0_R_CR4
19	VIN0_D5	20	VIN0_D6
21	GND	22	GND
23	VIN0_D12	24	VIN0_D8
25	VIN0_D10	26	VIN0_D3
27	GND	28	GND
29	VIN0_D14	30	VIN0_D7
31	VIN0_D13	32	VOUT0_G_Y_YC4
33	GND	34	GND
35	VIN0_D15	36	VOUT0_B_CB_C8
37	VOUT0_CLK	38	VOUT0_G_Y_YC5
39	GND	40	GND
41	VOUT0_G_Y_YC8	42	VOUT0_B_CB_C6
43	VOUT0_G_Y_YC7	44	VOUT0_B_CB_C5
45	GND	46	GND
47	EXP_EVM_3V3	48	IP_EVM_12V
49	EXP_EVM_3V3	50	IP_EVM_12V
51	GND	52	GND
53	EXP_EVM_5V0	54	IP_EVM_12V
55	EXP_EVM_5V0	56	IP_EVM_12V
57	GND	58	GND
59	VOUT0_B_CB_C9	60	VOUT0_B_CB_C3
61	VOUT0_R_CR2	62	VOUT0_B_CB_C7
63	GND	64	GND
65	VOUT0_R_CR6	66	VOUT0_G_Y_YC3
67	VOUT0_R_CR5	68	VOUT0_G_Y_YC9
69	GND	70	GND
71	VOUT0_R_CR9	72	VIN0_CLK0
73	VOUT0_HSYNC	74	VOUT0_B_CB_C4
75	GND	76	GND
77	VIN0_D16	78	VOUT0_B_CB_C2
79	VIN0_D17	80	VOUT0_R_CR3
81	GND	82	GND
83	VIN0_D18	84	VIN0_D19
85	VOUT0_VSYNC	86	VIN0_D20
87	GND	88	GND
89	NC	90	NC

Table 3-21. 128-Pin Video Expansion Connector (J28) (continued)

Pin Number	Pin Description	Pin Number	Pin Description
91	NC	92	VIN0_D21
93	GND	94	GND
95	VOUT0_AVID	96	VIN0_D22
97	NC	98	VOUT0_R_CR7
99	GND	100	GND
101	VIN0_FLD1	102	VOUT0_R_CR8
103	USB1_CE	104	VIN0_D23
105	GND	106	GND
107	NC	108	NC
109	NC	110	USB0_CE
111	GND	112	GND
113	PM_I2C_SCL	114	NC
115	PM_I2C_SDA	116	NC
117	GND	118	GND
119	NC	120	NC
121	GND	122	GND
123	GND	124	GND
125	GND	126	GND
127	GND	128	GND

Table 3-22 provides the pinout details of the 128-pin board-to-board GPMC expansion connector (J19).

Table 3-22. 128-Pin GPMC Expansion Connector (J19)

Pin Number	Pin Description	Pin Number	Pin Description
1	McA5_AXR0_EXO	2	PM_I2C_SCL
3	GND	4	GND
5	GPMC_nCS3	6	PM_I2C_SDA
7	EXP_GPMC_nCS0	8	OSC_WAKE
9	GND	10	GND
11	GPMC_nCS2	12	GPMC_A22
13	GPMC_nCS1	14	GPMC_A23
15	GND	16	GND
17	GPMC_WEN	18	GPMC_nCS4
19	McA5_AXR1	20	VOUT1_R_CR0
21	GND	22	GND
23	GPMC_OEN_REN	24	VOUT1_R_CR1
25	GPMC_nBE1	26	MMC2_DAT1
27	GND	28	GND
29	VOUT1_G_Y_YC1	30	MMC2_DAT2
31	MMC2_DAT0	32	MMC2_DAT3
33	GND	34	GND
35	VOUT1_B_CB_C1	36	VOUT1_B_CB_C2
37	VOUT1_B_CB_C0	38	MMC2_CLK
39	GND	40	GND
41	VOUT1_FLD_EXP	42	GPMC_WAIT0
43	GPMC_D0	44	McA5_AFSX_EXP
45	GND	46	GND

Table 3-22. 128-Pin GPMC Expansion Connector (J19) (continued)

Pin Number	Pin Description	Pin Number	Pin Description
47	EXP_EVM_3V3	48	IP_EVM_12V
49	EXP_EVM_3V3	50	IP_EVM_12V
51	GND	52	GND
53	EXP_EVM_5V0	54	IP_EVM_12V
55	EXP_EVM_5V0	56	IP_EVM_12V
57	GND	58	GND
59	GPMC_D2	60	VOUT1_G_Y_YC0
61	GPMC_D5	62	GPMC_nBE0_YC0
63	GND	64	GND
65	GPMC_D7	66	GPMC_D4
67	GPMC_D9	68	GPMC_D3
69	GND	70	GND
71	GPMC_D12	72	GPMC_D1
73	GPMC_D11	74	McA5_ACLKX
75	GND	76	GND
77	GPMC_D10	78	GPMC_nADV_ALE
79	GPMC_CLK	80	GPMC_D6
81	GND	82	GND
83	GPMC_D15	84	GPMC_D8
85	NC	86	GPMC_D13
87	GND	88	GND
89	NC	90	NC
91	AUXOSC_MXI	92	NC
93	GND	94	GND
95	NC	96	MMC0_DAT0
97	UART2_CTSn_EXP	98	MMC0_DAT1
99	GND	100	GND
101	SPI0_nCS0	102	GPMC_D14
103	SPI0_SCLK	104	MMC0_DAT2
105	GND	106	GND
107	GPMC_A21	108	SPI0_MOSI
109	SPI0_nCS1	110	SPI0_MISO
111	GND	112	GND
113	MMC0_CLK	114	DCAN0/UART2_RX
115	MMC0_CMD	116	MMC0_DAT3
117	GND	118	GND
119	EXP_UART0_RXD	120	DCAN0/UART2_TX
121	GND	122	GND
123	GND	124	GND
125	GND	126	GND
127	GND	128	GND

Table 3-23 shows the pinout details of the 128-pin board-to-board MCASP expansion connector (J30).

Table 3-23. 128-Pin MCASP Expansion Connector

Pin Number	Pin Description	Pin Number	Pin Description
1	PM_I2C_SCL	2	I2C2_SDA/UART2_TXD_EXP
3	GND	4	GND
5	PM_I2C_SDA	6	I2C2_SCL/UART2_RXD_EXP
7	EXP_MCA2_AXR0	8	I2C0_SDA
9	GND	10	GND
11	MCA1_AXR2	12	I2C0_SCL
13	EXP_MCA2_AXR1	14	I2C1_SDA
15	GND	16	GND
17	MCA1_AXR3	18	I2C1_SCL
19	EXP_MCA2_ACLKX	20	MCA0_AXR3
21	GND	22	GND
23	MCA2_AXR2	24	MCA0_AXR2
25	EXP_MCA2_AFSX	26	NC
27	GND	28	GND
29	AUD_CLKIN2	30	AUD_CLKIN0
31	MCA2_AXR3	32	MCA0_AFSR
33	GND	34	GND
35	MCA1_AXR1	36	MCA0_ACLKX
37	MCA1_AXR0	38	MCA0_AFSX
39	GND	40	GND
41	VOUT1_G_Y_YC8	42	MCA1_AFSX
43	VOUT1_B_CB_C9	44	MCA0_AXR1
45	GND	46	GND
47	EXP_EVM_3V3	48	IP_EVM_12V
49	EXP_EVM_3V3	50	IP_EVM_12V
51	GND	52	GND
53	EXP_EVM_5V0	54	IP_EVM_12V
55	EXP_EVM_5V0	56	IP_EVM_12V
57	GND	58	GND
59	AUD_CLKIN1	60	VOUT1_G_Y_YC4
61	MDIO_MDIO	62	MCA0_AXR5
63	GND	64	GND
65	MDIO_MDCLK	66	MCA0_AXR4
67	MCA1_ACLKX	68	MCA0_AXR0
69	GND	70	GND
71	COUT1_B_CB_C3	72	MCA1_ACLKR
73	VOUT1_B_CB_C4	74	NC
75	GND	76	GND
77	COUT1_B_CB_C6	78	MCA1_AFSR
79	VOUT1_B_CB_C5	80	VOUT1_G_Y_YC7
81	GND	82	GND
83	VOUT1_B_CB_C8	84	VOUT1_R_CR7
85	VOUT1_B_CB_C7	86	VOUT1_VSYNC
87	GND	88	GND
89	VOUT1_G_Y_YC3	90	VOUT1_R_CR8
91	VOUT1_G_Y_YC5	92	NC

Table 3-23. 128-Pin MCASP Expansion Connector (continued)

Pin Number	Pin Description	Pin Number	Pin Description
93	GND	94	GND
95	VOUT1_G_Y_YC6	96	MCA0_AXR9
97	VOUT_G_Y_YC9	98	VOUT1_HSYNC
99	GND	100	GND
101	VOUT1_R_CR4	102	NC
103	VOUT1_R_CR6	104	MCA0_ACLKR
105	GND	106	GND
107	VOUT1_R_CR5	108	NC
109	VOUT1_CLK	110	NC
111	GND	112	GND
113	VOUT1_R_CR9	114	VOUT1_AVID
115	NC	116	NC
117	GND	118	GND
119	NC	120	NC
121	GND	122	GND
123	GND	124	GND
125	GND	126	GND
127	GND	128	GND

Table 3-24 shows the pinout details of the 64-pin board-to-board GPMC expansion connector (J31).

Table 3-24. 64-Pin GPMC Expansion Connector

Pin Number	Pin Description	Pin Number	Pin Description
1	VOUT1_R_CR3	2	MCA3_ACLKX
3	GND	4	GND
5	EXP_UART0_TXD	6	GPMC_A20
7	MCA3_AXR0	8	GPMC_A18
9	GND	10	GND
11	VOUT1_R_CR2	12	GPMC_A19
13	MCA3_AXR1	14	GPMC_A17
15	GND	16	GND
17	MMC2_DAT7	18	MMC2_DAT5
19	MMC2_DAT6	20	VOUT1_G_Y_YC2
21	GND	22	GND
23	VOUT0_FLD_EXP	24	MCA3_AXR2
25	IO_EXP2_GP3	26	MCA3_AXR3
27	GND	28	GND
29	CLK32OUT	30	MCA3_AFSX
31	MCA4_ACLKX	32	EXP_UART0_CTSn
33	GND	34	GND
35	NC	36	EXP_UART0_RTSn
37	NC	38	GPMC_A16
39	GND	40	GND
41	NC	42	UART2_RTSn_EXP
43	NC	44	RSTOUTn
45	GND	46	GND
47	NC	48	IO_EXP2_GP1

Table 3-24. 64-Pin GPMC Expansion Connector (continued)

Pin Number	Pin Description	Pin Number	Pin Description
49	GPIO_VS_1	50	IO_EXP2_GP2
51	GND	52	GND
53	MCA4_AXR0	54	MCA4_AXR1
55	EXP_WARM_RESET	56	MCA4_AFSX
57	GND	58	GND
59	APP_PORz	60	MMC2_DAT4
61	GND	62	GND
63	GND	64	GND

Schematics

Figure A-1 through Figure A-38 show the schematics of the DM385 device.

Figure A-1. Version History

VERSION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	02/01/2012	SCHEMATICS "MS_TI_DM385EVM_REVA_SCH(VERSION 1.06)" IS TAKEN AS REFERNCE AND CHANGES ARE MADE FOR REVB AS LISTED BELOW	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
0.02	14/01/2012	1)MIC94060YC6 (U27 & U70) ICs ARE REPLACED WITH MIC94062YC6. 2)THE ESD PROTECTION ICs TPD2E007DCKR (U95,U96,U97) IS ADDED NEAR THE LINE-IN,LINE-OUT & HP-OUT JACK. 3)THE ESD PROTECTION ICs ESDALC6V1P6 (D12 & D13) IS ADDED ALONG THE MMC CONNECTOR LINES. 4)SWITCH IC SN74CB3Q3257PWR (U98) IS ADDED FOR GPMC ADDRESS PIN MUXING. TP71 REMOVED 5)A DECOUPLING CAPACITOR(C688) IS INCLUDED ON PIN B7(HDDDA_VREF) IN TMS320DM385. 6)NAME OF PIN B7 IN TMS320DM385 IS CORRECTED AS HDDAC_VREF FROM HDDDAC_VREF. 7)R273 IS MADE IN TO DNI. 8)R250 IS CHANGED TO 2.67K. 9)R44,R45,R46 ARE CHANGED TO 165OHM. 10)R481 IS MADE IN TO DNI AND R241 IS MADE IN TO 0 OHM. 11)A PUSH BUTTON SWITCH (SW12) IS INCLUDED FOR OSC_WAKE.	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
0.03	20/01/2012	1) R43 VALUE CHANGED TO 46.7K 2) R579 VALUE CHANGED TO 26.7K 3) U98 OE SIGNAL AND UNUSED INPUTS PULLED DOWN TO GND 4) ESDALC6V1P6 DEVICE(D12 & D13) DELETED AND ADDED TPD4E001(U99 & U100) ON MMC LINES 5) R26 AND R43 MADE AS DNI AND R58 IS MOUNTED 6) C689, C690 AND C691 ARE ADDED FOR U70 7) C692 AND C693 ADDED FOR U27 8) C694 ADDED FOR U98 9) SWAPPED THE MMC1 SIGNALS ON U99 AND U100 FOR ROUTING CONVENIENCE	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
1.00	24/01/2012	1) Baselined as 1.00	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
1.01	07/03/2012	THE RoHS NON COMPLIANT COMPONENTS ARE REPLACED WITH THE ALTERNATIVES THAT ARE RoHS COMPLIANT: 1) T494A106M016AS (C321,C323) ARE REPLACED BY T494A106M016AT. 2) 9C06031A2212FKHFT (R64,R142,R178) ARE REPLACED BY RC0603FR-0722K1L. 3) 9C04021A10R0JLHF3 (R85,R89,R90,R94) ARE REPLACED BY ERJ-2GEJ100X. 4) TDA04H0SK1 (SW9,SW10,SW11) ARE REPLACED BY GDH04S04.	MISTRAL DESIGN TEAM	MANJUNATHA BM	KRISHNA PRASAD A
1.02	09/05/2016	SATA INTERFACE DNI'd (J23,J24,J25,J26,U86,C310,C350,C343,C323,C351,C344,C318,C349,C334,C321, C348,C335,C683,R479,R486,R485,R482,LD10,LD11)	MISTRAL DESIGN TEAM	KRISHNA PRASAD A	KRISHNA PRASAD A

REV NO.	NATURE OF CHANGE	APPROVED BY	DATE

MISTRAL **Mistral Solutions [P] Ltd.**
#60 Adarsh regent,100 Feet Ring Road, Domlur Extension
Banglore 560 071. Ph : +91-80-30912600. Fax :+91-80-2535 6444

Drawn by: MISTRAL DESIGN TEAM | Approved by: KRISHNA PRASAD A
Date: Monday, May 31, 2010 | Date Monday, August 08, 2016
Design file path: D:\SVN\TI_DM3\X_50\07_HARDWARE\SCsEMATICS\DM385\MS_TI_DM385EVM_REVB_SCH.DSN

Title VERSION HISTORY
Size C | Document Number MS_TI_DM385EVM_REVB_SCH | Rev B
Date: Monday, August 08, 2016 | Sheet 2 of 39

Figure A-2. DM385 Block Diagram

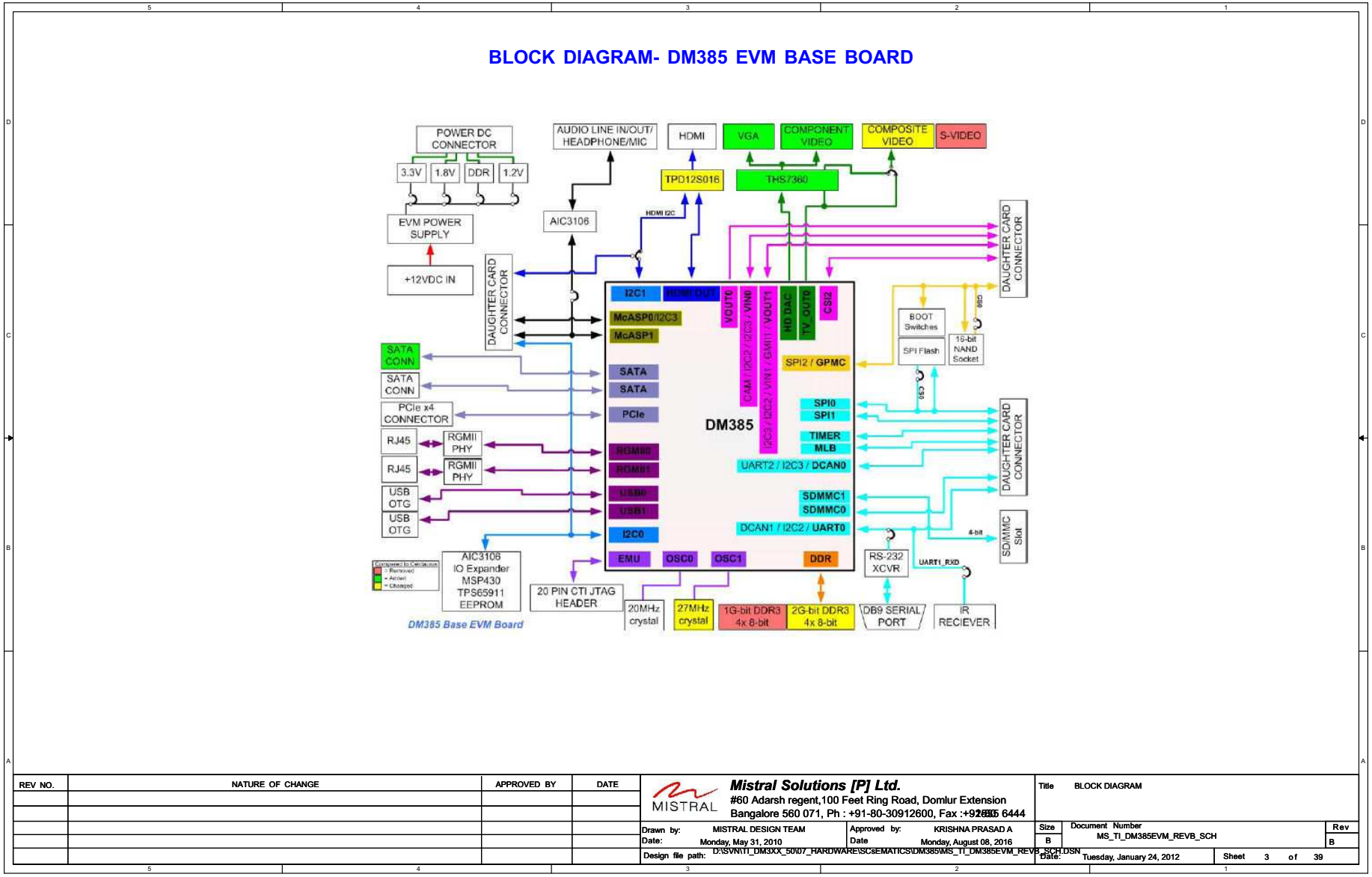


Figure A-3. Memory Map

MEMORY MAP TO BE UPDATED

ETHERNET-GPMC	
NAND-GPMC	
DDR-0	
SPI FLASH	
I2C DEVICES	
I2C0- AUDIO CODEC	0011000
I2C0- EEPROM	1010000
I2C0- PCF8575-1	0100000
I2C0- PCF8575-2	0100011
I2C1- HDMI	
I2C2- PCF8575-3	0100000
PMI2C	

I2C POWER MONITORS---MSP430

PM_I2C ADDRESS	
PLL_1V8	1000000
HDMI_CSI_1V8	1000001
CVDD_ARM	1000010
VDDQ_DM_1V5	1000011
VDDA_1V8	1000101
DVDD_GPMC	1000110
CVDD_DSP	1001001
CORE_VDD	1001000
DVDD	1000100
DVDD_C	1000111
VMMC	1001010

GPIO ASSIGNMENT(SAME AS CENTAURUS)

GPIO NAME	SOURCE	PURPOSE
ENET_INT	GP1[10]	ETHERNET
PCF8575_INT_IO1	GP1[4]	I NTERRUPT
TPS_INT1	TPS659113-- INT 1	INTERRUPT FROM PMIC
EN_BCK2_LS	TPS659113-- GPIO 7	ENABLING LOAD SWITCH
EN_TPS62350 (REMOVED)	TPS659113-- GPIO 6	ENABLING CVDD_HDVICP
EN_BCK3_TPS65232	TPS659113-- GPIO 2	ENABLING PCI_3V3
EN_TPS51116	TPS659113-- GPIO 0	ENABLING DDR SUPPLY
MSP430_INT	PCF8575 DEVICE-1	INTERRUPT FOR MSP430
EXP_ETH_RESET	PCF8575 DEVICE-1	ETHERNET RESET
TPS_SLEEP	PCF8575 DEVICE-1	SLEEP FOR TPS659113
PCI_SW_RESETn	PCF8575 DEVICE-1	PCI RESET
IR_REMOTE_OFF	PCF8575 DEVICE-1	IR SENSOR CONTROLLING
UART0_OFF	PCF8575 DEVICE-1	UART-0 CONTROLLING
GPMC_ADD_SELn	PCF8575 DEVICE-1	TO SELECT EITHER GPMC OR HDMI LINES.
SW_VOUT_EN	TDA04H0SK1 DEVICE	VIDEO SW ENABLE
GPMC_nWP	TDA04H0SK1 DEVICE	GPMC WRITE PROTECT
RESET_GPIO	TDA04H0SK1 DEVICE	ENABLING PCI POR BUFFER

GPIO ASSIGNMENT (NEWLY ADDED)

GPIO NAME	SOURCE	PURPOSE
ENET_WoL_INT	GP0[12]	WoL INTERRUPT
HDMI_CT_HPD	PCF8575 DEVICE -3	ENABLING LOAD SWITCH
HDMI_LS_OE	PCF8575 DEVICE -3	ENABLING LEVEL SHIFTER
DISABLE_SD	PCF8575 DEVICE -3	SD AND SF CHANNEL CONTROL OF VIDEO AMPLIFIER
DISABLE_SF	PCF8575 DEVICE -3	
BYPASS_SD	PCF8575 DEVICE -3	TO BYPASS LPF OF SD AND SF IN VA
BYPASS_SF	PCF8575 DEVICE -3	
FILTER1	PCF8575 DEVICE -3	SELECTABLE FILTER FOR SF CHANNELS
FILTER1	PCF8575 DEVICE -3	
IO_EXP2_GP1	PCF8575 DEVICE -2	GPIO USED IN CATLOG
IO_EXP2_GP2	PCF8575 DEVICE -2	GPIO USED IN CATLOG
MCA0_DEC_A MCA0_DEC_B	PCF8575 DEVICE -2	MCASP0 DECODER SELECT LINES
MCA1_MUX_SEL	PCF8575 DEVICE -2	MCASP1 MUX SELECT LINES
MCA0/1/3_RSEL_A MCA0/1/3_RSEL_B	PCF8575 DEVICE -2	MCASP0/1/3_R DECODER SELECT LINES
PCF8575_INT_IO2	GP0[13]	INTERRUPT
MCA0_AXR9	PCF8575 DEVICE -2	GPIO USED IN VC BOARD
IO_EXP2_GP3	PCF8575 DEVICE -2	GPIO USED IN VC BOARD
MCA5_MUX_OE	PCF8575 DEVICE -2	TO SELECT B/T GPIO N MCA5_AHCLKX
VOUT_FLD_SEL1	PCF8575 DEVICE -3	TO PROVIDE THE PIN MUXING OPTION FOR VOUT0/1_FLD PIN
VOUT_FLD_SEL2	PCF8575 DEVICE -3	
GPIO_VC_1	PCF8575 DEVICE -2	GPIO USED ON THE APPLICATION BOARD.
GPIO_VC_2	PCF8575 DEVICE -2	
MCA1_MUX2_nOE	PCF8575 DEVICE -2	MCASP1 MUXING SELECTION.

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Title: MEMORY MAP
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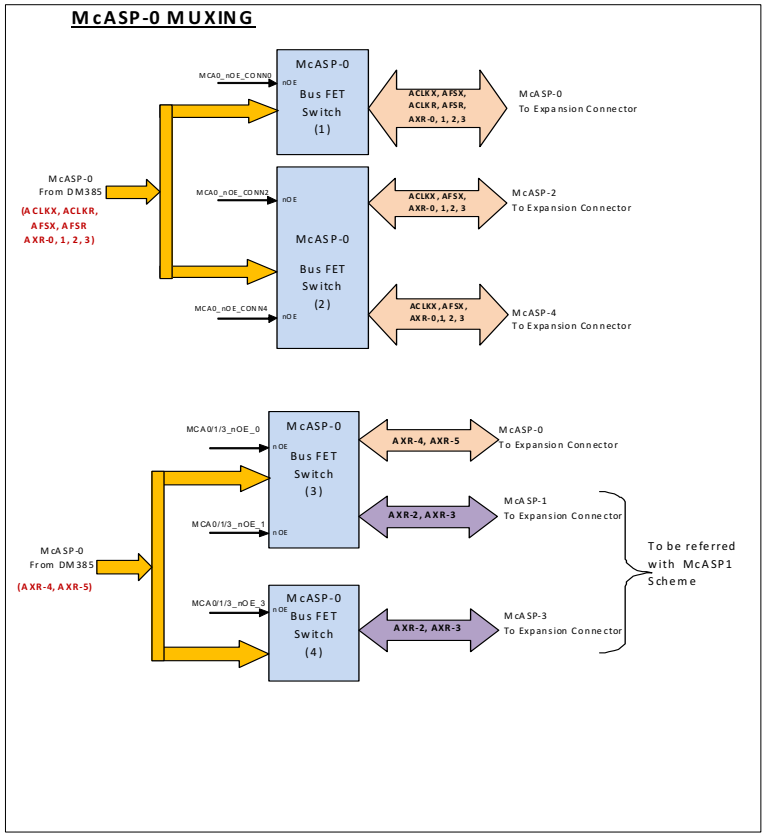
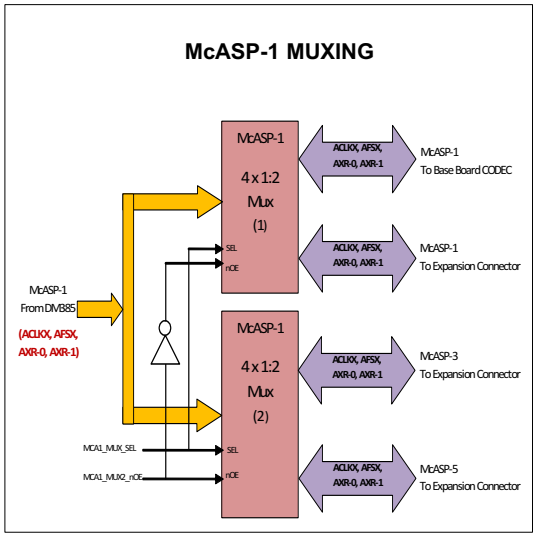
Figure A-4. McASP Muxing





To get McASP0 _AXR [4,5] on EXP Connector	Enable : MCA0/1/3_nOE_0
To get McASP1 _AXR [2,3] on EXP Connector	Enable : MCA0/1/3_nOE_1
To get McASP3 _AXR [2,3] on EXP Connector	Enable : MCA0/1/3_nOE_3

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Title: MCASP MUXING BLK DIAGRAM

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Figure A-5. DM385 McASP

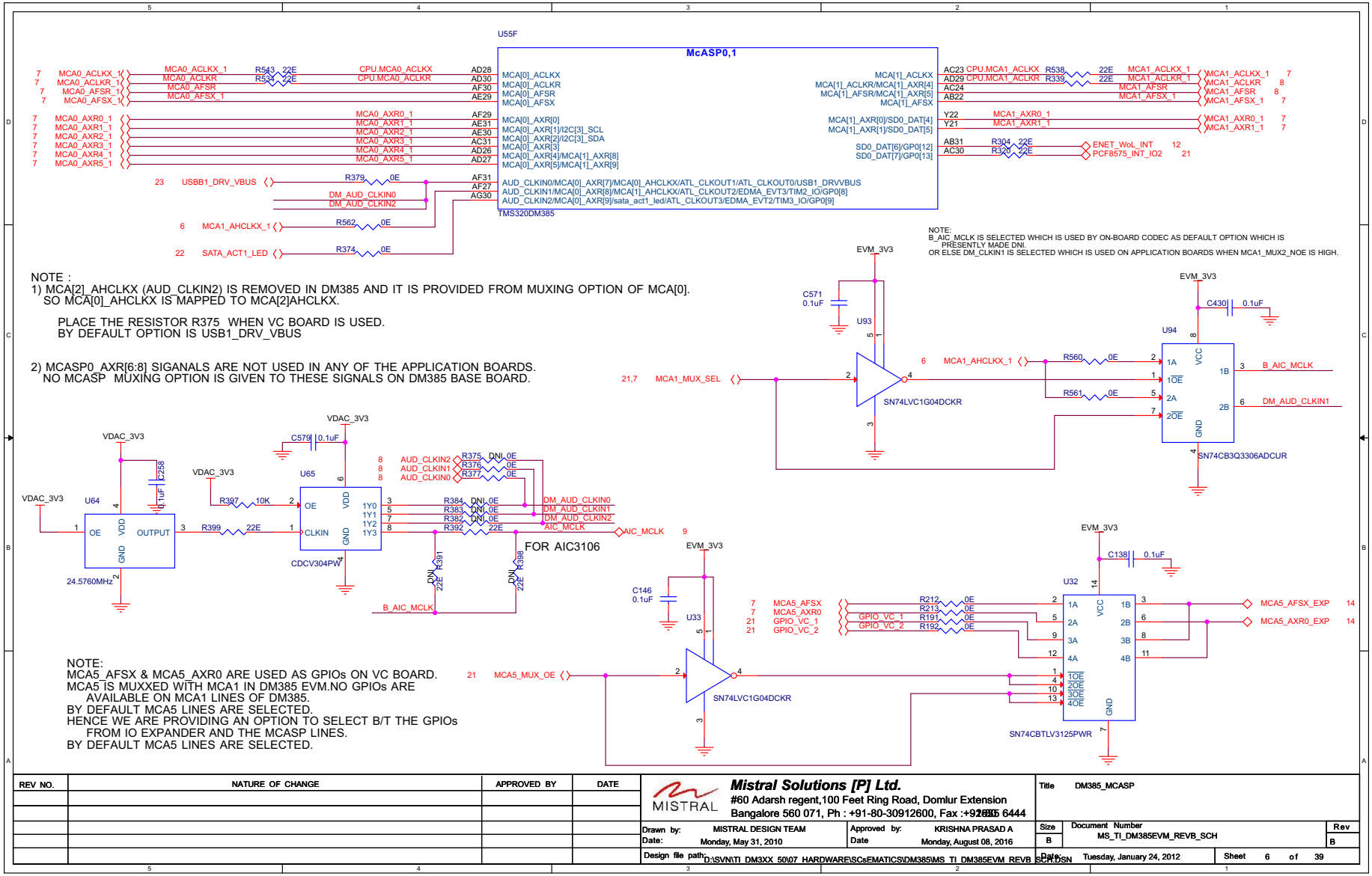
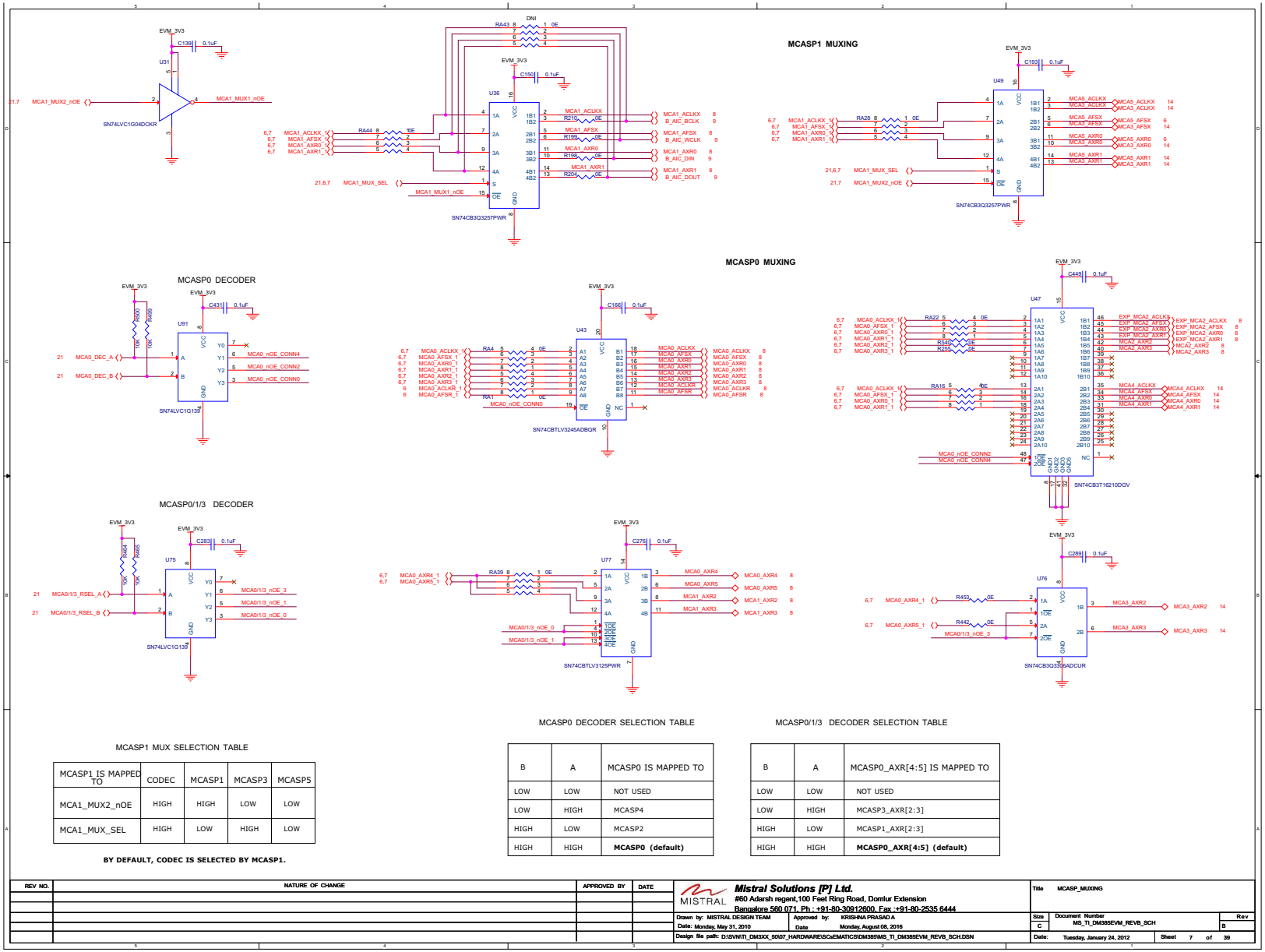


Figure A-6. McASP Muxing and Decoders



MCASP1_IS MAPPED TO	CODEC	MCASP1	MCASP3	MCASP5
MCA1_MUX2_nOE	HIGH	HIGH	LOW	LOW
MCA1_MUX_SEL	HIGH	LOW	HIGH	LOW

B	A	MCASP0 IS MAPPED TO
LOW	LOW	NOT USED
LOW	HIGH	MCASP4
HIGH	LOW	MCASP2
HIGH	HIGH	**MCASP0 (default)**

B	A	MCASP0_AXR[4:5] IS MAPPED TO
LOW	LOW	NOT USED
LOW	HIGH	MCASP3_AXR[2:3]
HIGH	LOW	MCASP1_AXR[2:3]
HIGH	HIGH	**MCASP0_AXR[4:5] (default)**

Figure A-7. McASP B-B Connection

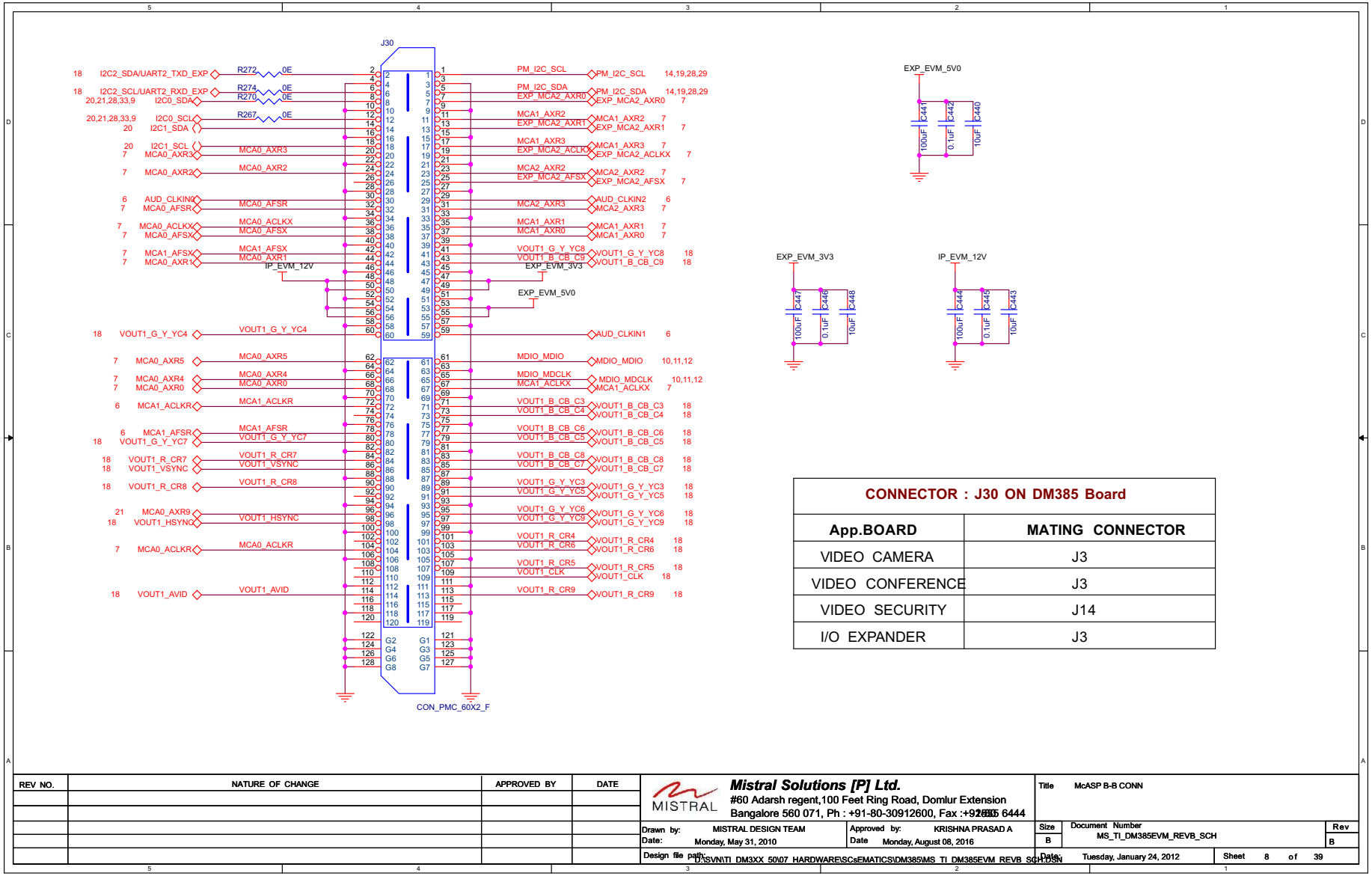


Figure A-8. AIC3106

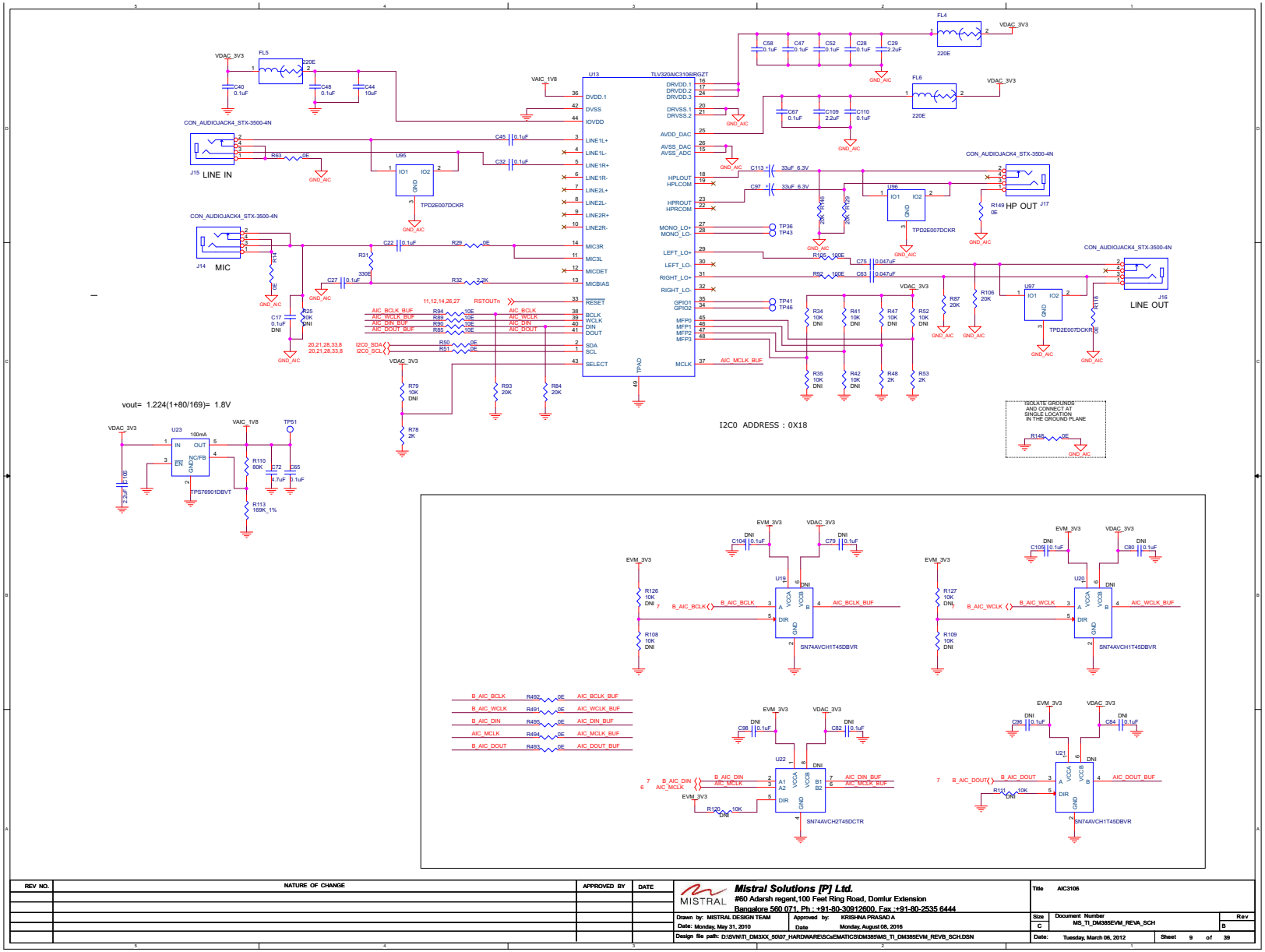


Figure A-9. GMII0 Interface

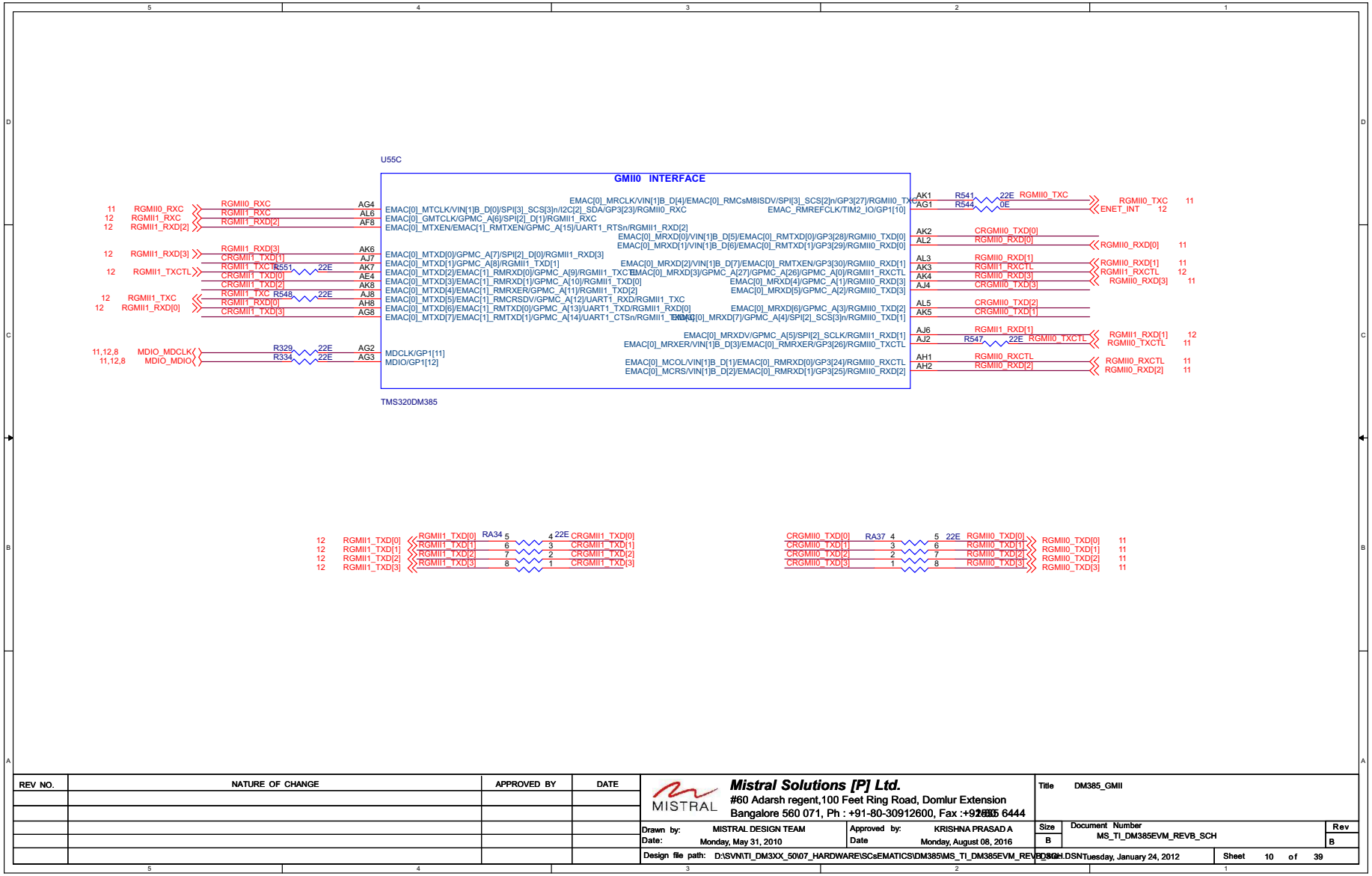


Figure A-10. Ethernet Controller 0

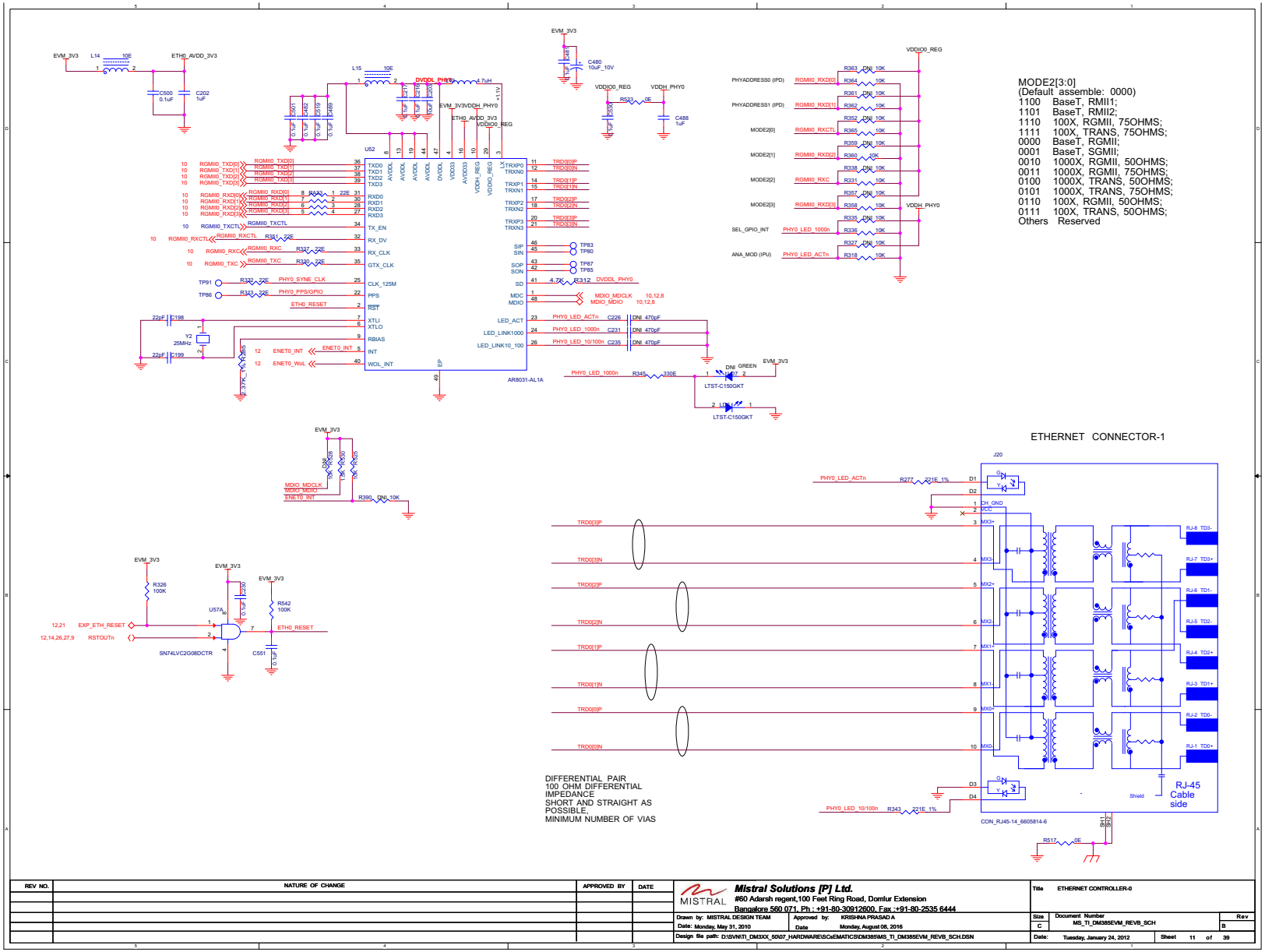


Figure A-11. Ethernet Controller 1

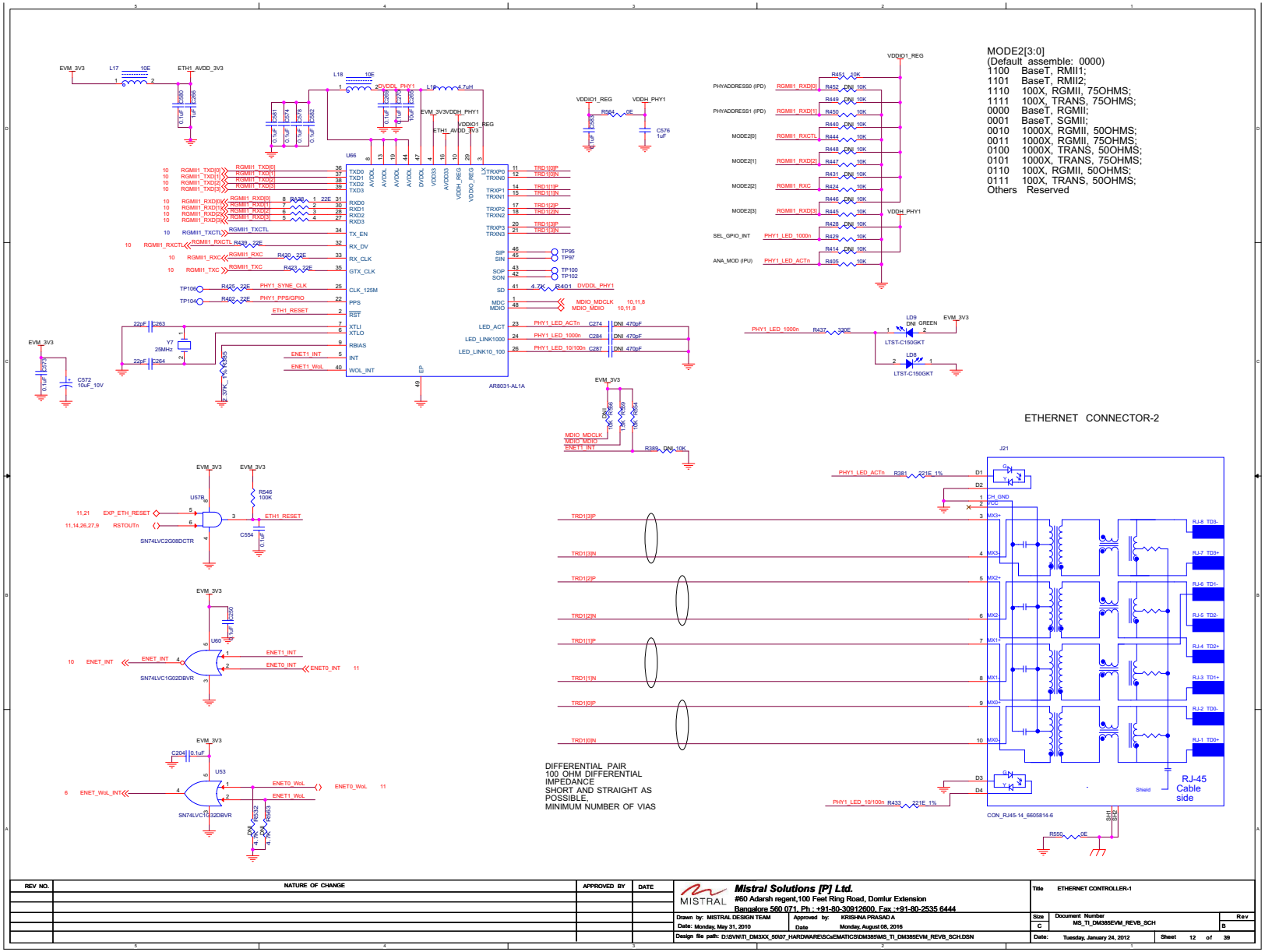
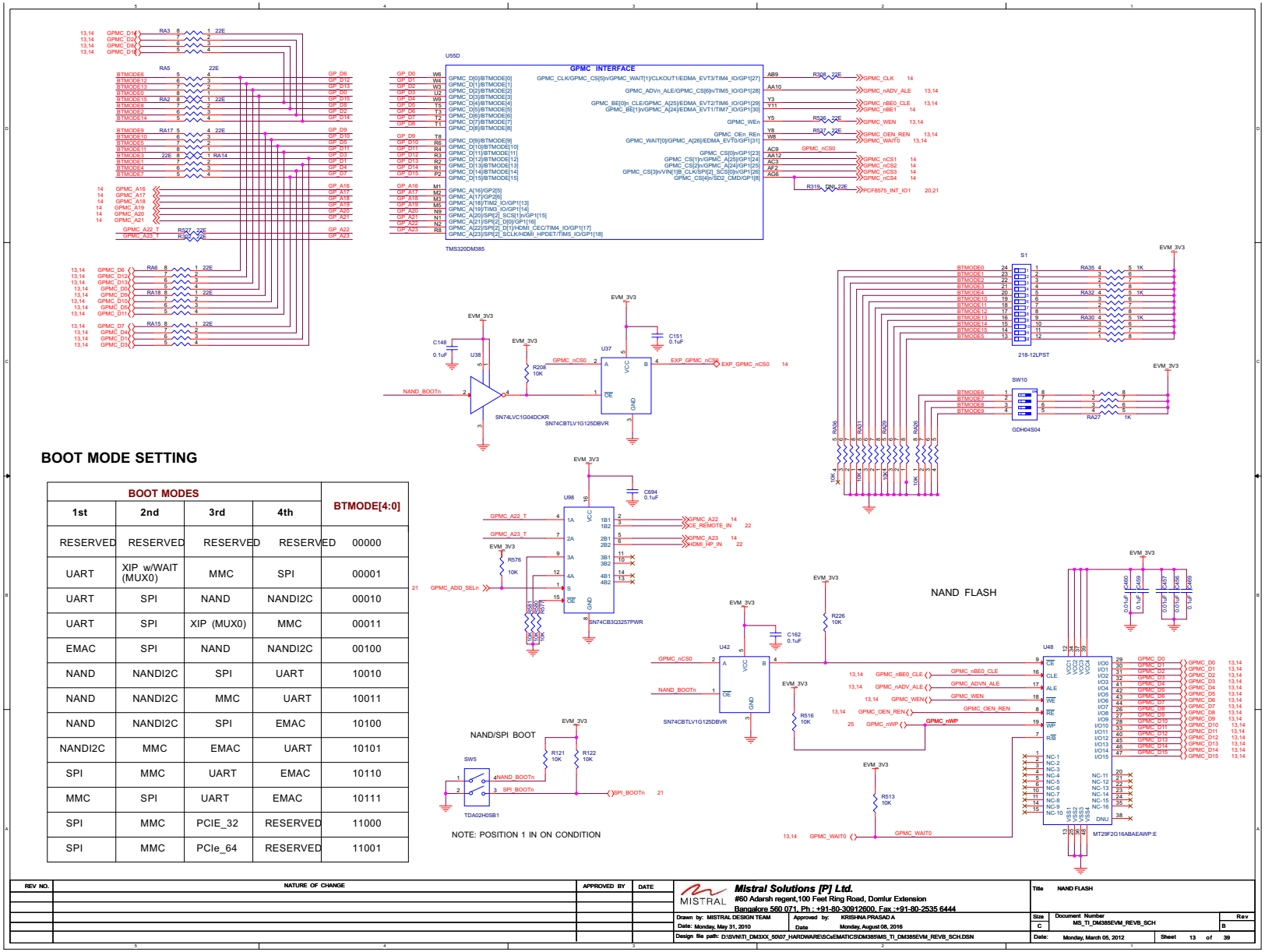


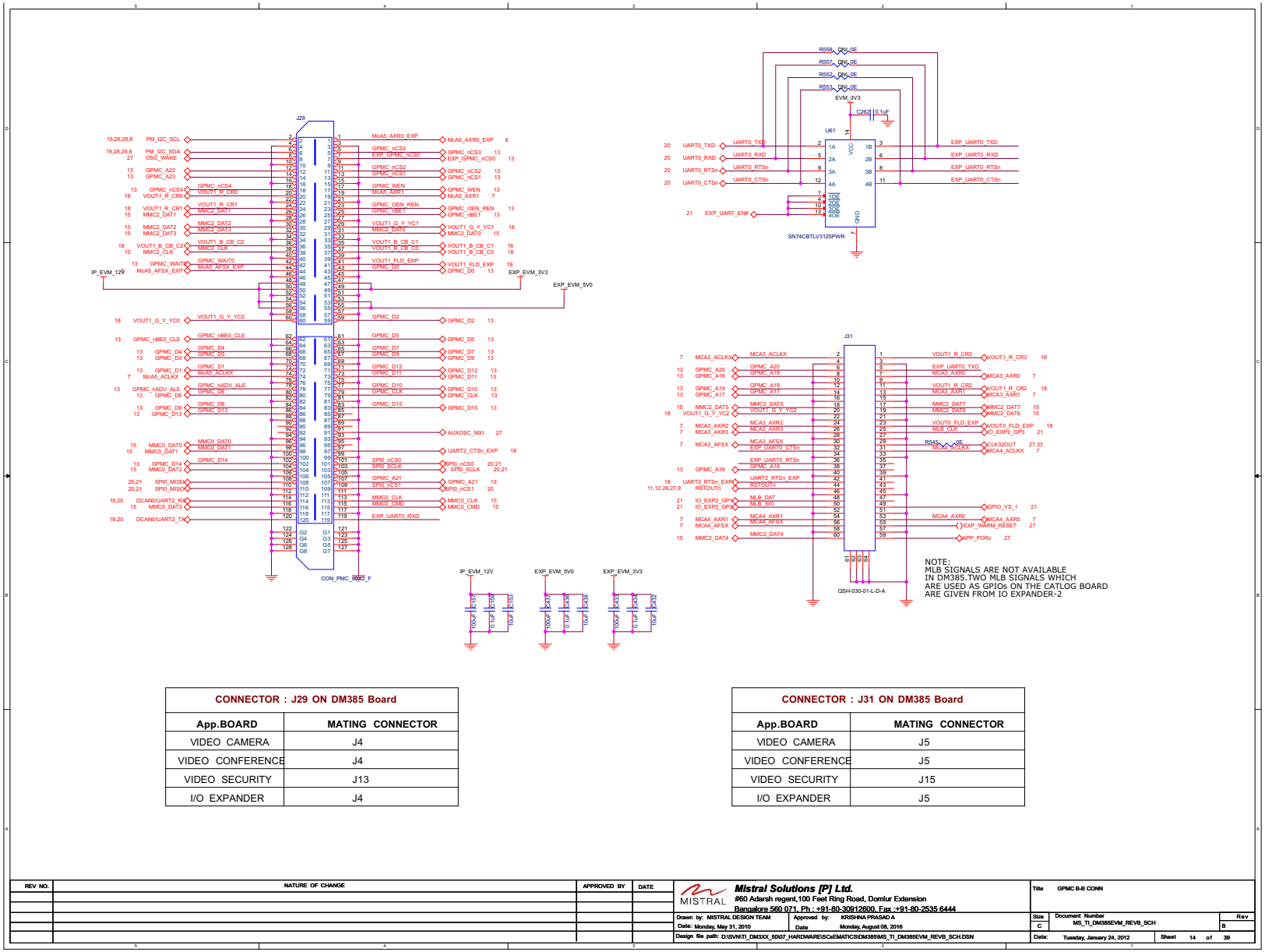
Figure A-12. NAND Flash



BOOT MODE SETTING

BOOT MODES				BTMODE[4:0]
1st	2nd	3rd	4th	
RESERVED	RESERVED	RESERVED	RESERVED	00000
UART	XIP w/WAIT (MUX0)	MMC	SPI	00001
UART	SPI	NAND	NANDI2C	00010
UART	SPI	XIP (MUX0)	MMC	00011
EMAC	SPI	NAND	NANDI2C	00100
NAND	NANDI2C	SPI	UART	10010
NAND	NANDI2C	MMC	UART	10011
NAND	NANDI2C	SPI	EMAC	10100
NANDI2C	MMC	EMAC	UART	10101
SPI	MMC	UART	EMAC	10110
MMC	SPI	UART	EMAC	10111
SPI	MMC	PCIE_32	RESERVED	11000
SPI	MMC	PCIe_64	RESERVED	11001

Figure A-13. GPMC B-B Connector



CONNECTOR : J29 ON DM385 Board	
App.BOARD	**MATING CONNECTOR**
VIDEO CAMERA	J4
VIDEO CONFERENCE	J4
VIDEO SECURITY	J13
I/O EXPANDER	J4

CONNECTOR : J31 ON DM385 Board	
App.BOARD	**MATING CONNECTOR**
VIDEO CAMERA	J5
VIDEO CONFERENCE	J5
VIDEO SECURITY	J15
I/O EXPANDER	J5

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Figure A-14. DM385 MMC0, MMC1, and MMC2

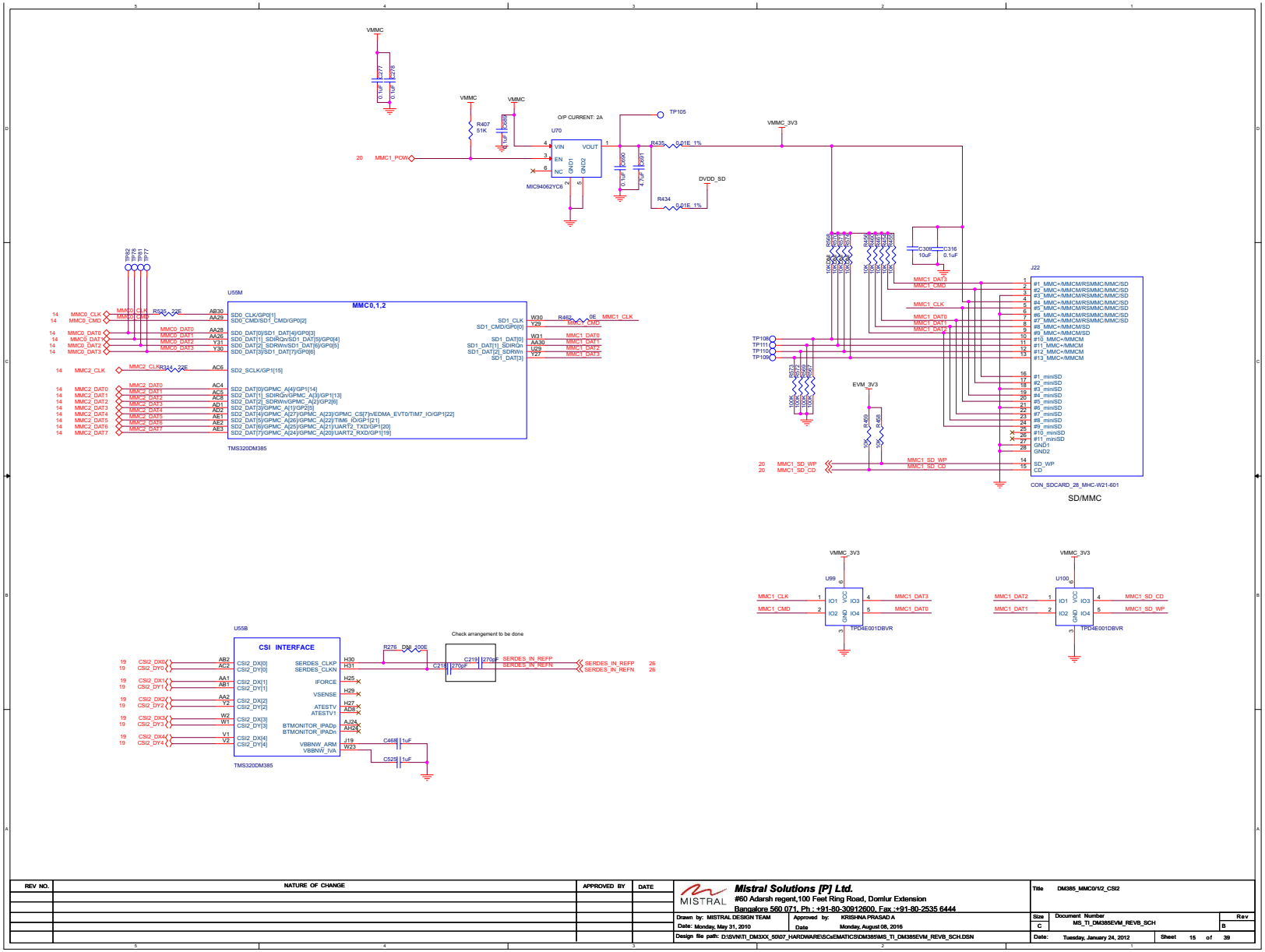


Figure A-15. DM385 DDR0 Terminations

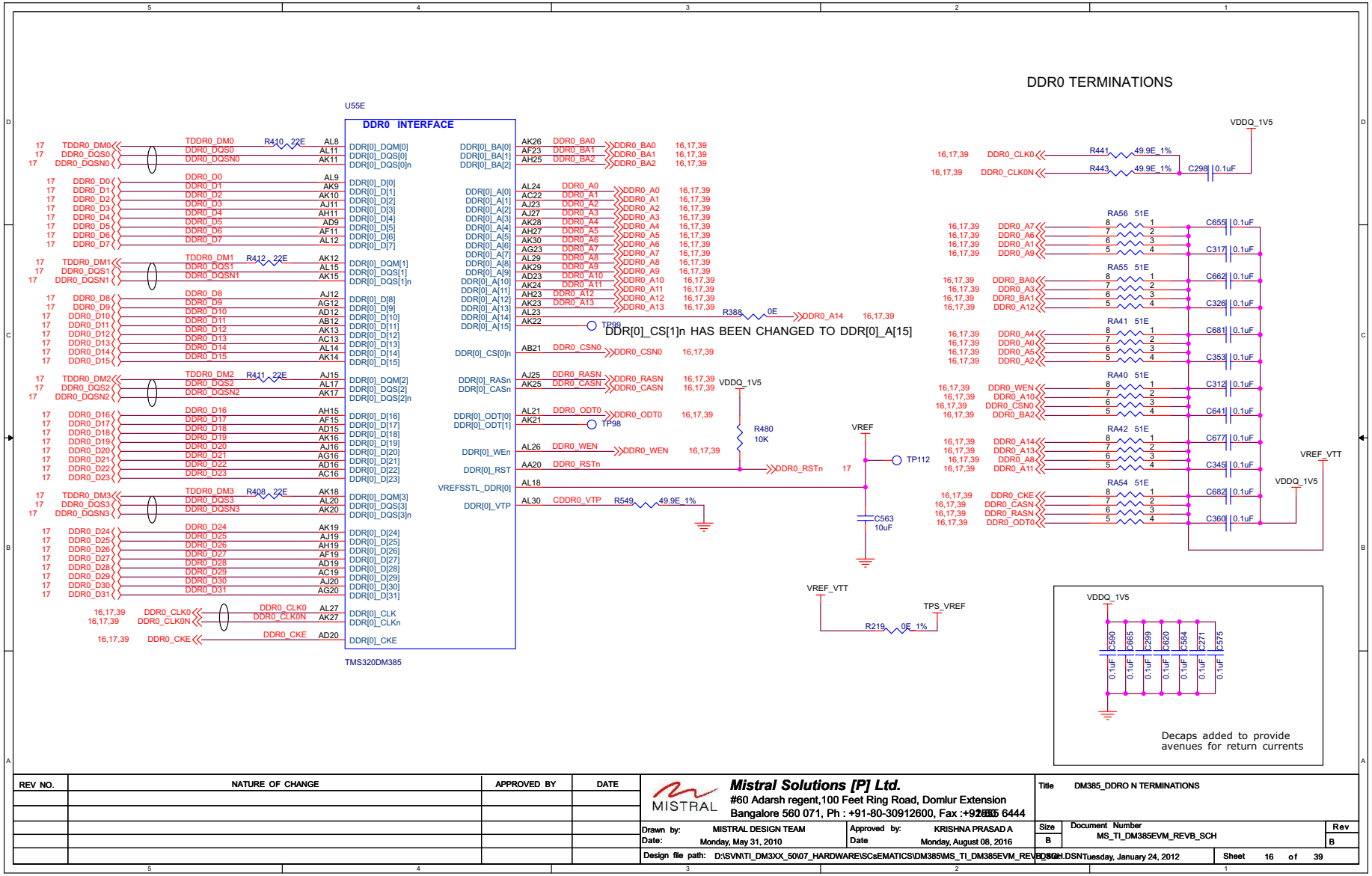


Figure A-16. DDR0-0, DDR0-1, DDR0-2, and DDR0-3

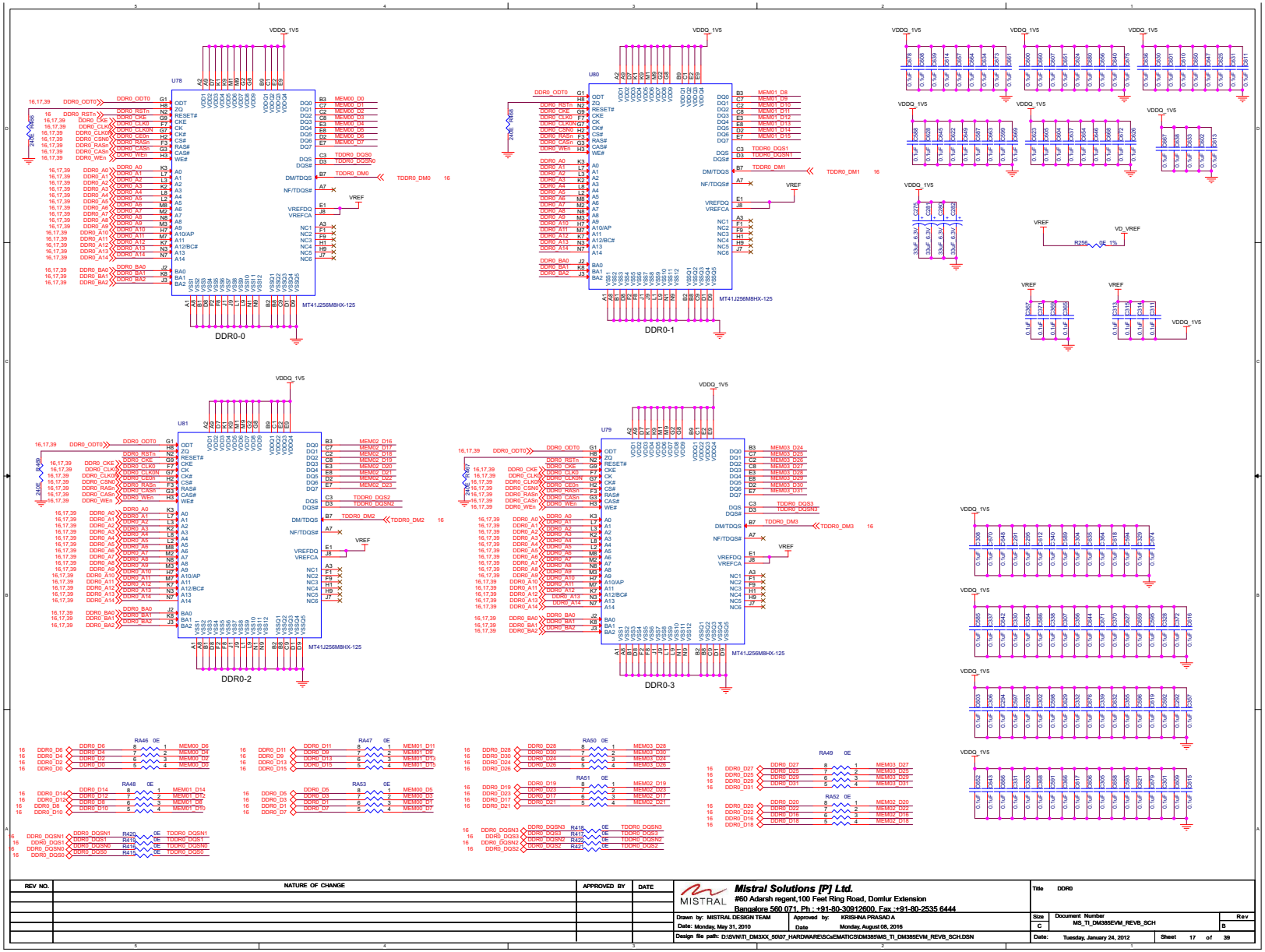
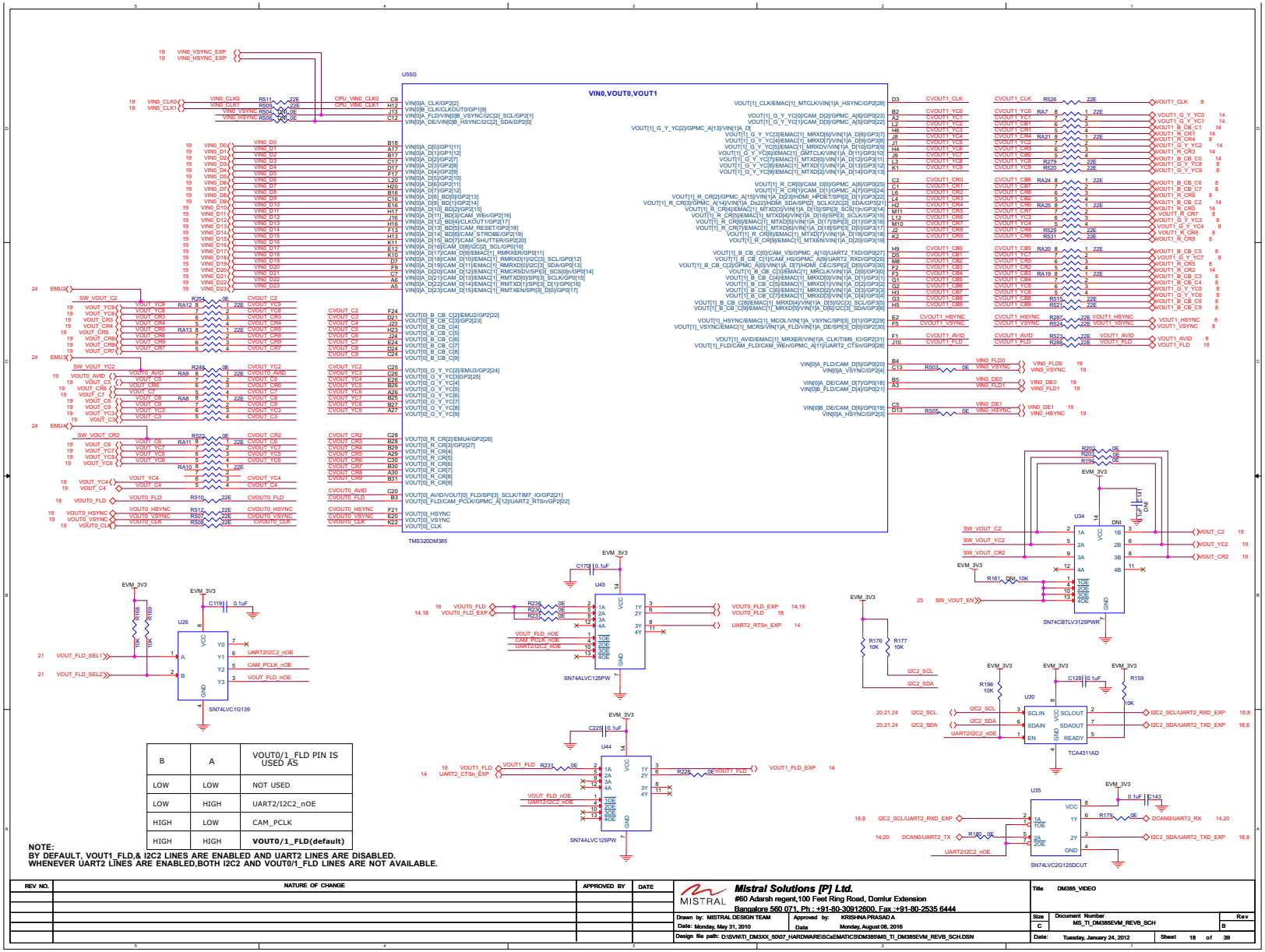
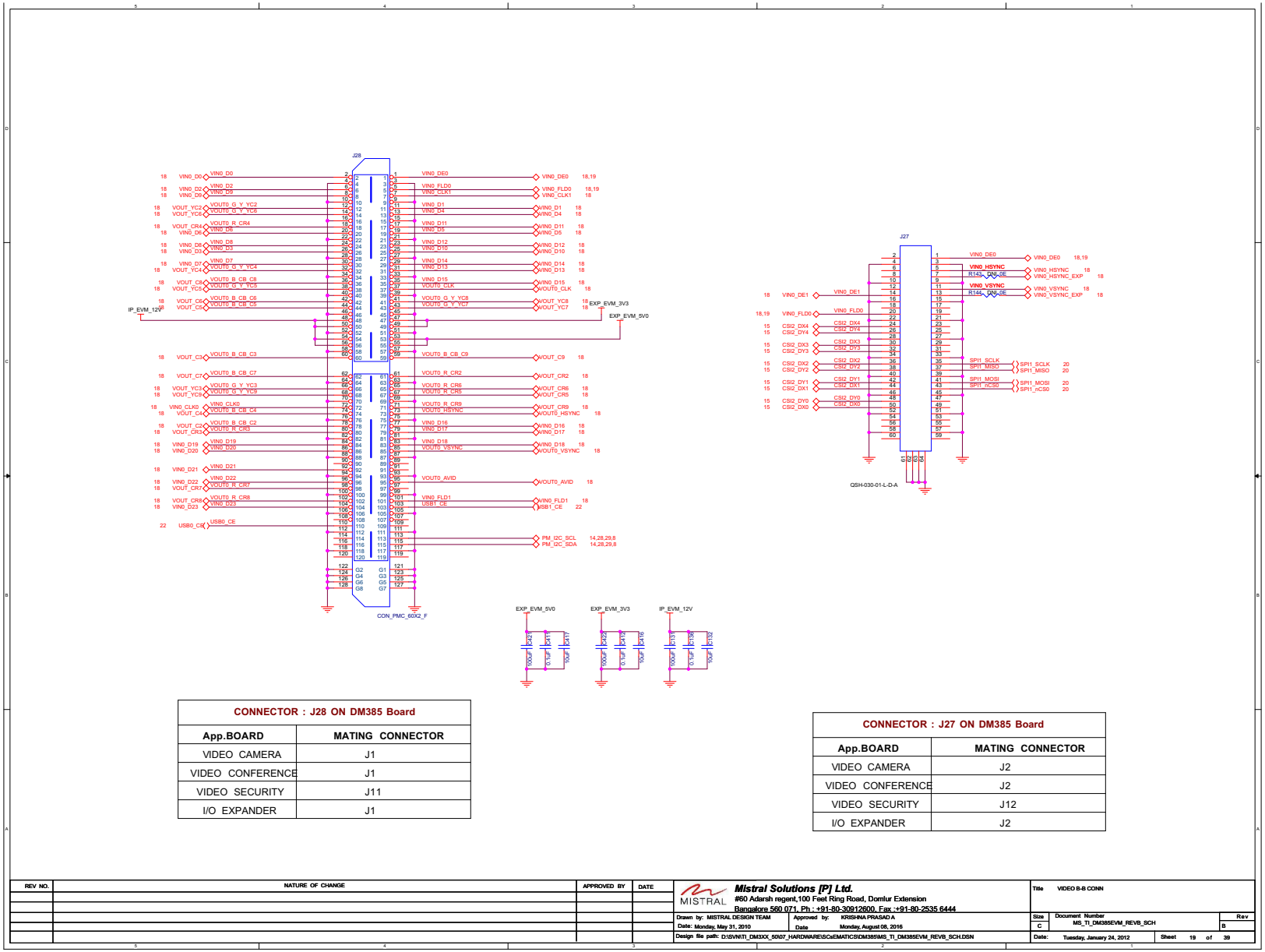


Figure A-17. DM385 VIN0, VOUT0, and VOUT1



B	A	VOUT0/1_FLD PIN IS USED AS
LOW	LOW	NOT USED
LOW	HIGH	UART2/I2C2_nOE
HIGH	LOW	CAM_PCLK
HIGH	HIGH	**VOUT0/1_FLD(default)**

Figure A-18. Video B-B Connector



CONNECTOR : J28 ON DM385 Board	
App.BOARD	MATING CONNECTOR
VIDEO CAMERA	J1
VIDEO CONFERENCE	J1
VIDEO SECURITY	J11
I/O EXPANDER	J1

CONNECTOR : J27 ON DM385 Board	
App.BOARD	MATING CONNECTOR
VIDEO CAMERA	J2
VIDEO CONFERENCE	J2
VIDEO SECURITY	J12
I/O EXPANDER	J2

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Figure A-19. DM385 Serial Interfaces

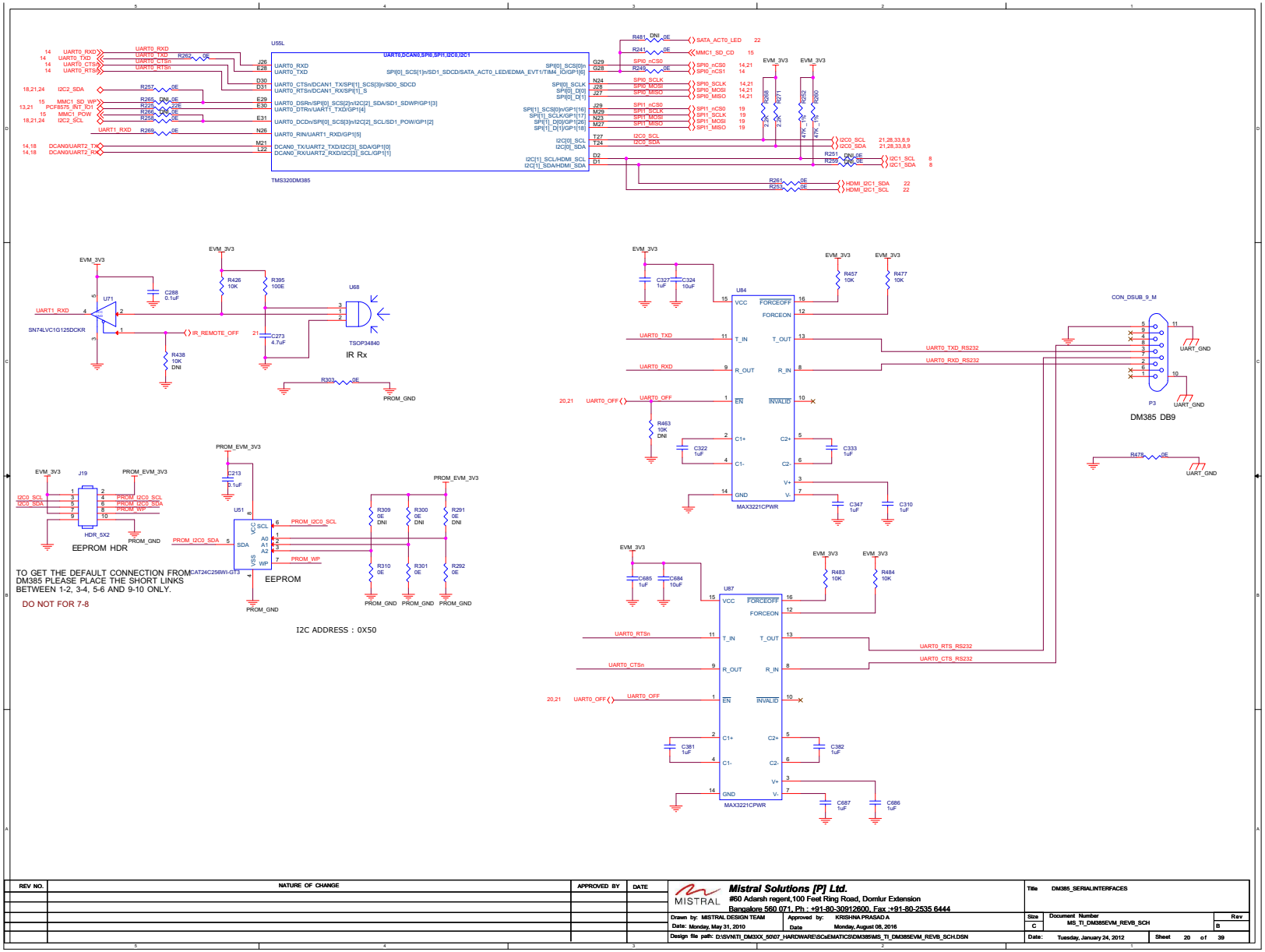

Figure A-20. SPI Flash

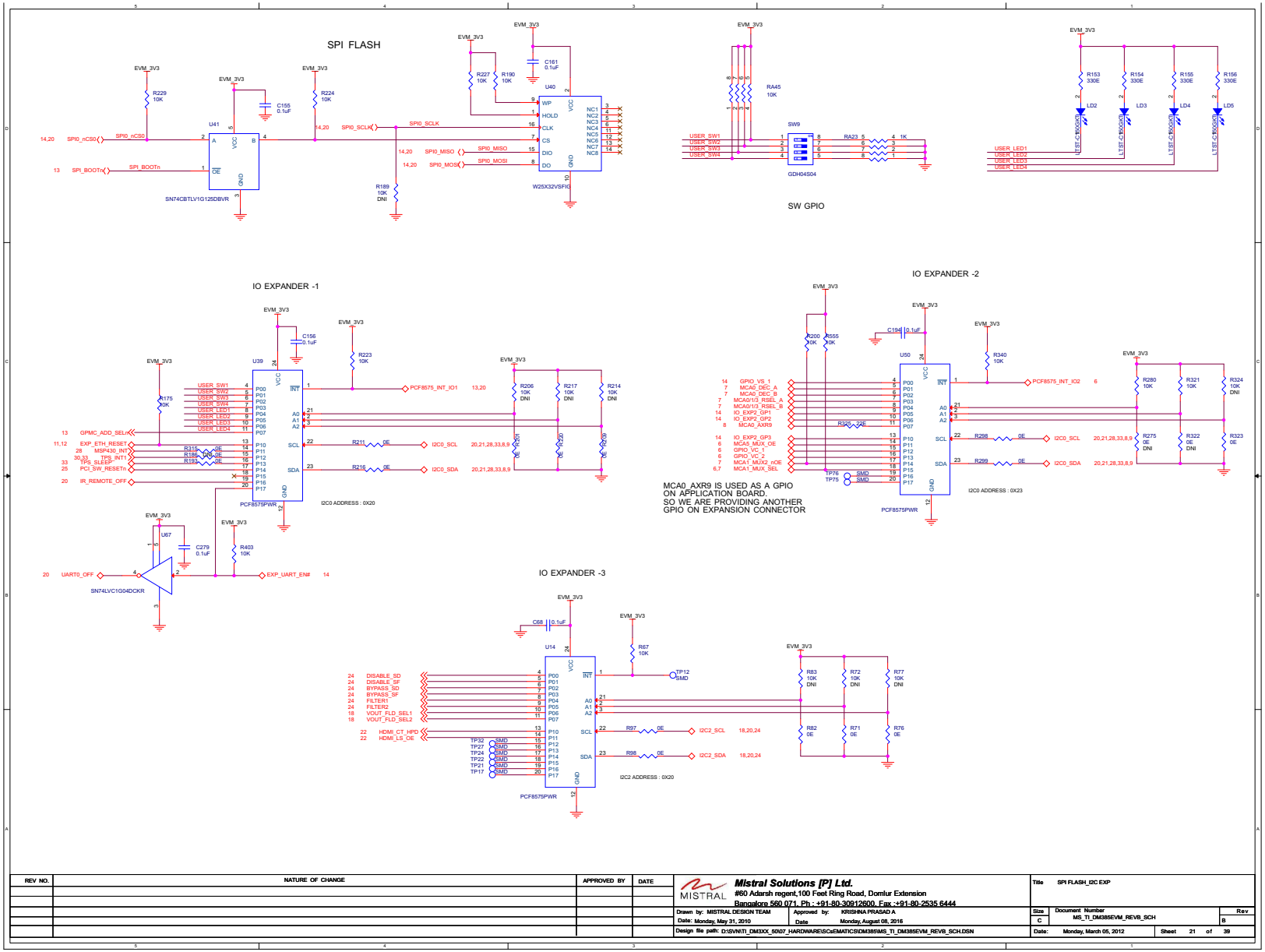

Figure A-21. DM385 HDMI, SATA, USB0, and USB1

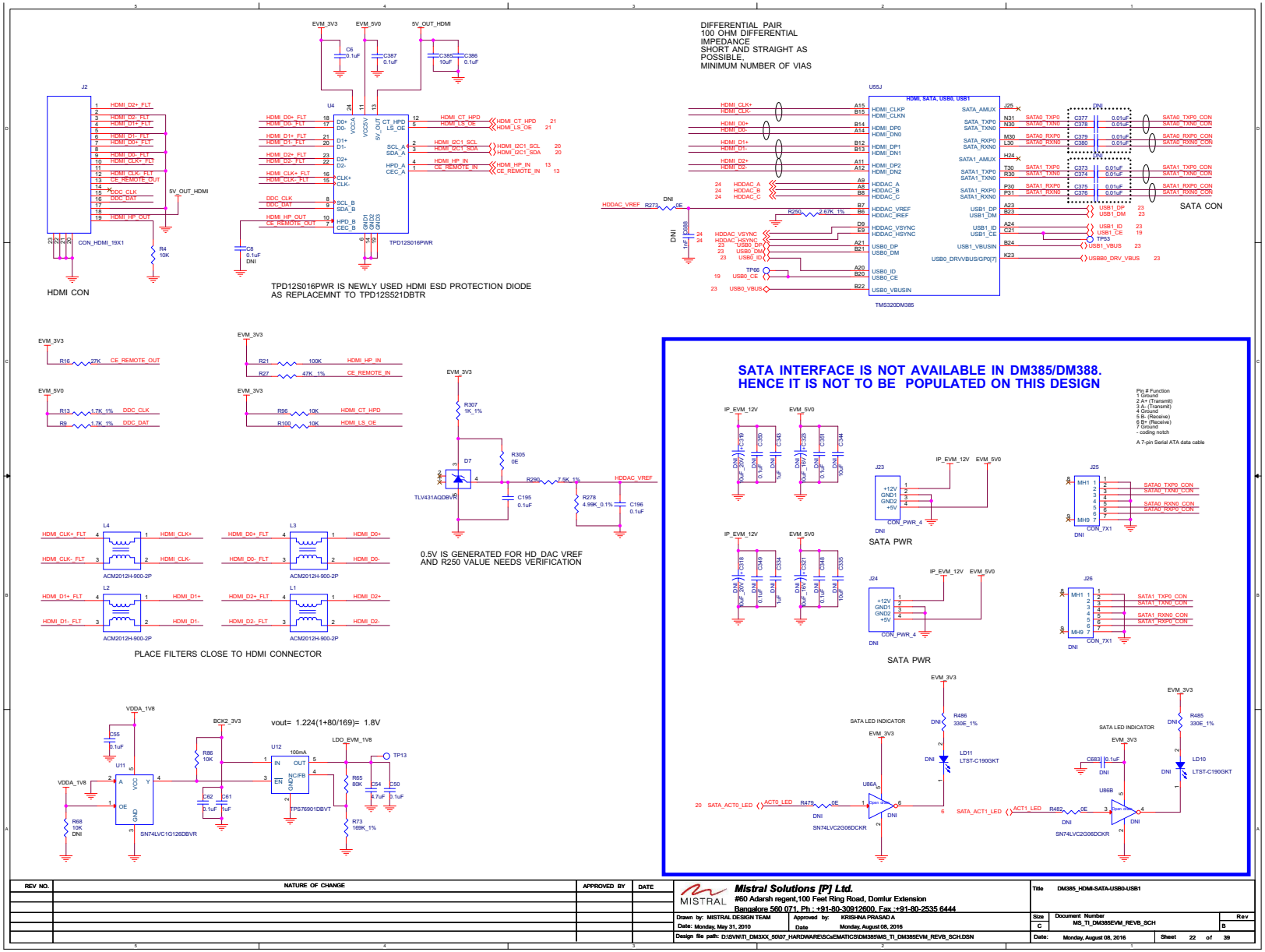

Figure A-22. USB Interface

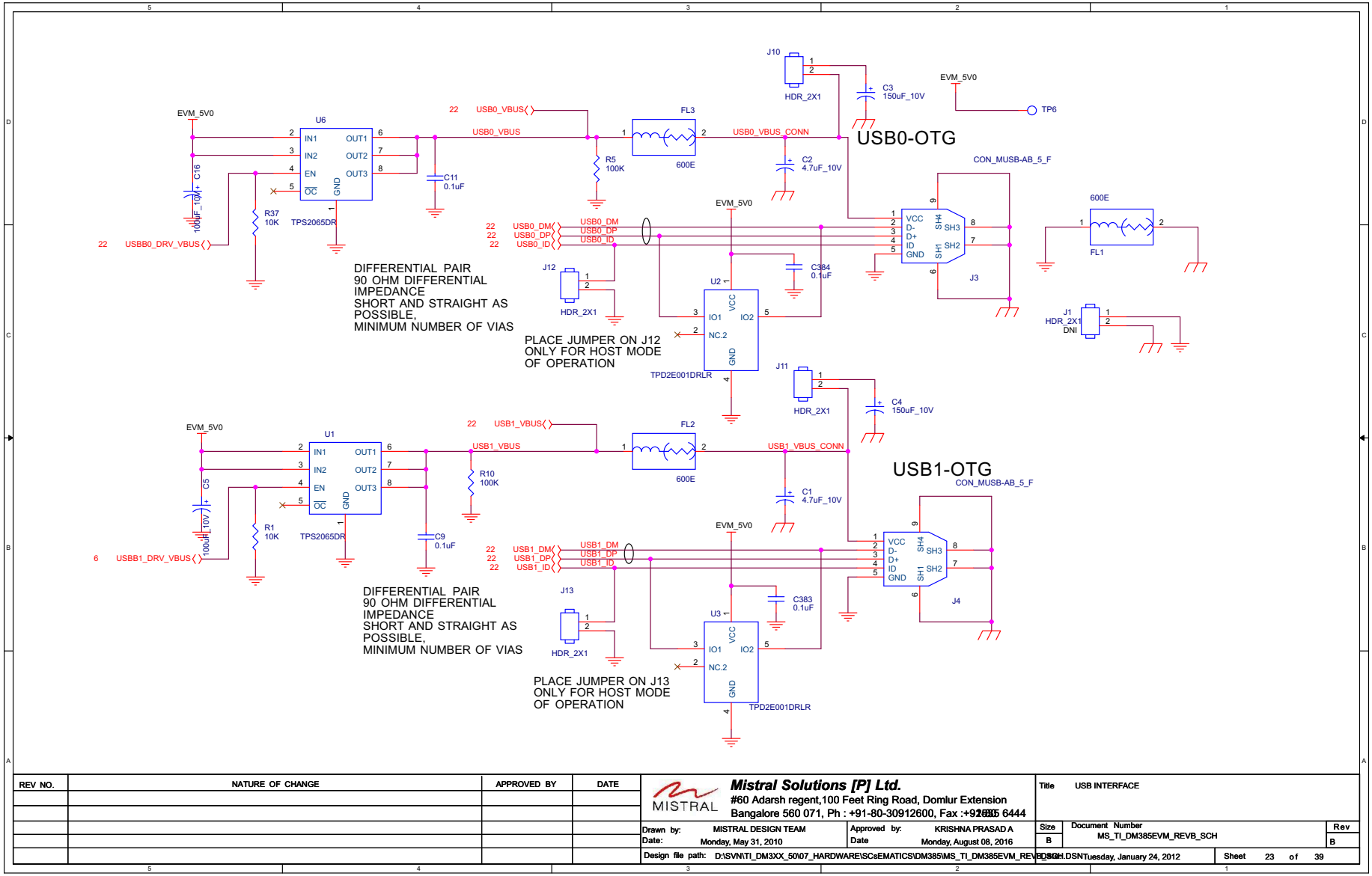

Figure A-23. DM385 PCIe, JTAG, and Video

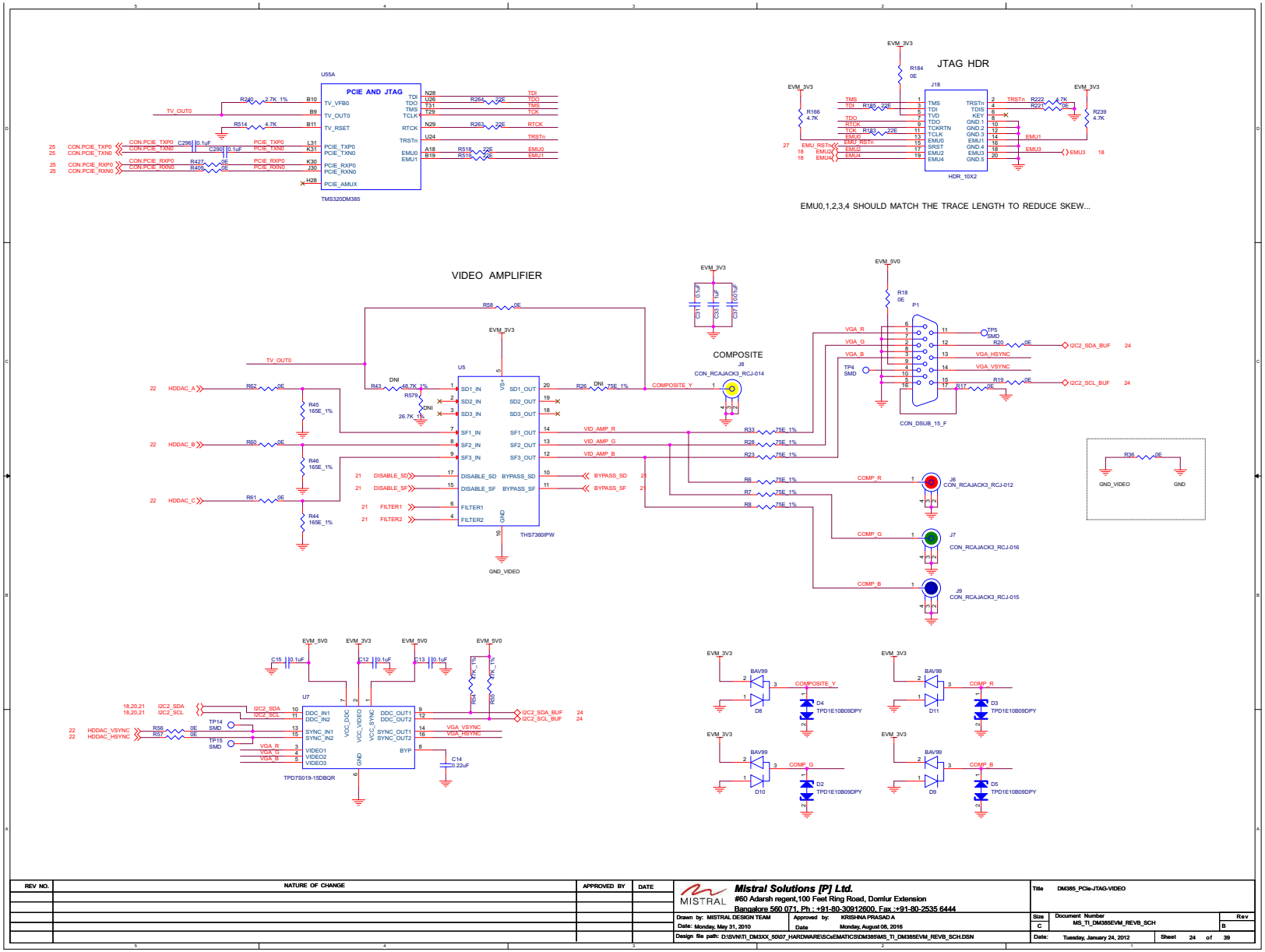

Figure A-24. PCIe Connector

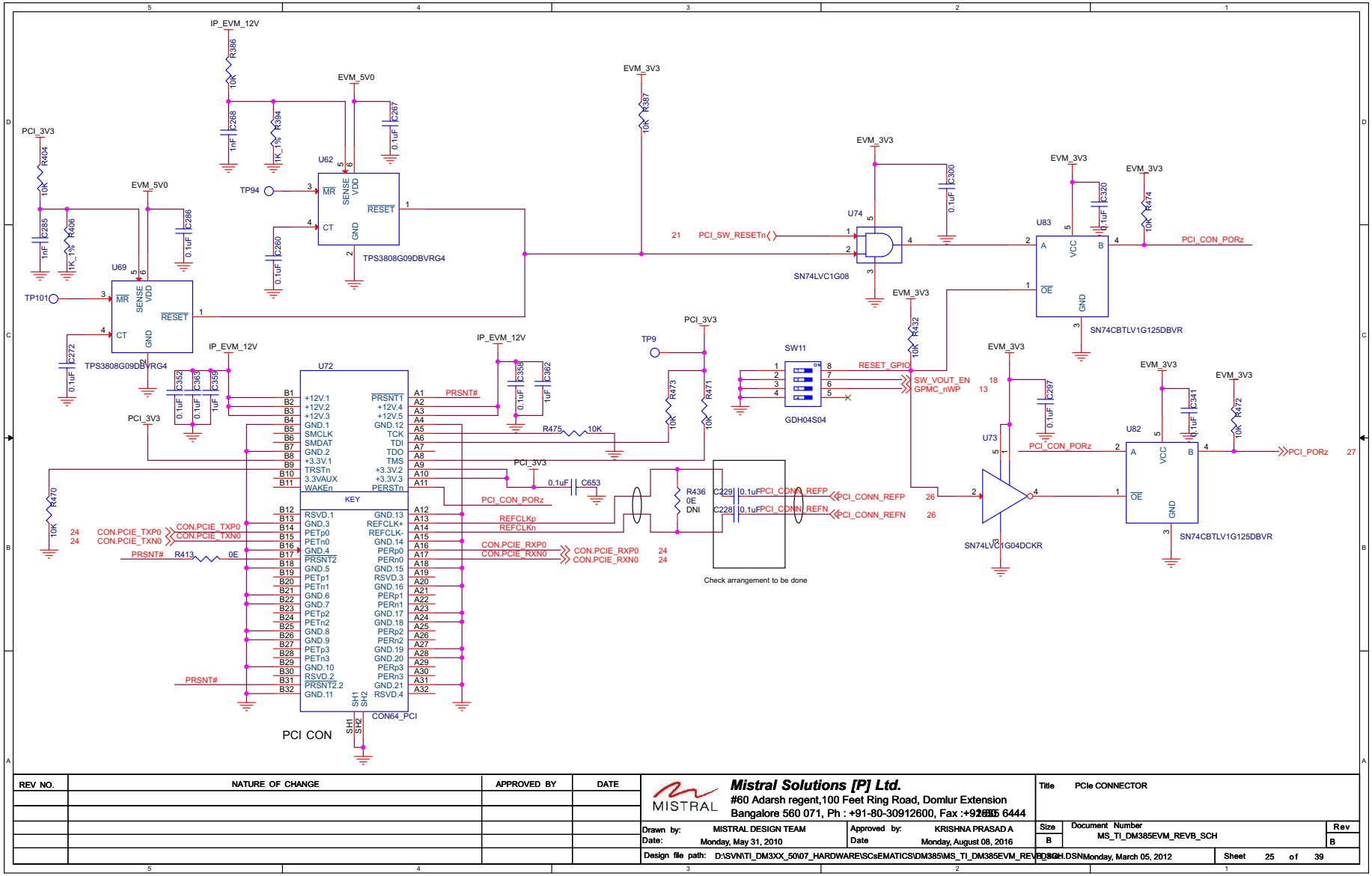

Figure A-25. SerDes Clocks

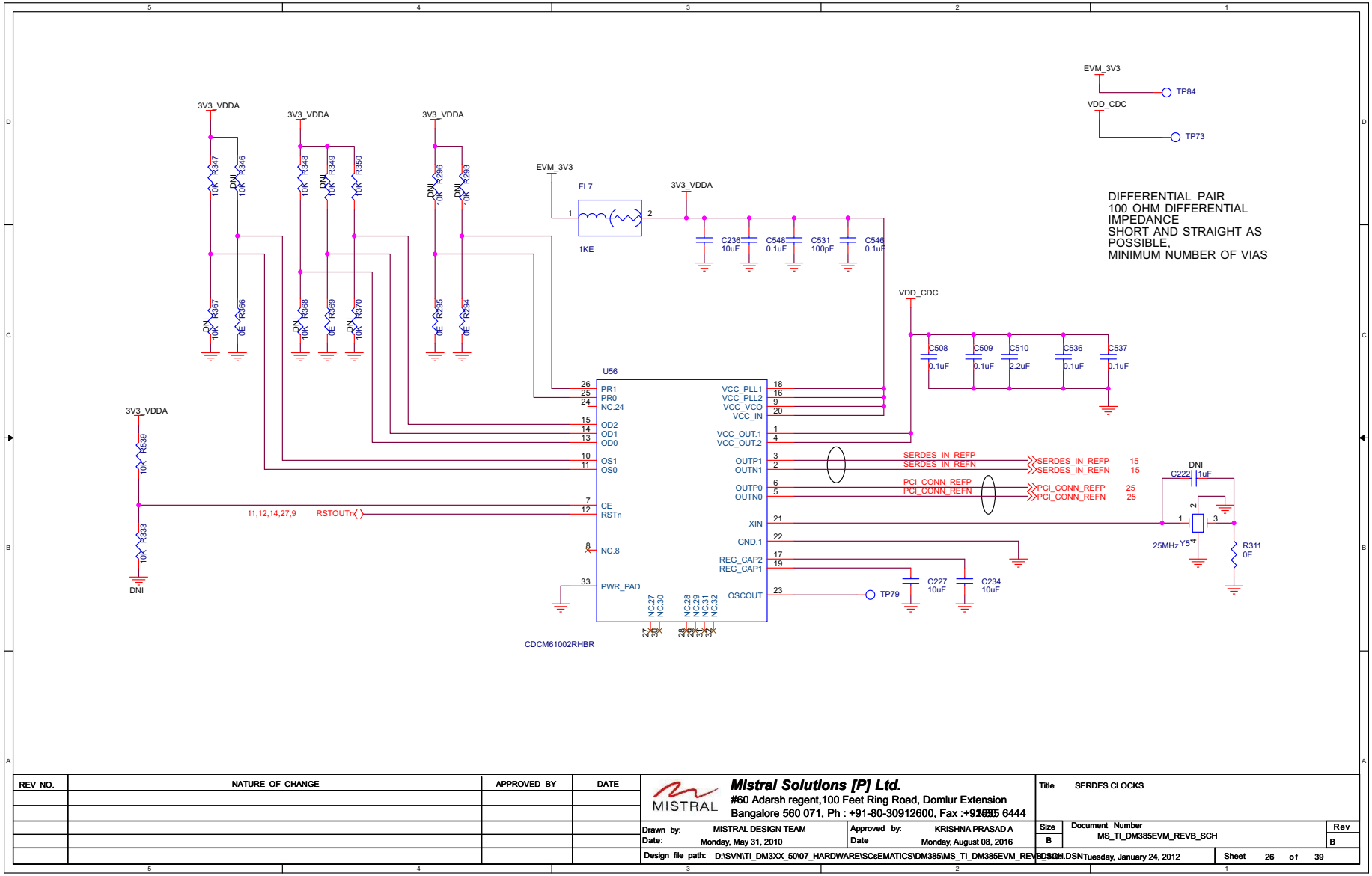

Figure A-26. DM385 Clocks

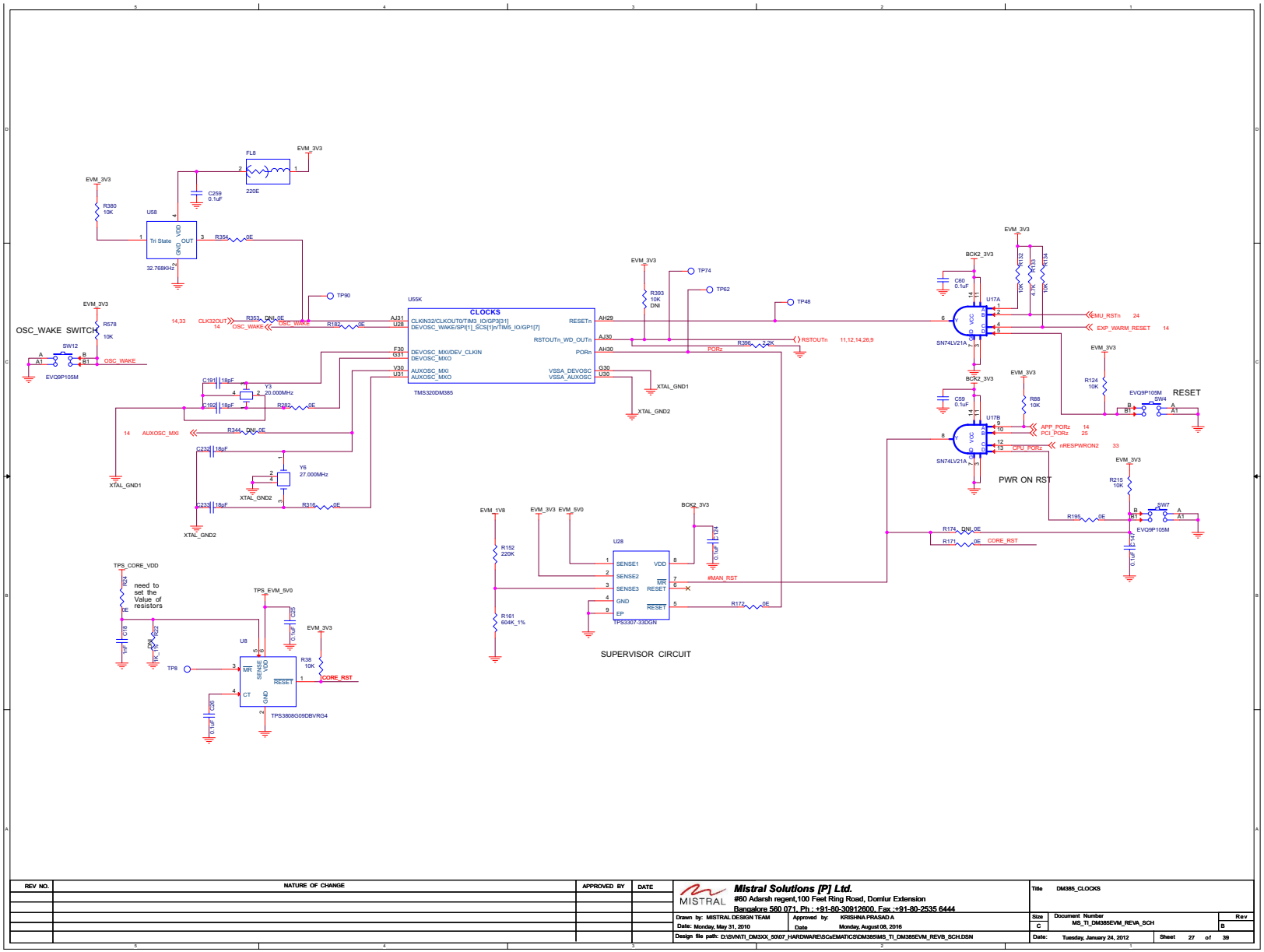

Figure A-27. Power Monitor CPU

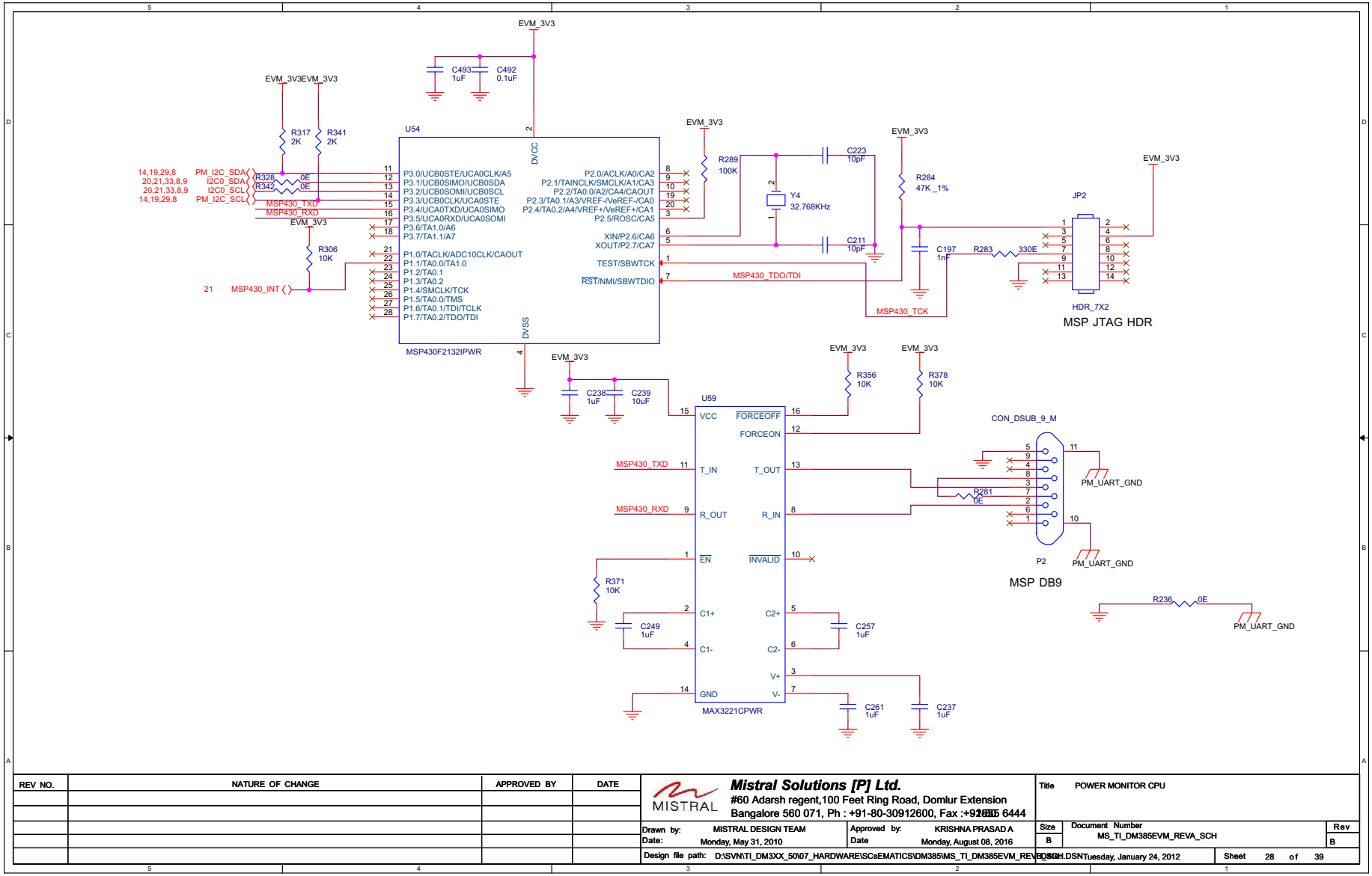

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Figure A-28. Power Monitors

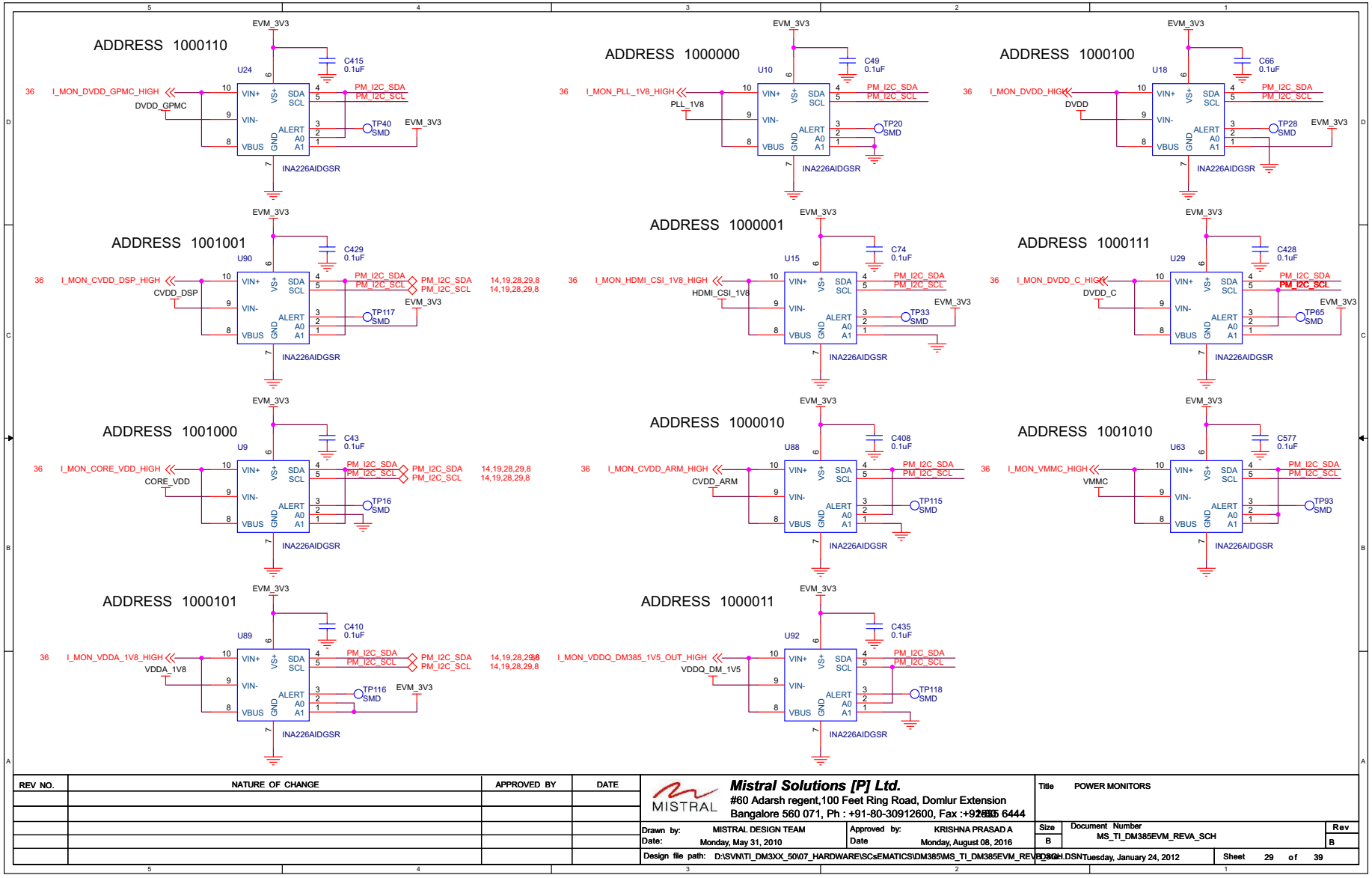

Figure A-29. DM385 Power

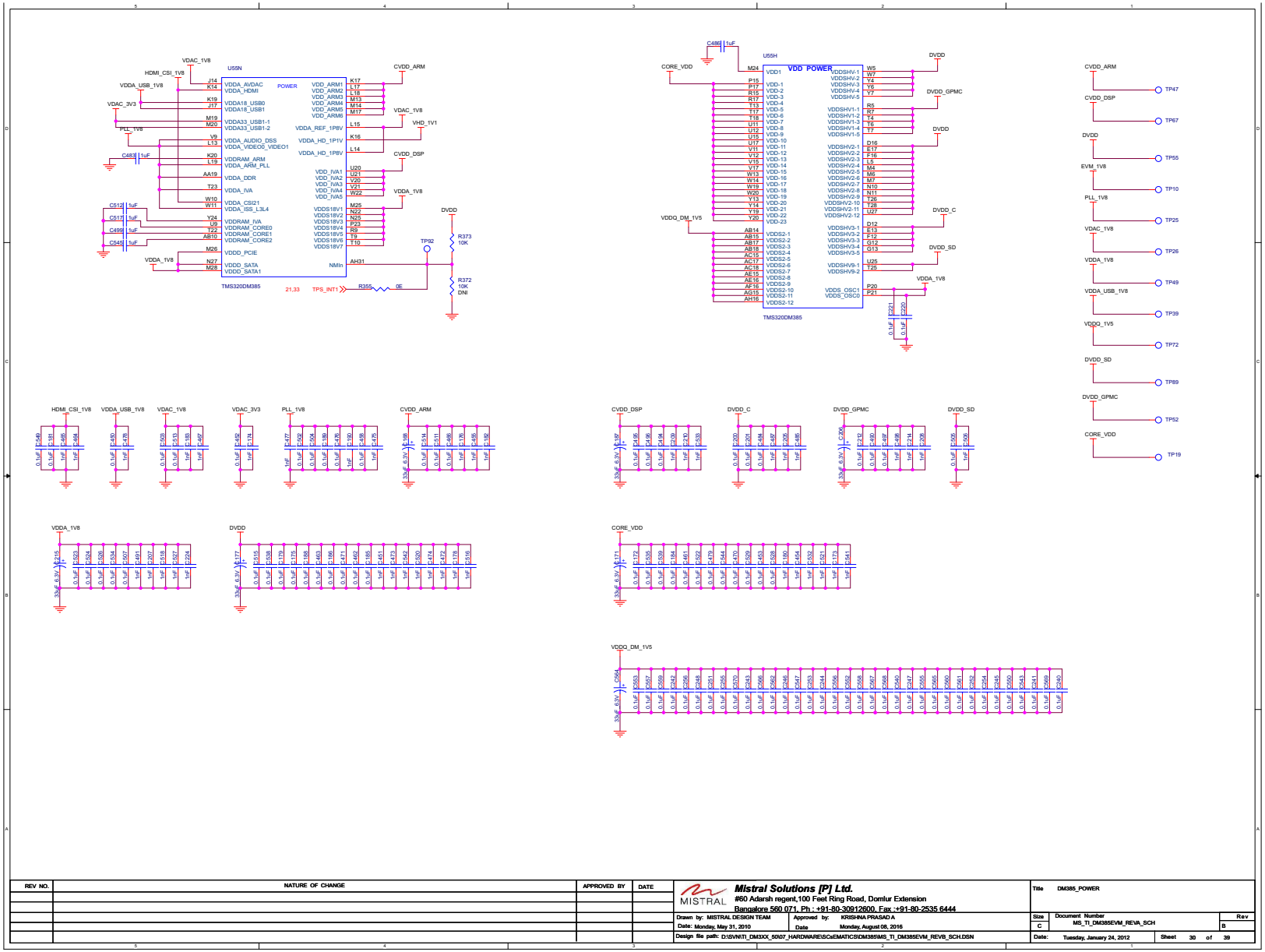

Figure A-30. DM385 VSS

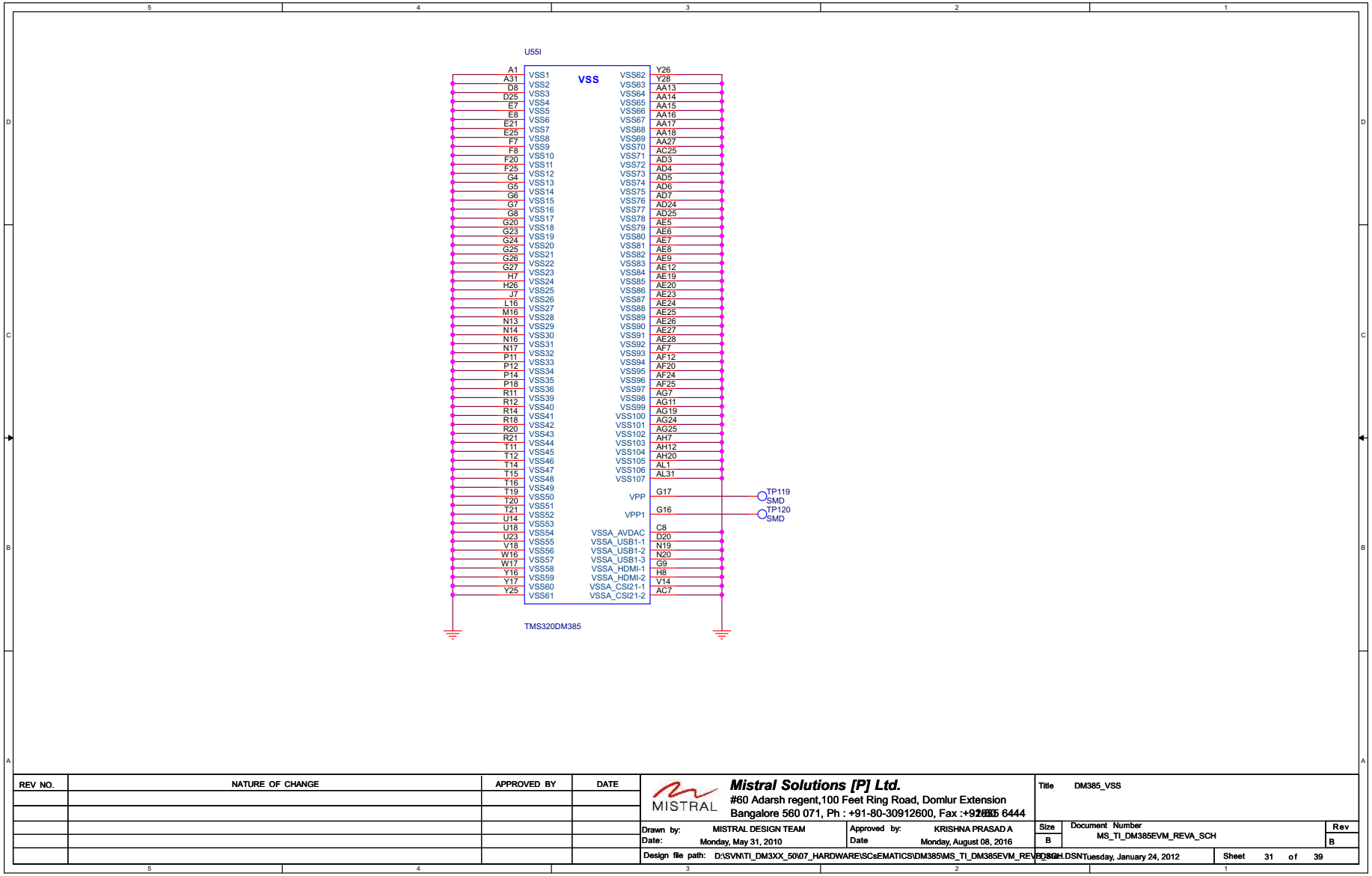

Figure A-31. TPS659113-A

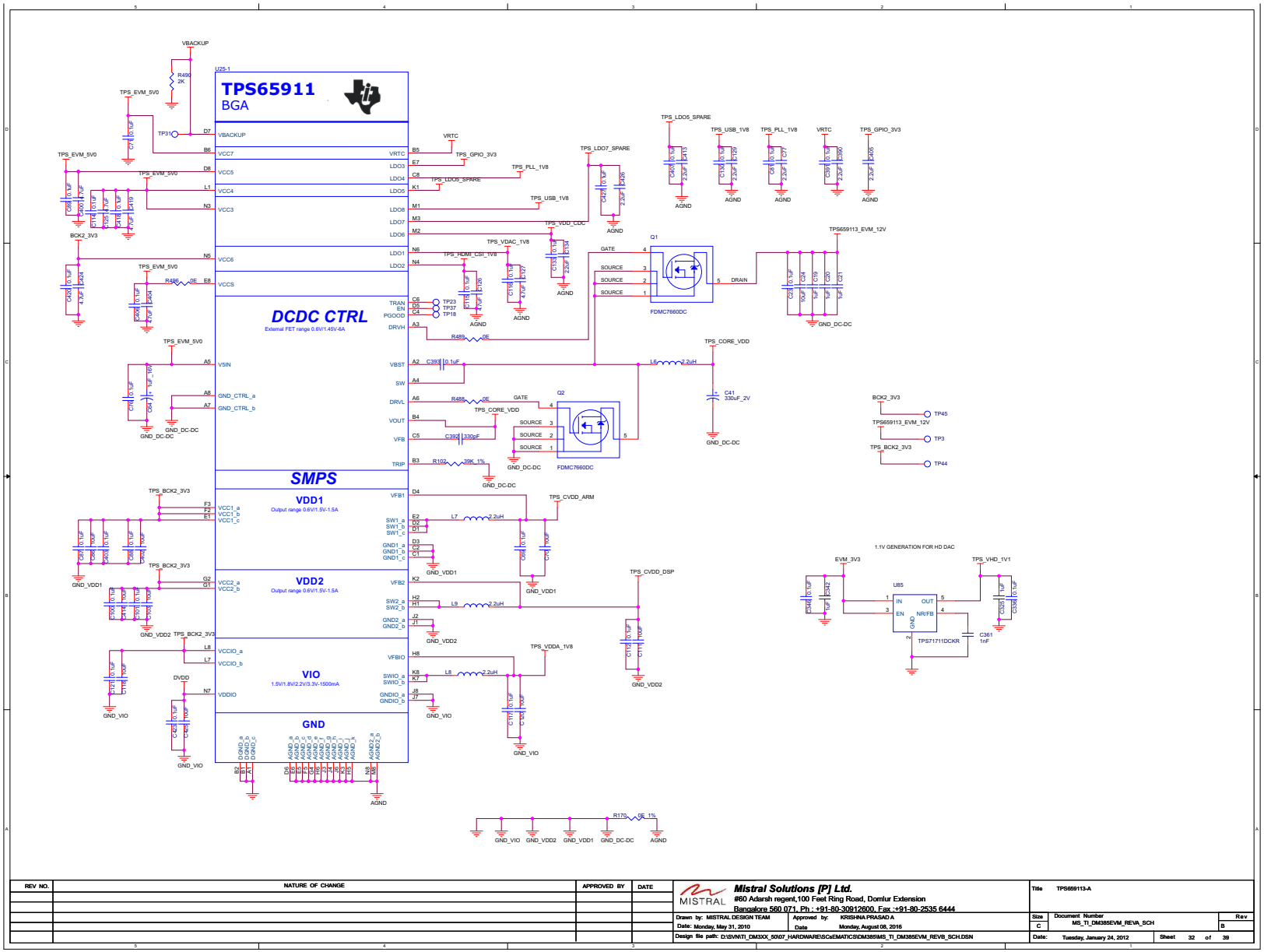

Figure A-32. TPS659113-B

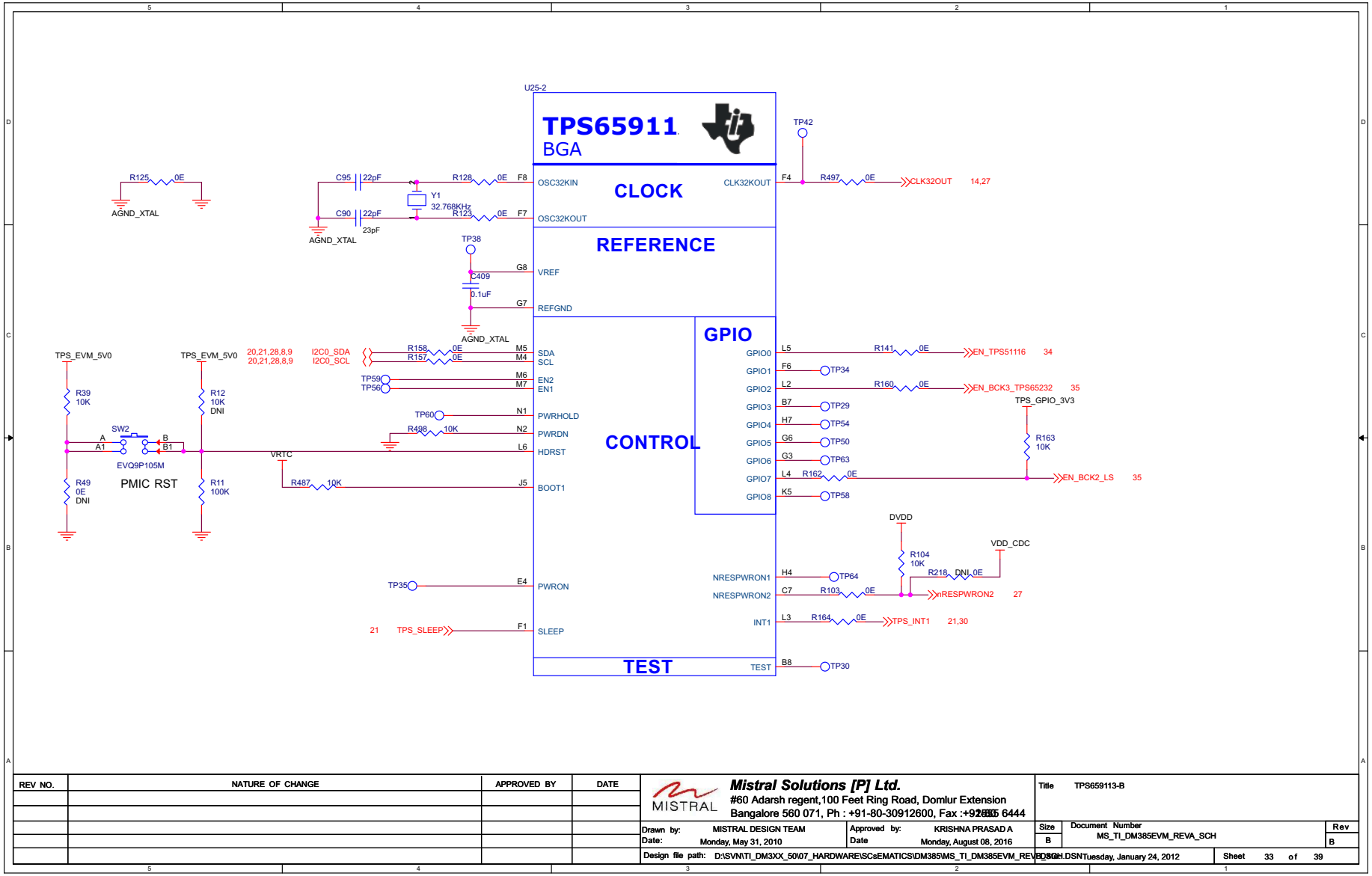

Figure A-33. TPS51116

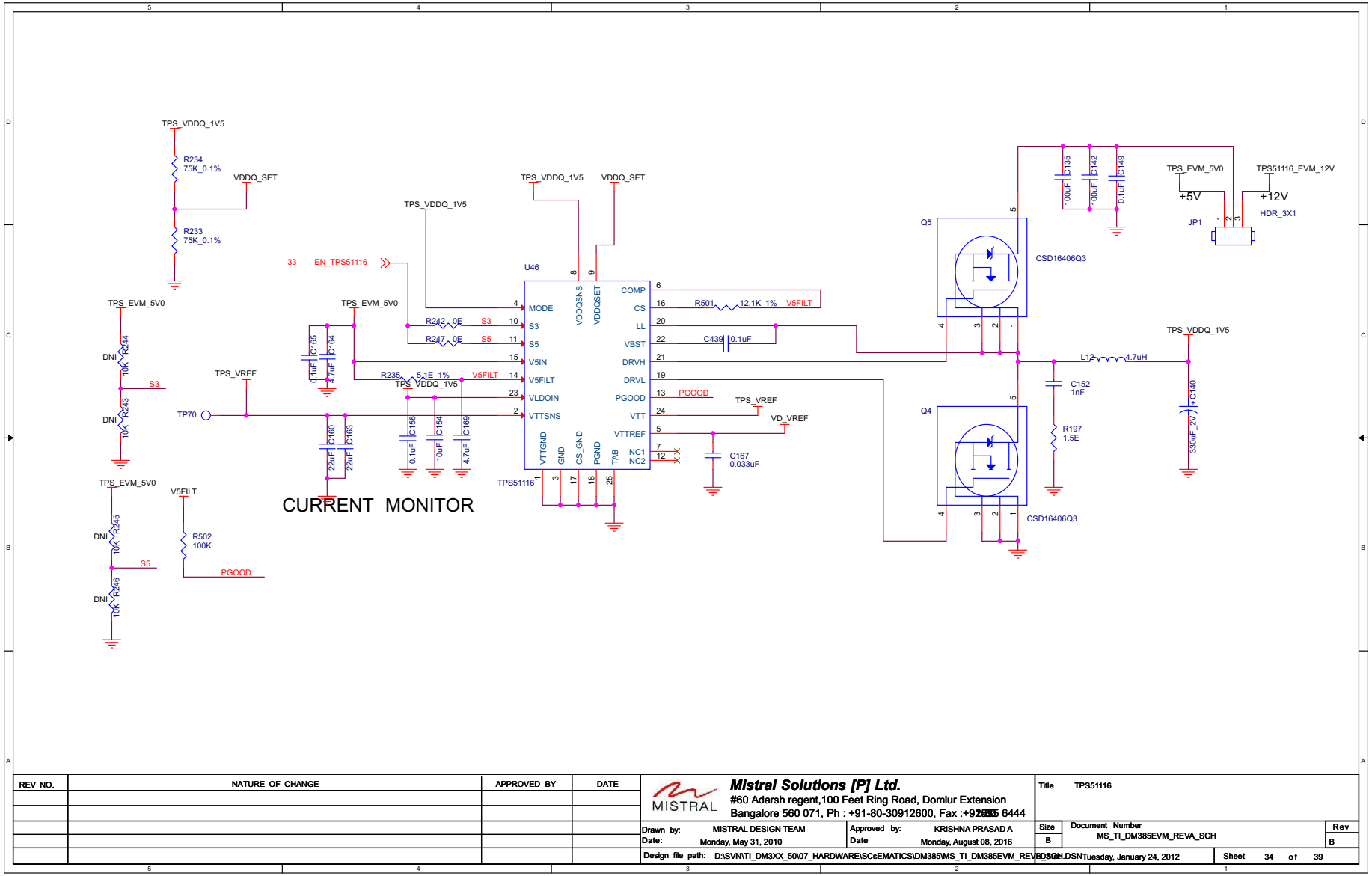

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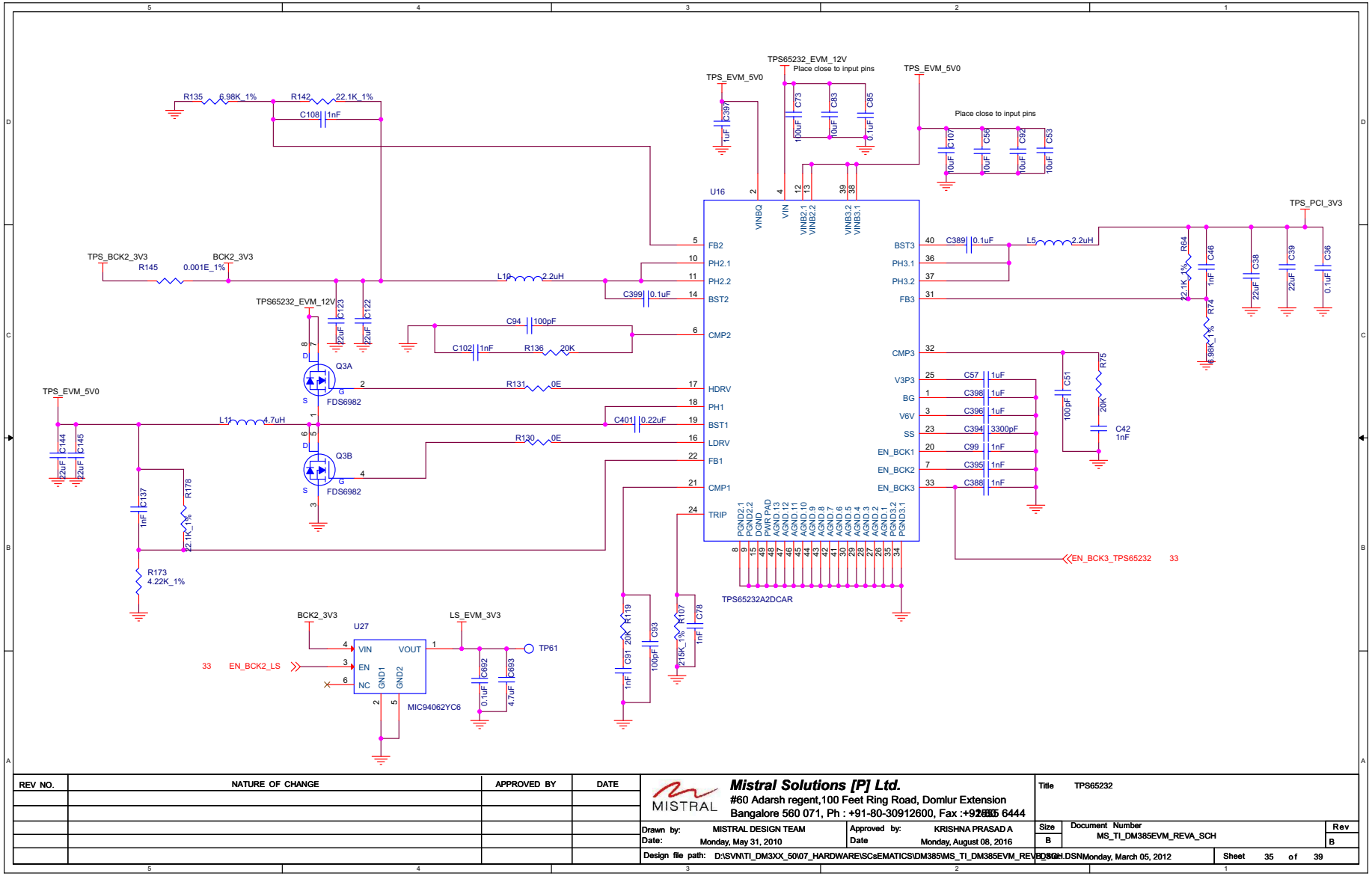
Figure A-34. TPS65232



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Design file path: D:\SVN\TI_DM3XX_50\07_HARDWARE\SCsEMATICS\DM385\MS_TI_DM385EVM_REVB_SCH.DSN
Monday, March 05, 2012
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Figure A-35. Power Selection

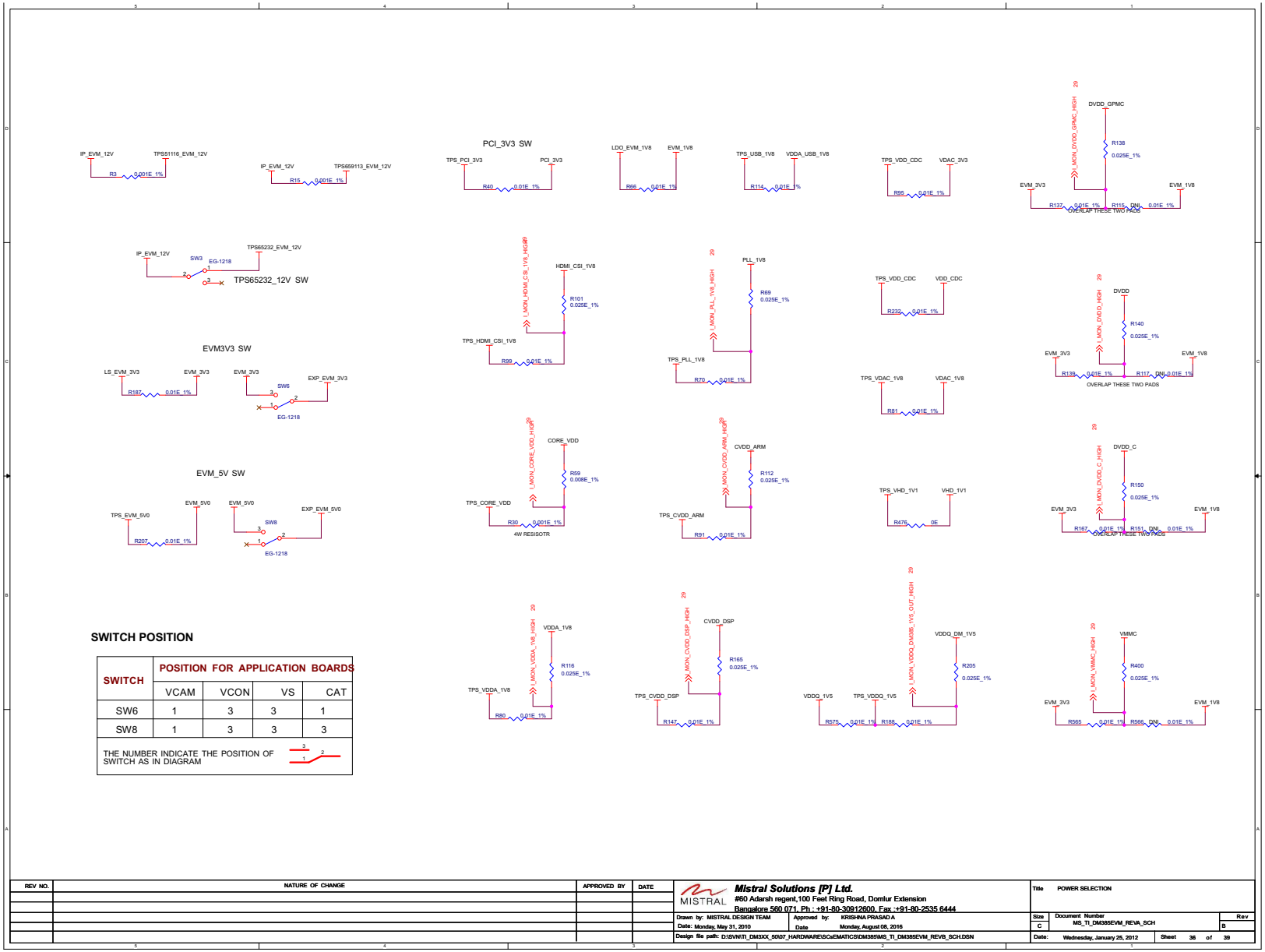

Figure A-36. Power In

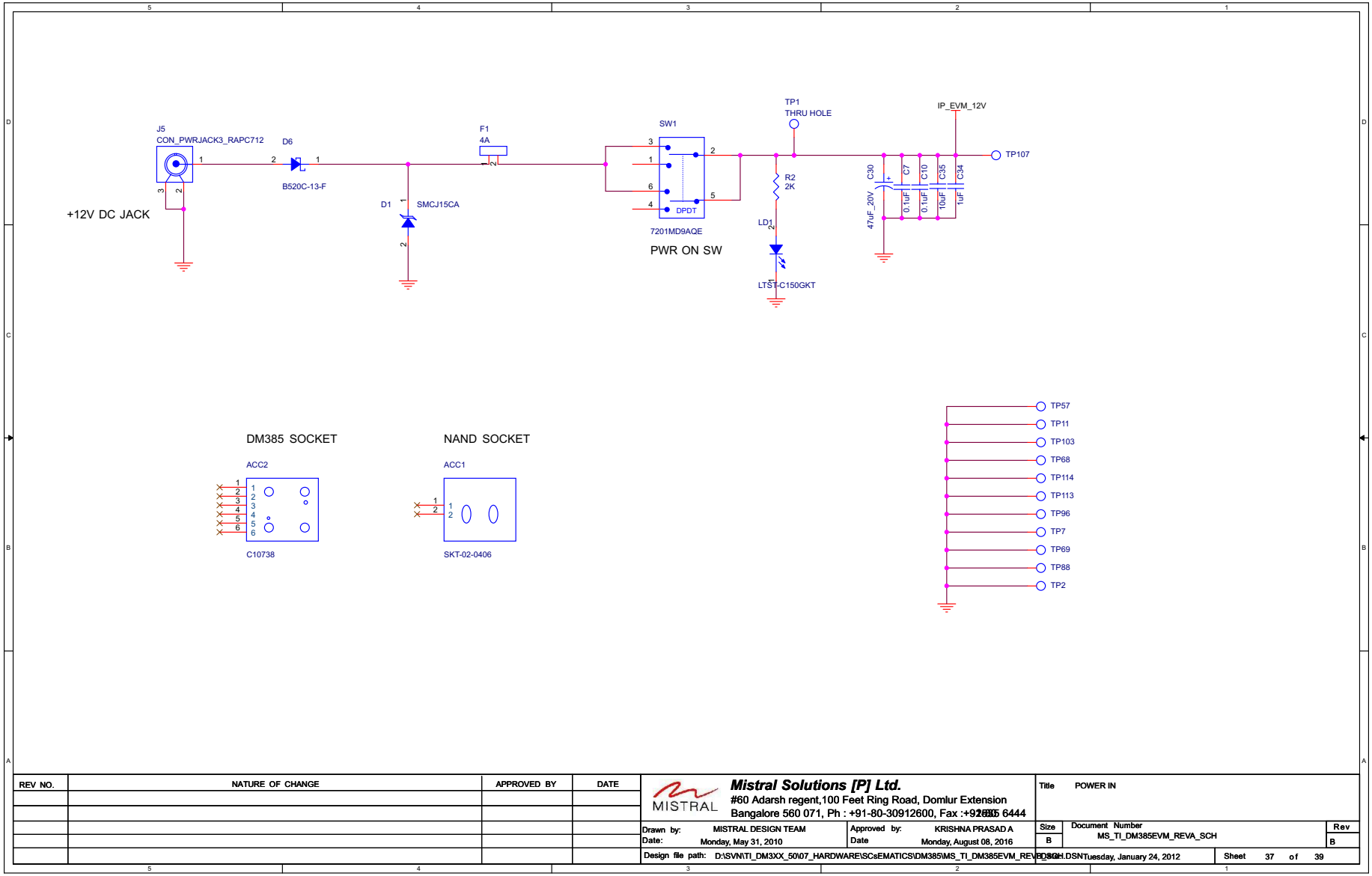

Figure A-37. Changes in Schematics

SL NO#	CHANGES IN THE SCHEMATICS COMPARED TO CENTAURUS.
1	MLB SIGNALS ARE REMOVED.
2	ONE MORE SATA (SATA1) CONNECTOR ADDED.
3	S-VIDEO SIGNALS REMOVED.
4	NEW DDR PART IS ADDED(ONLY FOR DDR0). DDR1 IS REMOVED.
5	COMPOSITE VIDEO SIGNALS ARE TAKEN THROUGH VIDEO AMPLIFIER IC PROVIDING OPTION FOR DIRECT CONNECTION.
6	HDDAC SIGANLS ARE CONNECTED TO VIDEO AMPLIFIER THS7360IPW AND THEN THE OUTPUT ARE CONNECTED TO VGA CONN AND ALSO TO COMPONENT VIDEO CONNECTORS(RGB).
7	27 MHz CRYSTAL IS ADDED INSTEAD OF 22.579MHz.
8	IO EXPANDER-3 WITH I2C2 ADDRESS 0X20 IS ADDED. INTERRUPT PCF8575_INT_VA FROM THIS IC IS GIVEN TO SD0_DAT[6]/GP0[12].
9	HDMI ESD SUPPRESSOR TPD12S016RKTR IS ADDED INSTEAD OF TPD12S521DBTR. HDMI_CT_HPD AND HDMI_LS_OE SIGNALS ARE TAKEN FROM NEWLY ADDED IO EXPANDER-2 WHOSE INTERRUPT IS CONNECTED TO SD0_DAT[7]/GP0[13].
10	MCASP0 AND MCASP1 MUXING IS ADDED. 2:4 DECODER IS USED TO ENABLE SWITCHING. IO EXPANDER-2 IS USED TO ENABLE DECODER.
11	EXPANSION CONNECTOR(DRI) TO GET POWER TO THE BB IS REMOVED. POWER SELETION SECTION IS MODIFIED ACCORDINGLY.
12	OPTION TO SELECT I2C2 OR UART2 SIGNALS IS PROVIDED.BUFFERS USED ARE ENABLED BY I2C2/UART2_SEL SIGNAL FROM IO EXPANDER-1.
13	SINCE THE MLB_DAT AND MLB_SIG IS NOT AVAILABLE IN DM385 TWO GPIOs FROM IO EXPANDER -2 IS GIVEN TO EXPANSION CONNECTOR WHICH ARE USED AS GPIOs ON THE CATLOG BOARD.
14	POWER VDDQ_CENT_1V5 IS CHANGED TO VDDQ_DM_1V5
15	SATA INDICATOR LED IS ADDED.
16	MCA_AXR[6:8] SIGNALS ARE REMOVED FROM THE CONNECTOR SIDE.
17	MCA_AXR[9] SIGNAL WHICH IS USED AS GPIO IN VC BOARD IS TAKEN FROM IO EXPANDER-2
18	BUS FET SWITCH IS ADDED THROUGH WHICH UART0 SIGNALS ARE CONNECTED TO EXPANSION CONNECTOR.
19	I2C2 BUFFER IS ADDED AND SIGNALS ARE GIVEN TO IO EXPANDER-3 AND VGA CONNECTOR.
20	POWER MONITORING IC INA220 IS UPDATED WITH INA226.
21	SN74CBTLV3384PW(U3 & U40) ICs ARE REPLACED WITH SN74CB3Q3257PWR.DECODER USED FOR MCASP1 MUXING IS REMOVED.
22	R399,R392,R254,R248,R522 ---0E RESISTORS ARE REPLACED WITH 22E. R579,R494 ARE REMOVED.
23	PCA9306(U85 & U102) ICs ARE REPLACED WITH TCA4311A.
24	OPTION FOR SELECTING MCA5_AFSR/AXR0 OR GPIOs FOR VC BOARD FROM IO EXPANDER-2 IS PROVIDED USING MUX.
25	GPIO (IO_EXP2_GP3) FROM IO EXPANDER-2 IS PROVIDED TO COMPENSATE FOR MLB_CLK SIGNAL.
26	0E OPTION IS GIVEN FOR VIN[0]A_VSYNC/GP2[4](C13).0E OPTION IS GIVEN FOR VIN[0]A_HSYNC/GP2[3] (D13)
27	IO EXPANDER-1 INTERRUPT PCF8575_INT_IO1 IS CHANGED FROM GP1[8] TO GP1[4].
28	MUXING OPTION IS GIVEN TO SELECT DIFFERENT FUNCTIOS OF VOUT0/1_FLD PINS.ONE MORE DECODER IS ADDED TO SELECT ONE FUNCTION AT A TIME.
29	I2C2/UART2_SEL SIGNAL IS REMOVED FROM THE IO EXPANDER-1 & IS TAKEN FROM DECDER WHICH BY DEFAULT SELECT VOUT0/1_FLD SIGNAL.
30	IO EXPANDER-1 INTERRUPT IS TAKEN FROM GP1[4] INSTEAD OF GP[8].
31	U68 & ITS BIASING CIRCUITRY (1.2V FOR TPS_CVDD_HDVICP) OF CENTARAUS IS REMOVED AND ALSO U22(INA226) IS REMOVED
32	TPS71711DCKR IS ADDED NEWLY TO GENERATE 1.1V FOR HD DAC
33	TPD6E001 ESD SUPPRESSOR IS ADDED
34	INA220 IS UPDATED TO INA226
35	U80,U81,U106 & U112 ARE DELETED.TPD7S019 (U7) IS ADDED.
36	RA86 IS REPLACED WITH 0E SERIES RESISTORS. R476 PACKAGE ISCHANGED TO 0402.
37	EN_TPS62350 SIGNAL FROM TPS659113 IS REMOVED AS WE HAVE HAVE REMOVED TPS62350 IC.
38	Q6 & Q7 ARE REMOVED.SN74LVC2G06DCK(U86) IS ADDED IN THE SATA LED INDICATOR SECTION. Y6 CRYSTAL MA-506 27.0000M-C0: (FUND):ROHS IS REPLACED WITH NEW PART ABM8-27.000MHZ-B2-T.

SL NO#	CHANGES IN THE SCHEMATICS COMPARED TO CENTAURUS.
39	CLOCK DRIVER IC IDT74FCT38075DCGI(U65) IS CHANGED TO CDCV304PW.
40	CODEC SIGNALS FROM MCASP MUXING STAGE IS PASSED THROUGH BUFFER ICs SN74AVCH1T45DBVR (U19,U20,U21) & SN74AVCH2T45DCTR (U22). BUFFER ICs ARE MADE DNI.OE RESISTOR OPTION IS GIVEN TO BYPASS THE BUFFER STAGE.
41	RESISTOR DIVIDER CKT TO GET VREF FOR DDR INTERFACE IS REMOVED AND VD_VREF IS TAKEN FROM TPS51116(PIN 5) DIRECTLY.
42	A15 & B15 SIGNALS ARE SWAPPED.N30 & N31 SIGNALS ARE SWAPPED.P20 & P21 ARE CHANGED FROM VSS TO VDDS_OSC1 & VDDS_OSC0 respectively.
43	TESTPOINTS TP128,TP129 & TP130 ARE REMOVED AND J25,H24 & H28 OF DM385 IS MADE NC.
44	GPIO_VS_1 FROM IO EXPANDER-2 IS ADDED TO COMPENSATE FOR MLBP_CLKp SIGNAL ON CENTAURUS. THIS SIGNAL IS USED AS GPIO ON VS BOARD.
45	AN OR-GATE(U53) IS ADDED TO ENABLE THE WAKE-on-LAN FUNCTIONALITY OF ATHEROS CHIP. PCF8575_INT_VA INTERRUPT FROM IO EXPANDER-3 IS TERMINATED TO A TESTPOINT.INSTEAD OF THIS SIGNAL, ENET_WoL_INT INTERRUPT IS CONNECTED TO GP0[12] OF DM385.
46	C64 IS CHANGED TO PART NO# F931C105MAA, RJ-45 SYMBOL UPDATED. FL10,FL11,FL12,FL13 (TCE1210) IS REPLACED WITH TCM1210.
47	TPD2E001(U122) ESD PROTECTION DEVICE FOR COMPOSITE VIDEO SIGNAL IS ADDED. TPD3E001(U123) ESD PROTECTION DEVICE FOR COMPONENT VIDEO SIGNALS IS ADDED.
48	R59 IS CHANGED TO 8mE.
49	INA226 DEVICES ARE ADDED TO MONITOR DVDD,DVDD_C AND VMMC
50	PLL_1V8,HDMI_CSI_1V8 & DVDD_GPMC POWER LINES ARE MONITORED INSTEAD OF BCK2_3V3,EVM_5V0 & VDDQ_1V5 POWER LINES USING U10,U15 & U24 RESPECTIVELY.
51	20MHz CRYSTAL (Y3) IS CHANGED TO SMALLER SIZE PACKAGE CRYSTAL WITH PN# 403C11A20M00000.
52	L6 IS CHANGED FROM 2.7uH TO 2.2uH. Q1 & Q2 IS CHANGED TO FDMC7660DC FROM FDS8812NZ.
53	R179 & R427 ARE REMOVED FROM THE DESIGN.

REV NO.	NATURE OF CHANGE	APPROVED BY	DATE

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Drawn by: MISTRAL DESIGN TEAM | Approved by: KRISHNA PRASAD A
Date: Monday, May 31, 2010 | Date: Monday, August 08, 2016
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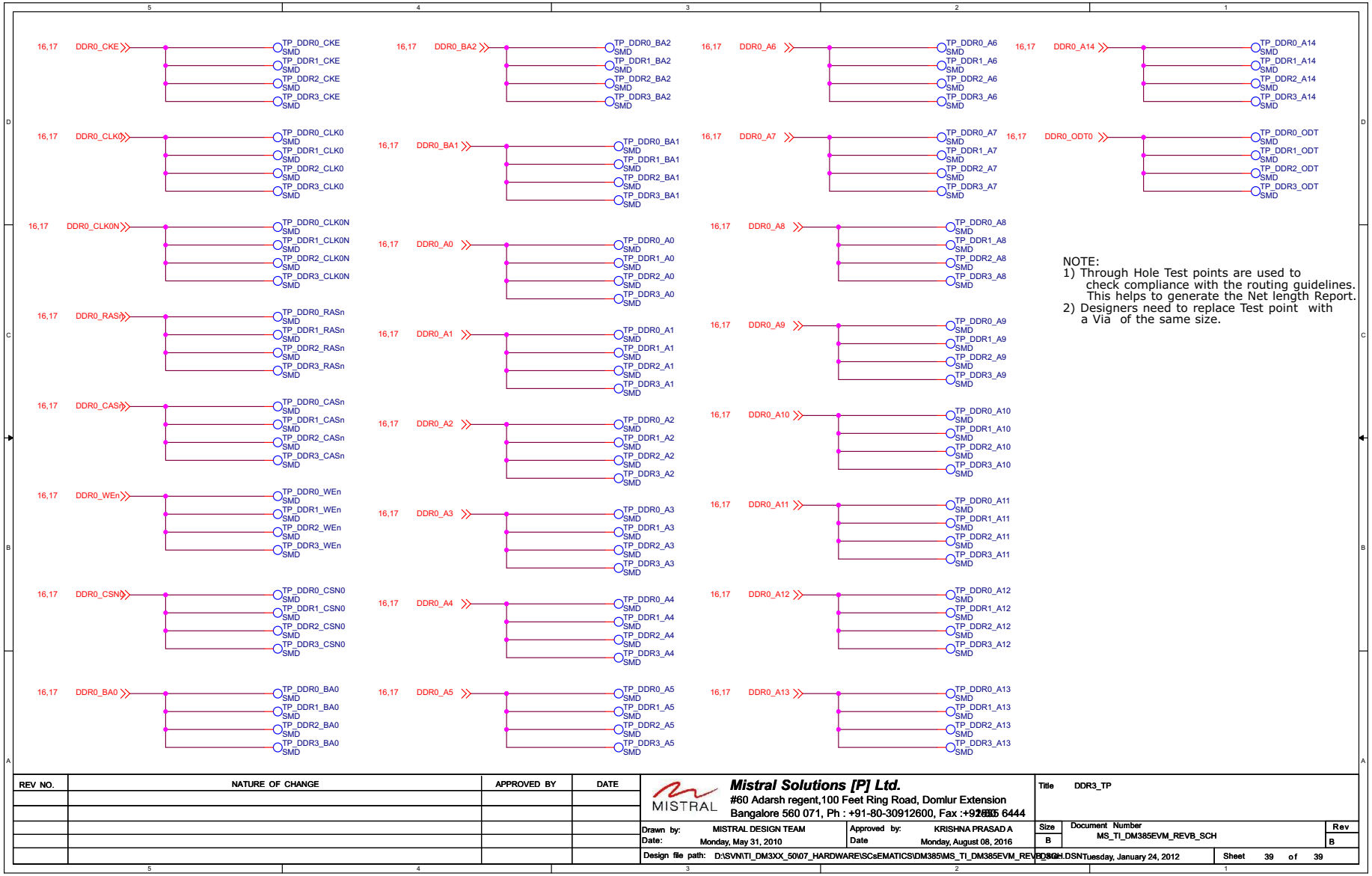
Title: SCH_CHANGES
Size: C | Document Number: MS_TI_DM385EVM_REVB_SCH | Rev: B
Date: Tuesday, January 24, 2012 | Sheet 38 of 39

Figure A-38. DDR3_TP



Assembly Drawings

The assembly prints for the DM388 device are the same as the assembly prints for the DM385 device. Figure B-1 and Figure B-2 show the assembly prints.

Figure B-1. Assembly Drawing (Top Side)

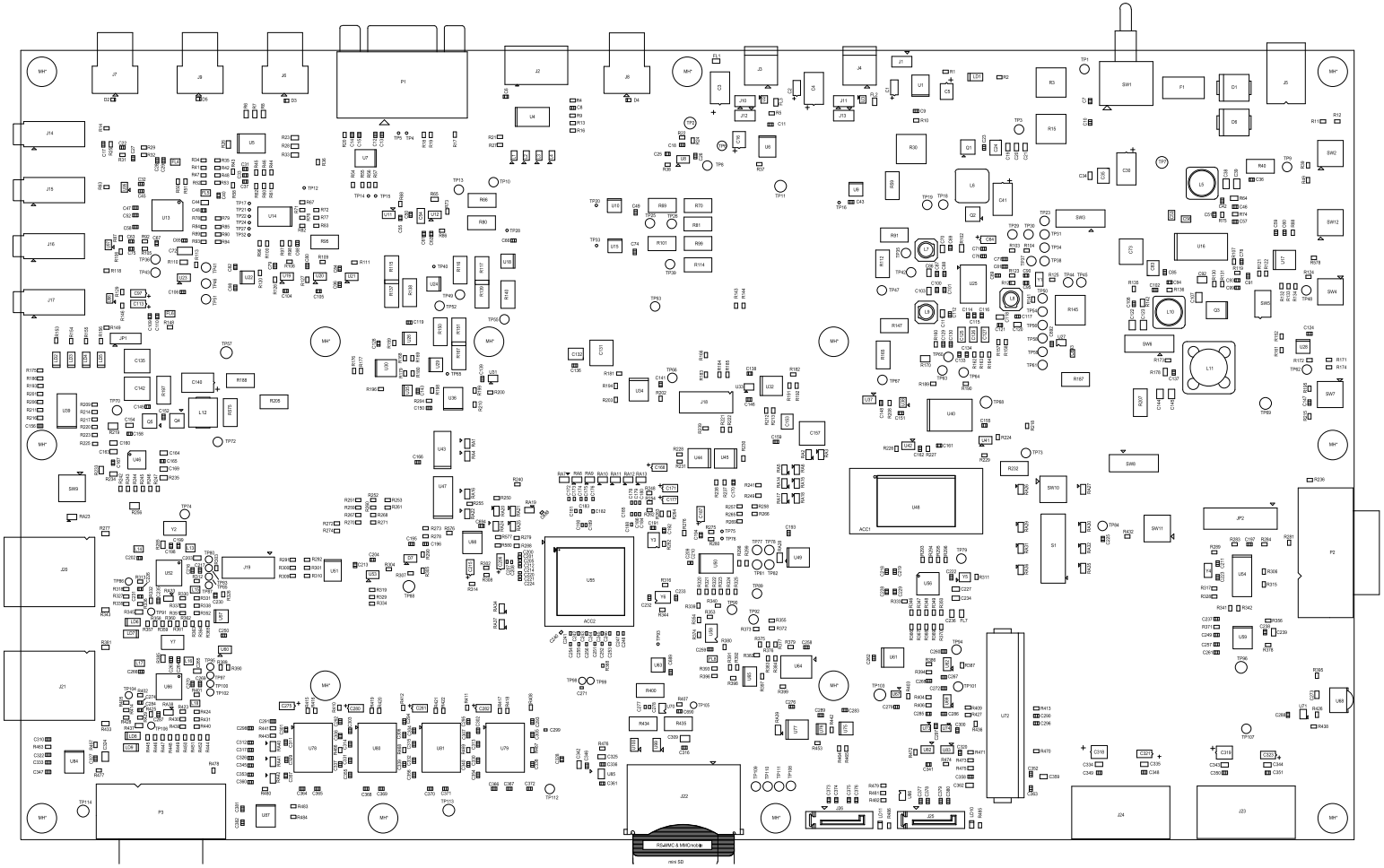
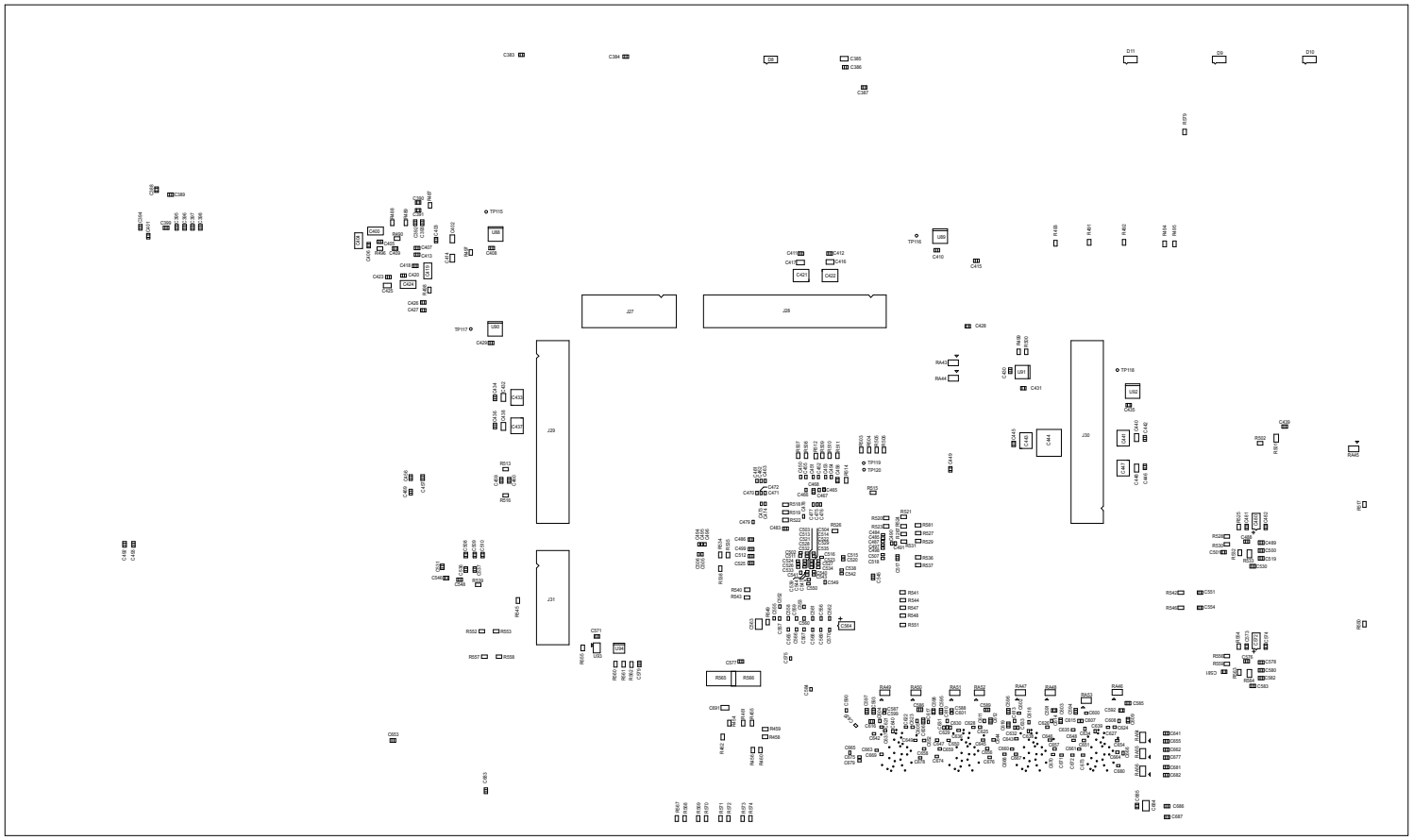


Figure B-2. Assembly Drawing (Bottom Side)



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