OMAP5912 Multimedia Processor Display Interface Reference Guide

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Preface

Read This First

About This Manual

This document describes the display interface of the OMAP5912 multimedia processor.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

Documentation that describes the OMAP5912 device, related peripherals, and other technical collateral, is available in the OMAP5912 Product Folder on TI's website: www.ti.com/omap5912.

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Display Interface

This document describes the display interface of the OMAP5912 multimedia processor.

1 Overview

This document discusses the following components of the display interface:

- ❏ LCD module
- ❏ LCD data conversion module
- ❏ LED pulse generator
- ❏ Display interface

2 LCD Module

The device includes an LCD controller that interfaces with most industry-standard LCD displays through embedded or discrete timing controllers. The LCD controller operates only in single-panel mode (dual-panel mode is not supported). The module is designed to work with a separate RAM block to provide data to the FIFO at the front end of the LCD controller data path at a rate sufficient to support the chosen display mode and resolution.

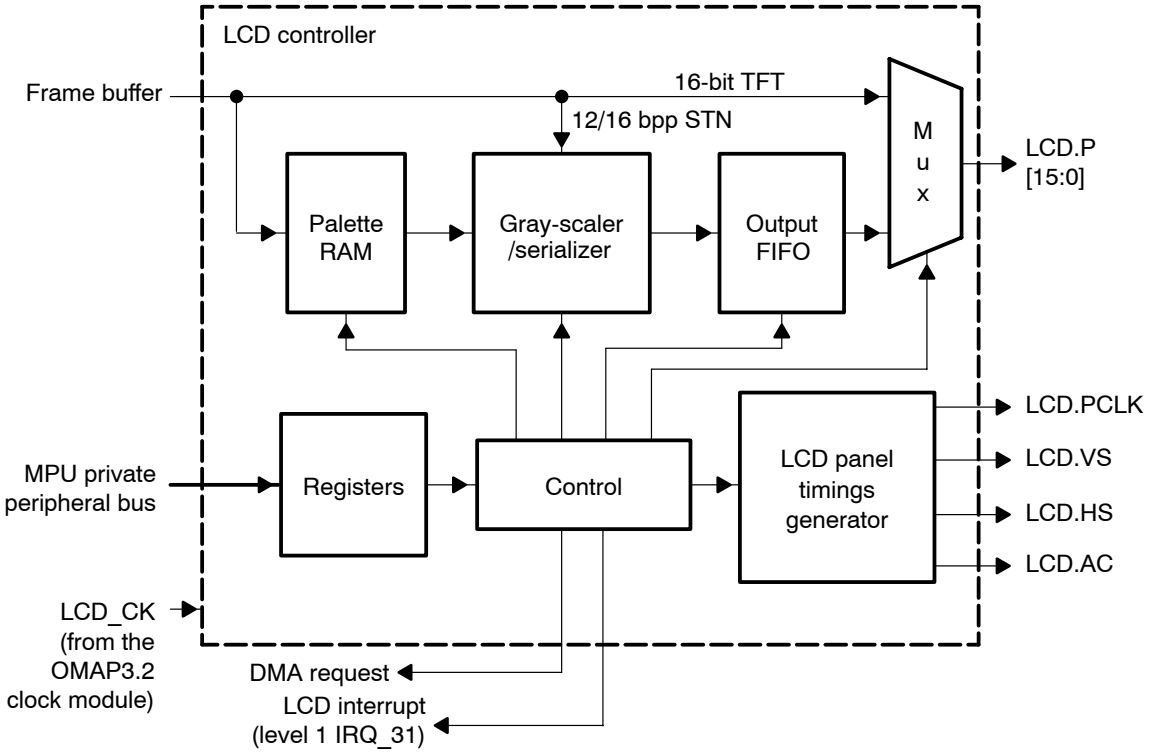
The panel size is programmable and can be any width (line length) from 16 to 1024 pixels, in 16-pixel increments. The number of lines is set by programming the total number of pixels in the LCD. The total frame size is programmable up to 1024×1024.

Frame sizes and frame rates supported in specific applications depend on the available memory bandwidth allowed by the application.

The screen is intended to be mapped to the frame buffer as one contiguous block, where each horizontal line of pixels is mapped to a set of consecutive bytes of words in the frame memory.

Figure 1 shows the LCD controller in detail.

Figure 1. LCD Controller



The LCD controller's principal features are:

- Dedicated 64-entry x 16-bit FIFO
- Dedicated LCD DMA channel for LCD display
- Programmable display including support for 1-, 2-, 4-, 8-, 12-, and 16-bit graphics modes
- Programmable display resolutions up to 1024 pixels by 1024 lines
- Support for passive monochrome (STN) displays
- Support for passive color (STN) displays
- Support for active color (TFT) displays
- Patented dithering algorithm, providing:
  - 15 grayscale levels for monochrome passive displays
  - 3375 colors for color passive displays

- 65536 colors for active color displays
- 256-entry x 12-bit palette
- Programmable pixel rate
- Pixel clock plus horizontal and vertical synchronization signals
- ac-bias drive signal
- Active display-enable signal

Frame buffer data can be formatted for 1-, 2-, 4-, 8-, 12-, or 16-bit pixel sizes. A 16-entry x 12-bit palette supports the 1-, 2-, and 4-bit pixel sizes, whereas a larger 256-entry x 12-bit palette supports the 8-bit pixel size. The 12-bit and 16-bit pixel sizes provide data that bypasses the palettes. The data is then processed according to the desired type of display.

For passive monochrome panels, the 4-bit value indexed from the least significant bits of the palette is passed to the patented dither logic, where the desired brightness is created using temporal dithering. The pixels are passed to the panel via a 4-wire interface, 4 pixels in parallel per pixel clock.

For passive color panels showing 8-bit color or less, an entry from the palette is transferred simultaneously into three parallel dither engines, one for each of the red, green, and blue colors. These values are converted by the three patented temporal dithering logic blocks to provide up to 256 colors out of a possible 3375 colors (15 x 15 x 15). The pixels are passed to the panel via an 8-wire interface, 2 2/3 pixels per clock.

For passive color panels showing 12- or 16-bit color, the data from the frame buffer is passed directly into the dither logic, bypassing the palette. The three parallel dither engines then provide up to 3375 colors. The 16-bit color mode uses only the most significant four bits of each color channel. The pixels are also passed to the panel via an 8-wire interface, 2 2/3 pixels per clock.

For active color panels showing 8-bit color or less, an entry from the palette is expanded from 12 bits to 16 bits and passed to the display, providing up to 256 colors out of a possible 4096 (16 x 16 x 16) colors. The pixels are passed to the panel via a 16-wire interface, 1 pixel per clock.

For active color panels showing 12-bit color, the data is also expanded from 12 bits to 16 bits to provide up to 4096 colors. The pixels are passed to the panel via a 16-wire interface, 1 pixel per clock.

For active color panels showing 16-bit color, the data is passed directly to the display (bypassing palette and dither logic), providing up to 65536 colors. The pixels are passed to the panel via a 16-wire interface, 1 pixel per clock.

The active color modes can also be used with an external DAC to drive a video monitor. The LCD line clock pin functions as a horizontal synchronization (HSYNC) signal, and the frame clock pin functions as a vertical synchronization (VSYNC) signal.

Table 1 shows the details of the LCD controller signals.

Table 1. Interface to LCD Panel Signal Descriptions

Name	Type	Destination	Description
LCD.P[15:0]	Out	LCD panel display	I/O pins used to transfer 4, 8, or 16 data values at a time to the LCD display. For monochrome displays, each signal represents a pixel; for passive color displays, groupings of three signals represent one pixel (red, green, and blue). LCD.P[3:0] is used for monochrome displays of 2, 4, and 8 BPP; LCD.P[7:0] is used for color STN displays and LCD.P[15:0] is used for active (TFT) mode.
LCD.PCLK	Out	LCD panel display	Pixel clock used by the LCD display to clock the pixel data into the line shift register. In passive mode, the pixel clock transitions only when valid data is available on the data lines. In active mode, the pixel clock transitions continuously, and the ac-bias pin is used as an output enable to signal when data is available on the LCD pins.
LCD.HS	Out	LCD panel display	Line clock used by the LCD display to signal the end of a line of pixels that transfers line data from the shift register to the screen and to increment the line pointer(s). Also used by TFT displays as the horizontal synchronization signal.
LCD.VS	Out	LCD panel display	Frame clock used by the LCD display to signal the start of a new frame of pixels. Also used by TFT displays as the vertical synchronization signal.
LCD.AC	Out	LCD panel display	ac-bias used to signal the LCD display to switch the polarity of the power supplies to the row and column axis of the screen to counteract DC offset. Used in TFT mode as the output enable to signal when data is latched from the data pins using the pixel clock.

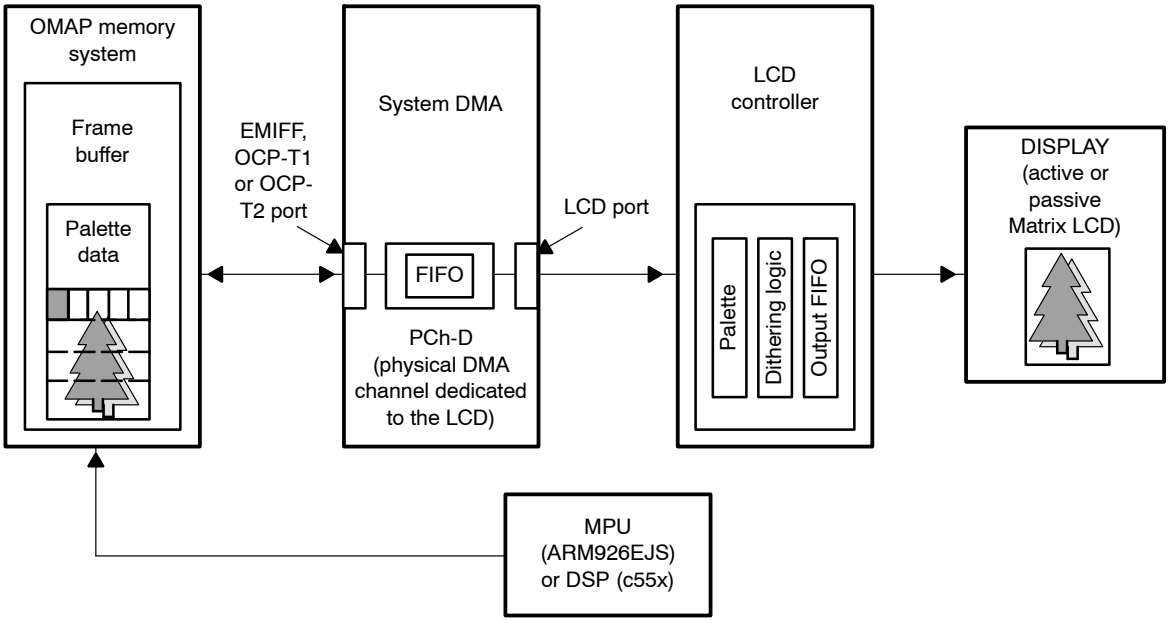
The pixel clock frequency is derived from the clock provided to the LCD controller (LCD_CK) from the clock management logic and is programmable from OMAP3.2 clock management logic (see the *Multimedia Processor OMAP 3.2 Subsystem Reference Guide (SPRU749)*). Each time new data is supplied to the LCD data pins, the pixel clock is toggled to latch the data into the LCD display serial shifter. The line clock toggles after all pixels in a line have been transmitted to the LCD driver and a programmable number of pixel clock wait states have elapsed both at the beginning and end of each line. In passive mode, the frame clock toggles during the first line of the screen, and the beginning and end of each frame is separated by a programmable number of line-clock wait states. Horizontal front porch (HFP) and horizontal back porch (HBP) must be programmed to zero in passive mode.

In active mode, the frame clock is asserted at the end of a frame after a programmable number of line-clock wait states occurs. In passive display mode, the pixel clock does not transition during wait state insertion or when the line clock is asserted. Finally, the ac-bias (LCD.AC) can be configured to transition each time a programmable number of line clocks occurs.

2.1 LCD Controller Environment

The LCD controller provides the necessary control signals to interface the memory directly to the external display through a dedicated DMA channel, as seen in Figure 2.

Figure 2. Data Flow from Microprocessor to Display



The MPU, or the DSP, stores the image to be displayed in a frame buffer. The frame buffer is used to supply enough encoded pixel values to fill the entire screen at least once.

The palette and the picture data are both in system memory. The palette loading mode (PLM) can be switched around so that only the picture data, only the palette data, or both are loaded at a given time (the palette is loaded only when it changes, then the PLM bit-field returns to picture-only mode).

The working copy of the palette resides in the LCD controller itself. See section 2.2, *LCD Controller Operation,* for descriptions of each block.

A specific system DMA channel dedicated to the LCD controller (LCh-D) is in charge of transferring data from the frame buffer to the LCD controller. Data is fetched, then transits into a 64*33-bit FIFO. The 33rd bit is added for frame-synchronization purposes. However, the internal LCD controller receives 16-bit data from the DMA FIFO with each request.

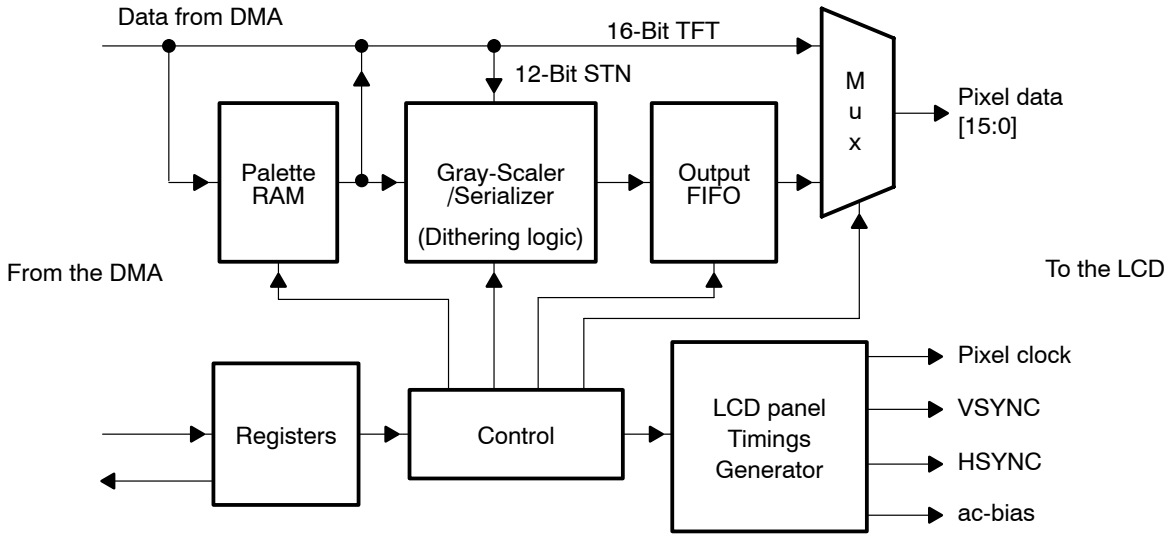
The following section describes the LCD controller operation in detail.

2.2 LCD Controller Operation

The LCD controller essentially consists of three blocks: a palette RAM, dithering logic, and an output FIFO, all associated with a control block operating through registers and a timing generator.

Figure 3 illustrates the LCD controller logic.

Figure 3. LCD Controller Operation Overview (Passive and Active Display Modes)



The LCD controller supports single-panel mode displays with programmable sizes. The display can be any width (line length) from 16 to 1024 pixels in 16-pixel increments (bit pixels per line (PPL) in the LCD timing 0 register). The number of lines is set by programming the lines per panel (LPP) field of the LCD timing 1 register (see section 2.3.3, *LCD Timing 1 Register*). The total video frame size is programmable up to 1024 x1024.

The screen is intended to be mapped to the frame buffer as one continuous block, where each line of pixels is mapped to a set of consecutive bytes or words in the frame buffer.

Two types of display technologies are supported:

- ❏ Passive, also known as super-twisted nematic, or STN
- ❏ Active, also known as thin film transistor, or TFT panels configured with the LCD TFT bit (LcdTFT) in the control register

See section 2.3.1, *LCD Control Register* for more information. Both monochrome and color modes are supported (LCD monochrome bit (LcdBW) in the control register).

In passive STN mode, a total of 3375 possible colors is available, allowing 16, 256, or 3375 colors to be displayed in each frame, depending on the color depth (number of bits per pixel: BPP). Fifteen grayscale levels are available for monochrome screens. See the *Dithering Logic* section, for information regarding the number of colors displayed versus BPP and screen technology.

In active TFT mode, whatever the color depth, 4096 colors can be displayed, except in the 16 BPP mode, where up to 64K colors are supported. See the *Dithering Logic* section for information regarding the number of colors displayed versus BPP and screen technology.

Note:

The active monochrome configuration is intentionally not considered in the remainder of this document.

Frame Buffer

The frame buffer is a memory area used to supply enough encoded pixel values to fill the entire screen one time. It is a part of the memory which is connected either to EMIFF, OCP-T1, or OCP-T2 port. A portion of the LCD controller frame buffer is used as a 32-byte buffer for 1-, 2-, 4- , 12-, and 16-BPP mode operation, or as a 512-byte buffer for 8 BPP mode of operation. The buffer is used to store the current display depth and a look-up palette, which is nonzero-filled for 8BPP and lower modes.

The 32-byte buffer is used to load the 16 entries of the palette for 1-, 2-, 4-, 12-, and 16-BPP encoding, or the 512-byte buffer is used to load the entire 256-entry palette for 8-BPP encoding.

Not all of the 16 entries of the palette are used in 1- and 2-BPP modes. However, all 16 palette entries are loaded regardless. The unused palette entries must be zero-filled.

The palette is not used in 12- or 16-BPP modes, but is still required. The 32 bytes of the palette are zero-filled, except for the first entry, where a 3-bit field provides the information on the number of bits-per-pixel.

Each time a new frame is fetched from the frame buffer, the LCD controller palette is first loaded with data contained within the palette buffer. Normally, this buffer is placed immediately preceding the frame buffer image data to simplify programming of the LCD DMA channel (see *Multimedia Processor Direct Memory Access (DMA) Support Reference Guide (SPRU755)*). However, using the dual-frame feature of the LCD DMA channel, the palette can be placed anywhere within the frame buffer. Separating the palette from the image data is necessary to enable the *pan-and-scan* or *virtual desktop* feature enabled by the LCD DMA channel, and can be useful in other situations. When the palette buffer is in data loading mode only, you do not have to load the palette each time. PLM = 10 in the control register; see subsection *Palette Loading (PLM)*.

Figure 4 and Figure 5 show the palette entry organization.

Figure 4. 16-Entry Palette/Buffer Format (1, 2, 4, 12, 16 BPP)

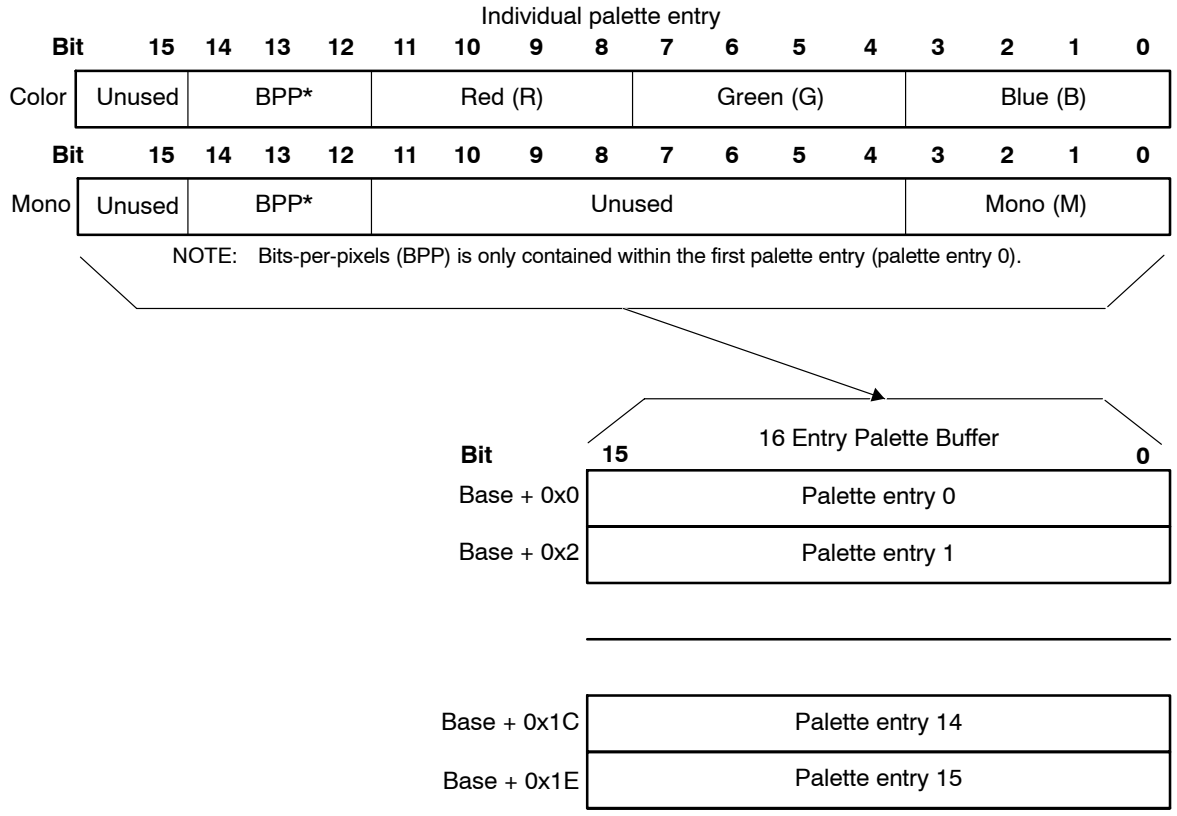
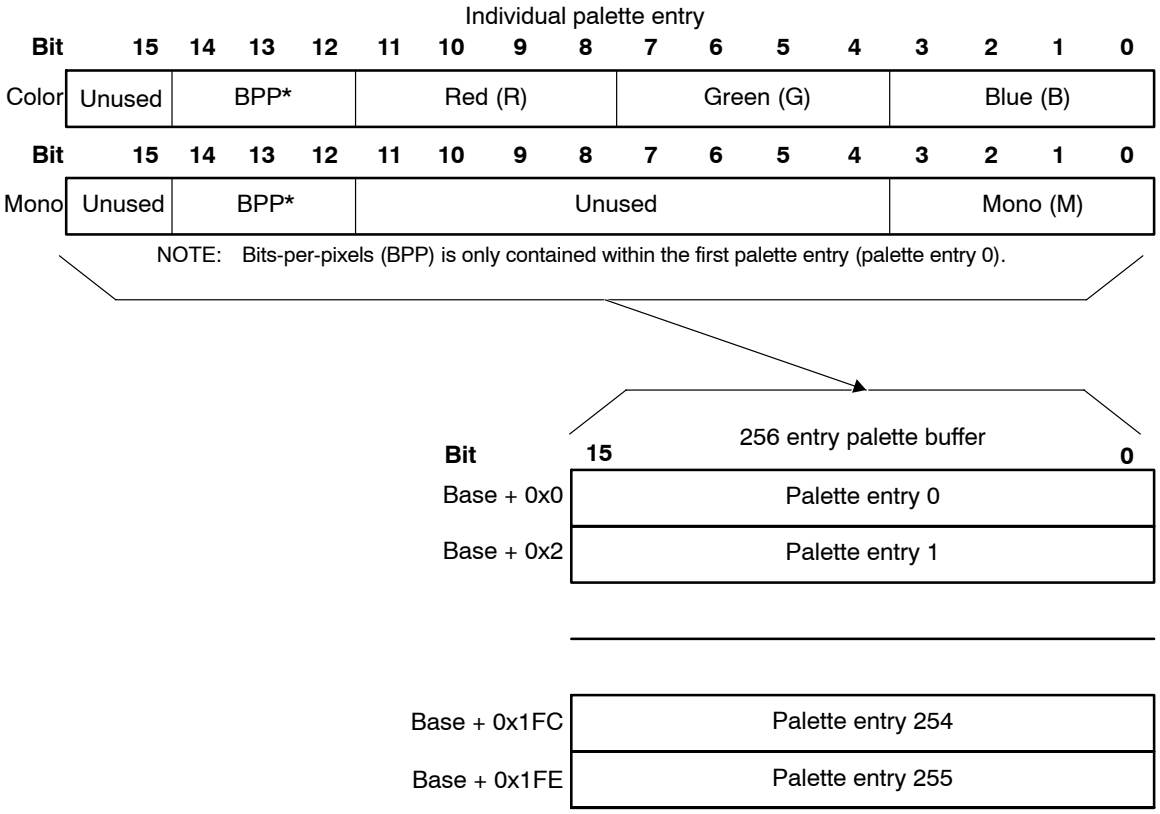


Figure 5. 256-Entry Palette/Buffer Format (8 BPP)



Bits 12, 13, and 14 of the first palette entry select the number of bits-per-pixel to be used in the following frame and thus, the number of palette RAM entries.

The bits-per-pixel (BPP) bit-field is decoded by the LCD to correctly unpack pixel data. It also configures the palette size to 16 or 256 entries.

Table 2 shows the BPP encoding in palette entry 0.

Table 2. Bits-Per-Pixel Encoding for Palette Entry 0 Buffer

Bit	Name	Description
14:12	BPP	Bits-per-pixel
		000: 1 BPP
		001: 2 BPP
		010: 4 BPP
		011: 8 BPP
		1xx: 12 BPP in passive mode (LcdTFT=0 and 565 STN =0),
		16 BPP in passive mode (LcdTFT=0 and 565 STN =1),
		16 BPP in active mode (LcdTFT=1).

Notes: 1) Eight 1-bit pixels, four 2-bit pixels, and two 4-bit pixels are packed into each byte, and 12-bit pixels are right justified on (16-bit) word boundaries (in the same format as palette entry).

2) For 565 STN, see the 16 BPP STN mode bit in the control register section.

The pixel data buffer contains one encoded pixel value for each pixel present on the display. Hence, the number of pixel data values depends on the size of the screen (i.e., 1024 x 768 = 786,432 encoded pixel values). Again, each pixel data value can be 1, 2, 4, 8, 12, or 16 bits wide.

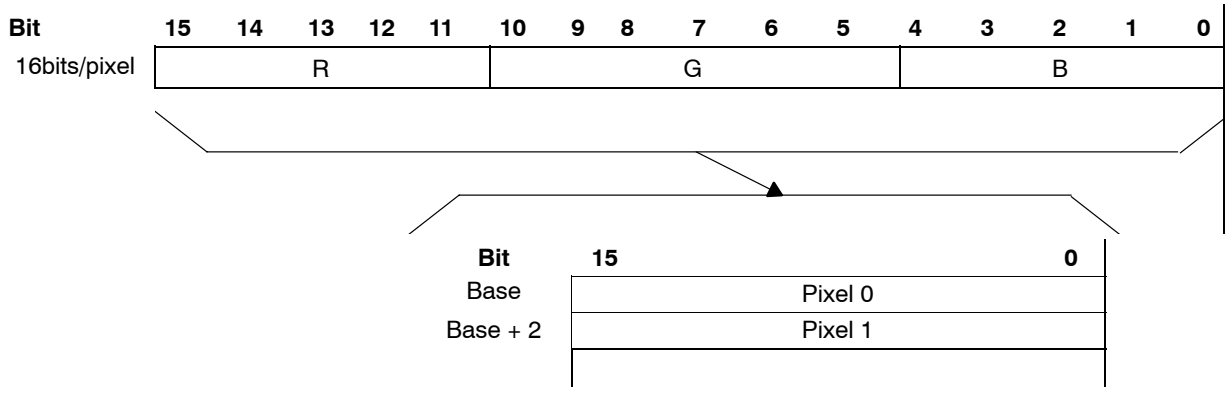
The following figures show the memory organization within the frame buffer for each pixel encoding size.

The LCD controller is fed with 16-bit data from the LCD DMA channel. In 16- and 12-BPP modes, this data is unaffected by LCDCB0 or LCDCB1 configuration bits.

16-BPP Mode (TFT)

Figure 6 shows one RGB representation in 16-BPP (TFT) mode.

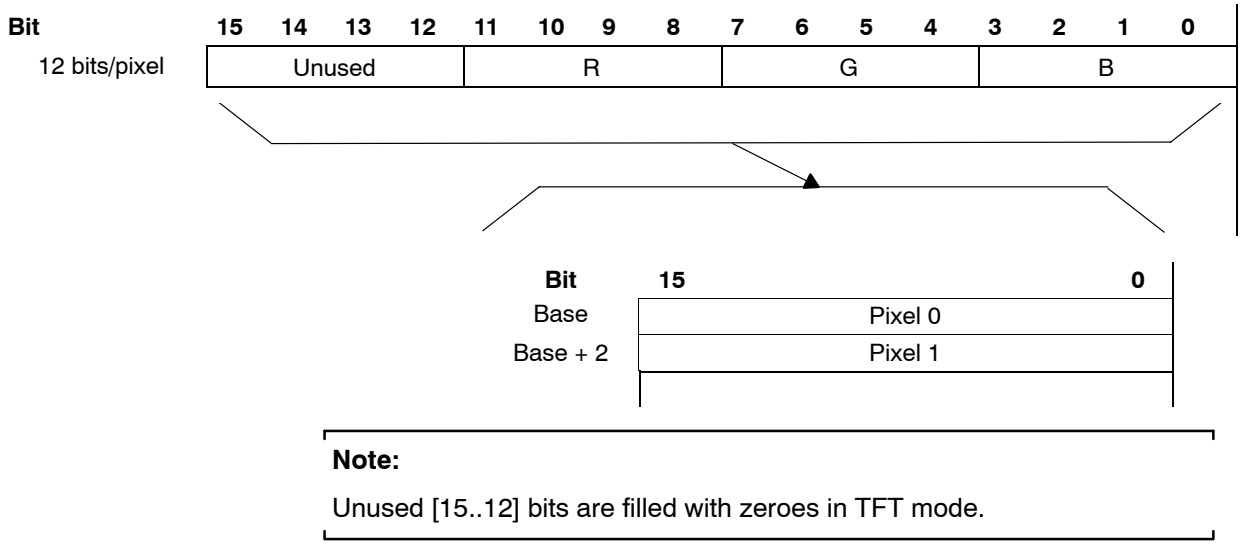
Figure 6. 16-BPP Data Memory Organization (TFT Mode Only)—Little Endian



12-BPP Mode

Figure 7 shows the RGB representation in 12-BPP mode.

Figure 7. 12-BPP Data Memory Organization—Little Endian



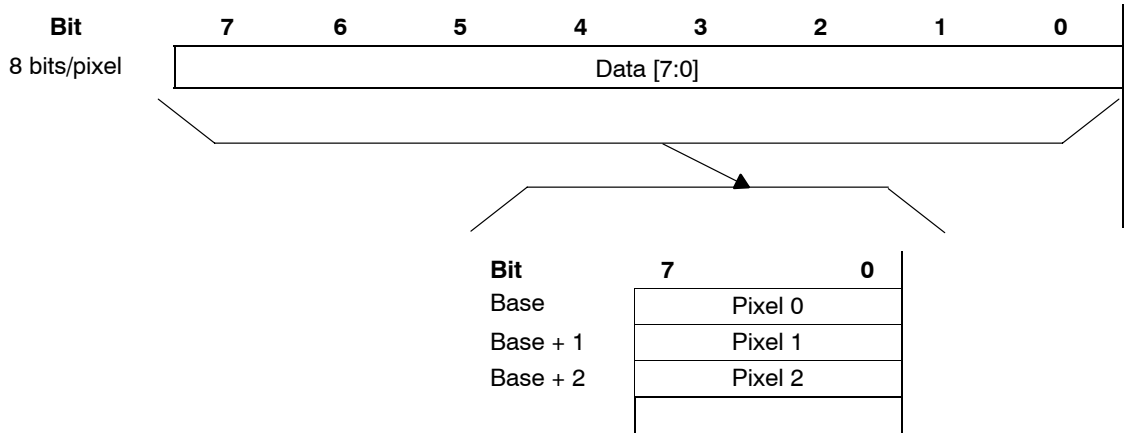
Note:

Unused [15..12] bits are filled with zeroes in TFT mode.

8-BPP Mode

Figure 8 shows the format of the data in 8-BPP mode.

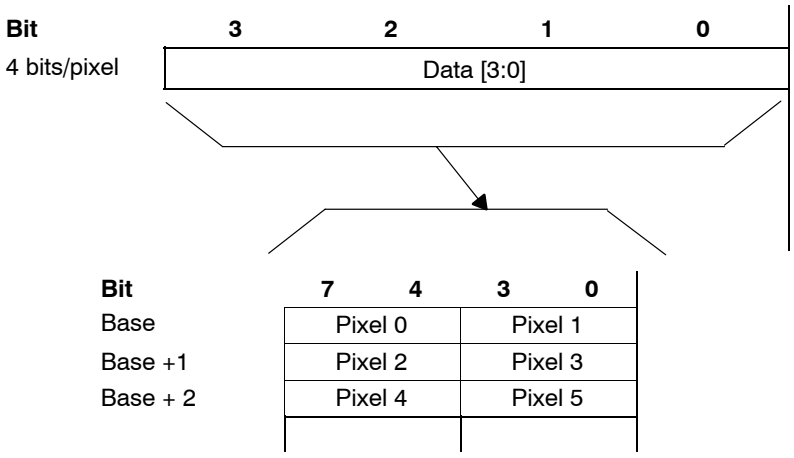
Figure 8. 8-BPP Data Memory Organization



4-BPP Mode

Figure 9 shows the format of the data in 4-BPP mode.

Figure 9. 4-BPP Data Memory Organization



2-BPP Mode

Figure 10. 2-BPP Data Memory Organization

Bit	7 6	5 4	3 2	1 0
Base	Pixel 0	Pixel 1	Pixel 2	Pixel 3
Base + 1	Pixel 4	Pixel 5	Pixel 6	Pixel 7
Base + 2	Pixel 8	Pixel 9	Pixel 10	Pixel 11

1-BPP Mode

Figure 11. 1-BPP Data Memory Organization

Bit	7	6	5	4	3	2	1	0
Base	P0	P1	P2	P3	P4	P5	P6	P7
Base + 1	P8	P9	P10	P11	P12	P13	P14	P15

The top and bottom addresses of the frame buffer (palette entries + pixels data) are programmed in the DMA controller.

The equations shown in Table 3 are used to calculate the total frame buffer size (in bytes) to program in the system DMA, based on varying pixel size encoding and screen sizes.

Table 3. Frame Buffer Size According to BPP

BPP	Frame Buffer Size
1	32 + (Lines * Columns) / 8
2	32 + (Lines * Columns) / 4
4	32 + (Lines * Columns) / 2
8	512 + (Lines * Columns)
12/16	32 + 2 * (Lines * Columns)

It is important to understand that BPP has two different meanings:

- In this section, BPP refers to how pixels are stored in memory. 1, 2, 4, 8, 12, or 16 are the different representations of the pixel within the frame buffer.
- BPP can also refer to how the panel views the pixels. This usage refers to which BPP the panels support (the actual interface, not the memory representation). The supported output panels are:
  - 1 BPP for monochrome panels, packed onto 8 (or 4) data lines
  - 3 BPP (1 bit each for red, green, and blue) for passive matrix technologies (output of dithering logic), packed onto 8 data lines
  - 12 BPP for STN (4, 4, 4) panels
  - 16 BPP for TFT (5, 6, 5) panels

Palette

The encoded pixel values stored in the frame buffer are used as pointers to index the 16-bit-wide palette. Palette entries are configured differently according to the mode used. See Figure 4 and Figure 5 for details.

The number of colors supported is given by $2^{\text{number of BPP}}$. These $2^{\text{number of BPP}}$ colors are to choose within the palette that limits them to $2^4 = 16$ grayscales in monochrome mode, and $2^{12} = 4096$ colors in color mode, where 4 and 12 are the effective palette width in each case (*effective* meaning dedicated to the monochrome/color scales coding).

16 grayscales and 4096 colors are numbers obtained after passing through the palette. A redundancy introduced at the dithering logic step reduces these numbers when displaying. As the dithering logic is bypassed in active mode, there is no redundancy and 4096 different colors are really available. For more detail, see the section *Dithering Logic,* Table 4, *Color/Grayscale Intensities and Modulation Rates,* and Table 5, *Number of Colors/Grayscales Available on Screen.*

❑ ***Passive Matrix Technology***

The palette is bypassed in 12 BPP. In palette plus data or in palette-only modes (PLM = 00 or 01), the first entry is read to acquire the number of BPP. All other entries or useless bits in the first entry are filled with zeroes. But in data-only mode (PLM = 10), the palette is not loaded with every frame.

Note:

Henceforth, the palette is said to be *bypassed* in 12- and 16-BPP modes. The 12-bit values are directly supplied to the dither logic when passive mode is enabled, while the 16-bit values are directly sent to the panel when active mode is enabled. The *bypass* term can be misleading in PLM = 00 or 01 configurations, considering that the palette must be read, at least for the first entry that contains the information of the color depth. The rest is zero-filled and not taken into consideration. In PLM = 10 (data-only mode), the palette is bypassed.

❑ ***Active Matrix Technology***

The palette is bypassed in 16 BPP, allowing 2^{16} = 65536 = 64K colors to be displayed.

Dithering Logic

❑ ***Passive Matrix Technology***

Once a palette entry is selected by the encoded pixel value from the look-up palette, its content is sent to the color/grayscale space/time-based dither generator. The monochrome data, as well as each component, is encoded on 4 bits: red, green, and blue (RGB) in color mode. See individual palette entry in Figure 4 and Figure 5. Each 4-bit value is processed by one dither block. Three separate dither blocks are used in the color mode. These 4-bit values are used to select one of the 16 intensity levels. The gray/color intensity is controlled by turning individual pixels on and off at varying periodic rates. More intense grays/colors are produced by making the average time that the pixel is off longer than the average time that it is on. The dither generator also uses the intensity of adjacent pixels in its calculations to give the screen image a smooth appearance. The proprietary dither algorithm is optimized to provide a range of intensity values that match the eye's visual perception of color/gray gradations.

Table 4 summarizes the duty cycle and resultant intensity level for all 16 color/grayscale levels.

Table 4. Color/Grayscale Intensities and Modulation Rates

Dither Value (4-Bit Value from Palette)	Intensity (0% is White)	Modulation Rate (Ratio of ON to ON+OFF Pixels)
0000	0.0%	0
0001	11.1%	1/9
0010	20.0%	1/5
0011	26.7%	4/15
0100	33.3%	3/9
0101	40.0%	2/5
0110	44.4%	4/9
0111	50.0%	1/2
1000	55.6%	5/9
1001	60.0%	3/5
1010	66.6%	6/9
1011	73.3%	11/15
1100	80.0%	4/5
1101	88.9%	8/9
1110	100.0%	1
1111	100.0%	1

Two of the 16 dither values (shaded in the table) are identical (most intense), which leads to redundancy in the colors.

This redundancy limits the choice to 15 (instead of 16) grayscales and 3375 (instead of 4096) colors. Note that $3375 = 15^3$ which means the equivalent of 15 color scales for each component (R, G, and B).

- ***Active Matrix Technology***

  The dithering logic is always bypassed in active displays. Hence, there is no redundancy introduced at this step, still allowing the choice of the $2^{\text{number of BPP}}$ within the whole 4096 colors.

  Remember that monochrome mode is deliberately not considered in active mode.

Table 5 lists the number of colors/grayscales available on the screen according to both the display technology and the color depth.

Table 5. Number of Colors/Shades of Gray Available on Screen

	Passive Mode (LcdTFT = 0)		Active Mode (LcdTFT = 1)
Number of BPP	**Monochrome (LcdBW = 1)**	**Color (LcdBW = 0)**	**Color Only (LcdBW = 0)**
1	2 palette entries to select within 15 grayscales	2 palette entries to select within 3375 possible colors	2 palette entries to select within 4096 possible colors
2	4 palette entries to select within 15 grayscales	4 palette entries to select within 3375 possible colors	4 palette entries to select within 4096 possible colors
4	16 palette entries to select within 15 grayscales	16 palette entries to select within 3375 possible colors	16 palette entries to select within 4096 possible colors
8	Not relevant since it would consist of 256 palette entries to select within 15 grayscales, but exists anyway	256 palette entries to select 3375 possible colors	256 palette entries to select within 4096 possible colors
12	X	3375 possible colors	4096 possible colors
16	X	3375 possible colors (565 STN = 1)	Up to 65536 possible colors

The Output FIFO

- ***Passive Matrix Technology***

  The LCD controller contains a 2-entry by 8-bit wide output FIFO that is used to store pixel data before it is driven out to the LCD pins. Each time a modulated pixel value is output from the dither generator, it is placed into a serial shifter. The size of the shifter is controlled by programming the color/monochrome select bit (LcdBW) in the control register. The shifter can be configured to be 4 or 8 bits wide. Single-panel monochrome screens use either four or eight data lines; single-panel color screens use eight data pins. Once the correct number of pixels has been placed within the shifter, the value is transferred to the top of the output FIFO. The value is then transferred down until it reaches the last empty location within the FIFO. As values reach the bottom of the FIFO, they are driven out one by one onto the LCD data pins on the edge selected by the invert pixel clock (IPC) bit (see subsection *Invert Pixel Clock (IPC)*).

- ***Active Matrix Technology***

  The output FIFO is bypassed in TFT mode.

LCD Inputs

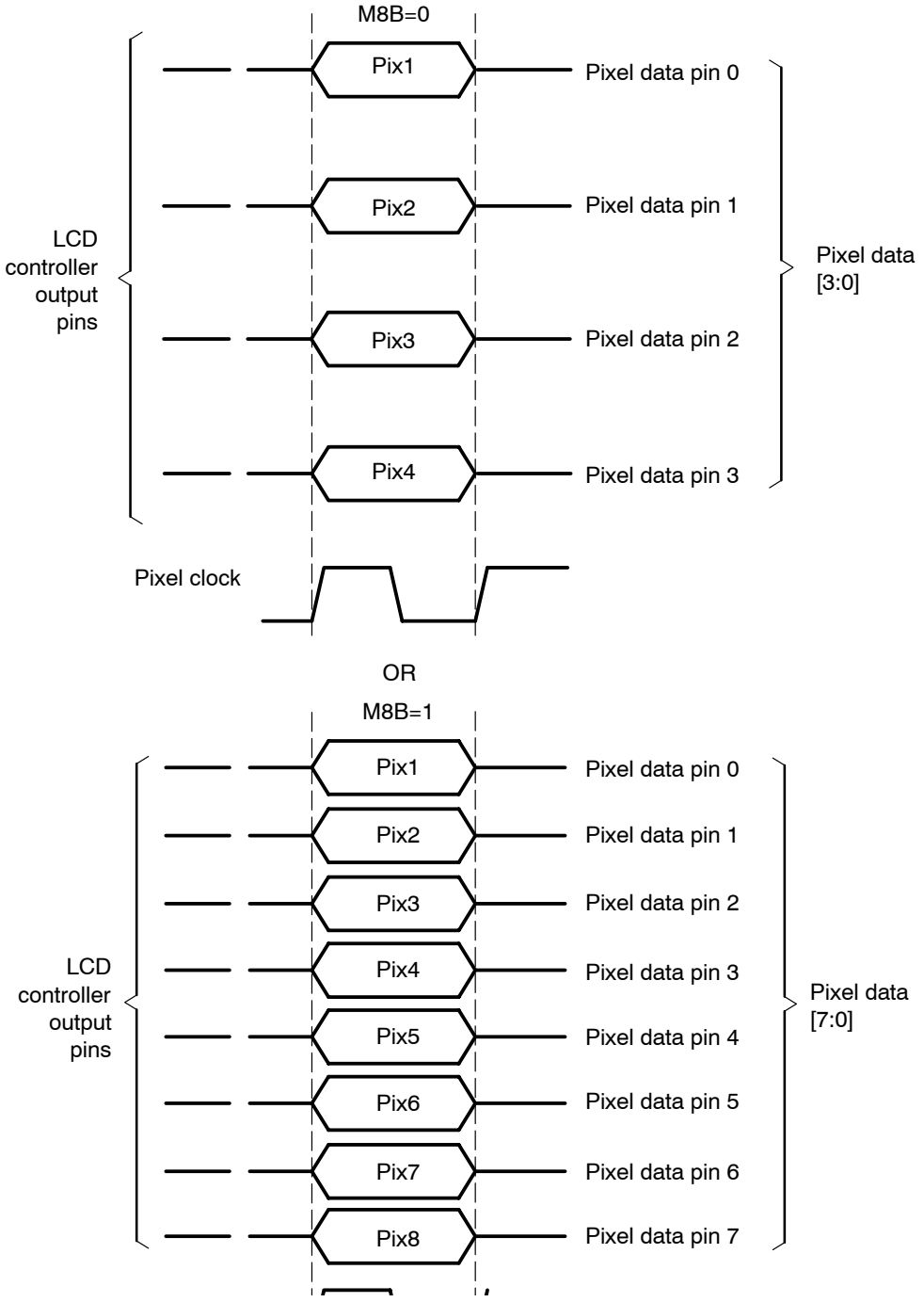
Depending on the type of panel used, the LCD controller is programmed to use either 4-, 8-, 12-, or 16-pixel data output pins. See Table 9, *LCD Controller Data Pin Utilization for Mono/Color Passive/Active Panels.*

- ***Passive Matrix Technology—Monochrome Mode***

  Monochrome displays use 4- or 8-bit data lines, according to the mono 8-bit mode (see subsection *Mono 8 Bit Mode (M8B*). Each line represents one pixel (ON or OFF), which means that at each pixel clock, 4 or 8 pixels, respectively, are sent to the screen.

  Figure 12 shows the passive monochrome mode (IPC = 0, see IPC bit in section 2.3.4, *LCD Timing 2 Register*).

Figure 12. Passive Monochrome Mode



❑ ***Passive Matrix Technology– Color Mode***

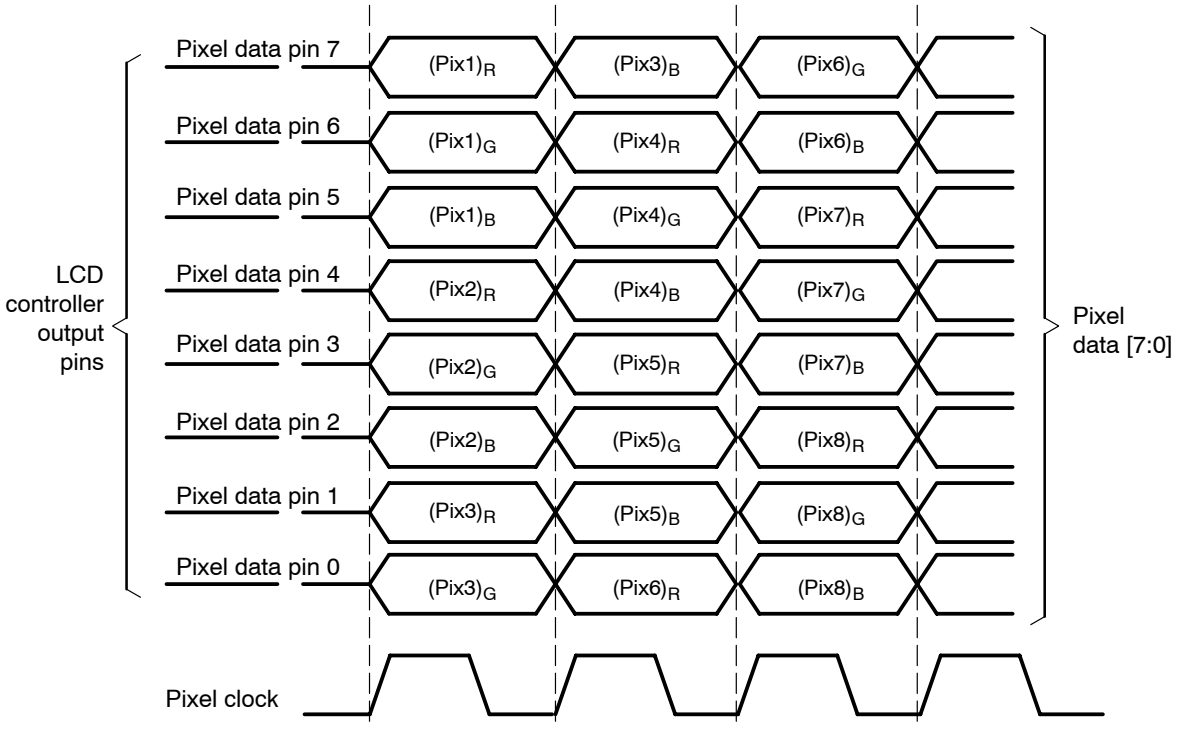
Color passive displays use eight data input lines. Each line represents one color component (red, green, or blue). 2 2/3 pixels are sent to the screen at each pixel clock.

Note:

8 data lines, 1 line per color component, 3 color components per pixel lead to 2 2/3 pixels on 8 data lines.

Figure 13 shows the passive color mode (IPC = 0, see IPC bit in section 2.3.4, *LCD Timing 2 Register*).

Figure 13. Passive Color Mode



After the pixel clock toggles three times, the situation returns to its initial state. At the fourth clock cycle, the figure becomes identical to itself, i.e., the number of pixels displayed is an integer.

- ***Active Matrix Technology***

  In TFT displays, the dithering logic and the output FIFO are always bypassed. This means that data output from the palette is sent directly to the display. In 16-BPP mode, even the palette is bypassed so that data passes directly from the memory to the panel without being processed.

  Consequently, at each pixel clock, only one pixel is sourced to the display.

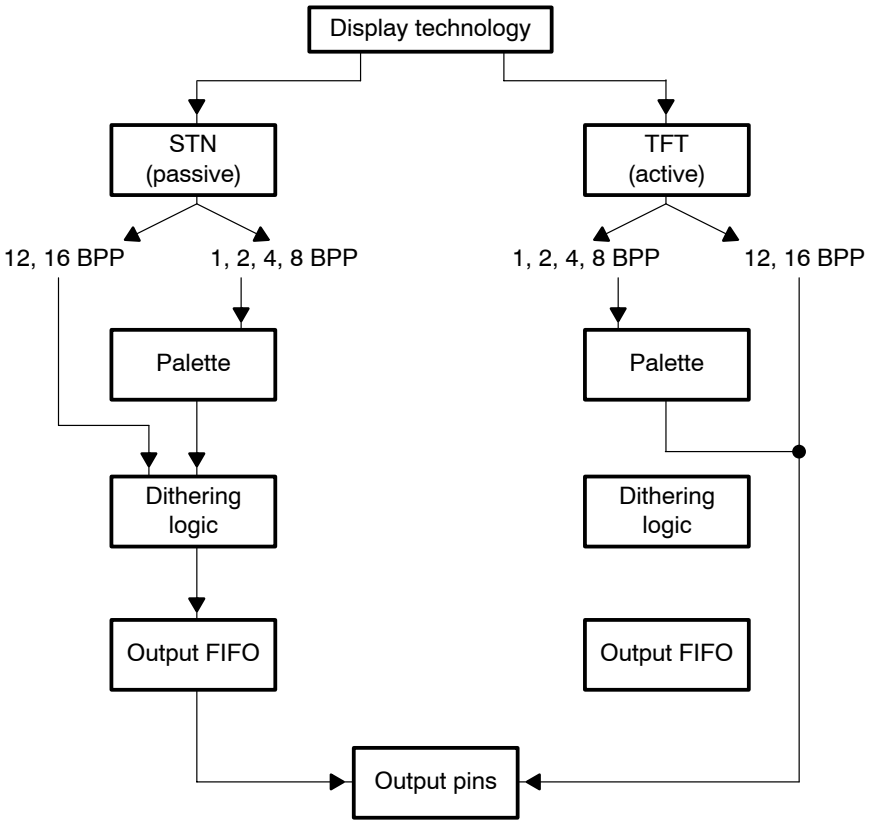
Table 6 is a summary of the number of pixels displayed on the screen at each pixel clock for the different technologies.

Table 6. Number of Pixels Displayed per Pixel Clock

Number of Pixels	Display
1	TFT
2 2/3	STN color
4	Mono 4 bit
8	Mono 8 bit

Figure 14 shows the different data paths depending on the screen technology and the color depth.

Figure 14. LCD Controller Data Paths



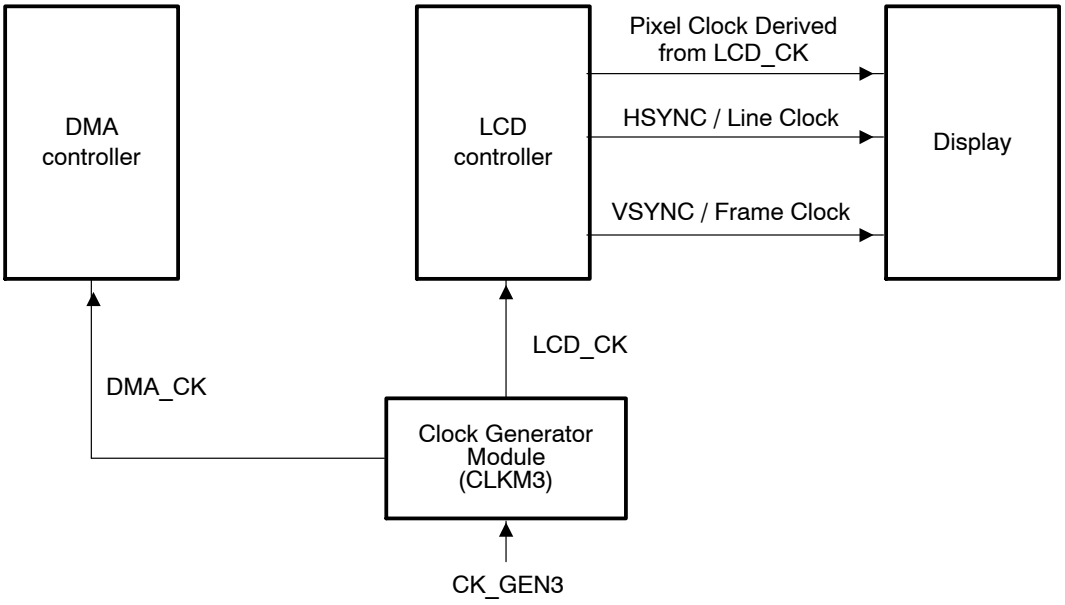
2.2.1 Control Blocks

The previous section explained the data flow from the memory to the LCD panel and the different modules they pass through. The whole process is governed by the registers and timing described in this section.

Timing

This section details the various clocks and signals. Figure 15 shows input and output LCD controller clocks.

Figure 15. Input and Output Clocks



Pixel Clock

The pixel clock frequency is derived from the LCD clock (LCD_CK), which belongs to the traffic controller (TC) domain. It is the output of the on-chip PLL: LCD_CK = (CK_GEN3/1, 2, 4, or 8). See *Multimedia Processor OMAP 3.2 Subsystem Reference Guide (SPRU749)* and *Multimedia Processor Clocks Reference Guide (SPRU751).*

You can program the pixel clock from LCD_CK / 2 to LCD_CK / 255. The divider is called PCD (see subsection *Pixel Clock Divider*).

In any case, the LCD_CK frequency must always be lower than or equal to the TC_CK frequency.

The pixel clock is used by the LCD display to clock the pixel data into the line shift register.

- **Passive Matrix Technology**

  In passive mode, the pixel clock only transitions when valid data is available on the data lines.

  It does not transition during wait state insertion or when the line clock is asserted.

❑ **Active Matrix Technology**

In active mode, the pixel clock transitions continuously as long as the LCD is enabled, depending on the pxl_gated bit in the LCD Control register (see section 2.3.1, *LCD Control Register*). Setting the pxl_gated bit to 1 allows the pixel clock to toggle only when there is valid data to display.

Line Clock (HSYNC)

The line clock toggles after all pixels in a line have been transmitted to the LCD driver and a programmable number of pixel clock wait states has elapsed both at the beginning and end of each line.

For more information, see the section *Horizontal Synchronization Pulse Width*.

❑ **Active Matrix Technology**

The line clock is also used by TFT displays as the horizontal synchronization signal (HSYNC).

The timings of the line clock pins are programmable to support:

❑ Delay insertion both at the beginning and end of each line. See subsection *Horizontal Front Porch (HFP) Bits* and subsection *Horizontal Back Porch (HBP)Bit*.

❑ Line clock polarity. See subsection *Invert HSYNC (IHS) Bit*.

❑ Line clock pulse width, driven on rising or falling edge of pixel clock. See subsection *Horizontal Synchronization Pulse Width (HSW)*, subsection *HSYNC/VSYNC Rise or Fall Programmable (RF)*, and subsection *HSYNC/VSYNC ON or OFF (ON_OFF) Bits*.

Frame Clock (VSYNC)

The frame clock toggles after all lines in a frame have been transmitted to the LCD driver and a programmable number of line clock cycles has elapsed both at the beginning and end of each frame.

For more information, see the section *Vertical Synchronization Pulse Width*.

❑ **Passive Matrix Technology**

In passive mode, the frame clock toggles during the first line of the screen.

- **Active Matrix Technology**

The frame clock occurs between two frames. In active mode, it is asserted at the end of the previous one and after a programmable number of line clock wait states (VFP) has elapsed.

The frame clock is also used by TFT displays as the vertical synchronization signal (VSYNC).

The timings of the frame clock pins are programmable to support:

- Delay insertion both at the beginning and end of each frame. See subsection *Vertical Front Porch (VFP) Bits* and subsection *Vertical Back Porch (VBP) Bits*.
- Frame clock polarity. See subsection *Invert VSYNC (IVS) Bit.*
- Frame clock pulse width, driven on rising or falling edge of pixel clock. See subsection *Vertical Synchronization Pulse Width (VSW),* subsection *Horizontal Synchronization Pulse Width (HSW)*, subsection *HSYNC/VSYNC Rise or Fall Programmable (RF)*, and subsection *HSYNC/VSYNC ON or OFF(ON_OFF) Bits*.

ac-Bias

The ac-bias signal can be configured to transition each time a programmable number of line clocks occurs.

- **Passive Matrix Technology**

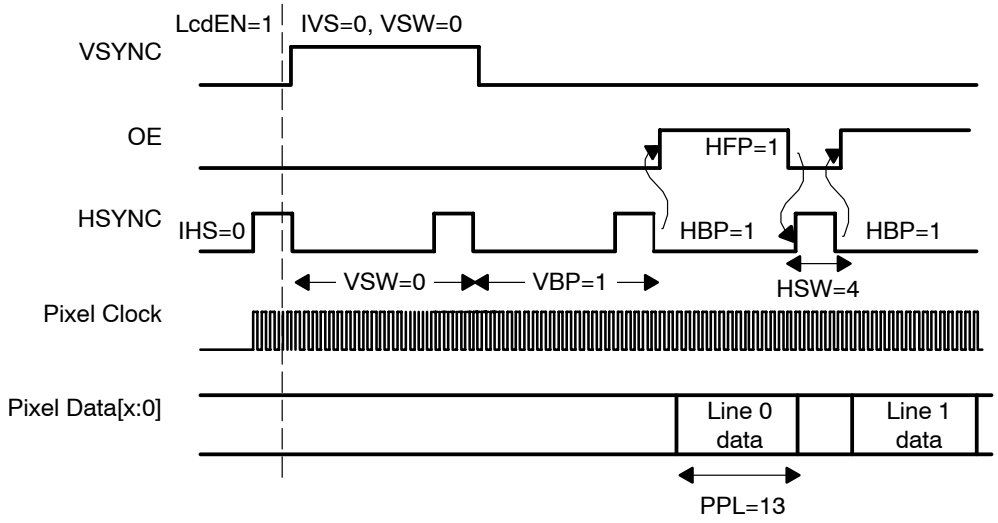
  To prevent a dc charge within the screen pixels, the power and ground supplies of the display are periodically switched. The LCD controller signals the display to switch the polarity by toggling the ac-bias pin.

- **Active Matrix Technology**

  Used in TFT mode, it acts as an output enable to signal when data must be latched from the data pins using the pixel clock.

  Figure 16 shows the different signals toggling in active mode.

Figure 16. Active (TFT) Mode Timing



NOTE: Ensure that HFP, HBP, PPL, and VSW values are programmed to the required value minus 1.

See the register sections, especially sections 2.3.2, *LCD Timing 0 Register*, and 2.3.3*, LCD Timing 1 Register*, for more details on the notations.

2.2.2 Interrupts

Interrupt Sources

Several situations can generate an interrupt:

- ❏ Input and output FIFOs underrun errors
- ❏ Frame synchronization error
- ❏ When the last active frame has completed after the LCD is disabled (maskable)
- ❏ After a programmed number of transitions of the ac-bias pin (passive mode)
- ❏ When the display has reached the user-programmed line number (maskable)
- ❏ VSYNC interrupt after every end of frame (maskable)
- ❏ Palette loading (maskable)

Every hardware-detected event signals an interrupt request to the interrupt controller.

Each interrupt is signaled by a bit in the LCD controller status register. Each of the LCD status bits signals an interrupt request as long as the bit is set. Once the bit is cleared, the interrupt is cleared. Read/write bits are called status bits; read-only bits are called flags. Status bits are referred to as “sticky” (that is, once set by hardware, they must be cleared by software). Read-only flags are set and cleared by hardware; writes have no effect.

Some interrupts are also maskable. For masked bits, see section 2.3.1, *LCD Control Register.*

Note:

A synchronization interrupt occurs if the LCD display information settings that you programmed, such as pixels-per-line, lines per frame, color/monochrome mode, and bits-per-pixel, are not in accordance with the size of the video buffer size programmed in the DMA.

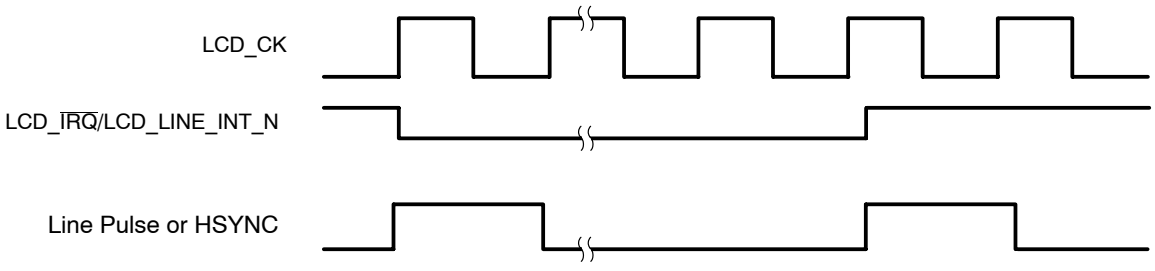
Tearing Effect

A synchronization mismatch between the frame buffer and the display refreshes can lead to images that appear to be torn on the screen.

To avoid this, a synchronization mechanism is needed between the LCD controller and the logical channel (LCh) that updates the frame buffer. For this purpose, a line comparator is implemented in the LCD controller, which delivers an interrupt when the display reaches a predefined line number. This interrupt is a level signal and stays active during the programmed line of the display.

See subsection *Line Interrupt (line_int*). Figure 17 shows the line interrupt output signal behavior for line_int_clr_sel = 1 (see subsection *Line Interrupt Clear Select Bit (line_int_clr_sel)*).

Figure 17. Line Interrupt Output Signal Transitions



Note that lcd_nirq and lcd_line_int_n have the same behavior and are active low signals.

The line interrupt must be connected as a DMA request line to the system DMA. This can then be used by any generic LCh (LCh 0-15) to synchronize a block transfer (BS).

Since all interrupts and DMA request inputs and outputs are brought out to OMAP top level boundary, the DMA request mapping is not predefined. See the chip top-level specification for the exact DMA request mapping.

2.2.3 LCD Subpanel Display Support

Principle

The subpanel display register supports the ability to display only the first or last X lines of the panel and send a fix contents for the others.

This functionality is used for power-saving. To display an image to a small portion of the screen (example: from line 0 to line 15), the data is read from system memory (frame buffer) via the DMA. For line 16 up to line N , where N is the number of lines per panel (LPP), data is read from an LCD register (DPD: default pixel data) instead of through the DMA. By reading into a register, there is no more access to the frame buffer, and power is saved. There is no need to go off-chip and do memory reads. In addition, the DMA can shut off its clocks during this DPD value filling.

For more information on the subpanel functionality, see section 2.3.6, *LCD Subpanel Display Support.*

2.3 Registers

The LCD controller contains eight registers:

- ❏ Four control registers
- ❏ Two status registers (including one display status register)
- ❏ One register related to the subpanel mode
- ❏ One specific register to define the line number where a line interrupt occurs

Table 7 shows the LCD controller registers and their physical addresses.

Table 7. LCD Controller Registers

Name	Offset	Description
LcdControl	0x 00	LCD control register
LcdTiming0	0x 04	LCD timing 0 register
LcdTiming1	0x 08	LCD timing 1 register
LcdTiming2	0x 0C	LCD timing 2 register
LcdStatus	0x 10	LCD status register
LcdSubpanel	0x 14	LCD subpanel display register
LcdLineInt	0x 18	Line interrupt register
LcdDisplayStatus	0x 1C	Display status register

2.3.1 LCD Control Register (LcdControl)

The LCD control register (LcdControl) contains bit-fields to enable/disable the LCD controller to define:

- ❏ The height and width of the screen being controlled
- ❏ Color or monochrome mode
- ❏ Passive or active display
- ❏ Polarity of the control lines
- ❏ Pulse width of the line and frame clocks
- ❏ The pixel clock and ac-bias frequency
- ❏ The number of delays to insert before/after each line and after each frame
- ❏ Interrupt mask bits

An additional control field exists to tune the DMA performance, based on the type of memory system in which the LCD controller is used. This field controls the placement of a minimum delay between each LCD palette request to ensure that enough bus bandwidth is given to other system accesses (see section *FIFO DMA Request Delay*). This field is only used for palette load.

Table 8 describes the LCD control register bits.

Figure 18. LCD Control Register (LcdControl)

Offset: 0h 00 **LCD Control: LCD Control Register** **Read/Write**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved							565 STN	TFT Map	LCD CB1	PLM		FDD			
Reset	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FDD				PXL_GATED	LINE_INT_CLR_SEL	M8B	LCD CB0	Lcd TFT	LINE_INT_MASK	LINE_INT_NIRQ_MASk	LOAD MASK	DONE-MASK	VSYNC_MA	LCD BW	LCD EN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: The reserved bits' reset values are undefined, but reserved bits return 1s when read.

Table 8. LCD Control Register (LcdControl) Bit Descriptions

Bit	Name	Description
24	565 STN	12-BPP (565) mode 0: Off. 1: On (16-bit data in frame buffer, but only 12 bits are dithered and sent out).
23	TFT Map	TFT alternate signal mapping 0: Output pixel data for 1, 2, 4, 8, and 12 BPP modes is right aligned on pixel data [11:0]. 1: Output pixel data for 1, 2, 4, 8, and 12 BPP modes is converted to 5,6,5 format and uses pins [15:0].
22	LCDCB1	LCD control bit 1. Used in conjunction with LCD control bit 0 to control the mapping of pixel data from the frame buffer to the output bus. See Table 10 for the proper settings for this bit.
21:20	PLM	Palette loading mode 00: Palette and data loading 01: Palette loading 10: Data loading 11: Not connected
19:12	FDD	FIFO DMA request delay Encoded value (0-255) used to specify the number of LCD_CK cycles. The input FIFO DMA request must be disabled. The clock count starts after 16 words are read in the input FIFO. Programming FDD=00h disables this function.
11	PXL_GATED	Pixel gated (for TFT mode only) 0: Pixel clock always toggles. 1: Pixel clock only toggles when there is valid data to display.
10	LINE_INT_CLR_SEL	Line interrupt clear select bit 0: TIPB should write 0 to clear line interrupt status register. 1: Line interrupt status register is reset at the end of the line.

Table 8. LCD Control Register (LcdControl) Bit Descriptions (Continued)

Bit	Name	Description
9	M8B	Mono 8-bit mode 0: Pixel data [3:0] is used to output four pixel values to the panel at each pixel clock transition. 1: Pixel data [7:0] is used to output eight pixel values to the panel at each pixel clock transition. This bit is ignored in all other modes.
8	LCDCB0	LCD control bit 0. Used in conjunction with LCD control bit 1 to control the mapping of pixel data from the frame buffer to the output bus. See Table 10 for the proper settings for this bit.
7	LcdTFT	LCD TFT 0: Passive or STN display operation enabled; dither logic is enabled. 1: Active or TFT display operation enabled. External palette and DAC required. Dither logic and output FIFO bypassed. Pin timing changes to support continuous pixel clock, output enable, VSYNC, and HSYNC.
6	line_int_mask	Line interrupt mask (dedicated line) 0: Masks the dedicated line interrupt (line_int), which is connected to the lcd_line_int_n dedicated output line. 1: Mask not active.
5	line_int_nirq_mask	Line interrupt mask 0: The line_int_nirq interrupt is masked. 1: The line_int_nirq interrupt is unmasked.
4	LoadMask	Load mask 0: Masks the loaded palette interrupt, which is connected to the lcd_nirq shared output line. 1: Mask not active.
3	DoneMask	Done mask 0: Masks the frame done (Done) interrupt, which is connected to the lcd_nirq shared output line. 1: Mask not active.
2	VSYNC_mask	LCD VSYNC interrupt mask 0: Interrupt to the lcd_nirq is masked. 1: Interrupt to the lcd_nirq is unmasked.
1	LcdBW	LCD monochrome 0: Color operation enabled. 1: Monochrome operation enabled.
0	LcdEn	LCD controller enable 0: LCD controller disabled. 1: LCD controller enabled.

LCD Enable (LcdEn)

The LCD enable (LcdEn) bit is used to enable and disable all LCD controller operation: When LcdEn=0, the LCD controller is disabled. When LcdEn=1, the LCD controller is enabled.

Note:

You must program all other control bit-fields before setting LcdEn = 1, and must also disable the LCD controller when changing the state of any control bit within the LCD controller.

You can program the LCD control register (LcdControl) last, and configure all twenty-five bit fields at the same time via a word32 write to the register. If you clear LcdEn bit while the LCD controller is enabled, you can complete transmission of the current frame before being disabled. Completion of the current frame is signaled by the LCD controller to the DMA by setting the frame done (Done) bit within the LCD controller status register (see section 2.3.5, *LCD Controller Status Register*), which generates an interrupt request.

If the LCD controller is disabled, the signals on pixel data [15:0] pins are set to 0 and the pixel clock, frame clock, line clock, and ac-bias signals are set to their inactive state. This can be 0 or 1, depending on the inversions programmed in the timing 2 register (see section 2.3.4, *LCD Timing 2 Register*).

LCD Monochrome (LcdBW)

The color/monochrome select (LcdBW) bit is used to determine whether the LCD controller operates in color or monochrome mode. When LcdBW = 0:

- Color mode is selected.
- Palette entries are 12 bits wide, providing up to 4096 colors in active (TFT) mode and up to 3375 colors in passive (STN) color mode (see *Palette*).
- All three dither blocks are used (in passive mode only: LcdTFT = 0), one for each color component (R, G, B).

When LcdBW=1:

- Monochrome mode is selected.
- Palette entries are 4 bits wide *effective* (15 levels of grayscale, see *Palette*).
- 4 or 8 data lines are enabled, according to the mono 8-bit mode (M8B).

Table 9 shows which set of LCD data pins (Pixel Data […]) is used for each mode of operation.

Table 9. LCD Controller Data Pin Utilization for Mono/Color Passive/Active Panels

Color/Mono BPP	Passive/Active Panel	Pins
Mono 1, 2, 4	Passive	Pixel data [3:0]
Mono 8	Passive	Pixel data [7:0]
Color 1,2,4,8,12, 16 (565 STN = 1)	Passive	Pixel data [7:0]
Color 1,2,4,8,12	Active	Pixel data [11:0] or pixel data [15:0] according to TFT map bit in LCD control register
Color 16	Active	Pixel data [15:0]

Note:

Unused pixel data bits always remain low.

LCD Vertical Synchronization Mask (VSYNC_mask)

The LCD VSYNC_mask masks the VSYNC interrupt in the status register going to the lcd_nirq when VSYNC_mask bit is 0. When it is 1, the VSYNC bit affects the lcd_nirq. (See subsection *VSYNC Interrupt*.)

LCD Done Mask (DoneMask)

The LCD done mask (DoneMask) bit masks the path between the frame done interrupt and lcd_nirq, see subsection *Frame Done (Read-Only)*.

When DoneMask = 0, the frame done interrupt is masked.

When DoneMask = 1, the frame done interrupt is not masked.

LCD Loading Mask (LoadMask)

The LCD loading mask (LoadMask) bit masks the path between the palette loading interrupt signal in the LCD status register, and lcd_nirq.

When LoadMask = 0, the loading interrupt is masked.

When LoadMask = 1, the loading interrupt is not masked.

Line Interrupt Mask (line_int_nirq_mask)

This line_int_nirq_mask bit masks the path going to the shared interrupt (lcd_nirq).

When line_int_nirq_mask = 0, the path between the line interrupt and lcd_nirq (shared line) is masked. When line_int_nirq_mask = 1, it is unmasked: any interrupt, among those who share the lcd_nirq output line, can occur, including the line interrupt when the display reaches the programmed line number.

Line Interrupt Mask (Dedicated Line) (line_int_mask)

This line_int_mask bit masks or unmasks the connection to the dedicated top-level entity signal lcd_line_int_n, which is set to 0 when the display reaches the user-programmed line number. (See subsection *Line Interrupt,* and Figure 33, *Line Interrupt Path*).

When line_int_mask = 0, the connection is masked.

When line_int_mask = 1, the connection is unmasked.

Note:

When this bit is disabled, the line_int still can be used as source to generate lcd_nirq.

LCD TFT (LcdTFT)

The LCD TFT (LcdTFT) bit selects whether the LCD controller operates in passive (STN) or active (TFT) display control mode.

When LcdTFT = 0, passive or STN mode is selected. LCD data flows from the frame buffer memory, via the LCD dedicated DMA channel, to the palette (the palette is bypassed for 12 and 16 BPP modes) to the dithering logic and the output FIFO before being output on the LCD data pins.

Figure 19 and Figure 20 describe the clocks and data pin behaviors in monochrome and color passive modes, respectively.

Figure 19. Monochrome Passive Mode Pixel Clock and Data Pin Timing

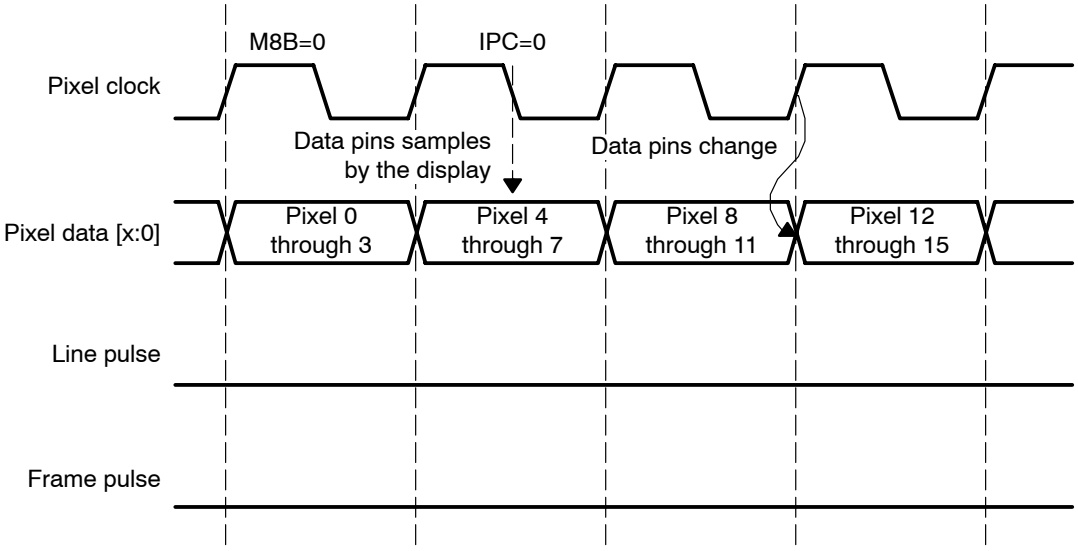
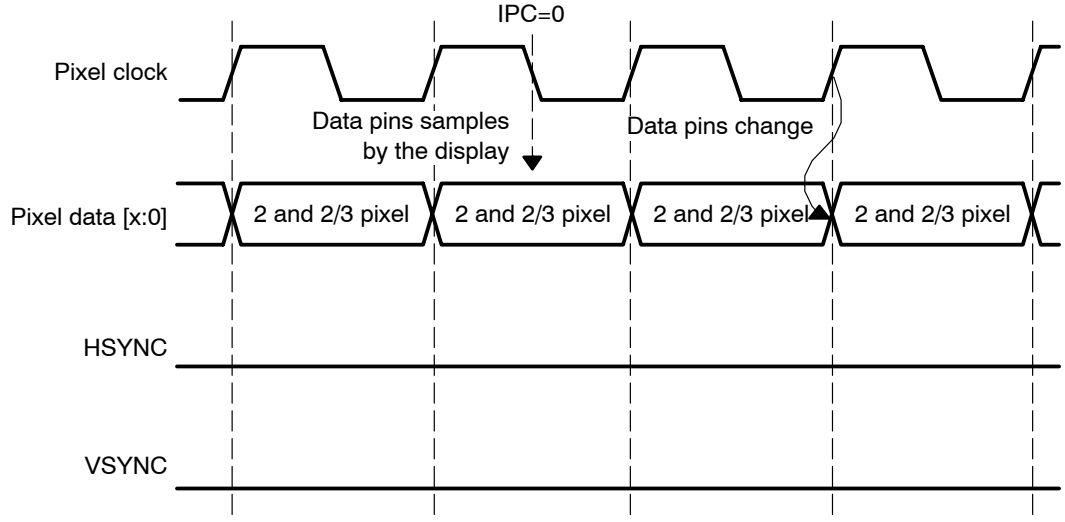


Figure 20. Color Passive Mode Pixel Clock and Data Pin Timing



When LcdTFT = 1, active or TFT mode is selected.

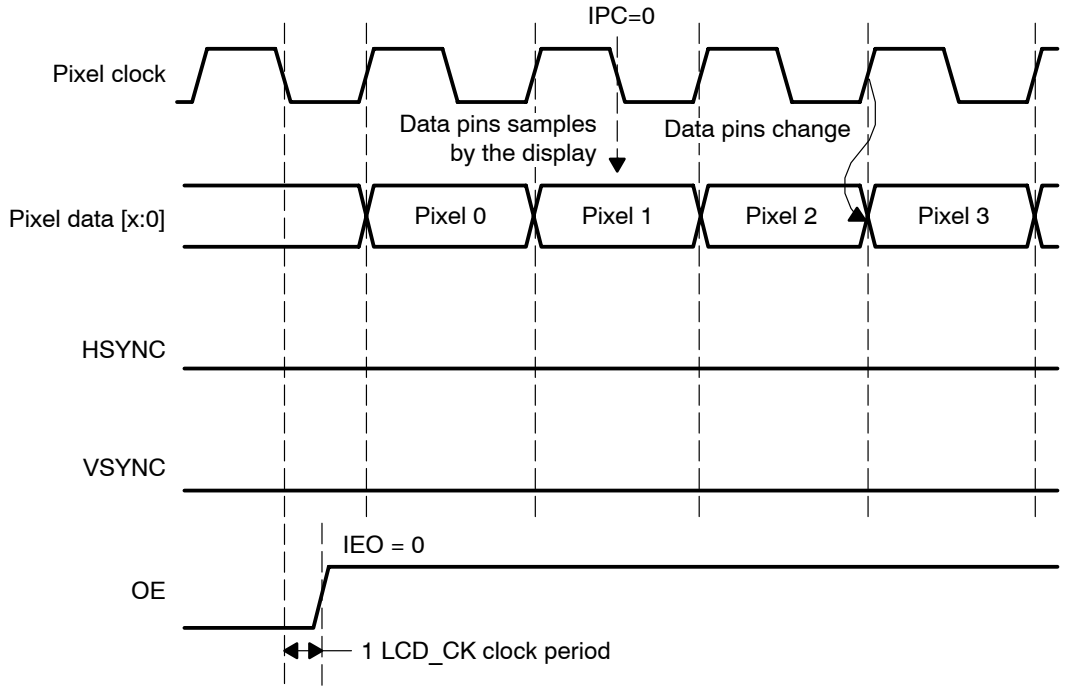
Video data is transferred via the DMA from memory to the input FIFO, then is unpacked and used to select an entry from the palette (for 1, 2, 4, and 8 bits-per pixel modes), just as in passive mode.

The value read from the palette, however, bypasses both the LCD dither logic and the output FIFO to be output on the LCD data pins in TFT mode. The pixel size within the frame buffer is increased to 16 bits when 12- or 16-bit pixel encoding mode is enabled (BPP=1XX).

Remember that the palette is bypassed in 12 BPP for passive mode and 16 BPP for active mode The palette is also bypassed in 12 BPP TFT, because it is derived from the 16 BPP mode. See Figure 14, *LCD Controller Data Paths*.

Figure 21 describes the clocks and data pin behaviors in active mode.

Figure 21. Active Mode Pixel Clock and Data Pin Timing



The size of the pixel encoding is increased in TFT mode because the LCD dither logic is bypassed, i.e., the dither logic only supports 4 bits to encode each color component R, G, B that limits the pixel encoding size in passive mode. Increasing the size of the pixel representation allows a total of 64K colors to be addressed using an off-chip palette in conjunction with the LCD controller.

LCD Control Bit 0 (LCDCB0)

Bit LCDCB0, together with LCDCB1, controls the mapping of graphics data on the output pins. Table 10 shows the settings required for each graphics mode.

Table 10. Control Bit 0 and Control Bit 1 Mapping by Display Types

Display Type	Mode	Control bit 0	Control Bit 1
Passive monochrome	1 BPP	0	1
	2 BPP	0	1
	4 BPP	0	1
	8 BPP	0	0
Passive color	2 BPP	0	1
	4 BPP	0	1
	8 BPP	0	0
	12 BPP	0	0
	16 BPP	0	0
TFT	2 BPP	0	1
	4 BPP	0	1
	8 BPP	0	0
	12 BPP	0	0
	16 BPP	0	0

Mono 8 Bit Mode (M8B)

The mono 8-bit mode (M8B) bit selects whether four or eight data lines are used to output pixel data to the LCD screen. When M8B = 0, pixel data [3:0] is used to output four pixel values to the LCD panel at each pixel clock transition. When M8B = 1, pixel data [7:0] is used to output eight pixel values to the LCD panel at each pixel clock transition.

Note:

M8B does not affect any of the color modes or TFT.

Line Interrupt Clear Select Bit (line_int_clr_sel)

The line_int_clr_sel bit selects between two methods that clear the bit in the status register. You can select either an automatic clear or a TIPB write. When line_int_clr_sel = 0, write 0 in the line_int status bit to clear the interrupt. When line_int_clr_sel = 1, the line interrupt bit in the status register is reset at the end of the programmed line.

Gated Pixel Clock (pxl_gated)

The pxl_gated bit selects between gated or not gated pixel clock when in TFT mode.

When pxl_gated = 0, the pixel clock always toggles.

When pxl_gated = 1, the pixel clock does not toggle when there is not valid data to display. This is a power saving option.

FIFO DMA Request Delay (FDD)

The 8-bit FIFO DMA request delay (FDD) field is used to select the minimum number of LCD_CK cycles to wait between the servicing of each DMA request issued by the LCD controller, sending an address to the input FIFO.

The goal is to ensure enough bandwidth to other system accesses. A delay of FDD cycles is inserted for every 16 words read from the input FIFO. This function is a concern only in 8 BPP mode, where the palette is 256 words.

When FDD = 00h, the FIFO DMA request delay function is disabled. This function is only used for palette loading.

Palette Loading (PLM)

The 2-bit palette loading field describes how the palette loading behaves when each new frame is loaded from memory.

- In 00 mode, the data in the frame buffer represents the palette data and the picture data. Both palette and picture data are loaded.
- 01 is the palette-only mode. The data in the frame buffer just represents a new palette to be loaded. This data is loaded and placed into the palette. Be sure to turn off the LCD after getting the loading interrupt, or the LCD behavior will be unpredictable.
- When in data loading mode (PLM = 10), the data in the frame buffer only represents the picture data (data-only). This data is then used as an index (in the palette) or sent directly out. This mode assumes the palette was previously loaded. There is no need to keep loading the palette if it is not changing. As a matter of fact, in data-only mode, the BPP is fixed and can not change on the fly since the palette is not loaded at every frame.
- 11 mode is reserved.

LCD Control Bit 1 (LCDCB1)

The LCD control bit 1 is used in conjunction with LCD control bit 0 to control the mapping of pixel data from the frame buffer to the output bus.

Refer to Table 10 for the appropriate settings for these bits.

TFT Alternate Signal Mapping (TFT Map)

This bit is relevant only if LcdTFT = 1.

This bit field controls how the TFT pixel data is output. Via this feature, 12-BPP data can be output to all 16-bit LCD pins (this also applies to 1-, 2-, 4-, and 8-BPP). This feature allows you to switch BPP modes on the fly, duplicating the 12-bit output data across the 16 data lines if they are already hardwired to the 16 data lines.

Figure 22 shows how the four red, four green, and four blue bits are mapped to all pixel data [15:0] output pins when this bit is set to 1.

Figure 22. TFT Alternate Signal Mapping Output

Pins	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data	R3	R2	R1	R0	R3	G3	G 2	G1	G0	G 3	G2	B3	B2	B1	B0	B3

When this bit is 0, the four red, four green, and four blue data are right aligned on pixel data [11:0]. The upper pixel data [15:12] are set to 0. There is no duplication.

16 BPP STN Mode (565 STN)

This bit is relevant only if LcdTFT = 0, but has no effect in 1-, 2-, 4- and 8-BPP modes.

If 565 STN = 0, the frame buffer organization is in 12 BPP mode. In this mode, each color component is encoded in 4 bits, as shown in Table 11.

Table 11. 12-Bit STN Data in Frame Buffer

Unused				**Red**				**Green**				**Blue**			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data ignored				R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

If 565 STN = 1, the 16 BPP STN mode is selected. The only difference between this mode and the 12-BPP mode is how the pixel data is organized in the frame buffer and which bits are sent to the dither logic.

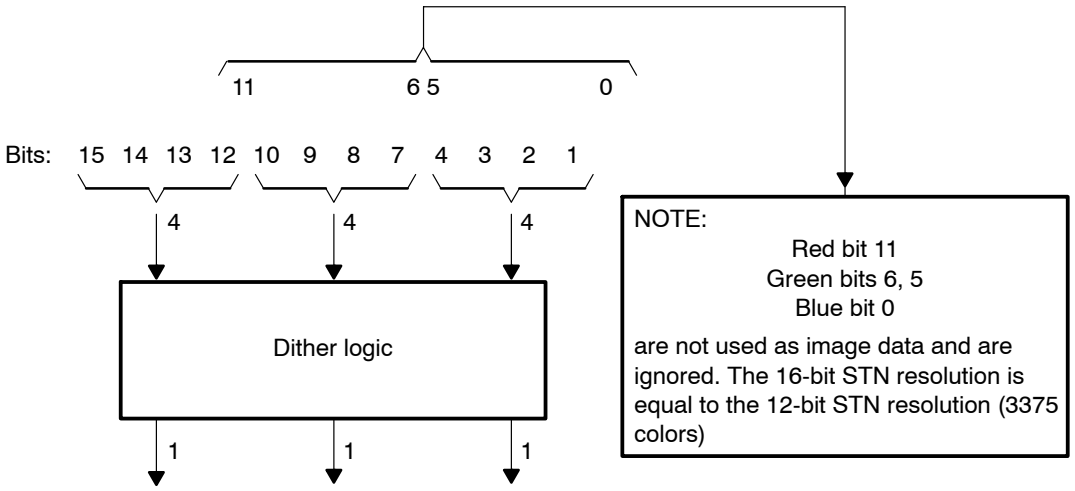
16 bit STN mode appears in the frame buffer memory as shown in Table 12.

Table 12. 16-Bit STN Data in Frame Buffer

Red					**Green**						**Blue**				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Nevertheless, 16-bit STN mode only sends 12 bits to the dithering logic as well as the 12-BPP STN mode. The LSB bit of the red component (bit 11), the two LSBs of green (bits 6 and 5), and the LSB of blue (0) are not sent to the dithering logic.

Figure 23. 16 BPP STN Mode



This 12-BPP (5-6-5) mode can be used if the operating system does not support 12 BPP in the frame buffer. Data is arranged in 16 BPP instead, but only 12 bits are dithered and sent to the display.

2.3.2 LCD Timing 0 Register (LcdTiming0)

LCD timing 0 register (LcdTiming0) contains four bit-fields that are used as modulus values for a collection of down counters. This register controls HSYNC-signal generation.

Figure 24. LCD Timing 0 Register (LcdTiming0)

Offset: 0x 04 **LcdTiming0: LCD Timing 0 Register** **Read/Write**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	HBP								HFP							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSW						PPL									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Table 13. LCD Timing 0 Register (LcdTiming0) Bit Descriptions

Bit	Name	Description
31:24	HBP	Horizontal back porch The encoded value (from 1−256) used to specify the number of pixel clock periods to add to the beginning of a line transmission before the first set of pixels is output to the display *(program to value required minus 1).* Note that pixel clock is held in its inactive state during the beginning of line wait period in passive display mode and is permitted to transition in active display mode.
23:16	HFP	Horizontal front porch The encoded value (from 1−256) used to specify the number of pixel clock periods to add to the end of a line transmission before line clock is asserted *(program to value required minus 1).* Note that pixel clock is held in its inactive state during the end of line wait period in passive display mode and is permitted to transition in active display mode.
15:10	HSW	Horizontal synchronization pulse width The encoded value (from 1−64) used to specify the number of pixel clock periods to pulse the line clock at the end of each line *(program to value required minus 1).* Note that pixel clock is held in its inactive state during the generation of the line clock in passive display mode and is permitted to transition in active display mode.
9:0	PPL	Pixels per line The encoded value (from 16−1024) used to specify the number of pixels contained within each line on the LCD display *(program to value required minus 1).*

Pixels-Per-Line (PPL)

The pixels-per-line (PPL) bit-field is used to specify the number of pixels in each line on the screen. It represents the screen width. PPL is a 10-bit value. Taking into account that the bottom 4 bits of this register are not used and always read 1, it is possible to support displays in which the number of pixels-per-line ranges between 16 and 1024. PPL is used to count the correct number of pixel clocks that must occur before the line clock can be pulsed.

Notes:

PPL must be programmed to the value required minus 1 (0x27F for a 640-pixel-per-line LCD panel).

PPL must be a multiple of 16 pixels.

Horizontal Synchronization Pulse Width (HSW)

The 6-bit horizontal synchronization pulse width (HSW) field is used to specify the pulse width of the line clock in passive mode, or horizontal synchronization pulse in active mode. The line clock (or HSYNC) is asserted each time a line or row of pixels is output to the display and a programmable number of pixel clock delays have elapsed. When line clock is asserted, the value in HSW is transferred to a 6-bit down counter that uses the programmed pixel clock frequency to decrement. When the counter reaches zero, the line clock is negated. HSW can be programmed to generate a line clock pulse width ranging from 1–64 pixel clock periods (program to value required minus 1).

Note:

The pixel clock does not transition during the line clock pulse in passive display mode, but it transitions in active display mode.

Horizontal Front Porch (HFP)

The 8-bit horizontal front porch (HFP) field is used to specify the number of dummy pixel clocks to insert at the end of each line or row of pixels before pulsing the line clock pin. Once a complete line of pixels is transmitted to the LCD driver, the value in HFP is used to count the number of pixel clocks to wait before pulsing the line clock. HFP generates a wait period ranging from 1–256 pixel clock cycles (program to value required minus 1).

Note:

The pixel clock does not transition during these dummy pixel clock cycles in passive display mode, but it transitions continuously in active display mode.

Horizontal Back Porch (HBP)

The 8-bit horizontal back porch (HBP) field is used to specify the number of dummy pixel clocks to insert at the beginning of each line or row of pixels. After the line clock for the previous line has been negated, the value in HBP is used to count the number of pixel clocks to wait before starting to output the first set of pixels in the next line. HBP generates a wait period ranging from 1–256 pixel clock cycles (program to value required minus 1).

Note:

The pixel clock does not transition during these dummy pixel clock cycles in passive display mode, but it transitions continuously in active display mode.

2.3.3 LCD Timing 1 Register (LcdTiming1)

LCD timing 1 register (LcdTiming1) contains four bit-fields that are used as modulus values for a collection of down counters. This register controls VSYNC-signal generation.

Figure 25. LCD Timing 1 Register (LcdTiming1)

Offset: 0h 08 **LcdTiming1: LCD Timing 1 Register** **Read/Write**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VBP								VFP							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VSW						LPP									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 14. LCD Timing 1 Register (LcdTiming1) Bit Descriptions

Bit	Name	Description
31:24	VBP	Vertical back porch The value (from 0–255) used to specify the number of line clock periods to add to the beginning of a frame before the first set of pixels is output to the display. Note that line clock transitions during the insertion of the extra line clock periods.
23:16	VFP	Vertical front porch The value (from 0–255) used to specify the number of line clock periods to add to the end of each frame. Note that the line clock transitions during the insertion of the extra line clock periods.
15:10	VSW	Vertical synchronization pulse width In active mode (LcdTFT=1), the encoded value (from 1–64) used to specify the number of line clock periods *(program to value required minus 1)* to pulse the frame clock (VSYNC) pin at the end of each frame *after* the end of frame wait (VFP) period elapses. The frame clock is used as VSYNC signal in active mode. In passive mode (LcdTFT=0), the encoded value (from 1–64) used to specify the number of extra line clock periods to insert *after* the vertical front porch (VFP) period has elapsed. Note that the width of the frame clock (VSYNC) is not affected by VSW in passive mode, and that the line clock transitions during the insertion of the extra line clock periods *(program to value required minus 1).*
9:0	LPP	Lines per panel The encoded value (from 1–1024) used to specify the number of lines per panel. It represents the total number of lines on the LCD.

Lines Per Panel (LPP)

The lines per panel (LPP) bit-field is used to specify the number of lines or rows per LCD panel being controlled. It represents the total number of lines for the entire LCD display (the screen height). LPP is a 10-bit value, which represents between 1−1024 lines per panel. LPP is used to count the correct number of line clocks that must occur before the frame clock can be pulsed.

Note:

LPP must be programmed to the value required minus 1 (0xC7 for 200 lines per panel).

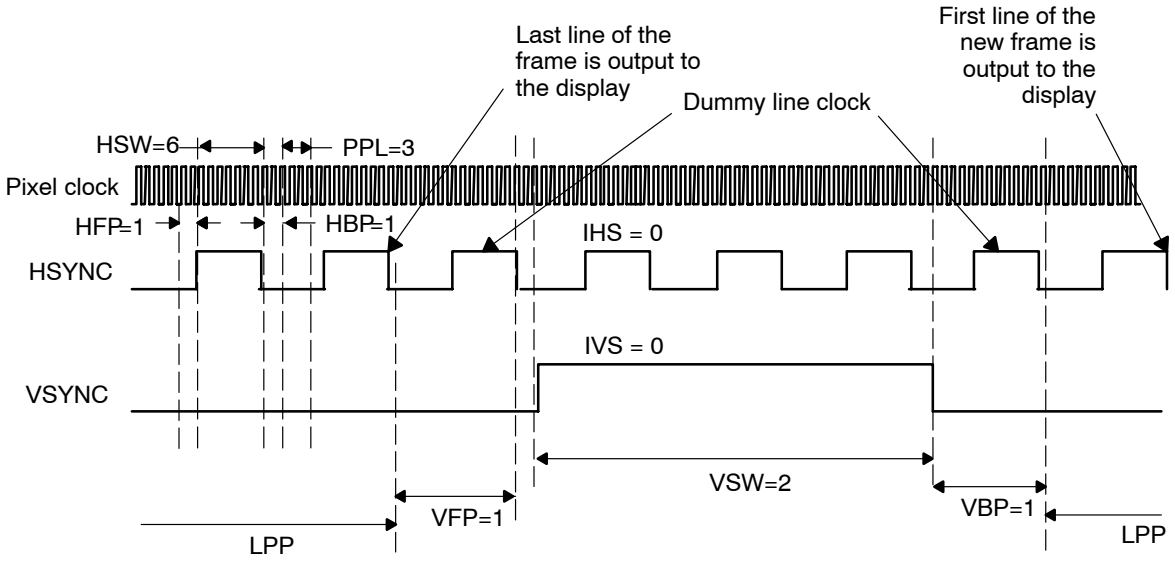
Vertical Synchronization Pulse Width (VSW)

The 6-bit vertical synchronization pulse width (VSW) field is used to specify the pulse width of the vertical synchronization pulse in active mode or is used to add extra dummy line clock cycles between the vertical front porch and vertical back porch in passive mode.

- Active matrix technology

  In active mode (LcdTFT=1), VSYNC is asserted each time the last line or row of pixels from the previous frame is output to the display and a programmable number of line clock delays (VFP) has elapsed. When the frame clock (VSYNC) is asserted, the value in VSW is transferred to a 6-bit down counter that uses the line clock frequency to decrement. When the counter reaches zero, the frame clock (VSYNC) is negated. VSW can be programmed to generate a vertical synchronization pulse width ranging from 1−64 line clock periods (program to value required minus 1, see Figure 26). The following frame starts after VSYNC is deasserted and a programmable number of line clock delays (VBP) has elapsed.

Figure 26. Active Matrix Timing



NOTE: Remember that most of the parameters (HSW, HFP, PPL, HBP) must be programmed to value required minus 1.

- Passive matrix technology

  In passive mode (LcdTFT=0), VSW does not affect the timing of the frame clock, but instead can be used to add extra line clock cycles between the end and beginning of frame line clock cycle counts. The total number of line clock cycles that are inserted between each frame is equal to the sum of the values in VFP, VSW, and VBP. A counter is used to insert dummy line clock cycles between frames by first using the value in VFP, then VSW, then VBP. You must ensure that the sum of the values in the three fields is equal to the total number of line clock cycles that are needed between frames.

  The LCD controller frame clock pin is asserted on the rising-edge of the first pixel clock for each frame. The frame clock remains asserted for the remainder of the first line as pixels are output to the display, also during the assertion of the first line clock for the frame, and then negated on the rising-edge of the first pixel clock of the second line of each frame.

Note:

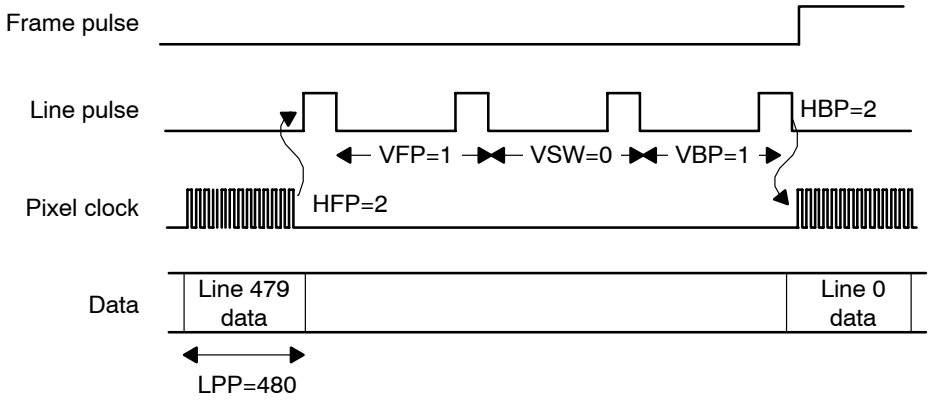
The pixel clock does not transition during the whole dummy line clock periods that are inserted in passive mode before the frame pulse.

The line clock does transition during the insertion of the dummy line clock cycles. VSW must be long enough to load the palette.

Vertical Front Porch (VFP)

The 8-bit vertical front porch (VFP) field is used to specify the number of line clocks to insert at the end of each frame. Once a complete frame of pixels is transmitted to the LCD display, the value in VFP is used to count the number of line clock periods to wait. After the count has elapsed, the VSYNC signal is pulsed in active mode or extra line clocks are inserted as specified by the VSW bit-field in passive mode. VFP generates from 0–255 line clock cycles (see Figure 27).

Figure 27. Passive Mode End of Frame Timing



NOTE: Remember that VSW must be programmed to value required minus 1.

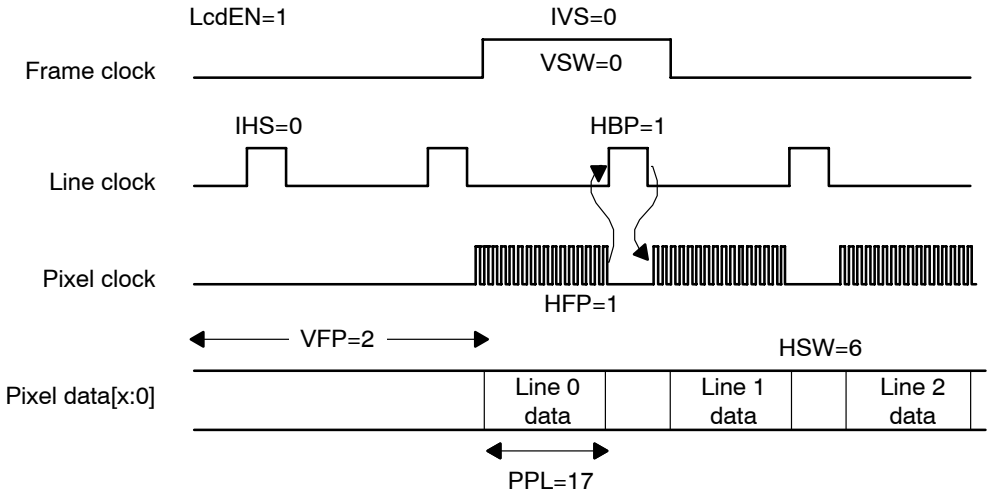
Note:

The line clock transitions during the generation of the VFP line clock periods.

Vertical Back Porch (VBP)

The 8-bit vertical back porch (VBP) field is used to specify the number of line clocks to insert at the beginning of each frame. The VBP count starts just after the VSYNC signal for the previous frame has been negated for active mode, or the extra line clocks have been inserted as specified by the VSW bit-field in passive mode. After this has occurred, the value in VBP is used to count the number of line clock periods to insert before starting to output pixels in the next frame. VBP generates from 0–255 extra line clock cycles (see Figure 28).

Figure 28. Passive Mode Beginning of Frame Timing



Note:

The line clock transitions during the generation of the VBP line clock wait periods. Note also that you must adjust the value of VBP, to allow enough line clock cycles to elapse; this allows the palette to be completely filled via the DMA, and allows a sufficient number of encoded pixel values to be input from the frame buffer, processed by the dither logic, then placed in the output FIFO, ready to be output to the LCD data lines.

2.3.4 LCD Timing 2 Register (LcdTiming2)

The LCD timing 2 register (LcdTiming2) contains nine different bit-fields that are used to control various functions associated with the timing of the LCD controller.

Figure 29. LCD Timing 2 Register (LcdTiming2)

Offset: 0h 0C **LcdTiming2: LCD Timing 2 Register** **Read/Write**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved						ON_OFF	RF	IEO	IPC	IHS	IVS	ACBI			
Reset	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ACB								PCD							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15. LCD Timing 2 Register (LcdTiming2) Bit Descriptions

Bit	Name	Description
31-26	-	Reserved
25	ON_OFF	HSYNC/VSYNC pixel clock control on/off (should be ON only when in TFT mode) 0: Line clock (HSYNC) and frame clock (VSYNC) are driven on opposite edges of pixel clock than the pixel data. 1: Line clock (HSYNC) and frame clock (VSYNC) are driven according to bit 24.
24	RF	Program HSYNC/VSYNC RISE OR FALL 0: Line clock (HSYNC) and frame clock (VSYNC) are driven on falling edge of pixel clock, bit 25 must be set to 1. 1: Line clock (HSYNC) and frame clock (VSYNC) are driven on rising edge of pixel clock, bit 25 must be set to 1.
23	IEO	Invert output enable 0: ac-bias pin is active high in active display mode. 1: ac-bias pin is active low in active display mode. Active display mode: Data is driven out to the LCD data lines on programmed pixel clock edge when ac-bias is active,according to the IPC bit (see subsection *Invert Pixel Clock (IPC)*. Note that IEO is ignored in passive display mode.
22	IPC	Invert pixel clock 0: Data is driven on the LCD data lines on the rising-edge of the pixel clock. 1: Data is driven on the LCD data lines on the falling-edge of the pixel clock.
21	IHS	Invert HSYNC 0: Line clock (HSYNC) pin is active high and inactive low. 1: Line clock (HSYNC) pin is active low and inactive high. Active and passive mode: Horizontal synchronization pulse/line clock is active between lines, after end of line wait period.
20	IVS	Invert VSYNC 0: Frame clock (VSYNC) pin is active high and inactive low. 1: Frame clock (VSYNC) pin is active low and inactive high. Active mode: Vertical synchronization pulse is active between frames and after the end of the frame wait period. Passive mode: Frame clock is active during first line of each frame.
19:16	ACBI	ac-bias pin transitions per interrupt Value (from 0 to 15) used to specify the number of ac-bias pin transitions to count before setting the ac-bias count status bit signaling an interrupt request. The counter is frozen when bit ABC is set and is restarted when bit ABC is cleared by software. This function is disabled when ACBI=0x0000. This bit is only relevant in passive mode because it is used as an output enable in active mode. See subsection *Invert Output Enable (IEO)*. In active mode, this bit is ignored.

Table 15. LCD Timing 2 Register (LcdTiming2) Bit Descriptions (Continued)

Bit	Name	Description
15:8	ACB	ac-bias pin frequency (program to value required minus 1) Value (from 1 to 256) used to specify the number of line clocks to count before transitioning the ac-bias pin. This pin is used to periodically invert the polarity of the power supply to prevent dc charge build-up within the display. ACB = Number of line clocks/toggle of the ac-bias pin. This bit is relevant in passive mode because ac-bias is used as an output enable in active mode. In active mode, this bit is ignored.
7:0	PCD	Pixel clock divisor Value (from 2–255) used to specify the frequency of the pixel clock based on the LCD_CK frequency. Pixel clock frequency can range from LCD_CK /2 to LCD_CK /255. Pixel clock frequency = LCD_CK/PCD.

Pixel Clock Divider (PCD)

The 8-bit pixel clock divider (PCD) field is used to select the frequency of the pixel clock. PCD can generate a range of pixel clock frequencies from LCD_CK/2 to LCD_CK/255, where LCD_CK is derived from CK_GEN3 (see section *Timing)*. The pixel clock frequency must be adjusted to meet the required screen refresh rate. The refresh rate depends on:

- ❏ The number of pixels for the target display
- ❏ Whether monochrome or color mode is selected
- ❏ The number of pixel clock delays programmed at the beginning and end of each line
- ❏ The number of line clocks inserted at the beginning and end of each frame
- ❏ The width of the VSYNC signal in active mode or VSW line clocks inserted in passive mode
- ❏ The width of the line clock or HSYNC signal

All of these factors alter the duration of one frame transmission to the next. Different display manufacturers require different frame refresh rates, depending on the physical characteristics of the display. PCD is used to alter the pixel clock frequency in order to meet these requirements. Pixel clock is used to synchronously signal the device to drive data to the LCD data pins, and to signal the output FIFO to latch the data from the pins. The frequency of the pixel clock for a set PCD value or the required PCD value to yield a target pixel clock frequency can be calculated using the following equation:

PixelClock =LCD_CK / PCD

The pixel clock frequency is programmed taking into account the limitations shown in Table 16.

Table 16. Pixel Clock Frequency Programming Limitations

Type of Screen	Output (in Bits)	Min. Pixel Clock Divider
TFT 1, 2, 4, 8 BPP	12 (1 pixel)	2
TFT 12, 16 BPP	16 (1 pixel)	2
STN monochrome	4 (4 pixels)	4
STN monochrome	8 (8 pixels)	8
STN color	8 (2 2/3 pixels)	3

Note:

If PCD equals 0 or 1, the effect is undefined. Dividing the pixel clock frequency by an odd number distorts the duty cycle.

ac-Bias Pin Frequency (ACB)

The 8-bit ac-bias frequency (ACB) field is used to specify the number of line clock periods to count between each toggle of the ac-bias pin. After the LCD controller is enabled, the value in ACB is loaded to an 8-bit down counter, and the counter begins to decrement using the line clock. When the counter reaches zero it stops, the state of ac-bias pin is reversed, and the whole procedure starts again. The number of line clocks between each ac-bias pin transition ranges from 1–256 (program to value required minus 1). This line is used by the LCD display to periodically reverse the polarity of the power supplied to the screen to eliminate DC offset.

Note:

The ACB bit field has no effect in active mode. This is due to the fact that the pixel clock transitions continuously in active mode (when pixel_gated = 0); the ac-bias line is used as an output enable signal. The ac-bias is asserted by the LCD controller in active mode; this occurs whenever pixel data is driven out to the data pins to signal to the display when it can latch pixels using the pixel clock.

ac-Bias Line Transitions Per Interrupt (ACBI)

The 4-bit ac-bias line transitions per interrupt (ACBI) field is used to specify the number of line transitions to count before setting the ac-bias count status (ABC) bit in the LCD controller status register, which signals an interrupt request. After the LCD controller is enabled, the value in ACBI is loaded to a 4-bit down counter, and the counter decrements each time the ac-bias line state is inverted. When the counter reaches zero it stops, and the ac-bias count (ABC) bit is set in the status register. Once ABC is set, the 4-bit down counter is reloaded with the value in ACBI, and is disabled until ABC is cleared. Once ABC is cleared by the CPU, the down counter is enabled, and again decrements each time the ac-bias line is flipped. The number of ac-bias line transitions between each interrupt request ranges from 0 to 15. Programming ACBI = 0h0000 disables the ac-bias line transitions per interrupt function.

Note:

For the same reasons as in the previous section, this bit-field has no effect in active mode.

Invert VSYNC (IVS)

The invert VSYNC (IVS) bit is used to invert the polarity of the frame clock (VSYNC).

When IVS = 1, the frame clock (VSYNC) is active low.

When IVS = 0, it is active high.

Invert HSYNC (IHS)

The invert HSYNC (IHS) bit is used to invert the polarity of the line clock (HSYNC).

When IHS = 1, the line clock (HSYNC) is active low.

When IHS = 0, it is active high.

Invert Pixel Clock (IPC)

The invert pixel clock (IPC) bit is used to select the edge of the pixel clock that drives pixel data out onto the LCD data lines.

When IPC = 1, data is driven onto the LCD data lines on the falling edge of the pixel clock.

When IPC = 0, data is driven onto the LCD data lines on the rising edge of the pixel clock.

Invert Output Enable (IEO)

The invert output enable (IEO) bit is used to select the active or inactive state of the output enable signal in active display mode. In this mode, the ac-bias pin is used as an enable that signals the device when data is being actively driven out using the pixel clock.

When IEO = 1, the ac-bias pin is active low. In active display mode, data is driven onto the LCD data lines on the programmed edge of the pixel clock when ac-bias pin is in its active state (see subsection *Invert Pixel Clock (IPC).*

When IEO = 0, the ac-bias pin is active high.

Note:

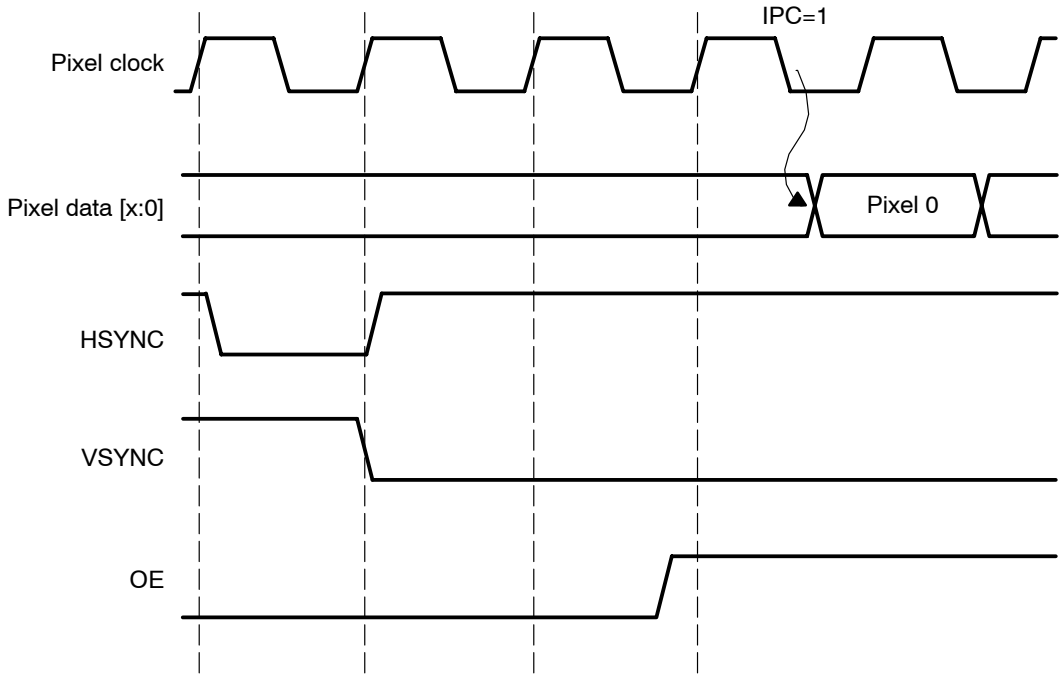
IEO does not affect the ac-bias pin in passive display mode.

HSYNC/VSYNC Rise or Fall Programmable (or not)(RF)

This bit determines whether the HSYNC/VSYNC is driven on the rising or falling edge of the pixel clock (see the HSYNC/VSYNC ON_OFF bit; ON_OFF must be turned on first). By default, the HSYNC and VSYNC signals are driven on the falling edge of the pixel clock, and the pixel data is driven on the rising edge of pixel clock. However, if the invert pixel clock (IPC) bit is set to 1, then the HSYNC and VSYNC signals are driven on rising edge of pixel clock and pixel data is driven on falling edge. By setting the RF bit and enabling it (ON_OFF = 1), you can control on which edge the signals are driven.

Figure 30 shows the timing when ON_OFF = 0 and IPC =1 in TFT mode.

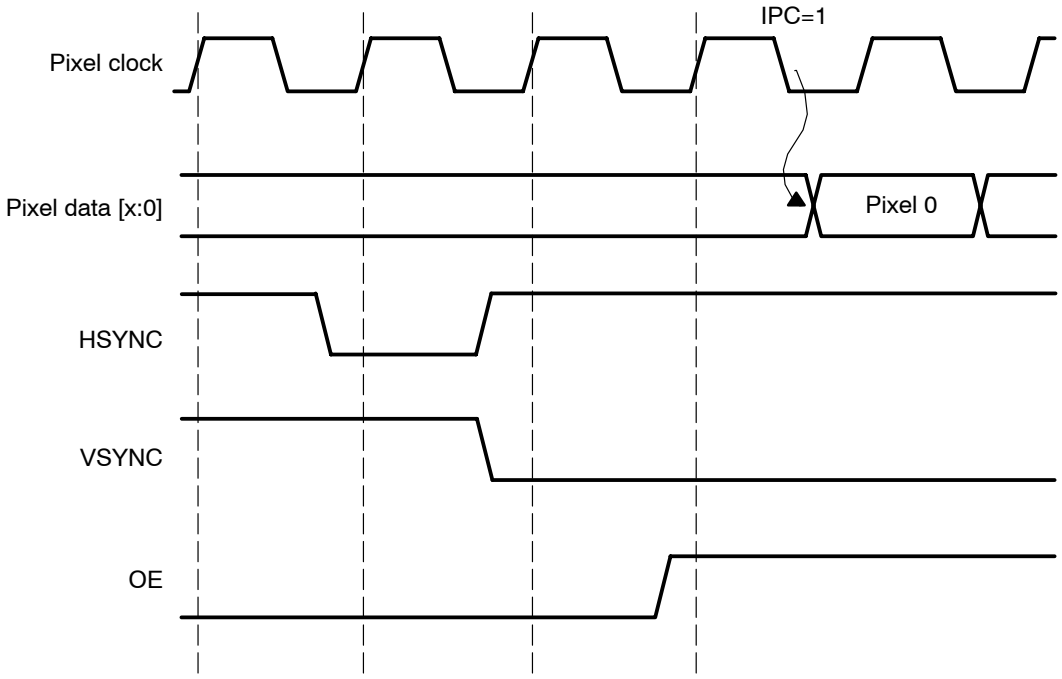
Figure 30. ON_OFF = 0, IPC = 1 in TFT Mode



- IPC = 1 means that pixel data is driven onto the LCD data lines on the falling edge of the pixel clock.
- ON_OFF = 0 means that HSYNC and VSYNC signals are driven on opposite edges of the pixel clock from pixel data (=> rising edge).

Figure 31 shows timing when ON_OFF = 1, RF = 0, and IPC = 1.

Figure 31. ON_OFF = 1, RF = 0, and IPC = 1



- When ON_OFF = 1, HSYNC and VSYNC signals are driven according to the RF bit.
- When RF = 0, HSYNC and VSYNC signals are driven on the falling edge of the pixel clock.
- When IPC = 1, pixel data is driven on the falling edge of the pixel clock.

HSYNC/VSYNC ON or OFF (ON_OFF)

This bit enables/disables the option to make HSYNC and VSYNC programmable.

- When ON_OFF = 1, HSYNC and VSYNC are driven according to the RF bit.
- When ON_OFF = 0, HSYNC and VSYNC are driven on opposite edges of the pixel clock from pixel data.

2.3.5 LCD Controller Status Register (LcdStatus)

The LCD controller status register (LcdStatus) contains seven bits that detect different events. Each of these hardware-detected events signals an interrupt request to the interrupt controller.

Figure 32. LCD Status Register (LcdStatus)

Offset: 0x 10 **LCDStatus: LCD Status Register** **Read/Write and Read-Only**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									LP	FUF	line_ int	ABC	Sync Lost	VS	Done
Reset	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0

NOTE: Read-only/clear-only bits are cleared by writing 0 to them.

Table 17. LCD Status Register (LcdStatus) Bit Descriptions

Bit	Name	Description
31:7	-	Reserved
6	LP	Loaded palette (read/clear-only) LP = 0, as long as the palette is not loaded. LP is set to 1 when the palette is loaded.
5	FUF	FIFO underflow status (read-only) FUF = 0, as long as FIFO has not underrun. FUF is set to 1 when the LCD dither logic is not supplying data to FIFO at a sufficient rate, FIFO has completely emptied, and data pin driver logic has attempted to take added data from FIFO.
4	line_int	Line interrupt (read/clear-only) Line_int = 0, as long as the display has not reached the programmed line yet, or if this interrupt has been cleared. Line_int is set to 1 when the display reaches the user-programmed line number and generates the interrupt.
3	ABC	ac-bias count status (read/clear only) ABC = 0, as long as ac-bias transition counter has not decremented to 0. See subsection *ac-Bias Line Transitions Per Interrupt (ACBI)*. ABC is set to 1 when the ac-bias transition counter has decremented to zero, indicating that the ac-bias output line has transitioned the number of times, specified by the ACBI control bit-field. Counter is reloaded with the value in ACBI but is disabled until you clear ABC.
2	Sync_ lost	Synchronization lost (read-only) When Sync_lost = 0, no frame synchronization error occurred. When Sync_lost = 1, frame synchronization lost occurred.

Table 17. LCD Status Register (LcdStatus) Bit Descriptions (Continued)

Bit	Name	Description
1	VS	VSYNC interrupt (read/clear only) VS = 0, as long as VSYNC interrupt is not generated. VS is set to 1 when the VSYNC interrupt occurs at the end of frame.
0	Done	Frame done (read-only) Done is set to 0, as long as the LCD is enabled. Done is set to 1 when the LCD is disabled and the active frame is just completed.

Frame Done (Done) (Read-Only)

When the LCD is disabled by clearing the LCD enable bit (LcdEn=0) in the LcdControl register, the LCD allows the current frame to complete before it is disabled. After the last set of pixels is clocked out onto the LCD data pins by the pixel clock, the LCD is disabled and Done is set.

- ❏ Done = 1 when the frame is complete.
- ❏ Done = 0, as long as the frame is not complete.

The frame done (Done) bit is a read-only bit signaling that the frame is complete. It is cleared when LcdEn bit is set to 1 (turned ON).

VSYNC Interrupt (VS) (Read/Clear-Only)

VSYNC interrupt occurs when the LCD reaches the end of the frame. This interrupt is shared with other LCD interrupts and is output on the lcd_nirq interrupt output line (see Figure 33, *Line Interrupt Path*). You can unmask the VSYNC interrupt by writing 1 to the VSYNC_mask bit in the LCD control register (see section 2.3.1, *LCD Control Register*).

To clear the VSYNC bit in the status register, you must write 0 to it.

- ❏ VSYNC = 1 signals that the end of frame occurred and generated the VSYNC interrupt.
- ❏ VSYNC = 0 if no VSYNC interrupt is generated.

Frame Synchronization Lost (Sync_lost) (Read-Only)

The frame synchronization lost (Sync_Lost) bit is set if the LCD controller detects a frame synchronization error. A frame synchronization error happens when the LCD attempts to read what it believes to be the first word of the video buffer but it cannot be recognized as such. This bit is cleared by disabling the LCD controller (LcdEn bit =0). This also resets the input FIFO in the DMA controller.

- Sync_lost = 1 when a frame synchronization lost occurred.
- Sync_lost = 0, as long as no frame synchronization error occurs.

ac-Bias Count Status (ABC) (Read/Clear-Only)

The ac-bias count status (ABC) bit is set each time the ac-bias line transitions a particular number of times, as specified by the ac-bias line transitions per interrupt (ACBI) field in LcdTiming2. If ACBI is programmed with a non-zero value, a counter is loaded with the value in ACBI and is decremented each time the ac-bias line reverses state. When the counter reaches zero, the ABC bit is set, which signals an interrupt request to the interrupt controller. The counter reloads using the value in ACBI, but does not start to decrement again until you clear ABC by writing 0 to the LCD status register.

- ABC = 1 when the ac-bias transition counter ACBI has decremented to 0.
- ABC = 0, as long as ACBI has not decremented to 0.

Line Interrupt (line_int) (Read/Clear-Only)

You can program the LCD to generate a line interrupt when the LCD reaches a certain line (n) in the display. This interrupt sets the line_int bit in the status register. This dedicated line interrupt can be connected to the hardware synchronized channel of the DMA. It can be used to prevent a tearing effect if double buffering is not implemented. See section *Tearing Effect,* for information on the use of this feature.

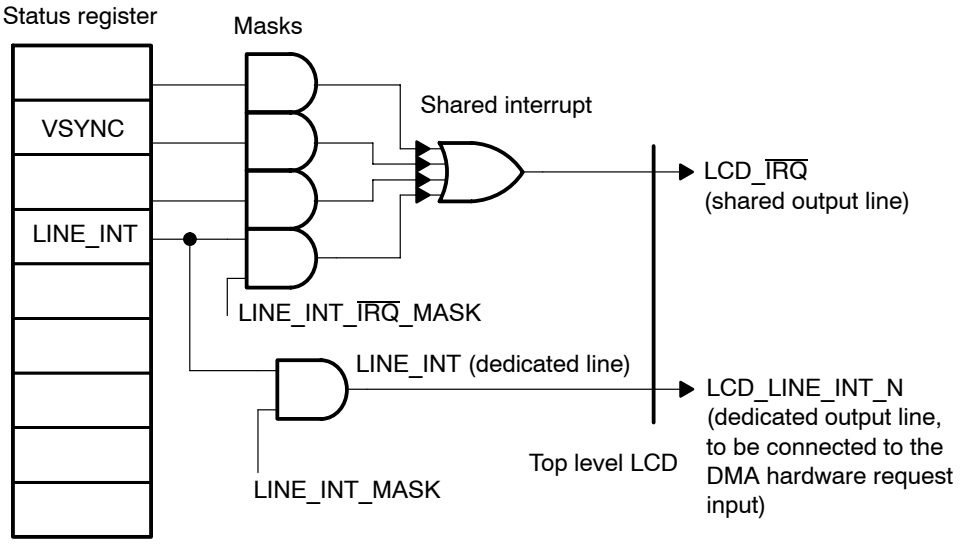
It is possible to connect the line_int interrupt to both the lcd_nirq interrupt output line and to a dedicated lcd_line_int_n output line.

On one hand, the line_int_mask bit masks the dedicated line interrupt. You can unmask it by writing 1 to the control register. Line_int is a status bit which can be cleared by writing 0 to it.

On the other hand, the line_int_nirq_mask bit in the control register masks the shared interrupt.

See Figure 33 for details.

Figure 33. Line Interrupt Path



- Line_int is set to 1 when the display reaches the user-programmed line number and generates the interrupt.
- Line_int = 0, as long as the programmed line is not reached.

The line_int bit is cleared if the TIPB writes 0 to it, or at the end of the programmed line according to the line_int_clr_sel bit in the control register.

FIFO Underflow Status (FUF) (Read-Only)

The FIFO underflow status (FUF) bit is set when the input FIFO is completely empty and the LCD data pins driver logic attempts to fetch data from the FIFO. This bit is cleared by disabling the LCD controller (LcdEn = 0). This also resets the input FIFO in the DMA controller.

- FUF = 1 when the dithering logic is not supplying data to the FIFO at a sufficient rate.
- FUF = 0, as long as FIFO has not underrun.

Loaded Palette (LP) (Read/Clear-Only)

The loaded palette (LP) bit is a read-only bit that is set after the LCD finished loading the palette into memory.

- LP = 1 when the palette is loaded.
- LP = 0, as long as the palette is not loaded.

In data-only (PLM = 10) and palette-plus-data (PLM = 00) modes, write 0 to clear the interrupt. However, in the palette only (PLM = 01) mode, LCD must be turned off in order to reset/clear the interrupt. Make sure not to turn off the LCD before getting the loading interrupt in this mode. See subsection *Palette Loading (PLM).*

2.3.6 LCD Subpanel Display Register (LcdSubpanel)

The LCD subpanel display register (LcdSubpanel) enables displaying only the first or last X lines of the panel and sending fixed content for the other lines.

Figure 34. LCD Subpanel Register (LcdSubpanel)

Offset: 0h 14 **LCDSubpanel: LCD Subpanel Register** **Read and Write**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPEN	Res	HOLS	Reserved			LPPT									
Reset	0	x	0	x	x	x	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18. LCD Subpanel (LcdSubpanel) Bit Descriptions

Bit	Name	Description
31	SPEN	Subpanel enable
		SPEN = 0: Subpanel function is disabled.
		SPEN = 1: Subpanel function is enabled.
30		RESERVED
29	HOLS	High or low signal
		The field indicates the position of the subpanel compared to the LPPT value.
		HOLS = 0: The image from the frame buffer is displayed below the LPPT value.
		HOLS = 1: The image from the frame buffer is displayed above the LPPT value.
28:26		RESERVED

Table 18. LCD Subpanel (LcdSubpanel) Bit Descriptions (Continued)

Bit	Name	Description
25:16	LPPT	Line per panel threshold Value (from 1 to 1023) delimiting the subpanel and the DPD parts of the screen. LPPT is a threshold value delimiting the subpanel and the DPD parts of the screen. It ranges from 1 to 1024 and should be programmed to value required minus one (0-1023).
15:0	DPD	Default pixel data DPD defines the default value of the pixel data sent to the panel for the lines until the LPPT threshold is reached or after passing the LPPT depending on HOLS mode.

DPD, LPPT, HOLS, and SPEN bit fields and bits are not considered if SPEN=0.

Default Pixel Data (DPD)

DPD defines a default value, which is sent to the display in either the top or bottom region of the screen delimited by the LPPT threshold. When displaying the DPD value, there is no DMA activity.

Line-per-Panel Threshold (LPPT)

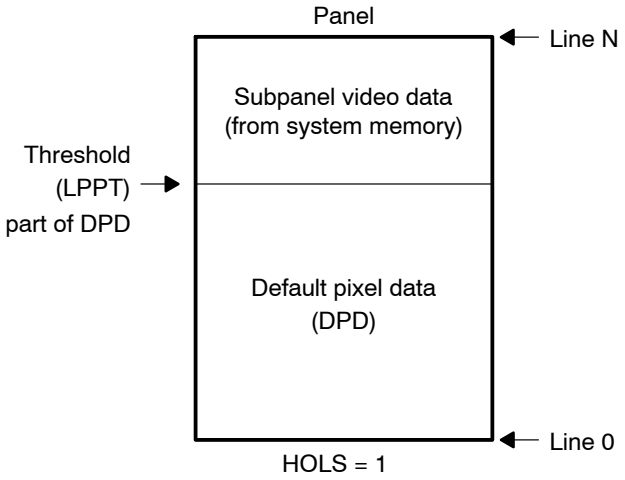
The line-per-panel threshold bit-field delimits the screen portion filled with data fetched from the frame buffer (the subpanel) and the rest of the screen filled with default pixel data (DPD). Note that the LPPT line number points on a line filled with a DPD value when HOLS = 1, but on a line filled with video data when HOLS = 0 (see Figure 35 and Figure 36).

High Or Low Signal (HOLS)

The HOLS bit indicates the position of the subpanel compared to the LPPT value.

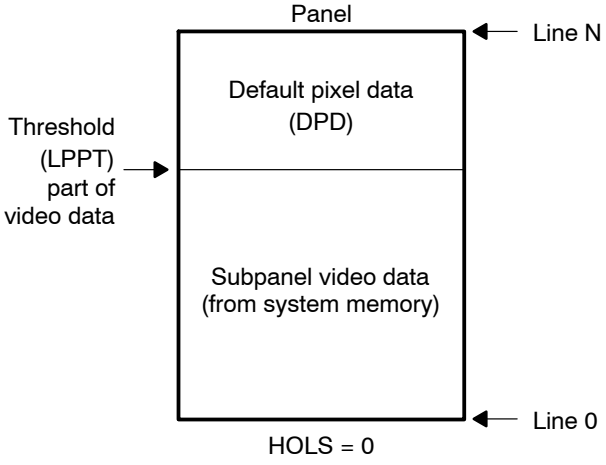
When HOLS = 1, the image from system memory is displayed above the threshold value. The threshold value is the line number where the DPD value begins to be displayed. The rest of the screen is filled with DPD value.

Figure 35. Subpanel Display: SPEN = 1, HOLS = 1



When HOLS = 0, the beginning of the screen is filled with DPD value until the LPPT excluded. From the LPPT line number, the rest of the screen (below LPPT) displays the image from system memory.

Figure 36. Subpanel Display: SPEN = 1, HOLS = 0



Note:

The bottom of the panel is line 0, and top line of the panel is line N (where N is the number of lines-per-panel).

For example, if you want to display four lines of video data at the bottom of the panel, the correct settings are HOLS = 0 and LPPT = 3. Here, the amount of video data to be transferred from the DMA_LCD channel is only four lines.

Note:

If the LPPT is above the number of LPP, then:

- When HOLS = 1: panel with default data (whole panel is filled with DPD value).
- When HOLS = 0: normal panel (whole panel is filled with video data from the frame buffer).

Subpanel Enable (SPEN)

This bit enables or disables the subpanel mode.

When SPEN = 0, subpanel mode is disabled.

When SPEN = 1, subpanel mode is enabled.

2.3.7 Line Interrupt Register (LcdLineInt)

The line interrupt register (LcdLineInt) enables you to program the line number in bits (0-9) where you want the line interrupt to be generated.

Figure 37. Line Interrupt Register (LcdLineInt)

Offset: 0h 18 **LCDLineInt: Line Interrupt Register** **Read and Write**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						LINE_INT_NUMBER									
Reset	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0

Table 19. Line Interrupt Register (LcdLine Int) Bit Descriptions

Bit	Name	Description
31:10	-	Reserved
9:0	Line_int_number	Line number at which line interrupt occurs. Programmable from line 0 up to line 1023.

2.3.8 Display Status Register (LcdDisplayStatus)

The display status register (LcdDisplayStatus) contains the line number currently being displayed.

Figure 38. Display Status Register (LcdDisplayStatus)

Offset: 0h 1C	LCDDisplayStatus: Display Status Register											Read-Only				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CURRENT_LINE_NUMBER									
Reset	x	x	x	x	x	x	1	1	1	1	1	1	1	1	1	1

Table 20. Line Interrupt Register (LcdDisplayStatus) Bit Descriptions

Bit	Name	Description
31:10	-	Reserved
9:0	Current_line_number	Line number being displayed. As the number of lines can be programmed from 1 to 1024, the current line number varies between 0 and 1023.

3 LCD Data Conversion Module

The LCD data conversion module (LCDCONV) supports two operation modes: the 16-bit LCD mode and the 18-bit LCD mode. The mode switching is done by setting the MODE_SET bit in the control register (LCDCONV_CONTROL_REG). The mode change is synchronized with the LCD pixel frame synchronization signal. At the active edge of the pixel frame synchronization, the MODE_SET bit in the control register is sampled and the right mode is set up accordingly. Software reads the MODE_STATUS bit in the control register to know whether the LCD mode has changed.

In 16-bit LCD mode, the 16-bit LCD pixel signal from the LCD controller bypasses the RGB look-up table and goes directly to the external LCD display. The LCD RGB look-up table is accessible only in this mode. The host microcontroller programs and reads back the contents of the RGB look-up table.

In 18-bit LCD mode, the 16-bit LCD pixel signal is converted to an 18-bit LCD pixel signal through an RGB look-up table. The input 16-bit LCD pixel signal is used as an index to a programmable RGB look-up table to generate an 18-bit pixel signal for the external LCD display. The OCP bus cannot access the RGB look-up table in this mode. An OCP bus read in this mode reads all zeros. For an OCP bus write, nothing is written to the RGB look-up table. The size of the look-up table is defined in Table 21.

Table 21. RGB Lookup Table Size

RGB Lookup Table	Lookup Table Size (Bits)	Index (LCD Input Pixel Bit)
R	32 x 6	0-4
G	64 x 6	5-10
B	32 x 6	11-15

3.1 Data Conversion

In the 18-bit mode, the 16-bit LCD signals (5 bits for R, 6 bits for G, and 5 bits for B) are used as the address for the LUT. The LUT is divided into three sections: R LUT 32x6 bits, G LUT 64x6 bits, and B LUT 32 x 6 bits. The word width of the three LUTs is 6 bits. The length of the LUT is 32 lines red, 64 lines green, and 32 lines blue. These correspond to the 16-bit RGB signal (5 red, 6 green, and 5 blue) address decoding. The user can program the content of the LUT so that the application determines which conversion algorithm is necessary. The converted 18-bit LCD signals are mapped to the LCDCONV LCD_PIXEL_OUT output ports. The LCDCONV output LCD signal consists of two parts: LCD_PIXEL_OUT[15:0], RED_LSB and BLUE_LSB. The mapping is as follows:

In 18-bit mode:

- LCD_PIXEL_OUT[15:11] <= R_LUT[5:1]
- LCD_PIXEL_OUT[10:5] <= G_LUT[5:0]
- LCD_PIXEL_OUT[4:0] <= B_LUT[5:1]
- RED_LSB <= R_LUT[0]
- BLUE_LSB <= B_LUT[0]

In 16-bit mode:

- LCD_PIXEL_OUT[15:0] <= LCD_PIXEL_IN[15:0]
- RED_LSB <= LCD_PIXEL_IN[15]
- BLUE_LSB <= LCD_PIXEL_IN[4]

Table 22 summarizes the mapping for the16-bit and 18-bit modes.

Table 22. LCD 16-Bit to 18-Bit Conversion

	RED						GREEN						BLUE					
LCD pixel input to LDCONV	15	14	13	12	11		10	9	8	7	6	5	4	3	2	1	0	
LCD pixel output (16-bit mode)	R4	R3	R2	R1	R0	R4 (R_LSB)	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4 (B_LSB)
LCD output 1(18-bit mode)	R5	R4	R3	R2	R1	R0 (R_LSB)	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0 (B_LSB)

Figure 39 shows the 16-bit to 18-bit LCD data block.

Figure 39. 16-Bit to 18-Bit LCD Data Block

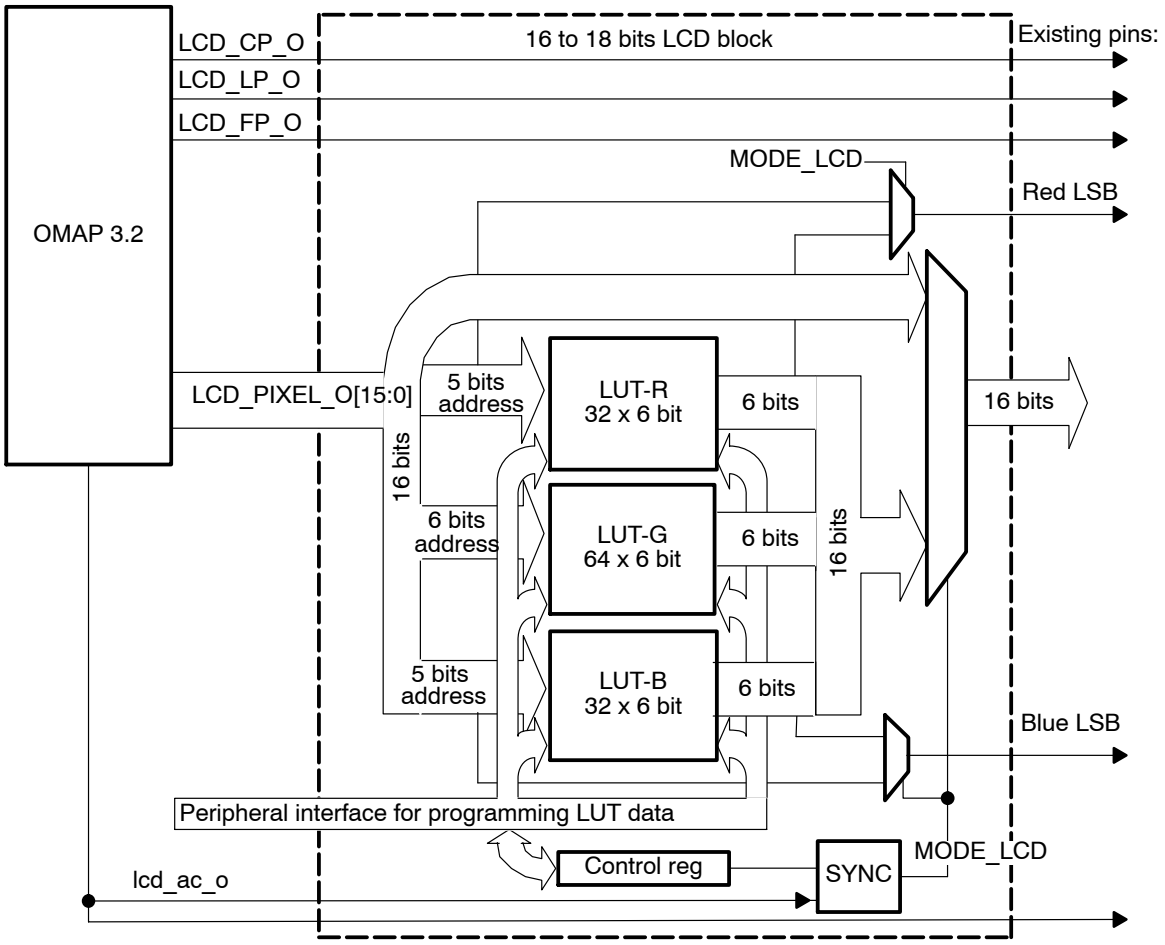


Table 23. Top Level I/O Signals

Signal Name	I/O	Description	Reset
		Clock and Reset:	
CLK	Input	Free-running OCP bus clock	N/A
RST_N	Input	Asynchronous global reset, active low	N/A
		OCP Bus Interface Signals	
MADDR[7:0]	Input	OCP address bus from the master	N/A
MCMD[2:0]	Input	Input transfer command (idle, read, write mode only)	N/A
MDATA[7:0]	Input	OCP data bus from the master	N/A

Table 23. Top Level I/O Signals (Continued)

Signal Name	I/O	Description	Reset
SDATA_OUT[7:0]	Output	OCP data bus to the master	0
SCMDACCEPT	Output	OCP command accepts transfer	0
SRESP	Output	OCP response field from the slave to transfer request from the master	0
		LCD signals	
LCD_PIXEL_IN[15:0]	Input	Pixel signals from the LCD controller	N/A
LCD_AC	Input	LCD frame sync from the LCD controller	N/A
LCD_PIXEL_OUT[15:0]	Output	Pixel signals to the external LCD display	LCD_PIXEL_IN [15:0]
RED_LSB	Output	Red LSB signal for the 18-bit LCD mode	LCD_PIXEL_IN [15]
BLUE_LSB	Output	Blue LSB signal for the18-bit LCD mode	LCD_PXIEL_IN [4]

3.2 Software Interface

Table 24. Register Summary

Base Address = FFFE 3000

Address	Type	Bit	Name	Description
0x0000 -0x001F	MG register file	5:0	R look-up table	32 x 6 look-up table for R signal
		6:7	Reserved	Read as 0, no impact on write
0x0020 –0x003F	MG register file	5:0	B look-up table	32 x 6 look-up table for B signal
		6:7	Reserved	Read as 0, no effect on write
0x0040– 0x007F	MG register file	5:0	G look-up table	64 x 6 look-up table for G signal
		6:7	Reserved	Read as 0, no impact on write
0x0080	Register	3:0	LCDCONV_CONTROL_REG	Control register
		4:7	Reserved	Read as 0, no effect on write
0x0084	Register	7:0	DEV_REV_REG	Device revision register, read only

The RGB look-up table icon consists of 128 x 6-bit, two-port MG RAM as shown in Table 24. The host microcontroller can program and read the RAM only in 16-bit mode. In 18-bit mode, the content of the look-up table is sent directly to the LCD display.

Table 25. Control Register (LCDCONV_CONTROL_REG)

Bit	Name	Function	R/W	Reset
7:4	Reserved	Reserved.	R	0
3	LCD_AC_EDGE	This bit represents the active edge of the LCD frame sync signal. 0: Active edge is positive. 1: Active edge is negative.	R/W	0
2	CLOCK_EN	Enables the write clock to RGB look-up table RAM	R/W	0
1	MODE_STATUS	Actual mode of LCD. 0: 16-bit mode. 1: 18-bit mode.	R	0
0	MODE_SET	This bit represents the software setup for the LCD mode. The actual mode switching occurs at the active edge of the pixel frame sync signal. 0: 16-bit mode. 1: 18-bit mode.	R/W	0

The control register has four control bits.

The CLOCK_EN bit gates the clock to the module. When this bit is on, the OCP bus clock clocks the RGB look-up table. When this bit is set to 0, the RGB look-up table clock is turned off. The OCP bus clock always clocks the control register.

The two mode-control bits are MODE_SET and MODE_STATUS. The MODE_STATUS bit is a read-only bit that represents the actual state of the LCD display mode. The MODE_SET bit is used for LCD mode programming. Software programs this bit to choose either the 18-bit mode or the 16-bit mode for the LCD. The actual mode switching occurs only at the next active edge of the pixel frame synchronization signal. When the mode is switched, the MODE_STATUS bit is updated to the MODE_SET bit. Using these two mode bits, the software can monitor the control register to determine whether the mode switching has occurred.

The active edge of the pixel frame synchronization signal is programmable. The LCD_AC_EDGE bit represents the polarity of the pixel frame synchronization and is used for the mode switching.

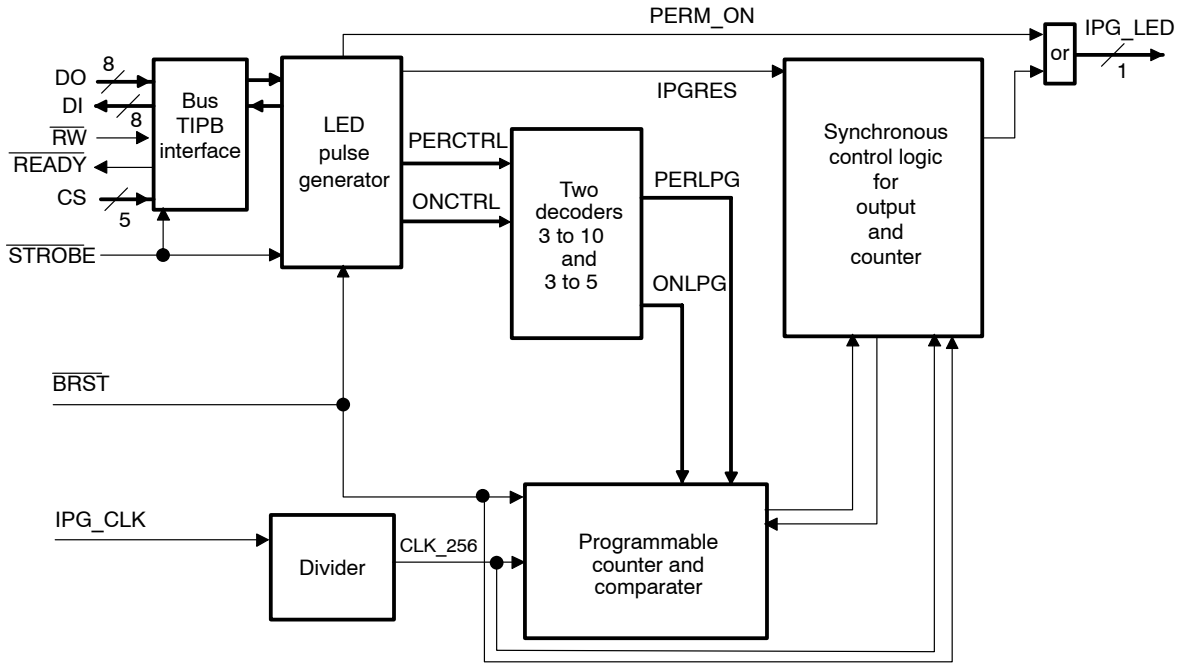
3.3 Bus Interface

The host microcontroller accesses the RGB look-up table and the control register through the OCP bus. The LDCONV module supports only 8-bit OCP bus access. No burst mode is supported. The RGB look-up table is accessible only by the OCP bus in the 16-bit mode. In the 18-bit mode, an OCP read reads in all zeros, and an OCP write does nothing to the RGB look-up table.

4 LED Pulse Generator

The LED pulse generator (LPG) module controls an indication LED (see Figure 40). The blinking period is programmable between 152 ms and 4 s, and the LED can be switched on permanently.

Figure 40. LED Pulse Generator Block Diagram



4.1 Features

The LPG has the following features:

- ❏ Divider generating a 256-Hz frequency clock
- ❏ TIPB control interface
- ❏ Two 8-bit registers to control the whole LPG block
- ❏ Decoder for three blink-frequency control bits (LPG2-0)
- ❏ Decoder for three pulse-width control bits (LPG5-3)
- ❏ Programmable counter with integrated comparison for the PWM
- ❏ Synchronous control logic for the output and the counter
- ❏ Multiplexer to generate a faster clock for testing

Table 26 lists the LPG functional I/O signals.

Table 26. LPG Functional I/O Signals

Name	Description	Type	Size	Active Level	Reset Level
nRESET	Asynchronous general reset	IN	1	0	--
LPG_CLK	LPG functional clock, 32-kHz frequency	IN	1	--	--
LPG_LED	Control LED signal	OUT	1	1	0

4.2 LPG Design

LCR bit 6 = 0 resets the whole PWM circuit (but not the control register) and switches off the LED. It is possible to switch on the LED independently from the PWM circuit with bit 7 of the LCR (1 = permanent light). The reset PWRON is active-low and resets the whole LPG (with the control register) and the output LPG_LED to zero asynchronously.

4.3 LPG Power Management

The LPG input clock comes from the 32-kHz ULPD clock, because it must work even when the system is in deep sleep mode. The internal clock of the LPG runs with 256 Hz, so the power consumption of this block can be neglected. Nevertheless, the LPG_CLK must be switched off if LPG is not used.

4.4 LPG Registers

LPG registers are mapped in the MPU address space.

Two instances of LPG are mapped in the device:

- First LPG: LPG_1 address is FFFB:D000
- Second LPG: LPG_2 address is FFFB:D800

Table 27 lists the LPG receive and transmit registers. Table 28 and Table 31 describe the register bits.

Table 27. LED Pulse Generator Receive and Transmit Registers

Register	Description	Access	Field Size	Offset (hex)
LCR	LPG control	R/W	8 bits	0x00
PMR	Power management	R/W	8 bits	0x04

Table 28. LPG Control Register (LCR)

Bit	Name	Function	R/W	Reset
7	PERM_ON	Set high to force permanent light on. Asynchronous writing and reading.	R/W	0
6	LPGRES	LPG counter reset active low. Asynchronous writing and reading.	R/W	0
5:3	ONCTRL	Time LED is on parameter. Asynchronous writing and reading.	R/W	000
2:0	PERCTRL	LED blink frequency. Asynchronous writing and reading.	R/W	000

The blinking period of the LED is determined with the LCR bits 2-0.

Table 29. LED Blinking Period

LCR Bit 2	LCR Bit 1	LCR Bit 0	Period of LED	No. of Clock Cycles
0	0	0	125 ms	32
0	0	1	250 ms	64
0	1	0	500 ms	128
0	1	1	1 s	256
1	0	0	1.5 s	384
1	0	1	2 s	512
1	1	0	2.5 s	640
1	1	1	3 s	768

The on-time of the LED is determined with the LCR bits 5-3.

Table 30. LED On Time

LCR Bit 5	LCR Bit 4	LCR Bit 3	Time LED On	No. of Clock Cycles
0	0	0	3.889 ms	1
0	0	1	7.789 ms	2
0	1	0	15.59 ms	4
0	1	1	31.39 ms	8
1	0	0	46.59 ms	12
1	0	1	62.59 ms	16
1	1	0	78.39 ms	20
1	1	1	93.59 ms	24

Table 31. Power Management Register (PMR)

Bit	Name	Function	R/W	Reset
0	CLK_EN	Functional clock enable: 1: Clock enabled. 0: Clock disabled. Asynchronous writing and reading.	R/W	0

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