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Memory Interfaces

This document describes the memory interfaces of the OMAP5912 multimedia processor.

1 Introduction

This document describes the following interfaces:

- SDRAM (external memory interface fast, or EMIFF)
- Asynchronous and synchronous burst memory (external memory interface slow, or EMIFS)
- NAND flash (software controller)
- Internal static RAM

1.1 SDRAM Interface

The following gives a brief overview of the EMIFF. Please see the *Multimedia Processor OMAP 3.2 Subsystem Reference Guide (SPRU749)* for a detailed description of the EMIFF. The OMAP EMIFF is an SDRAM controller that manages access by the various initiators of an OMAP-based system. It can support one 16-bit device or two 8-bit devices. The external interface data bus width is always 16 bits.

The EMIFF supports the following devices:

- Standard single-data-rate SDRAM
- Low-power single-data-rate SDRAM
- Standard double-data-rate SDRAM
- Mobile double-data-rate SDRAM

In terms of capacity and organization of memory components, the EMIFF can handle:

- 1G-bit, 512M-bit, 256M-bit, 128M-bit, 64M-bit, and 16M-bit devices
- Two-bank 16M-bit devices, two-bank or four-bank devices for 64M-bit devices, four-bank devices only for any other capacity
- x8 (two devices) or x16 (single device) data bus configuration, except for the 1G-bit device: the EMIFF supports only a x16-1G-bit device (single device). The maximum external SDRAM configuration is 128 megabytes.

Program the SDRAM_TYPE field of the EMIFF interface SDRAM configuration register to specify the physical configuration of the devices.

The SDRAM type selection is the first action required from the software driver, using the SDRAM_TYPE field of the EMIF SDRAM operation register.

The SDRAM controller supports:

- The self-refresh mode (idle), autorefresh, and other operating modes (HPHB, LPLB, and POM0 modes)
- MRS command and extended MRS command for:
  - DDR SDRAM and low-power SDRAM, sent via the SDRAM request manager
  - SDR SDRAM, all burst sizes, between 1 and 32 consecutive accesses
  - DDR SDRAM, only bursts of 8
- Two pipelined levels of request from the SDRAM request manager to enable page interleave timing and reduce overhead cycles by the burst interruption mechanism.

1.2 Asynchronous and Synchronous Burst Memory Interface (EMIFS)

The synchronous/asynchronous external memory interface slow (EMIFS) supports most common memory interface protocols through a flexible programming and timing signals control. The following serves to give a brief overview of the EMIFS. Please see the Multimedia Processor OMAP 3.2 Subsystem Reference Guide (SPRU749) for a detailed description of the EMIFS.

The EMIFS can control up to six devices without adding any external logic through six independent chip-selects and through dedicated memory interface control signals. Two configurable options are supported:

- Four chip-selects. Each can support up to 64M bytes of addressable memory:
  - CS0 from 0000:0000 to 03FF:FFFF
  - CS1 from 0400:0000 to 07FF:FFFF
  - CS2 from 0800:0000 to 0BFF:FFFF
  - CS3 from 0C00:0000 to 0FFF:FFFF
- Six chip-selects. Two can support up to 64M bytes of addressable memory, and four can support up to 32M bytes of addressable memory:
  - CS0 from 0000:0000 to 03FF:FFFF
  - CS1_a from 0400:0000 to 05FF:FFFF
  - CS1_b from 0600:0000 to 07FF:FFFF
  - CS2_a from 0800:0000 to 09FF:FFFF
  - CS2_a from 0A00:0000 to 0BFF:FFFF
  - CS3 from 0C00:0000 to 0FFF:FFFF

The EMIFS supports common external memory control signals:

- OE
- WE
- ADV
- BE[0–1]
- BE[2–3]
- BAA
- Ready
- Device CLK
- RST
- WP

Each chip-select (CS) controls an address range with dedicated configuration registers to ensure compliance with the protocol and timing constraints of the external device associated with it. Each chip-select configuration register supports dynamic configuration.

The EMIFS can support 16-bit and 32-bit external device width. Based on the CS configuration, the interface adjusts the access size (splitting word32) according to the external device attached to the CS.

An 8-bit device width is not supported without adding external logic.

The EMIFS can control multiplexed address and data memory devices without adding external logic based on CS configuration. The multiplexing scheme is supported for synchronous and asynchronous access mode.

Both multiplexed and nonmultiplexed devices can be supported with the same integrated circuit (IC) on different chip-selects (embedded IC non-multiplexed memories and external multiplexed devices).

The EMIFS behavior conforms to the little-endian protocol. It supports 8-,16-, or 32-bit asynchronous and synchronous read, 4- x 32-bit synchronous burst read, and 8-, 16-, or 32-bit asynchronous write.

The EMIFS is a multimaster memory interface. It supports flexible and programmable arbitration protocol (LRU priority ordering or dynamic time-based priority ordering).

At boot time or at run time, CS0 and CS3 address mapping can be swapped.

The EMIFS includes a programmable time-out to prevent the system from hanging with nonresponding devices. Automatic access completion with interrupt and status logging are issued on time-out events.

The EMIFS supports dynamic local idle mode control. The EMIFS also supports IC deep power-down mode request synchronization.

2 Memory Interfaces for the EMIFS

There are a number of different memory types that can connect with the EMIFS interface. These memory types will share the same pins on the device, but their functionalities and controlling logic may differ.

The memory types and their associated controlling logic is:

- Non-multiplexed NOR flash—controlled by EMIFS directly
- Address/Data multiplexed NOR flash—controlled by EMIFS directly
- 8−bit NAND flash—controlled by the EMIFS directly (software NAND flash controller)
- 16−bit NAND flash—controlled by EMIFS directly (software NAND flash controller)

Some of these controllers can be used simultaneously. See Figure 2, for details on simultaneous connections of these memory types. The different combinations are:

- Non-multiplexed NOR on EMIFS and 16−bit NAND on EMIFS

The following sections describe the different external memory controllers that use the EMIFS pins.

2.1 Software NAND Flash Controller

This section describes how to connect OMAP to a NAND flash using only the EMIFS logic (referred to throughout this document as the Software NAND flash controller). The software NAND flash controller can connect to either 8-bit or 16-bit NAND flashes.

2.1.1 NAND Flash Software Controller Overview

The features of the system are as follows:

- The NAND flash device is mapped on one of the chip-selects of the EMIFS interface of the device.
- One 8-bit- or 16-bit-wide interface NAND flash device is supported on EMIFS. Either the MPU core or DSP core (hereafter called the processor) can access and control the NAND flash device.
- The processor manages the command sequence required for block erase, write, read, and block invalidation and management. To reduce processor overhead, either the system DMA (GDMA) or the DSP DMA can be used to write or read blocks of data to/from the NAND flash device.
- There is one option for ECC calculation:
  - The MPU core or DSP core calculates the ECC by software.

Some NAND flash devices require that CS be low during the read access time (tR); hereafter, these devices are called NAND CE Care. Thus, a standard chip-select cannot be used for the NAND flash chip-select. However, some NAND flash devices do not require that CS be low during tR; these devices are called NAND CE Do Not Care. The chip-select can be used directly for them.

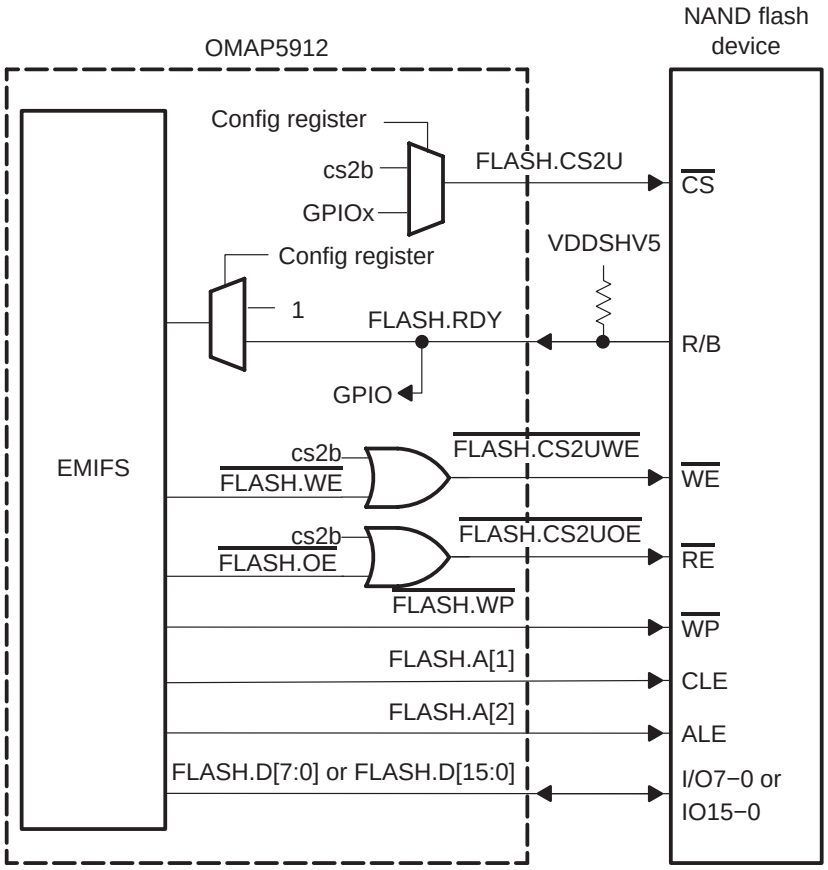
2.1.2 EMIFS Interface With NAND CE Care Flash Device Option

The interface of a NAND CE Care flash device to the OMAP is possible by using $\overline{\text{FLASH.CS2UOE}}$ (output enable) and $\overline{\text{FLASH.CS2UWE}}$ (write enable). The only exception to this policy is that several signals that are used for the NAND flash interface are muxed on signals that are needed for support of synchronous burst flash memories.

If both NAND and synchronous burst flash memories are required in the system, two solutions are available:

- Generate the NAND flash interface signals by GPIOs at some loss of system performance
- Use a NAND flash device that is NAND CE Do Not Care. Be careful to purchase an appropriate NAND flash device (most of the NAND flash devices manufactured are NAND CE Don’t Care-compliant).

Figure 1. NAND Flash Device Interface Schematic



- CS: Most NAND flash devices require that CS be low during the read access time (t_R). For example, the Samsung K9K1G08U0M device requires CS to be low during t_R. Thus, a standard OMAP chip-select cannot be used for the NAND flash chip-select. To resolve this issue, a GPIO is multiplexed on this pin so that the processor can directly control the state of the NAND flash chip-select during accesses. However, some NAND flash devices do not require that CS be low during t_R. For these types of flash devices, the OMAP chip-select can be used directly.
- R/B: During read or write operations the NAND flash device R/B signal goes low to indicate that the device is busy and that other operations must wait until completion. To signal the device that the operation has completed, the R/B signal of the NAND flash device can be connected to the FLASH.RDY that is multiplexed with a GPIO. The GPIO is programmed to create an interrupt on the rising edge of R/B.

Note: FLASH.RDY Signal

The FLASH.RDY signal is primarily intended for use with synchronous burst flash devices. If the system does have a synchronous burst flash device and the FLASH.RDY signal is required, then the NAND flash R/B must be connected on some other GPIO of the OMAP device. If another GPIO is used, the interface voltage range must be considered between the open drain output of the NAND flash and the OMAP5912. Otherwise, it is possible to remove this input requirement by the use of timers to create the delay and/or the use polling of the NAND flash device status register.

- $\overline{WE}$ and $\overline{RE}$: As explained before, during t_R some NAND flash devices require that $\overline{CS}$ be low and during this time $\overline{WE}$ and $\overline{RE}$ must not toggle. Thus, it is necessary to gate the OMAP chip-select, cs2b, with the $\overline{FLASH.WE}$ and $\overline{FLASH.0E}$ signals to create the $\overline{FLASH.CS2UWE}$ and $\overline{FLASH.CS2UOE}$, respectively.

  If the muxed signals are needed in the system, it is possible to generate $\overline{WE}$ and $\overline{RE}$ by GPIO with some performance impact and a more complicated programming model.

- CLE and ALE: The command latch enable (CLE) and address latch enable (ALE) signals are generated by the address pins of OMAP FLASH.A[1] and FLASH.A{2}, respectively, as shown in Table 1.

Table 1. CLE and ALE

CLE: FLASH.A[1]	ALE: FLASH.A[2]	System Address (cs2b)	Function
L	L	0x0A00 0000	Data read or write access
H	L	0x0A00 0002	Command write access
L	H	0x0A00 0004	Address write access
H	H	0x0A00 0006	Non-valid access condition

- I/O7:0 or I/015:0 : NAND flash devices have either 8- or 16-bit-wide data buses. The FLASH.D[15] signals of the OMAP connect directly to the NAND flash I/O signals.

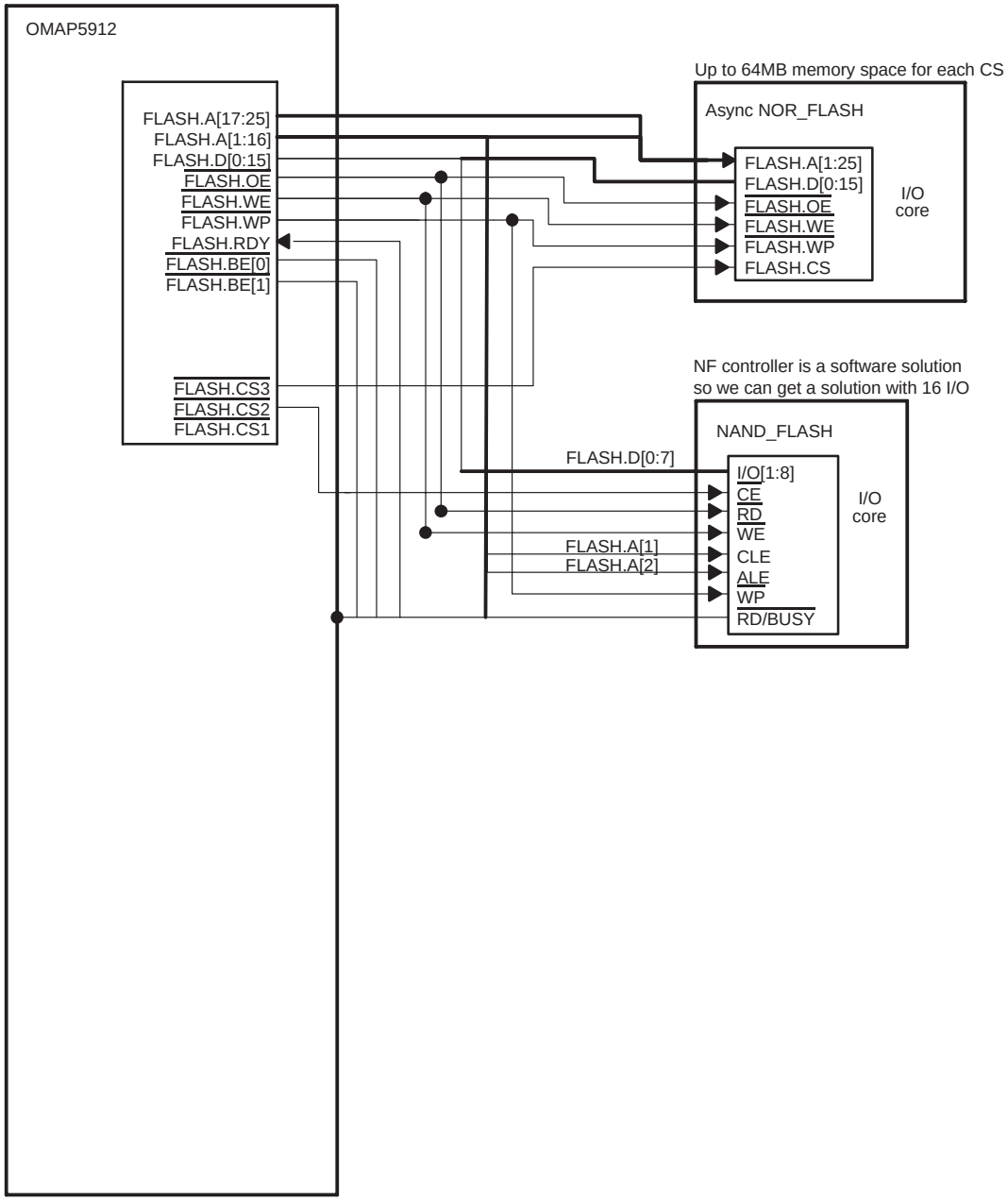
2.1.3 EMIFS Interface With NAND CE Do Not Care Flash Device Option

In this case, there is no dedicated signal to interface the NAND flash device. Instead, the standard NOR flash interface is used. Non-multiplexed NOR flash can also be connected at the same time.

The procedure to follow is the same as that described for NAND CE Do Not Care devices.

Figure 2 shows how NAND flash and an asynchronous NOR flash can be connected.

Figure 2. Software NFC with Non-multiplexed NOR



3 Frame Buffer

The frame buffer is used to store video frame before emission to an internal or external LCD controller.

Table 2. Test RAM Mapping

	L3 OCP T1			
	Start Address	**End Address**	**Size**	**Supported Access**
SRAM	2000 0000	2003 E7FF	250Kbytes	8/16/32-bit Ex/R/W

The frame buffer is connected to the L3 OCP-T1 port. It is accessible from the following systems:

- MPU core subsystem (ARM926EJS processor)
- DSP core subsystem (C55x DSP processor via the DSP MMU)
- System DMA (DMA OCPT1 port)

The frame buffer only supports READ/WRITE/IDLE accesses: an error is generated in other cases or if the address is incorrect. The frame buffer only supports 8-, 16-, and 32-bit access in little endian.

		Data Bus			
Access Size	**System Address**	**[31:24]**	**[23:16]**	**[15:8]**	**[7:0]**
8	xx00	-	-	-	D[7:0]
	xx01	-	-	D[7:0]	-
	xx10	-	D[7:0]	-	-
	xx11	D[7:0]		-	-
16	xx00	-	-	D[15:8]	D[7:0]
	xx10	D[15:8]	D[7:0]	-	-
32	xx00	D[31:24]	D[23:16]	D[15:8]	D[7:0]

The module is clocked up to 100 MHz with the TC2_CK on OCP T2 port.

The frame buffer only supports incrementing burst accesses.

Any invalid access is logged into the OCPT2_ATYPER register within OMAP3.2. The OCP bus error access corresponds to OCPT2_ATYPER[3] status bit.

Peripheral Reset

The software must ensure that no access is performed (including DSP/system DMA access) while the MPU core peripheral reset is asserted. Whenever the peripheral reset is active, the OCP interface is held in reset.

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Read This First

About This Manual

This chapter describes the memory interfaces of the OMAP5912 multimedia processor.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

Documentation that describes the OMAP5912 device, related peripherals, and other technical collateral, is available in the OMAP5912 Product Folder on TI's website: www.ti.com/omap5912.

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