TMS320C620x/C670x DSP Boot Modes and Configuration Reference Guide

Literature Number: SPRU642
July 2003

Texas Instruments

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Preface

Read This First

About This Manual

This document describes the boot modes and device configuration used by the TMS320C620x/C670x digital signal processors (DSPs) of the TMS320C6000™ DSP family. It also describes the available boot processes and explains how the device is reset.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

TMS320C6000 CPU and Instruction Set Reference Guide (literature number SPRU189) describes the TMS320C6000™ CPU architecture, instruction set, pipeline, and interrupts for these digital signal processors.

TMS320C6000 Peripherals Reference Guide (literature number SPRU190) describes the peripherals available on the TMS320C6000™ DSPs.

TMS320C6000 Technical Brief (literature number SPRU197) gives an introduction to the TMS320C62x™ and TMS320C67x™ DSPs, development tools, and third-party support.

TMS320C64x Technical Overview (SPRU395) gives an introduction to the TMS320C64x™ DSP and discusses the application areas that are enhanced by the TMS320C64x VelociTI™.

TMS320C6000 Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

TMS320C6000 Code Composer Studio Tutorial (literature number SPRU301) introduces the Code Composer Studio™ integrated development environment and software tools.

Code Composer Studio Application Programming Interface Reference Guide (literature number SPRU321) describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

TMS320C6x Peripheral Support Library Programmer's Reference (literature number SPRU273) describes the contents of the TMS320C6000™ peripheral support library of functions and macros. It lists functions and macros both by header file and alphabetically, provides a complete description of each, and gives code examples to show how they are used.

TMS320C6000 Chip Support Library API Reference Guide (literature number SPRU401) describes a set of application programming interfaces (APIs) used to configure and control the on-chip peripherals.

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Contents

Figures

Tables

Boot Modes and Configuration

This document describes the boot modes and device configuration used by the TMS320C620x/C670x digital signal processors (DSPs) of the TMS320C6000™ DSP family. It also describes the available boot processes and explains how the device is reset.

1 Overview

The C6000™ DSP uses a variety of boot configurations to determine what actions the devices are to perform after reset for proper device initialization. Each C6000 device has some or all of the following boot configuration options:

- Selection of the memory map, which determines whether internal or external memory is mapped at address 0.
- Selection of the type of external memory mapped at address 0 if external memory is mapped there.
- Selection of the boot process used to initialize the memory at address 0 before the CPU is released from reset.
- Device configurations.

2 Device Reset

The external device reset uses an active (low) signal, $\overline{\text{RESET}}$. While $\overline{\text{RESET}}$ is low, the device is held in reset and is initialized to the prescribed reset state. Most 3-state outputs are placed in the high-impedance state, and most other outputs are returned to their default states. The rising edge of $\overline{\text{RESET}}$ starts the processor running with the prescribed boot configuration. The $\overline{\text{RESET}}$ pulse may have to be increased if the phase-locked loop (PLL) requires synchronization following power up or when PLL configuration pins change during reset. For reset timing refer to the device-specific datasheet.

3 Memory Map

3.1 C6201/C6205/C6701 DSP Memory Map

The C6201/C6205/C6701 DSP has two memory maps, MAP 0 and MAP 1, summarized in Table 1. MAP 0 has external memory mapped at address 0 and MAP 1 has internal memory mapped at address 0.

Table 1. TMS320C6201/C6205/C6701 DSP Memory Map

Address Range (Hex)	Size (Bytes)	MAP 0	MAP 1
0000 0000−0000 FFFF	64K	External memory interface CE0	Internal program RAM
0001 0000−003F FFFF	4M−64K	External memory interface CE0	Reserved
0040 0000−00FF FFFF	12M	External memory interface CE0	External memory interface CE0
0100 0000−013F FFFF	4M	External memory interface CE1	External memory interface CE0
0140 0000−0140 FFFF	64K	Internal program RAM	External memory interface CE1
0141 0000−017F FFFF	4M−64K	Reserved	External memory interface CE1
0180 0000−0183 FFFF	256K	Internal peripheral bus EMIF registers	
0184 0000−0187 FFFF	256K	Internal peripheral bus DMA controller registers	
0188 0000−018B FFFF	256K	Internal peripheral bus HPI registers (C6201/C6701 DSP)†	
018C 0000−018F FFFF	256K	Internal peripheral bus McBSP0 registers	
0190 0000−0193 FFFF	256K	Internal peripheral bus McBSP1 registers	
0194 0000−0197 FFFF	256K	Internal peripheral bus timer0 registers	
0198 0000−019B FFFF	256K	Internal peripheral bus timer1 registers	
019C 0000−019F FFFF	256K	Internal peripheral bus interrupt selector registers	
01A0 0000−01A3 FFFF	256K	Reserved	
01A4 0000−01A8 FFFF	320K	Internal peripheral bus PCI registers (C6205 DSP only)†	
01A9 0000−01FF FFFF	6M−576K	Internal peripheral bus (reserved)	
0200 0000−02FF FFFF	16M	External memory interface CE2	
0300 0000−03FF FFFF	16M	External memory interface CE3	
0400 0000−3FFF FFFF	1G−64M	Reserved	
4000 0000−4FFF FFFF	256M	Reserved	
5000 0000−5FFF FFFF	256M	Reserved	
6000 0000−6FFF FFFF	256M	Reserved	
7000 0000−7FFF FFFF	256M	Reserved	
8000 0000−8000 FFFF	64K	Internal data RAM	
8001 0000−FFFF FFFF	2G−64K	Reserved	

† Address range is reserved on other devices.

3.2 C6202(B) DSP Memory Map

The C6202(B) DSP has two memory maps, MAP 0 and MAP 1, summarized in Table 2. The two memory maps are supersets of the C6201/C6701 DSP memory maps. All valid C6201/C6701 DSP address ranges are valid on the C6202(B) DSP.

Table 2. TMS320C6202(B) DSP Memory Map

Address Range (Hex)	Size (Bytes)	MAP 0	MAP 1
0000 0000−0003 FFFF	256K	External memory interface CE0	Internal program RAM
0004 0000−003F FFFF	4M−256K	External memory interface CE0	Reserved
0040 0000−00FF FFFF	12M	External memory interface CE0	External memory interface CE0
0100 0000−013F FFFF	4M	External memory interface CE1	External memory interface CE0
0140 0000−0143 FFFF	256K	Internal program RAM	External memory interface CE1
0144 0000−017F FFFF	4M−256K	Reserved	External memory interface CE1
0180 0000−0183 FFFF	256K	Internal peripheral bus EMIF registers	
0184 0000−0187 FFFF	256K	Internal peripheral bus DMA controller registers	
0188 0000−018B FFFF	256K	Internal peripheral bus expansion bus registers	
018C 0000−018F FFFF	256K	Internal peripheral bus McBSP0 registers	
0190 0000−0193 FFFF	256K	Internal peripheral bus McBSP1 registers	
0194 0000−0197 FFFF	256K	Internal peripheral bus timer0 registers	
0198 0000−019B FFFF	256K	Internal peripheral bus timer1 registers	
019C 0000−019C 01FF	512	Internal peripheral bus interrupt selector registers	
019C 0200−019C FFFF	256K−512	Internal peripheral bus power-down registers	
01A0 0000−01A3 FFFF	256K	Reserved	
01A4 0000−01A7 FFFF	256K	Internal peripheral bus McBSP2 registers	
01A8 0000−01FF FFFF	5.5M	Reserved	
0200 0000−02FF FFFF	16M	External memory interface CE2	
0300 0000−03FF FFFF	16M	External memory interface CE3	
0400 0000−3FFF FFFF	1G−64M	Reserved	
4000 0000−4FFF FFFF	256M	Expansion bus XCE0	
5000 0000−5FFF FFFF	256M	Expansion bus XCE1	
6000 0000−6FFF FFFF	256M	Expansion bus XCE2	
7000 0000−7FFF FFFF	256M	Expansion bus XCE3	
8000 0000−8001 FFFF	128K	Internal data RAM	
8002 0000−FFFF FFFF	2G−128K	Reserved	

3.3 C6203(B) DSP Memory Map

The C6203(B) DSP has two memory maps, MAP 0 and MAP 1, summarized in Table 3. The C6203(B) DSP memory map is very similar to the C6202 DSP memory map. The differences exist because of the increased amount of internal memory available on the C6203(B) DSP.

Table 3. TMS320C6203(B) DSP Memory Map

Address Range (Hex)	Size (Bytes)	MAP 0	MAP 1
0000 0000–0005 FFFF	384K	External memory interface CE0	Internal program RAM
0006 0000–003F FFFF	4M–384K	External memory interface CE0	Reserved
0040 0000–00FF FFFF	12M	External memory interface CE0	External memory interface CE0
0100 0000–013F FFFF	4M	External memory interface CE1	External memory interface CE0
0140 0000–0145 FFFF	384K	Internal program RAM	External memory interface CE1
0146 0000–017F FFFF	4M–384K	Reserved	External memory interface CE1
0180 0000–0183 FFFF	256K	Internal peripheral bus EMIF registers	
0184 0000–0187 FFFF	256K	Internal peripheral bus DMA controller registers	
0188 0000–018B FFFF	256K	Internal peripheral bus expansion bus registers	
018C 0000–018F FFFF	256K	Internal peripheral bus McBSP0 registers	
0190 0000–0193 FFFF	256K	Internal peripheral bus McBSP1 registers	
0194 0000–0197 FFFF	256K	Internal peripheral bus timer0 registers	
0198 0000–019B FFFF	256K	Internal peripheral bus timer1 registers	
019C 0000–019C 01FF	512	Internal peripheral bus interrupt selector registers	
019C 0200–019F FFFF	256K–512	Internal peripheral bus power-down registers	
01A0 0000–01A3 FFFF	256K	Reserved	
01A4 0000–01A7 FFFF	256K	Internal peripheral bus McBSP2 registers	
01A8 0000–01FF FFFF	5.5M	Reserved	
0200 0000–02FF FFFF	16M	External memory interface CE2	
0300 0000–03FF FFFF	16M	External memory interface CE3	
0400 0000–3FFF FFFF	1G–64M	Reserved	
4000 0000–4FFF FFFF	256M	Expansion bus XCE0	
5000 0000–5FFF FFFF	256M	Expansion bus XCE1	
6000 0000–6FFF FFFF	256M	Expansion bus XCE2	
7000 0000–7FFF FFFF	256M	Expansion bus XCE3	
8000 0000–8007 FFFF	512K	Internal data RAM	
8008 0000–FFFF FFFF	2G–512K	Reserved	

3.4 C6204 DSP Memory Map

The C6204 DSP has two memory maps, MAP 0 and MAP 1, summarized in Table 4. MAP 0 has external memory mapped at address 0 and MAP 1 has internal memory mapped at address 0.

Table 4. TMS320C6204 DSP Memory Map

Address Range (Hex)	Size (Bytes)	MAP 0	MAP 1
0000 0000−0000 FFFF	64K	External memory interface CE0	Internal program RAM
0001 0000−003F FFFF	4M−64K	External memory interface CE0	Reserved
0040 0000−00FF FFFF	12M	External memory interface CE0	External memory interface CE0
0100 0000−013F FFFF	4M	External memory interface CE1	External memory interface CE0
0140 0000−0140 FFFF	64K	Internal program RAM	External memory interface CE1
0141 0000−017F FFFF	4M−64K	Reserved	External memory interface CE1
0180 0000−0183 FFFF	256K	Internal peripheral bus EMIF registers	
0184 0000−0187 FFFF	256K	Internal peripheral bus DMA controller registers	
0188 0000−018B FFFF	256K	Internal peripheral bus XBUS registers	
018C 0000−018F FFFF	256K	Internal peripheral bus McBSP0 registers	
0190 0000−0193 FFFF	256K	Internal peripheral bus McBSP1 registers	
0194 0000−0197 FFFF	256K	Internal peripheral bus timer0 registers	
0198 0000−019B FFFF	256K	Internal peripheral bus timer1 registers	
019C 0000−019F FFFF	256K	Internal peripheral bus interrupt selector registers	
01A0 0000−01A3 FFFF	256K	Reserved	
01A4 0000−01A8 FFFF	320K	Reserved	
01A9 0000−01FF FFFF	6M−576K	Internal peripheral bus (reserved)	
0200 0000−02FF FFFF	16M	External memory interface CE2	
0300 0000−03FF FFFF	16M	External memory interface CE3	
0400 0000−3FFF FFFF	1G−64M	Reserved	
4000 0000−4FFF FFFF	256M	Expansion bus XCE0	
5000 0000−5FFF FFFF	256M	Expansion bus XCE1	
6000 0000−6FFF FFFF	256M	Expansion bus XCE2	
7000 0000−7FFF FFFF	256M	Expansion bus XCE3	
8000 0000−8000 FFFF	64K	Internal data RAM	
8001 0000−FFFF FFFF	2G−64K	Reserved	

4 Boot Processes

The boot process is determined by the boot configuration selected, as described in section 5. Up to three types of boot processes are available:

- **No boot process:** The CPU begins direct execution from the memory located at address 0. If SDRAM is used in the system, the CPU is held until SDRAM initialization is complete. Operation is undefined if invalid code is located at address 0.

- **ROM boot process**: The program located in external ROM is copied to address 0 by the DMA controller. Although the boot process begins when the device is released from external reset, this transfer occurs while the CPU is internally stalled. For the C620x/C670x DSP, these values are expected to be stored in little-endian format in the external memory, typically a ROM device.

  The transfer is automatically done by the DMA controller as a single-frame block transfer from the ROM to address 0. The DMA copies 64K bytes from CE1 to address 0, using default ROM timings. After completion of the block transfer, the CPU is unstalled and allowed to run from address 0.

- **Host boot process**: The CPU is internally stalled while the remainder of the device is released. During this period, an external host can initialize the CPU memory space as necessary through the host interface, including internal configuration registers, such as those that control the EMIF or other peripherals. Once the host is finished with all necessary initialization, it must set the DSPINT to complete the boot process. This transition causes the boot configuration logic to unstall the CPU. The CPU then begins execution from address 0. The DSPINT condition is not latched by the CPU, because it occurs while the CPU is stalled. Also, DSPINT unstalls the CPU only if the host boot process is selected. All memory may be written to and read by the host. This allows for the host to verify what it sends to the processor, if required. After the CPU is unstalled, the CPU needs to clear the DSPINT bit; otherwise, no more DSPINTs can be received.

Note:

The host interface used during host boot varies between different devices, depending on the host interface peripheral that is available on the device. Refer to the device-specific datasheet for the specific peripheral set. One of the following host interfaces is used for host boot:

- **Host Port Interface (HPI):** For devices with HPI, the HPI can be used for host boot. The HPI is always a slave interface, and needs no special configuration.
- **Expansion Bus (XBUS):** For devices with XBUS, the XBUS can be used for the host boot. The type of host interface is determined by a set of latched signals during reset.
- **Peripheral Component Interconnect (PCI):** For devices with PCI, the PCI can be used for the host boot.

5 Boot and Device Configuration

Several device settings are configured at reset to determine how the device operates. These settings include the boot configuration, the input clock mode, endian mode, and other device-specific configurations.

For the C620x/C670x DSP, the boot configuration is determined by the BOOTMODE[4:0] pin values. Table 5 lists all the values for BOOTMODE[4:0], as well as the associated memory maps and boot processes for the C620x/C670x DSP. For example the value 00000b on BOOTMODE[4:0] selects memory map 0; indicates that the memory type at address 0 is synchronous DRAM (SDRAM) and that no boot process is selected. SDWID is the SDRAM column width select bit in the EMIF SDRAM control register (SDCTL).

5.1 Memory at Reset Address

For the C620x/C670x DSP with multiple memory maps, the boot configuration determines the type of memory located at the reset address for processor operation, address 0 as shown in Table 5. When the boot configuration selects MAP 1, this memory is internal. When the device mode is in MAP 0, the memory is external. When external memory is selected, the boot configuration also determines the type of memory at the reset address. These options effectively provide alternative reset values to the appropriate EMIF control registers.

Table 5. TMS320C620x/C670x DSP Boot Configuration (BOOTMODE[4:0]) Summary

BOOTMODE[4:0]	Memory Map	Memory at Address 0	Boot Process
00000	MAP 0	SDRAM: SDWID = 0 (512 elements per row)†	None
00001	MAP 0	SDRAM: SDWID = 1 (256 elements per row)†	None
00010	MAP 0	32-bit asynchronous with default timing	None
00011	MAP 0	1/2× rate SBSRAM	None
00100	MAP 0	1× rate SBSRAM	None
00101	MAP 1	Internal	None
00110	MAP 0	External: default values	Host boot (HPI/XBUS/PCI)
00111	MAP 1	Internal	Host boot (HPI/XBUS/PCI)
01000	MAP 0	SDRAM: four 8-bit devices (SDWID = 0)	8-bit ROM with default timings
01001	MAP 0	SDRAM: two16-bit devices (SDWID = 1)	8-bit ROM with default timings
01010	MAP 0	32-bit asynchronous with default timing	8-bit ROM with default timings
01011	MAP 0	1/2× rate SBSRAM	8-bit ROM with default timings
01100	MAP 0	1× rate SBSRAM	8-bit ROM with default timings
01101	MAP 1	Internal	8-bit ROM with default timings
01110−01111	−	Reserved	−
10000	MAP 0	SDRAM: four 8-bit devices(SDWID=0)	16-bit ROM with default timings
10001	MAP 0	SDRAM: two 16-bit devices (SDWID = 1)	16-bit ROM with default timings
10010	MAP 0	32-bit asynchronous with default timing	16-bit ROM with default timings
10011	MAP 0	1/2× rate SBSRAM	16-bit ROM with default timings
10100	MAP 0	1× rate SBSRAM	16-bit ROM with default timings
10101	MAP 1	Internal	16-bit ROM with default timings
10110−10111	−	Reserved	−
11000	MAP 0	SDRAM: four 8-bit devices (SDWID = 0)	32-bit ROM with default timings
11001	MAP 0	SDRAM: two 16-bit devices (SDWID = 1)	32-bit ROM with default timings
11010	MAP 0	32-bit asynchronous with default timing	32-bit ROM with default timings
11011	MAP 0	1/2× rate SBSRAM	32-bit ROM with default timings
11100	MAP 0	1× rate SBSRAM	32-bit ROM with default timings
11101	MAP 1	Internal	32-bit ROM with default timings
11110−11111	−	Reserved	−

† SDWID is the SDRAM column width select bit in the EMIF SDRAM control register (SDCTL). See the *TMS320C6000 DSP External Memory Interface (EMIF) Reference Guide* (SPRU266).

5.2 C6201/C6701 DSP Boot and Device Configuration

The C6201/C6701 DSP latches the following configurations during device reset:

- **Boot Configuration:** The dedicated BOOTMODE[4:0] pins determine the device boot configurations as shown in Table 5.
- **Input Clock Mode:** The on-chip PLL frequency multiplier is configured through static CLKMODE input pins. Refer to the device-specific datasheet for details.
- **Endian Mode:** The LENDIAN input pin is used to configure the device to operate in either big endian (LENDIAN = 0) or little endian (LENDIAN = 1) mode.

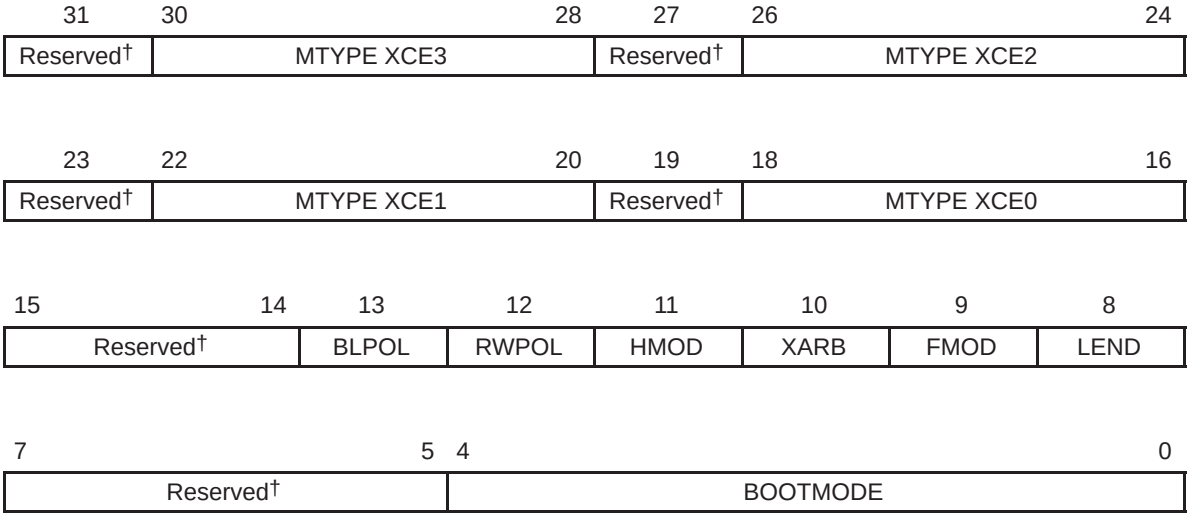
5.3 C6202(B)/C6203(B)/C6204 DSP Boot and Device Configuration

The C6202(B)/C6203(B)/C6204 DSP latches the following configurations during device reset:

- **Boot Configuration:** The pull-up/pull-down resistors on the XBUS are used to determine the boot configuration (XD[4:0] pins) and other device configurations (XD[31:5] pins) at reset. The XD[4:0] lines directly map to BOOTMODE[4:0] described in Table 5. Reserved configuration fields should be pulled-down.
- **Input Clock Mode:** Configured through the CLKMODE input pins at reset. Refer to the device-specific datasheet for details.
- **Endian Mode:** The pull-up/pull-down resistor on the XBUS XD[8] pin is used to configure the device to operate in either big endian (XD[8] = 0) or little endian (XD[8] = 1) mode.

Detailed description of boot and device configurations is shown in Figure 1 and described in Table 6.

Figure 1. TMS320C6202(B)/C6203(B)/C6204 DSP Boot and Device Configuration via Pull-Up/Pull-Down Resistors on XD[31:0]



† All reserved fields should be pulled down.

Table 6. TMS320C6202(B)/C6203(B)/C6204 DSP Boot and Device Configuration Description

XD Bit	Field	Value	Description
31	Reserved	0	Reserved. The reserved field should be pulled down.
30−28	MTYPE3	0−7h	XCE3 memory type .
		0−1h	Reserved
		2h	32-bit wide asynchronous interface
		3h−4h	Reserved
		5h	32-bit wide FIFO interface
		6h−7h	Reserved
27	Reserved	0	Reserved. The reserved field should be pulled down.

Table 6. TMS320C6202(B)/C6203(B)/C6204 DSP Boot and Device Configuration Description (Continued)

XD Bit	Field	Value	Description
26−24	MTYPE2	0−7h	XCE2 memory type.
		0−1h	Reserved
		2h	32-bit wide asynchronous interface
		3h−4h	Reserved
		5h	32-bit wide FIFO interface
		6h−7h	Reserved
23	Reserved	0	Reserved. The reserved field should be pulled down.
22−20	MTYPE1	0−7h	XCE1 memory type.
		0−1h	Reserved
		2h	32-bit wide asynchronous interface
		3h−4h	Reserved
		5h	32-bit wide FIFO interface
		6h−7h	Reserved
19	Reserved	0	Reserved. The reserved field should be pulled down.
18−16	MTYPE0	0−7h	XCE0 memory type.
		0−1h	Reserved
		2h	32-bit wide asynchronous interface
		3h−4h	Reserved
		5h	32-bit wide FIFO interface
		6h−7h	Reserved
15−14	Reserved	0	Reserved. The reserved field should be pulled down.
13	BLPOL		Determines polarity of the XBLAST signal when the DSP is a slave on the XBUS. When the DSP initiates a transfer on the expansion bus, XBLAST is always active low.
		0	XBLAST is active low.
		1	XBLAST is active high.

Table 6. TMS320C6202(B)/C6203(B)/C6204 DSP Boot and Device Configuration Description (Continued)

XD Bit	Field	Value	Description
12	RWPOL		Determines polarity of XBUS read/write signal.
		0	Write is active-high.
		1	Read is active-high.
11	HMOD		Host mode.
		0	External host interface operates in asynchronous slave mode.
		1	External host interface is in synchronous master/slave mode.
10	XARB		XBUS arbiter (status in expansion bus global control register (XBGC)).
		0	Internal XBUS arbiter is disabled.
		1	Internal XBUS arbiter is enabled.
9	FMOD		FIFO mode (status in expansion bus global control register (XBGC)).
		0	Glue is used for FIFO read interface in all XCE spaces operating in FIFO mode. XOE can be used in all XCE spaces.
		1	XOE is reserved for use only in $\overline{\text{XCE3}}$ for FIFO read mode. XOE is disabled in all other XCE spaces.
8	LEND		Little endian mode.
		0	System operates in big-endian mode.
		1	System operates in little-endian mode.
7−5	Reserved	0	Reserved. The reserved field should be pulled down.
4−0	BOOTMODE	0−1Fh	Determines the boot-mode of the device. See Table 5.

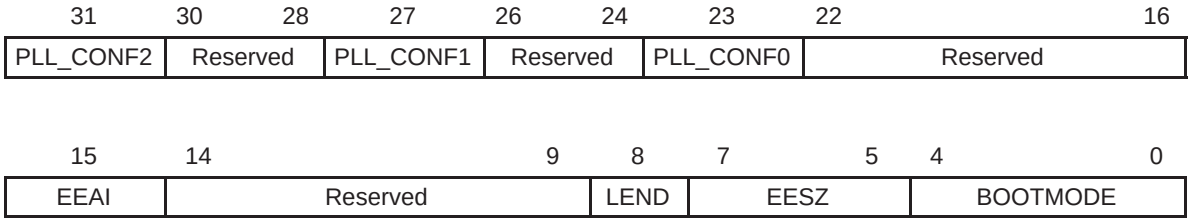
5.4 C6205 DSP Boot and Device Configuration

The C6205 DSP latches the following configurations during device reset:

- **Boot Configuration:** The pull-up/pull-down resistors on the EMIF data bus are used to determine the boot configuration (ED[4:0] pins), and other device configurations (ED[31:5] pins) at reset. The ED[4:0] lines directly map to BOOTMODE[4:0] described in Table 5. Reserved configuration fields should be pulled down.
- **Input Clock Mode:** The CLKMODE0 input pin is used in conjunction with the EMIF data bus pins to determine the input clock mode at reset. Refer to the device-specific datasheet for details.
- **Endian Mode:** The pull-up/pull-down resistor on the EMIF data bus ED[8] pin is used to configure the device to operate in either big endian (ED[8] = 0) or little endian (ED[8] = 1) mode.

Detailed description of boot and device configuration is shown in Figure 2 and described in Table 7.

Figure 2. TMS320C6205 DSP Boot and Device Configuration via Pull-Up/Pull-Down Resistors on ED[31:0]



† All reserved fields should be pulled down.

Table 7. TMS320C6205 DSP Boot and Device Configuration Description

ED Bit	Field	Value	Description
31	PLL_CONF2		On-chip PLL is enabled or disabled by CLKMODE0 pin. When CLKMODE0 = 0, on-chip PLL is bypassed. When CLKMODE0 = 1, CPU clock is determined by PLL_CONF2, PLL_CONF1, and PLL_CONF0 bits. See Table 8. Note that CLKMODE0 acts as a PLL enable pin and the ED pins (pins 31, 27, and 23) determine the PLL multiplier option.
30−28	Reserved	0	Reserved. The reserved field should be pulled down.

Table 7. TMS320C6205 DSP Boot and Device Configuration Description (Continued)

ED Bit	Field	Value	Description
27	PLL_CONF1		On-chip PLL is enabled or disabled by CLKMODE0 pin. When CLKMODE0 = 0, on-chip PLL is bypassed. When CLKMODE0 = 1, CPU clock is determined by PLL_CONF2, PLL_CONF1, and PLL_CONF0 bits. See Table 8. Note that CLKMODE0 acts as a PLL enable pin and the ED pins (pins 31, 27, and 23) determine the PLL multiplier option.
26−24	Reserved	0	Reserved. The reserved field should be pulled down.
23	PLL_CONF0		On-chip PLL is enabled or disabled by CLKMODE0 pin. When CLKMODE0 = 0, on-chip PLL is bypassed. When CLKMODE0 = 1, CPU clock is determined by PLL_CONF2, PLL_CONF1, and PLL_CONF0 bits. See Table 8. Note that CLKMODE0 acts as a PLL enable pin and the ED pins (pins 31, 27, and 23) determine the PLL multiplier option.
22−16	Reserved	0	Reserved. The reserved field should be pulled down.
15	EEAI		EEPROM autoinitialization.
		0	PCI uses default values.
		1	Read configure value from EEPROM.
14−9	Reserved	0	Reserved. The reserved field should be pulled down.
8	LEND		Little endian mode.
		0	System operates in big-endian mode.
		1	System operates in little-endian mode.
7−5	EESZ	0−7h	EEPROM size selection (EEPROM is always 16-bit).
		0	No EEPROM
		1h	1K
		2h	2K
		3h	4K
		4h	16K
		5h−7h	Reserved
4−0	BOOTMODE	0−1Fh	Determines the boot-mode of the device. See Table 5.

*Table 8. CPU Clock Rate as Determined by PLL_CONF*n *Bits* (*C6205 DSP)*

PLL_CONF*n* Bits (ED[31, 27, 23])	**CPU Clock Rate**
000	CLKIN × 1 (PLL Bypass)
001	CLKIN × 4
010	CLKIN × 8
011	CLKIN × 10
100	CLKIN × 6
101	CLKIN × 9
110	CLKIN × 7
111	CLKIN × 11

Index

B

C

D

M

N

O

R

T