High-Performance, High-Precision, Smart Sensing for Industrial Drives

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ABSTRACT

In higher end control applications such as servo drives, high-resolution feedback is required to provide precise phase current measurements for low-torque ripple and precision positioning; however, for some measurements, precise sample rates are more important than higher resolution, such as when making high-speed, low-side shunt current measurements. To support different accuracy requirements, the Delfino F2837x MCU architecture offers flexible ADCs that can support two resolution modes: 16-bit resolution at 1.1 MSPS and 12-bit resolution at 3.5 MSPS. It also features four independently integrated analog-to-digital converters (ADCs) that provide simultaneous conversions, thereby, enabling industrial drive systems to accurately monitor multiple signals in real time. For example, in a servo drive, designers can monitor the voltages and currents of a three-phase motor while simultaneously sampling high-frequency feedback from a resolver or SIN/COS transducer. In fact, the ADC resources on the F2837x can easily handle the monitoring requirements of a two motor system as well.

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1 Analog-to-Digital Converter (ADC)

The F2837xD includes four independent high-performance ADC modules which can be accessed by both CPU subsystems, allowing the device to efficiently manage multiple analog signals for enhanced overall system throughput. Each ADC module has a single sample-and-hold (S/H) circuit and using multiple ADC modules enables simultaneous sampling or independent operation. The ADC module is implemented using a successive approximation (SAR) type ADC with a configurable resolution of either 16-bits or 12-bits. For 16-bit resolution, the ADC performs differential signal conversions with a performance of 1.1 MSPS, yielding 4.4 MSPS for the device. In differential signal mode, a pair of pins (positive input ADCINxP and negative input ADCINxN) is sampled and the input applied to the converter is the difference between the two pins (ADCINxP – ADCINxN). A benefit of differential signaling mode is the ability to cancel noise that may be introduced common to both inputs. For 12-bit resolution, the ADC performs single-ended signal conversions with a performance of 3.5 MSPS, yielding 14 MSPS for the device. In single-ended mode, a single pin (ADCINx) is sampled and applied to the input of the converter.

The ADC triggering and conversion sequencing is managed by a series of Start-of-Conversion (SOCx) configuration registers. Each SOCx register configures a single channel conversion, where the SOCx register specifies the trigger source that starts the conversion, the channel to convert, and the acquisition sample window duration. Multiple SOCx registers can be configured for the same trigger, channel, and/or acquisition window. Configuring multiple SOCx registers to use the same trigger will cause that trigger to perform a sequence of conversions, and configuring multiple SOCx registers for the same trigger and channel can be used to oversample the signal.

The various trigger sources that can be used to start an ADC conversion include the General-Purpose Timers from each CPU subsystem, the ePWM modules, an external pin, and by software. Also, the flag setting of either ADCINT1 or ADCINT2 can be configured as a trigger source which can be used for continuous conversion operation.
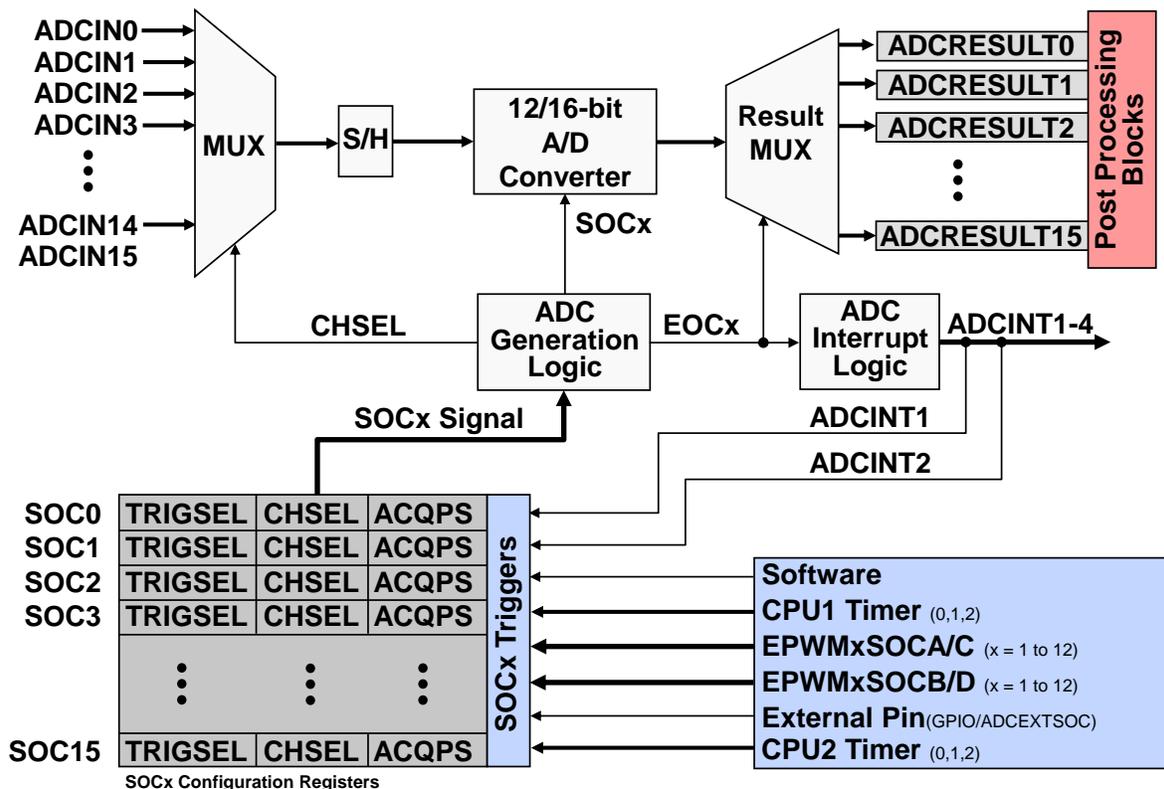

Figure 1. Analog-to-Digital Converter (ADC) Block Diagram

When multiple triggers are received at the same time, the ADC conversion priority determines the order in which they are converted. Three different priority modes are supported. The default priority mode is round robin, where no SOCx has an inherently higher priority over another, and the priority depends upon a round robin pointer. The round robin pointer operates in a circular fashion, constantly wrapping around to the beginning. In high priority mode, one or more than one SOCx is assigned as high priority. The high priority SOCx can then interrupt the round robin wheel, and after it has been converted the wheel will continue where it was interrupted. High priority mode is assigned first to SOC0 and then in increasing numerical order. If two high priority SOCx triggers occur at the same time, the lower number will take precedence. Burst mode allows a single trigger to convert one or more than one SOCx sequentially at a time. This mode uses a separate Burst Control register to select the burst size and trigger source.

After each SOCx channel conversion is completed, an end-of-conversion (EOC) signal can be used to trigger an ADC interrupt. Each ADC module has four configurable ADC interrupts (ADCINT1-4) which can be triggered by any of the EOC signals. The ADC can be configured to generate the EOC signal either at the beginning of the conversion or one cycle prior to the conversion being written into the result register. Generating the EOC signal at the beginning of the conversion provides "just-in-time" reading of the ADC results, which reduces the sample to output delay and enables faster system response.

To further enhance the capabilities of the ADC, each ADC module incorporates four post-processing blocks (PPB), and each PPB can be linked to any of the ADC result registers. The PPBs can be used for offset correction, calculating an error from a set-point, detecting a limit and zero-crossing, and capturing a trigger-to-sample delay. Offset correction can simultaneously remove an offset associated with an ADCIN channel that was possibly caused by external sensors or signal sources with zero-overhead, thereby saving processor cycles. Error calculation can automatically subtract out a computed error from a set-point or expected result register value, reducing the sample to output latency and software overhead. Limit and zero-crossing detection automatically performs a check against a high/low limit or zero-crossing and can generate a trip to the ePWM and/or generate an interrupt. This lowers the sample to ePWM latency and reduces software overhead. Also, it can trip the ePWM based on an out-of-range ADC conversion without any CPU intervention which is useful for safety conscious applications. Sample delay capture records the delay between when the SOCx is triggered and when it begins to be sampled. This can enable software techniques to be used for reducing the delay error.

2 Buffered Digital-to-Analog Converter (DAC)

The F2837xD includes three buffered 12-bit DAC modules that can provide a programmable reference output voltage capable of driving an external load. Values written to the DAC can take effect immediately or be synchronized with ePWM events.

3 Sigma-Delta Filter Module (SDFM)

The SDFM is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each channel can receive an independent delta-sigma modulator bit stream which is processed by four individually programmable digital decimation filters. The filters include a fast comparator for immediate digital threshold comparisons for over-current and under-current monitoring. Also, a filter-bypass mode is available to enable data logging, analysis, and customized filtering. The SDFM pins are configured using the GPIO multiplexer. A key benefit of the SDFM is it enables a simple, cost-effective, and safe high-voltage isolation boundary.

4   For More Information

- To learn more about DesignDRIVE software, tools and kits for industrial drives and servo control development, visit www.ti.com/tool/DesignDRIVE

- To learn even more on the sensing circuits included on the Delfino F2837x microcontrollers, see the device-specific product group and data sheet at: www.ti.com/delfino, the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8) or the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual* (SPRUHX5).

- To view online training on how to use DesignDRIVE solutions, see DesignDRIVE training portal.

- For an introduction and general overview to the TMS320F2837xD microcontroller, see *The TMS320F2837xD Architecture: Achieving a New Level of High Performance Technical Brief* (SPRT720)

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