TMS320C6657/55/54/52

Power-efficient DSPs for applications requiring high performance

Texas Instruments

Texas Instruments' TMS320C6657/55/54/52 digital signal processors (DSPs) are well suited for high-performance, low-power applications in areas such as machine vision and analytics, imaging, avionics and defense, power protection as well as certain infrastructure applications. These markets all have similar needs for high-performance, high-speed peripherals and power efficiency in small packaging. The C665x DSPs are based on TI's KeyStone™ multicore architecture and integrate single- or dual-core C66x DSPs to offer real-time performance that helps customers realize R&D savings while getting to market faster.

TI's C6657/55/54/52 DSPs are high-performance, multicore processors with fixed- and floating-point capabilities, delivering real-time performance with the speed and peripheral support needed for performance-intensive applications at the lowest power possible. The full-featured dual-core C6657 uses just 3.0W at 1 GHz (nominal temperature) while the more specialized single-core C6652, with its reduced feature set, is targeted for power-sensitive applications and uses ~1.5W at nominal temperature. The C665x DSPs also bring a new low price point for TI's C66x multicore processors, allowing customers to expand their use into new markets while using less board space with its smaller 21 × 21-mm package. These devices are also in a lower profile (2.99-mm height) package, enabling minimal overall product packaging size and weight.

With both fixed- and floating-point DSP cores on the same device, the C665x DSPs enable designers to take advantage of rapid algorithm prototyping and quick software redesigns, reducing costs and development time. Fewer C665x DSPs are needed to provide the same amount of processing power as previous generations and/or competitive products, so designers can enjoy simplified programming with fewer cores. Upgrading from previous versions of C64x and C67x DSPs is easy and quick, with 100% code compatibility.

Target applications

The C6657/55/54/52 DSPs have been designed to support high-performance applications including machine vision and analytics, imaging, avionics & defense, power protection as well as certain infrastructure applications. With a multicore architecture combined with hardware and software coprocessors and accelerators, the C665x DSPs deliver the performance needed at the best power efficiency possible.

Avionics & Defense – The C665x DSPs can be used in a variety of mission-critical applications ranging from Avionics and defense to public safety and radar. These applications have a demanding set of DSP requirements including need for high DSP performance as well as capability to handle both fixed- and floating-point computation. Large on-chip memories and multiple high-bandwidth I/O are critical for storing and transporting data. Solutions must also be scalable, power efficient and easy to use. DSPs must meet these demands while operating in extreme environments,

Key features

- Performance – fastest fixed- and floating-point DSP core
  - C6657 dual core at 1 GHz and 1.25 GHz
  - C6655 single core at 1 GHz and 1.25 GHz
  - C6654 single core at 850 MHz and 750 MHz
  - C6652 single core at 600 MHz
  - 80 GMACS /40 GFLOPS for the dual-core 1.25-GHz C6657
- Architecture
  - KeyStone architecture
  - Multicore Navigator
  - TeraNet – On-chip switch fabric
- Coprocessor accelerators (C6657/55 only)
  - TCP3d – Turbo Decoder
  - VCP2 ×2 – Viterbi Decoder
- High-speed input/output (I/O)
  - Serial RapidIO® V2.1 ×4 (C6657/55 only)
  - PCI Express Gen II single & double lanes (C6657/55/54 only)
  - Gigabit Ethernet port SGMII (C6657/55/54 only)
  - HyperLink (C6657/55 only)
  - DDR3
- C6657/55: 1333 MHz (32b)
- C6654/52: 1066 MHz (32b)
- Memory
  - 1 MB Local L2 memory dedicated per core
  - 1 MB shared L2 (C6657/55 only)
- Power @ nominal (65°C case temperature)
  - SmartReflex™ technology
  - C6657 @ 1 GHz ~3.0W
  - C6655 @ 1 GHz ~2.2W
  - C6654 @ 750 MHz ~2.0W
  - C6652 @ 600 MHz ~1.5W
- Temperature range (case temperatures)
  - 0°C to 85°C (commercial temp)
  - –40°C to 100°C (extended temp)
  - –55°C to 100°C (extended low temp – C6657 and C6655 only)
- Peripherals
  - Universal Parallel Port (UPP) and EMIF 16 (Muxed)
  - McBSP, UART, I^2C, SPI, GPIO
- Package: 21 × 21 mm FC-BGA

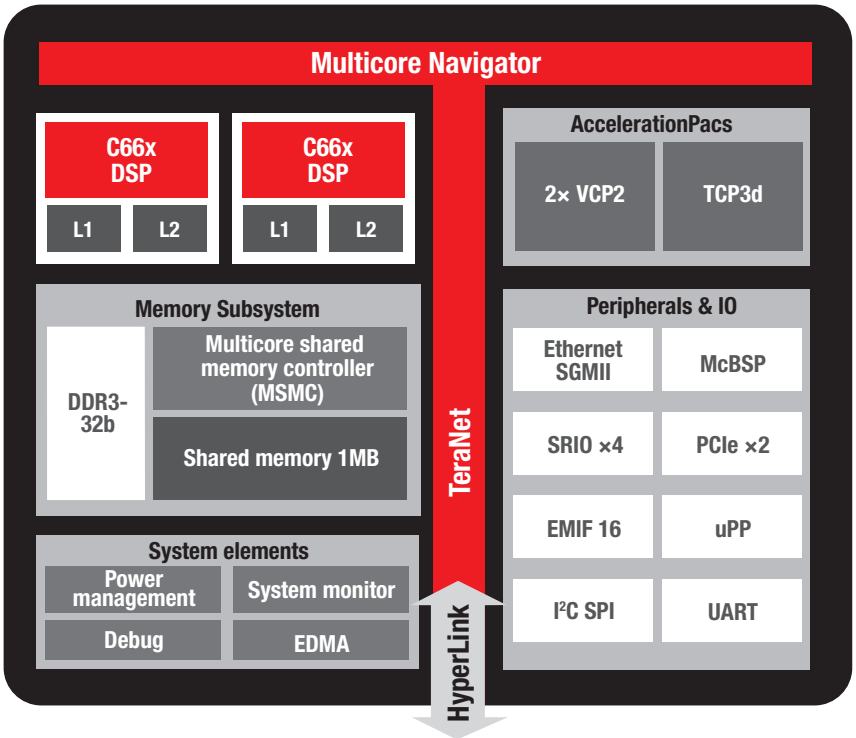
from –55°C to 100°C and beyond. TI has also optimized the power efficiency of these devices to industry leading levels—down to 2.2W (C6655) or 2.5W (C6657) at 1-GHz operation at nominal case temperature.

Machine Vision & Analytics – TI's DSP, such as C665x devices, provide best-in-class performance for real-time embedded analytics processing with scalable solutions from single camera solutions for traffic management and surveillance cameras to larger systems used in applications like inspection. As analytics systems continue to evolve and get closer to the end user, devices like the C665x are the right choice to help designers squeeze more performance out of their product, without sacrificing power. TI has also optimized the power efficiency of the devices used in these applications—down to 1.5W (C6652) and 2.0W (C6654) at nominal case temperature.

Power Protection & Grid Infrastructure – C665x devices offer high signal processing performance, up to 40 GFLOPS, at power consumptions targeted for fanless designs. The fixed- and floating-point capabilities of the C665x family of devices provides efficient real-time processing of sampled values in the small time windows required by protection relays or other grid monitoring equipment. TI offers libraries for common signal processing functions to make software development simple

High-performance solution for low-power, process-intensive applications

The TMS320C665x DSP family is designed specifically for high-performance, low-power applications. The family includes the dual-core C6657 (1 GHz or 1.25 GHz), single-core C6655 (1 GHz or 1.25 GHz), single-core C6654 (850 MHz and 750 MHz) and single-core C6652 (600 MHz). It also includes coprocessors and peripherals to drive any communications or avionics & defense-related applications. To make the transition from current C64x DSPs easier, the C665x is code compatible, allowing software reuse and maintaining value-added designs and IP. In addition, TI's C665x solution is scalable to meet the needs of all markets, from small portable designs to larger stationary equipment. With a common software base for a variety of products customers can realize the highest R&D efficiency possible as well as optimized product costs.

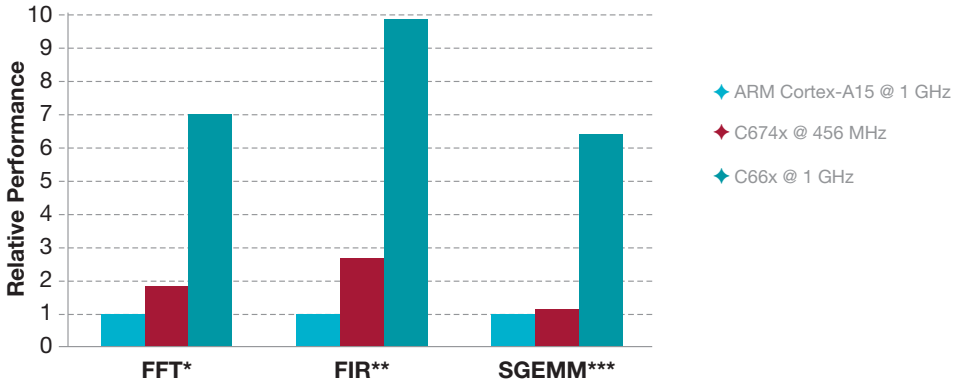


▲ *Figure 1: TMS320C6657 block diagram*

The C665x series is based on 40-nm process technology and delivers performance of up to 80 GMACs at 1.25 GHz, making it a cost-effective solution for high-performance programming challenges. With the addition of the floating-point capability, the C665x offers performance of up to 40 GFLOPS, making it a powerful communications processor as well. With both fixed- and floating-point processors on the same core, the C665x is able to perform up to 4 to 6 times faster than a fixed-point implementation alone (see Table 1 on the following page for more information). In addition, development and debug cycle time is significantly reduced from a three-month design cycle to just a few days.

The C665x DSPs integrate a large amount of on-chip memory organized as a two-level memory system, helping to minimize latency and increase system performance. The Level 1 (L1) program and data memories on the C665x device are 32 KB each per core. The Level 2 (L2) memory is shared between program and data space and is a total of 1,024 KB per core. The C6657 and C6655 devices also contain 1 MB of Multicore Shared Memory (MSM) that can be used as a shared L2 SRAM. A Multicore Shared Memory Controller (MSMC) prevents memory contention between the cores and arbitrates access to the shared memory between the cores and other IP blocks.

TI has included an optimized set of high-speed peripherals on the C665x devices including Serial RapidIO Gen2 (C6657/55) and PCI Express Gen2 (C6657/55/54). The Serial RapidIO port is a high-performance, low pin-count interconnect that creates a homogeneous interconnect environment, providing enhanced connectivity and control among the components. RapidIO is based on the memory and device addressing concepts where the transaction processing is managed completely by hardware. This enables the RapidIO interconnect to lower the system cost by providing lower latency, reduced overhead of packet data processing, and higher system bandwidth.



* Complex FFT, 1k points, single precision, floating point

** Complex block FIR, single precision, floating point, 128 samples, 16 coefficients

*** Complex matrix SGEMM 16×16

▲ *Figure 2. Performance comparison of C66x DSP core, C674x DSP core and ARM® Cortex®-A15 core*

The two-lane PCI express (PCIe) module on the device provides an interface between the DSP and other PCIe-compliant devices. The PCIe module provides low-pin-count, high-reliability, and high-speed data transfer at rates of 5.0 GBaud per lane on the serial links.

In addition C665x devices also include Universal Parallel Port (UPP) and two Multichannel Buffered Serial Ports (McBSP) ports. UPP allows a direct connection to an A/D or D/A converter and also enables a direct connection to an FPGA reducing the bill of materials and overall system cost and size. The collection of versatile interfaces on the C665x devices makes it easier for designers to migrate legacy designs to next generation systems with minimal board redesign.

KeyStone multicore architecture

TI's KeyStone multicore architecture implemented in the C665x devices maximizes the throughput of on-chip data flows to eliminate even the most remote possibility of bottlenecks, ensuring that the vast processing power of the device's C66x DSP cores can be utilized to the maximum. Central to this architecture is TeraNet, a packet-based fabric of high-speed non-blocking channels that delivers as much as 2 terabits per second of on-chip throughput. With TeraNet and an extensive two-layer memory structure, data flows freely and effectively through the C665x device.

Although it provides direct chip-to-chip connectivity for local devices, HyperLink is also integral to the internal processing architecture of the C665x device. HyperLink is a fast and efficient interface with low protocol overhead and high throughput, running at an aggregate speed of 40 GBaud (four lanes at up to 10 GBaud full duplex). Working in conjunction with Multicore Navigator, HyperLink transparently dispatches tasks to other local devices where they are executed as if they were being processed on local resources. HyperLink is available on both C6655 and C6657 devices.

In the KeyStone architecture, CorePac is defined as the main processing element in a multicore DSP. The CorePac includes the infrastructure that supports the DSP cores, including shared memory and memory controllers. There are three levels of memory in the KeyStone architecture. Each C66x CorePac has its own level-1 program (L1P) and level-1 data (L1D) memory. Additionally, each CorePac has a local level-2 unified memory (LL2). Each of the local memories can be independently configured as memory-mapped SRAM, cache or a combination of the two.

In addition, the KeyStone architecture includes a shared memory subsystem, comprising internal and external memory connected through the Multicore Shared Memory Controller (MSMC). The MSMC allows the CorePacs to dynamically share the internal and external memories for both program and data. The MSMC internal RAM offers flexibility to programmers by allowing portions to be configured as shared level-2 RAM (SL2) or shared level-3 RAM (SL3). SL2 RAM is cacheable only within the local L1P and L1D caches, while SL3 is additionally cacheable in the local L2 caches.

External memory is connected through the same memory controller as the internal shared memory, rather than to chip system interconnect as has been traditionally been done on embedded processor architectures, providing a fast path for software execution. External memory is always treated as SL3 memory and cacheable in L1 and L2.

The C6655 and C6657 devices also feature key coprocessing accelerators that offload processing tasks from the DSP engines, thereby enabling sustained high application processing rates. Both third-generation turbo decoders and voice channel decoding processors are offered for more efficient processing.

Multicore Navigator

A breakthrough feature of the KeyStone architecture is TI's innovative Multicore Navigator that essentially brings single-core simplicity to multicore devices. Multicore Navigator is designed to support hardware-assisted functional acceleration that utilizes an innovative packet-based hardware subsystem in KeyStone devices. With an extensive series of over 8,000 queues and a packet-aware DMA controller, it optimizes the packet-based communications of the on-chip cores by practically eliminating all copy operations. The extreme efficiency made possible by the Multicore Navigator results in a 100× performance gain in terms of the number of packets communicated per second over previous-generation cores.

The low latencies and zero interrupts ensured by Multicore Navigator as well as its transparent operations enable new and more effective programming models such as task dispatchers.

Moreover, several features inherent in Multicore Navigator, including dynamic software partitioning, shorten software development cycles significantly. With Multicore Navigator's "fire & forget" software tasking, developers save significant time and effort by defining repetitive tasks only once, and thereafter accessing and running these tasks automatically without additional coding efforts.

Lowest power consumption for performance

TI has a legacy of providing the lowest-power, highest-performance DSPs on the market. TI is able to achieve its ultimate low power through the combination of its process technology, including SmartReflex™ technology, and the proactive use of power management techniques, such as adaptive voltage scaling, to keep active power at a minimum. In addition, TI has leveraged its extensive knowledge in the high-performance applications market to establish multiple, dynamic power modes for the C665x devices, allowing customers a programmable strategy for optimizing power usage based on operation and use models for a particular market. At nominal conditions and use-case, the C665x devices deliver industry-leading power profiles—from <1.5W for the C6652 operating at 600 MHz to only 3W for the C6657 operating at 1 GHz.

TI's power-efficient architecture also enables designers to develop smaller, power-efficient portable devices for markets such as machine vision, grid infrastructure and medical imaging applications. The C665x enables multiple processors in previous designs to be consolidated down due to its better power profile coupled with higher performance than competitive products. With more processing performance in the same (or better) power envelope than previous generations of products, the C665x gives designers more freedom and processing room to develop high-performance applications.

Complete tools and support

TI provides a full suite of best-in-class Eclipse-based development and debug tools for the C665x devices, including: a new C compiler, an assembly optimizer to simplify programming and scheduling and a Windows® debugger interface for visibility into source code execution. TI's compiler generates highly efficient code that is "first-pass efficient" so there is less need to optimize it. TI's debug tools help developers to visualize problems and resolve them quickly, helping designers get products to the field faster while saving development resources.

The newly-released Processor SDK is a unified software platform for TI's processor families, including the C665x devices. In addition to TI-RTOS support for C665x devices, the Processor SDK platform includes board support packages, documentation, libraries, benchmarks, utilities and code examples that allow designers to seamlessly reuse and migrate software across TI processors.

TI also offers a low-cost evaluation module (EVM), the TMDSEVM6657L, for just U.S. $399 that helps customers quickly evaluate the performance of the C665x DSPs.

Additional information

To learn more about the C6657/55/54/52 DSPs, as well as TI's complete portfolio of multicore processors, please visit **here**. Discover how the C665x DSPs can add performance to your next power-efficient, computation-intensive application design.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265