

REV	DATE	NOTES
A	05/07/2014	PROTOTYPES
B	06/04/2014	BETA
C1	10/24/2014	BETA - CLEANUP
D	05/27/2016	ES 2.0
E	09/19/2016	ES 2.0 - UPDATE
E1	05/03/2017	DOC UPDATE FOR RELEASE

- SH01 - TITLE PAGE
- SH02 - ECN LIST
- SH03 - MAPPING/NOTES
- SH04 - SOC 1
- SH05 - SOC 2
- SH06 - SOC POWER
- SH07 - DDR3
- SH08 - VISIBILITY
- SH09 - BOOT/JTAG
- SH10 - I2C EXPANDER
- SH11 - MUX A/B/C
- SH12 - MUX D/E/F/G
- SH13 - MUX H/J/K
- SH14 - SD CARD/EEPROM/TMP
- SH15 - MEM NONVOLATILE
- SH16 - USB FTDI UART
- SH17 - CAN/SAFETY MCU
- SH18 - ETHERNET
- SH19 - POWER TPS443351DAP
- SH20 - POWER PMIC
- SH21 - POWER MISC SWITCHES
- SH22 - POWER MONITORS
- SH23 - POWER BENCH/MONITORS
- SH24 - VOUT LCD CONNECTOR
- SH25 - VOUT HDMI OUTPUT
- SH26 - VOUT FPD LINK
- SH27 - VIN DS90UH926Q
- SH28 - VIN CAMERA 1
- SH29 - VIN CAMERA 2
- SH30 - VIN CSI2
- SH31 - VIN HDMI IN-1
- SH32 - VIN HDMI IN-2
- SH33 - VIN HDMI IN-3
- SH34 - CPLD VOUT-1
- SH35 - CPLD VIN-1
- SH36 - TOOL HPC
- SH37 - TOOL POWER MONITOR

REVISION STATUS OF SHEETS

REV	SH	REV	SH	REV	SH	REV	SH	REV	SH	REV	SH	REV	SH	REV	SH	REV	SH

REV	C1	B	C1	B	B	A	E				OWN	DATE
SH	31	32	33	34	35	36	37				J.A.C.	05/27/2016
REV	E	B	A	A	A	A	A	C1	C1	C1	CHK	DATE
SH	21	22	23	24	25	26	27	28	29	30	T.W.K.	05/27/2016
REV	A	A	B	D	A	B	A	D	D		ENGR	DATE
SH	11	12	13	14	15	16	17	18	19	20	J.A.C.	05/27/2016
REV	E1	E	B	C1	D	D	E	D	D	#1	C.M.D.	05/27/2016
SH	1	2	3	4	5	6	7	8	9	10	RFC	DATE
											J.A.C.	05/27/2016
											ELISE	DATE
											J.A.C.	05/27/2016

**TEXAS INSTRUMENTS INCORPORATED**

Title: TDA3x/DRA76x/DM50x - 15X15 EVM

Page Contents: TITLE PAGE

Size: C      DOC NO: 517542      REV: E1

Date: Wednesday, May 03, 2017      Sheet 1 of 37

ECN Number	517540-E004
Date Requested	8/12/2016
Requester	Tony C.
Approvals	Tony C.
Assembly Number	517540-0001
Current Assembly Rev	D
New Assembly Rev	E
Date Implemented	8/12/2016
Implementation notes	

Item#	Init Date	Priority	Status	Description
				Logic From D to E PWB From D to E ASSY From D to E EEPROM D.1
ERS0				SHEET 7, ADD PULLUP TO DDR1_RST, R9500, 101370-1003R
ERS1				SHEET 21, FIX POWER HOLD GLITCH AND DISCONNECT BY DEFAULT.  U8044 FROM 102020-0009R (TPS3808G09DBVR) TO 102020-0033R(TPS3808G33DBV/RG4)  ADD R9505, R0201-NOPOP TE TO POWERHOLD_CLK  SHEET 10 POWERHOLD_CLK : U8006 IOEXP2_p26/TP8059
ERS2				SHEET 37: FIX LEAKAGE FROM FTDI BASED ON J6 ENTRY OBSERVATION. SAME FIX IS APPLIED TO FTDI POWER MEASUREMENT TOOL. ADD: 104446-1100R C8254 0.1uF 104446-1100R C8255 0.1uF 101370-1003R RJ1405 10K_A 101370-1003R RJ1406 10K_A 101689-0125R RU8016 74CBTLV1G125CRG4 101689-0125R RU8017 74CBTLV1G125CRG4 101689-0125R RU8018 74CBTLV1G125CRG4 101689-0125R RU8019 74CBTLV1G125CRG4 101370-1004R R9501 100K 101370-1004R R9502 100K 101370-1004R R9503 100K 101370-1004R R9504 100K
ERS3				Remove PB Free,Add RoHS EXEMPT

FUNCTION TABLE

INPUTS			INPUT/OUTPUT A	FUNCTION
S2	S1	S0		
L	L	L	Z	Disconnect
L	L	H	B1	A port = B1 port
L	H	L	B2	A port = B2 port
L	H	H	Z	Disconnect
H	L	L	Z	Disconnect
H	L	H	B3	A port = B3 port
H	H	L	B1	A port = B1 port
H	H	H	B2	A port = B2 port

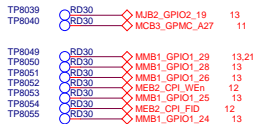
CAPACITOR SIZING FOR COMMERCIAL vs AUTOMOTIVE

CAPACITANCE	Commerical Size/X5R	Automotive Size/X7R
Vaule		
.1uF	0201	0402
.22uF	0201	0603
.47uF	0201	0603
1uF	0201	0603
2.2uF	0402	0603
4.7uF	0402	0805
10uF	0402	0805
22uF	0603	1206

DDR3 DEVICE OPTIONS

MT41K128M16JT-125 M:K 0-95C  
 MT41K128M16JT-125 IT:K -40-95C  
 MT41K128M16JT-125 AAT:K -40-105C

SINGLE NET NODES AVAILABLE FOR TEST POINTS



Sync w/ schematic from April 2

SVB COMPONENTS NOT POPULATED ON EVM

- SH05 - SOC 2
- J6116
- J6117
- J6118
- J6107
- J76
- J6102
- J83
- SH08 - VISIBILITY
- J1003
- J28
- SH09 - BOOT/JTAG
- R9261
- R9262
- R9263
- R9264
- R9265
- R9266
- R9267
- R9268
- R9269
- R9270
- R9271
- R9272
- R9273
- R9274
- R9275
- R9276
- R9283
- R9199
- R9200
- SW8
- SH15 - MEM NONVOLATILE
- J40
- Xu83 (socket)
- SH17 - CAN/SAFETY MCU
- J6108
- J6110
- J6109
- J6106
- SH23 - POWER BENCH/MONITORS
- J78
- J6103
- J6104
- J6105
- SH36 - TOOL HPC
- C3200
- C3201
- C3204
- C3205
- C3206
- C3207
- C3208
- C3209
- J3200
- Q2015
- Q2024
- R3202
- R3203
- R3204
- R3205
- R3207
- R3208
- R3209
- R3210
- R3211
- R3212
- R3213
- R3214
- R3215
- R3216
- R3217
- R3218
- R3219
- R3220
- R3221
- R4135
- R4136
- R4138
- R4139
- R9278
- R9279
- R9352
- R9353
- R9354
- U3201
- U3202
- U3203
- U3204

<b>TEXAS INSTRUMENTS INCORPORATED</b>		
Title: TDA3x/DRA76x/DM50x - 15X15 EVM		
Page Contents: MAPPING/NOTES		
Size: C	DOC NO: 517542	REV: B
Date: Wednesday, May 03, 2017	Sheet 3	of 37

8	H_GPMC_A00	E8	GPMC_AD0/RGMII1_RXD2/GPIO1_14/SYSBOOT0
8	H_GPMC_A01	F8	GPMC_AD1/RGMII1_RXD1/GPIO1_15/SYSBOOT1
8	H_GPMC_A02	B7	GPMC_AD2/RGMII1_RXD0/GPIO1_16/SYSBOOT2
8	H_GPMC_A03	A6	GPMC_AD3/QSPI1_RTCLK/GPIO1_17/SYSBOOT3
8	H_GPMC_A04	F7	GPMC_AD4/CAM_STROBE/GPIO1_18/SYSBOOT4
8	H_GPMC_A05	E7	GPMC_AD5/UART2_TXD/TIMER6/SP13_D1/GPIO1_19/SYSBOOT5
8	H_GPMC_A06	C6	GPMC_AD6/UART2_RXD/TIMER6/SP13_D0/GPIO1_20/SYSBOOT6
8	H_GPMC_A07	B6	GPMC_AD7/CAM_SHUTTER/TIMER4/SP13_SCLK/GPIO1_21
8	H_GPMC_A08	A5	GPMC_AD8/TIMER7/SP13_CS0/GPIO1_22/SYSBOOT8
8	H_GPMC_A09	D5	GPMC_AD9/CAP1_IN_PWM1_OUT/SP13_CS1/GPIO1_23/SYSBOOT9
8	H_GPMC_A10	C5	GPMC_AD10/TIMER2/GPIO1_24/SYSBOOT10
8	H_GPMC_A11	B5	GPMC_AD11/TIMER3/GPIO1_25/SYSBOOT11
8	H_GPMC_A12	D4	GPMC_AD12/SP11_28V/SYSBOOT12
8	H_GPMC_A13	B4	GPMC_AD13/RGMII1_RXC/GPIO1_27/SYSBOOT13
8	H_GPMC_A14	A4	GPMC_AD14/SP12_CS1/GPIO1_28/SYSBOOT14
8	H_GPMC_A15	C4	GPMC_AD15/SP12_CS0/GPIO1_29/SYSBOOT15
8	H_GPMC_CLK	C12	GPMC_CLK/RGMII1_TXCLK/OUT0/DMA_EVT1/EP01_0
8	H_GPMC_BEN0	D12	GPMC_BEN0/RGMII1_TXCTL/EHRPWW1A/DMA_EVT2/GPIO1_1
8	H_GPMC_BEN1	F12	GPMC_BEN1/RGMII1_TXD3/EHRPWW1B/DMA_EVT3/GPIO1_2
8	H_GPMC_ADVn	B10	GPMC_ADVn_ALE/RGMII1_TXD2/EHRPWW1_TRIPZONE_INPUT/CLKOUT1/DMA_EVT4/GPIO1_3
8	H_GPMC_OEn	A10	GPMC_OEn_RE/RGMII1_TXD1/EHRPWW_SYNC/CLKOUT2/GPIO1_4
8	H_GPMC_WEn	C10	GPMC_WEn/RGMII1_TXD0/EHRPWW_SYNC/GPIO1_5
8	H_GPMC_CS0	E9	GPMC_CS0/RGMII1_RXCTL/GPIO1_6
8	H_GPMC_CS1	F10	GPMC_CS1/QSP1_CS0/GPIO1_7
8	H_GPMC_CS2	A9	GPMC_CS2/QSP1_D3(I)/GPIO1_8
8	H_GPMC_CS3	B9	GPMC_CS3/QSP1_D2(I)/GPIO1_9
8	H_GPMC_CS4	C9	GPMC_CS4/QSP1_D0(I)/GPIO1_10
8	H_GPMC_CS5	D9	GPMC_CS5/QSP1_D1(I)/GPIO1_11
8	H_GPMC_CS6	C8	GPMC_CS6/QSP1_SCLK/GPIO1_12
8	H_GPMC_WAIT0	D8	GPMC_WAIT0/RGMII1_RXD3/QSP1_RTCLK/DMA_EVT4/GPIO1_13

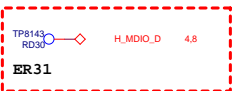
**GPMC**  
(Pwr Domain = VDDSHV2)  
(Opr Voltages = 1.8/3.3V)

### TDA3x\_ABF ES2.0

Package: 15X15mm, 367 BGA-FC, 0.65mm Pitch  
Pinlist: ADASLow\_pinlist\_Rev2.0.xlsx (Oct 26, 2015)  
Data Manual: TDA3x\_ABF\_ES2.0\_DM\_vA (Oct 2014)  
Symbol: IC\_TDA3x\_ABF\_367BGA\_v2.1 (Jun 03, 2016)  
TDA3x is pin compatible with DRA78x and DM50x devices

### Connectivity

8	H_I2C1_SCL	L3	I2C1_SCL	I2Cs (Pwr Domain = VDDSHV1) (Opr Voltages = 1.8/3.3V)
8	H_I2C1_SDA	L4	I2C1_SDA	
8	H_I2C2_SCL	L6	I2C2_SCL	
8	H_I2C2_SDA	L5	I2C2_SDA	
8	H_SPI1_SCLK	M2	SP11_SCLK/UART3_RXD/GPIO4_0	SPIs (Pwr Domain = VDDSHV1) (Opr Voltages = 1.8/3.3V)
8	H_SPI1_D1	U6	SP11_D1/UART3_CTS/GPIO4_1	
8	H_SPI1_D0	T5	SP11_D0/UART3_RTS/GPIO4_2	
8	H_SPI1_CS0	R5	SP11_CS0/UART3_TXD/GPIO4_3	
8	H_SPI1_CS1	R6	SP11_CS1/SP13_CS1/TIMER6/EHRPWW1_TRIPZONE_INPUT/GPIO4_4	
8	H_SPI2_SCLK	L1	SP12_SCLK/UART3_RXD/EHRPWW1A/TIMER3/GPIO4_5	
8	H_SPI2_D1	N4	SP12_D1/UART3_CTS/TIMER6/CAP1_IN_PWM_OUT/GPIO4_6	
8	H_SPI2_D0	R7	SP12_D0/UART3_RTS/TIMER1/GPIO4_7/SYSBOOT7	
8	H_SPI2_CS0	L2	SP12_CS0/UART3_TXD/EHRPWW1B/TIMER4/GPIO4_8	
8	H_UART1_RXD	F13	UART1_RXD/SP14_D1/QSP1_RTCLK/GPMC_A12/GPMC_A12/DCAN2_TX/GPIO4_13	
8	H_UART1_TXD	F14	UART1_TXD/SP14_D0/GPMC_A13/GPMC_A13/DCAN2_RX/GPIO4_14	
8	H_UART1_CTSn	F15	UART1_CTSn/REF_CLK1/UART3_RXD/GPMC_A16/SP14_SCLK/SP11_CS2/TIMER3/EHRPWW1_SYNC/CLKOUT0/VIN2A_HSYNCO/GPMC_A12/GPMC_CLK/DCAN1_TX/GPIO4_15	
8	H_UART1_RTSn	C14	UART1_RTSn/UART3_TXD/GPMC_A17/SP14_CS0/SP11_CS3/TIMER4/EHRPWW1_SYNC/GSP1_RTCLK/VIN2A_VSYNCO/GPMC_A13/DCAN1_RX/GPIO4_16	
8	H_UART2_RXD	D14	UART2_RXD/SP13_D1/QSP1_RTCLK/TIMER1/EHRPWW1A/CLKOUT0/VIN2A_HSYNCO/GPMC_A12/GPMC_CLK/DCAN1_TX/GPIO4_17	
8	H_UART2_TXD	D15	UART2_TXD/SP13_D0/TIMER2/EHRPWW1B/GPMC_A13/DCAN1_RX/GPIO4_18	
8	H_UART2_CTSn	F15	UART2_CTSn/XREF_CLK1/GPMC_A18/SP13_SCLK/QSP1_CS1/TIMER7/VIN2A_HSYNCO/GPMC_CLK/DCAN2_TX/GPIO4_19	
8	H_UART2_RTSn	F16	UART2_RTSn/CAP1n_PWM1_OUT/GPMC_A19/SP13_CS0/TIMER8/QSP1_RTCLK/VIN2A_VSYNCO/DCAN2_RX/GPIO4_20	
8	H_DCAN1_TX	N5	DCAN1_TX/GPIO4_9	DCAN1 & MCAN (Pwr Domain = VDDSHV1 & VDDSHV6) (Opr Voltages = 1.8/3.3V)
8	H_DCAN1_RX	N6	DCAN1_RX/GPIO4_10	
8	H_MCAN_TX	W7	MCAN_TX/VIN2A_DE0/VIN2A_HSYNCO/SP11_CS2/UART3_RXD/QSP1_CS1/GPMC_WAIT1/VIN1B_HSYNCO/VIN1B_DE/VGPIO4_11	
8	H_MCAN_RX	W6	MCAN_RX/CAM_nRESET/VIN2A_VSYNCO/SP11_CS3/UART3_TXD/GPMC_CS7/VIN1B_VSYNCO/GPIO4_12	
8	H_MDIO_MCLK	B19	MDIO_MCLK/SP14_D1/GPIO3_17	EMAC Switch (Pwr Domain = VDDSHV4) (Opr Voltages = 1.8/3.3V)
4,8	H_MDIO_D	B17	MDIO_D/SP14_D0/ESM_ERROR/GPIO3_18	
8	H_RGMII0_TXC	C16	RGMII0_TXC/CAM_STROBE/SP14_SCLK/MMC_CLK/GPIO3_19	
8	H_RGMII0_TXCL	C17	RGMII0_TXCTL/CAM_SHUTTER/SP14_SCLK/MMC_CMD/GPIO3_20	
8	H_RGMII0_TXD3	E16	RGMII0_TXD3/MMC_DAT0/GPIO3_21	
8	H_RGMII0_TXD2	E17	RGMII0_TXD2/CAP1_IN_PWM1_OUT/MMC_DAT1/GPIO3_22	
8	H_RGMII0_TXD1	F17	RGMII0_TXD1/MMC_DAT2/GPIO3_23	
8	H_RGMII0_TXD0	F17	RGMII0_TXD0/MMC_DAT3/GPIO3_24	
8	H_RGMII0_RXC	B18	RGMII0_RXC/CAM_STROBE/MMC_CLK/GPIO3_25	
8	H_RGMII0_RXCTL	C18	RGMII0_RXCTL/CAM_SHUTTER/MMC_CMD/GPIO3_26	
8	H_RGMII0_RXD3	B20	RGMII0_RXD3/MMC_DAT0/GPIO3_27	
8	H_RGMII0_RXD2	C20	RGMII0_RXD2/MMC_DAT1/GPIO3_28	
8	H_RGMII0_RXD1	C20	RGMII0_RXD1/MMC_DAT2/GPIO3_29	
8	H_RGMII0_RXD0	A20	RGMII0_RXD0/MMC_DAT3/GPIO3_30	



**DDR**  
(Pwr Domains = VDD5\_DDR1, VDD5\_DDR2, VDD5\_DDR3)  
(Opr Voltages = 1.35/1.5/1.8V)

DDR_A0	U4	H_DDR1_A0	7
DDR_A1	C1	H_DDR1_A1	7
DDR_A2	D3	H_DDR1_A2	7
DDR_A3	R4	H_DDR1_A3	7
DDR_A4	T4	H_DDR1_A4	7
DDR_A5	Y2	H_DDR1_A5	7
DDR_A6	N3	H_DDR1_A6	7
DDR_A7	N2	H_DDR1_A7	7
DDR_A8	U1	H_DDR1_A8	7
DDR_A9	D1	H_DDR1_A9	7
DDR_A10	D1	H_DDR1_A10	7
DDR_A11	U2	H_DDR1_A11	7
DDR_A12	D6	H_DDR1_A12	7
DDR_A13	R2	H_DDR1_A13	7
DDR_A14	R2	H_DDR1_A14	7
DDR_A15	V1	H_DDR1_A15	7

**EMIF1**  
Two 2Gbit x 16bits

DDR_BA0	B3	H_DDR1_BA0	7
DDR_BA1	A3	H_DDR1_BA1	7
DDR_BA2	D2	H_DDR1_BA2	7
DDR_CASn	F2	H_DDR1_CASn	7
DDR_CSn	B2	H_DDR1_CSNO	7
DDR_ODT	F1	H_DDR1_ODT	7
DDR_RASn	E3	H_DDR1_RASn	7
DDR_RST	N1	H_DDR1_RST	7
DDR_WEn	F3	H_DDR1_WEn	7
DDR_CLK_P	G1	H_DDR1_CLK_P	7
DDR_CLK_N	G2	H_DDR1_CLK_N	7

DDR_DOM0	A8	H_DDR1_DOM0	7
DDR_D1	Y6	H_DDR1_D1	7
DDR_D2	A7	H_DDR1_D2	7
DDR_D3	AB4	H_DDR1_D3	7
DDR_D4	Y5	H_DDR1_D4	7
DDR_D5	AA4	H_DDR1_D5	7
DDR_D6	Y6	H_DDR1_D6	7
DDR_D7	Y6	H_DDR1_D7	7
DDR_DQS0_P	AB5	H_DDR1_DQS0_P	7
DDR_DQS0_N	Y18	H_DDR1_DQS0_N	7

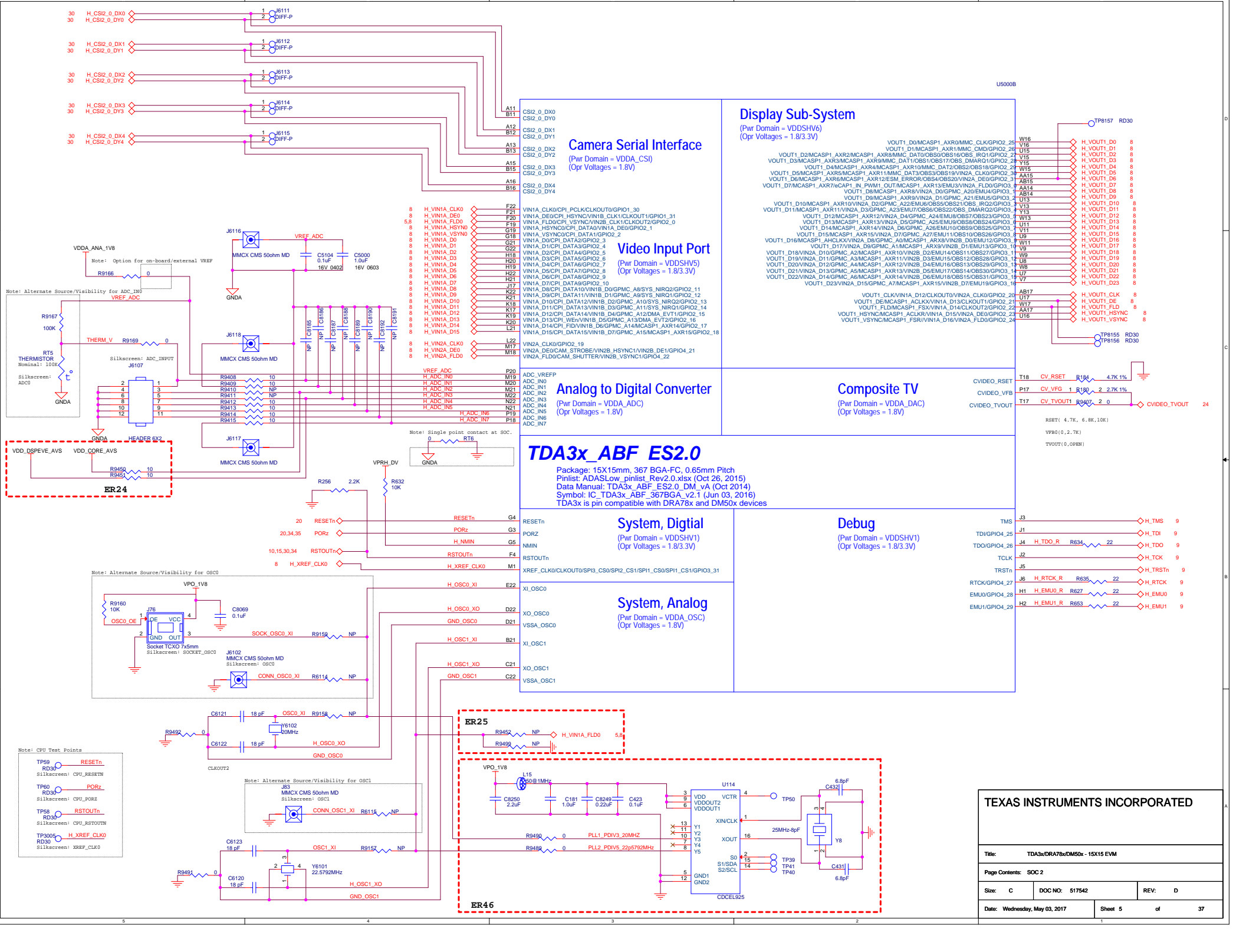
DDR_DOM1	AA18	H_DDR1_DOM1	7
DDR_D8	Y21	H_DDR1_D8	7
DDR_D9	AA21	H_DDR1_D9	7
DDR_D10	Y22	H_DDR1_D10	7
DDR_D11	AA19	H_DDR1_D11	7
DDR_D12	AB20	H_DDR1_D12	7
DDR_D13	Y17	H_DDR1_D13	7
DDR_D14	AB18	H_DDR1_D14	7
DDR_D15	AA20	H_DDR1_D15	7
DDR_DQS1_P	Y20	H_DDR1_DQS1_P	7
DDR_DQS1_N	Y20	H_DDR1_DQS1_N	7

DDR_DOM2	AB3	H_DDR1_DOM2	7
DDR_D16	AA2	H_DDR1_D16	7
DDR_D17	Y3	H_DDR1_D17	7
DDR_D18	V2	H_DDR1_D18	7
DDR_D19	V2	H_DDR1_D19	7
DDR_D20	V3	H_DDR1_D20	7
DDR_D21	U3	H_DDR1_D21	7
DDR_D22	Y2	H_DDR1_D22	7
DDR_D23	Y1	H_DDR1_D23	7
DDR_DQS2_P	W1	H_DDR1_DQS2_P	7
DDR_DQS2_N	W2	H_DDR1_DQS2_N	7

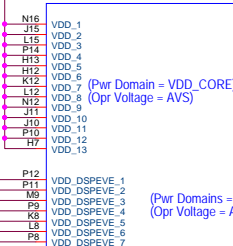
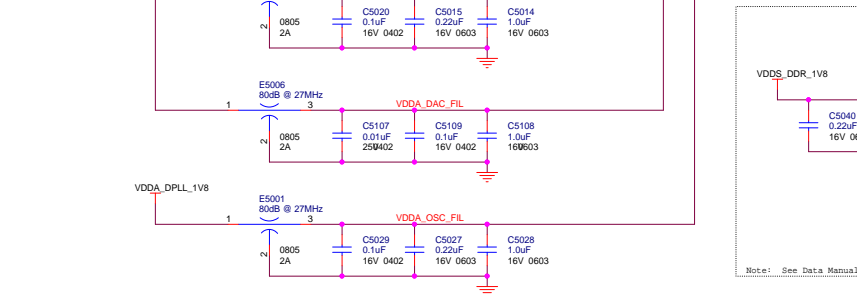
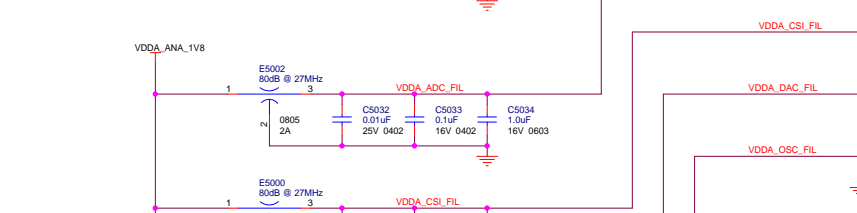
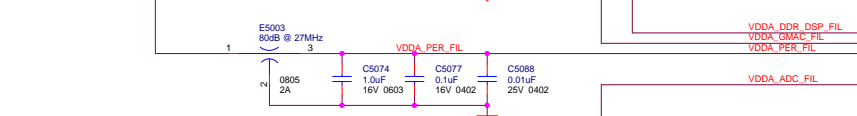
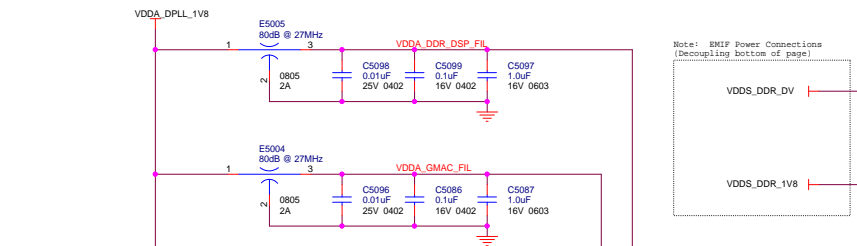
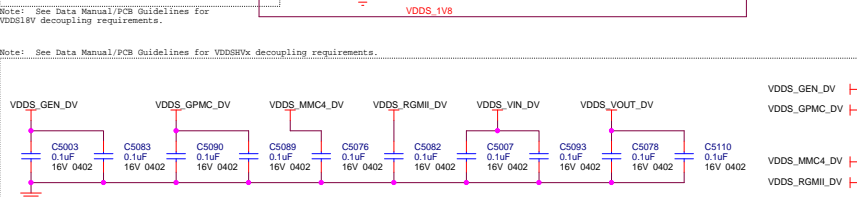
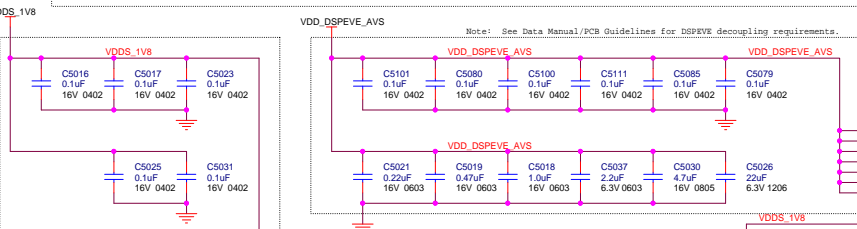
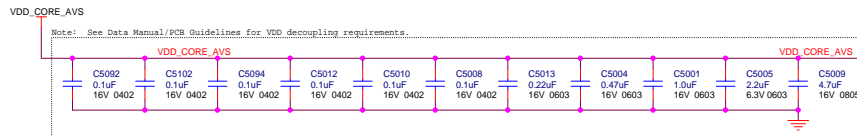
DDR_DOM3	W21	H_DDR1_DOM3	7
DDR_D24	U21	H_DDR1_D24	7
DDR_D25	T20	H_DDR1_D25	7
DDR_D26	U20	H_DDR1_D26	7
DDR_D27	R22	H_DDR1_D27	7
DDR_D28	V20	H_DDR1_D28	7
DDR_D29	W22	H_DDR1_D29	7
DDR_D30	U22	H_DDR1_D30	7
DDR_D31	T21	H_DDR1_D31	7
DDR_DQS3_P	T21	H_DDR1_DQS3_P	7
DDR_DQS3_N	T22	H_DDR1_DQS3_N	7

One 1Gbit x 8bits

DDR_ECC_DOM	AB13	H_DDR1_ECC_DOM	7
DDR_ECC_D0	Y11	H_DDR1_ECC_D0	7
DDR_ECC_D1	AA11	H_DDR1_ECC_D1	7
DDR_ECC_D2	Y9	H_DDR1_ECC_D2	7
DDR_ECC_D3	AA13	H_DDR1_ECC_D3	7
DDR_ECC_D4	AB11	H_DDR1_ECC_D4	7
DDR_ECC_D5	AA9	H_DDR1_ECC_D5	7
DDR_ECC_D6	AB9	H_DDR1_ECC_D6	7
DDR_ECC_D7	AA10	H_DDR1_ECC_D7	7
DDR_ECC_DOS_P	AB10	H_DDR1_ECC_DOS_P	7
DDR_ECC_DOS_N	AB10	H_DDR1_ECC_DOS_N	7



<b>TEXAS INSTRUMENTS INCORPORATED</b>			
Title: TDA3x/DRA7x/DM50x - 15X15 EVM			
Page Contents: SOC 2			
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**TDA3x\_ABF\_ES2.0**  
 Package: 15X15mm, 367 BGA-FC, 0.65mm Pitch  
 Pinlist: ADASLow\_pinlist\_Rev2.0.xlsx (Oct 26, 2015)  
 Data Manual: TDA3x\_ABF\_ES2.0\_DM\_vA (Oct 2014)  
 Symbol: IC\_TDA3x\_ABF\_367BGA\_v2.1 (Jun 03, 2016)  
 TDA3x is pin compatible with DRA78x and DM50x devices

**Power Domains & Returns**

(Pwr Domain = VDD\_DSP, VDD\_EVE)  
 (Opr Voltage = AVS)

(Pwr Domain = I/O Bias Supply)  
 (Opr Voltage = 1.8V)

(Pwr Domain = General I/O)  
 (Opr Voltage = 1.8/3.3V dual voltage supply)

(Pwr Domain = GPMC I/O)  
 (Opr Voltage = 1.8/3.3V dual voltage supply)

(Pwr Domain = MMC4 I/O)  
 (Opr Voltage = 1.8/3.3V dual voltage supply)

(Pwr Domain = RGMII I/O)  
 (Opr Voltage = 1.8/3.3V dual voltage supply)

(Pwr Domain = VIN1 I/O)  
 (Opr Voltage = 1.8/3.3V dual voltage supply)

(Pwr Domain = VOUT1 I/O)  
 (Opr Voltage = 1.8/3.3V dual voltage supply)

(Pwr Domain = I/O for Byte0, Byte2, ECC Byte, Addr Cmd Non-PoP)  
 (Opr Voltages = 1.35/1.5V)

(Pwr Domain = I/O for Addr Cmd PoP)  
 (Opr Voltages = 1.35/1.5V)

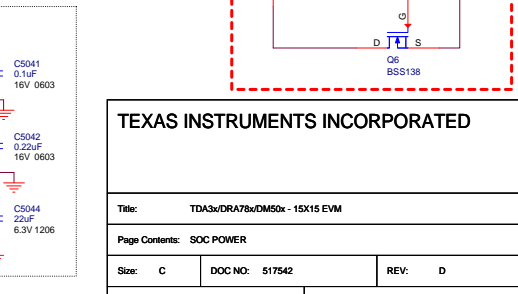
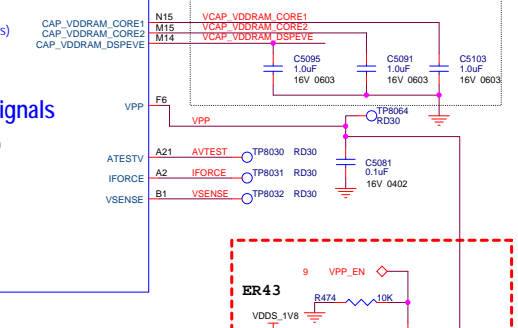
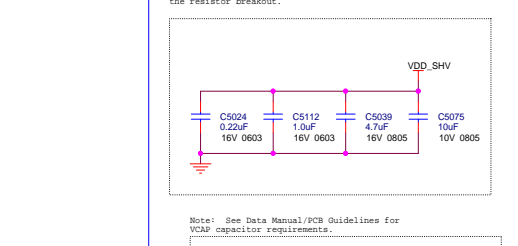
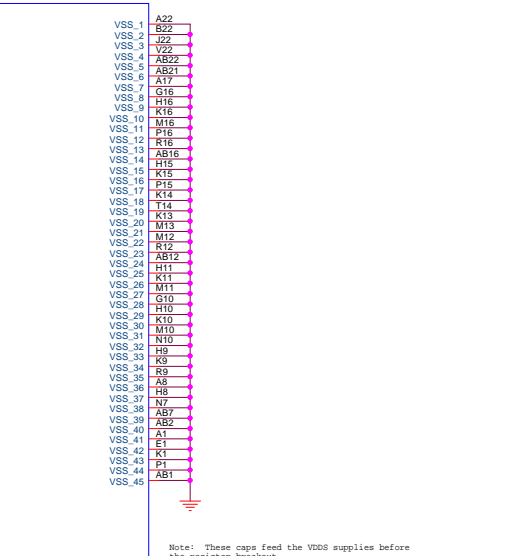
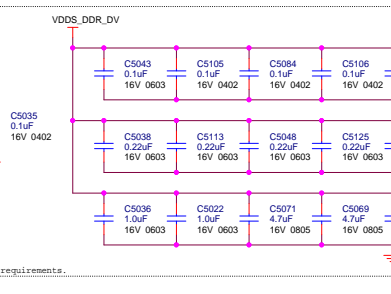
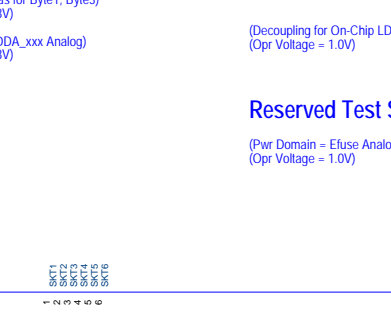
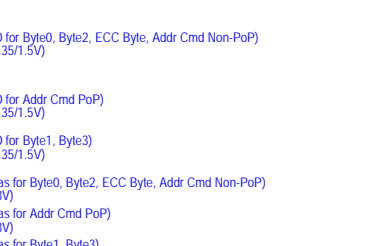
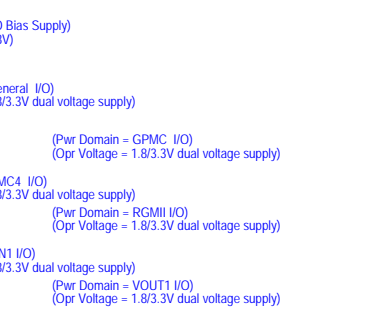
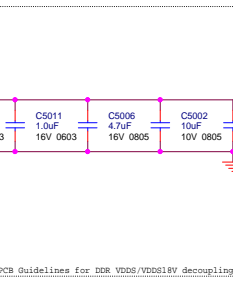
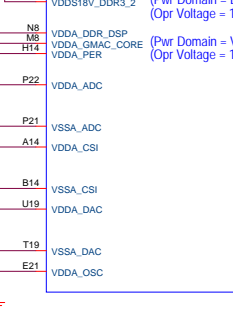
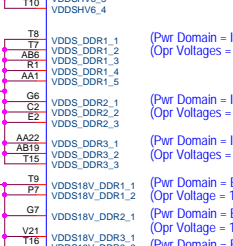
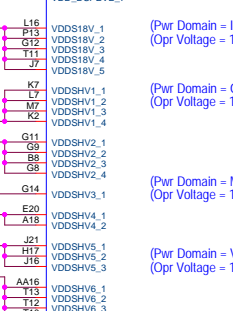
(Pwr Domain = I/O for Byte1, Byte3)  
 (Opr Voltages = 1.35/1.5V)

(Pwr Domain = Bias for Byte0, Byte2, ECC Byte, Addr Cmd Non-PoP)  
 (Opr Voltage = 1.8V)

(Pwr Domain = Bias for Addr Cmd PoP)  
 (Opr Voltage = 1.8V)

(Pwr Domain = Bias for Byte1, Byte3)  
 (Opr Voltage = 1.8V)

(Pwr Domain = VDDA\_XXX Analog)  
 (Opr Voltage = 1.8V)



**TEXAS INSTRUMENTS INCORPORATED**

Title: TDA3x/DRA78x/DM50x - 15X15 EVM

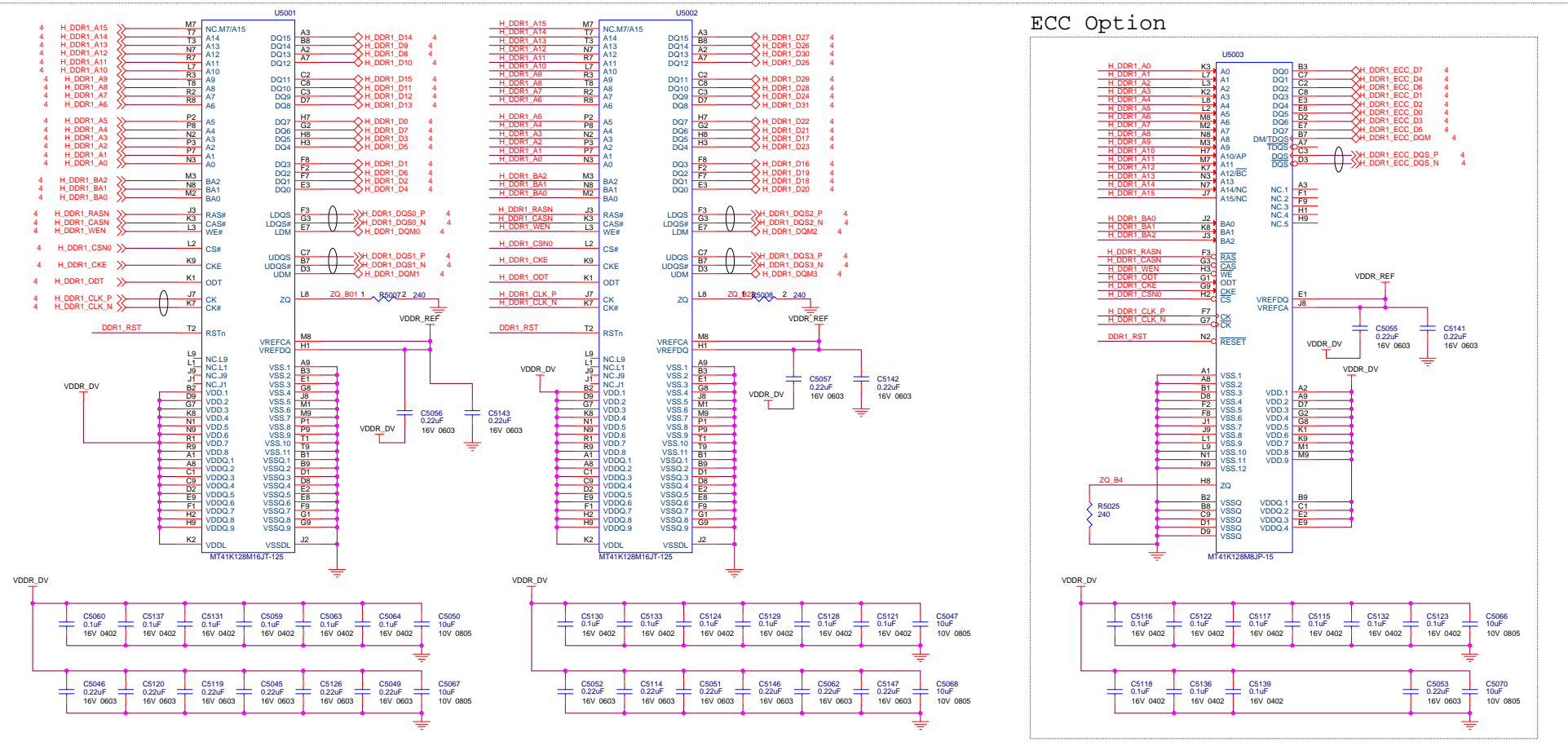
Page Contents: SOC POWER

Size: C DOC NO: 517542 REV: D

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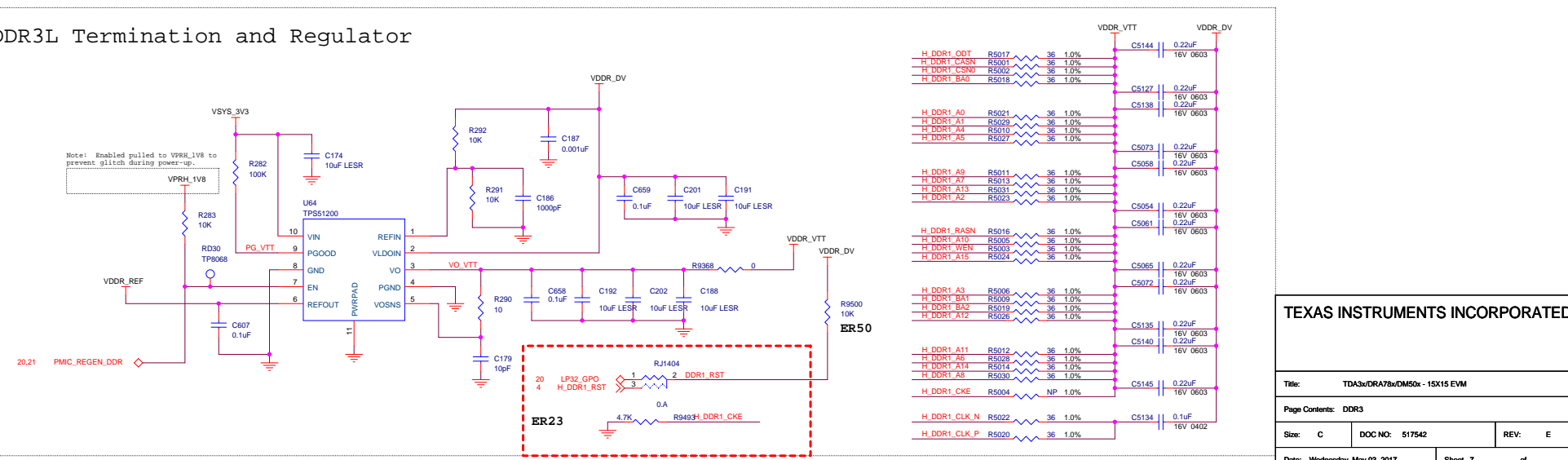
# DDR3L Memory

# ECC Option



Note: See Data Manual/PCB Guidelines for DDR3 implementation requirements.

# DDR3L Termination and Regulator



TEXAS INSTRUMENTS INCORPORATED

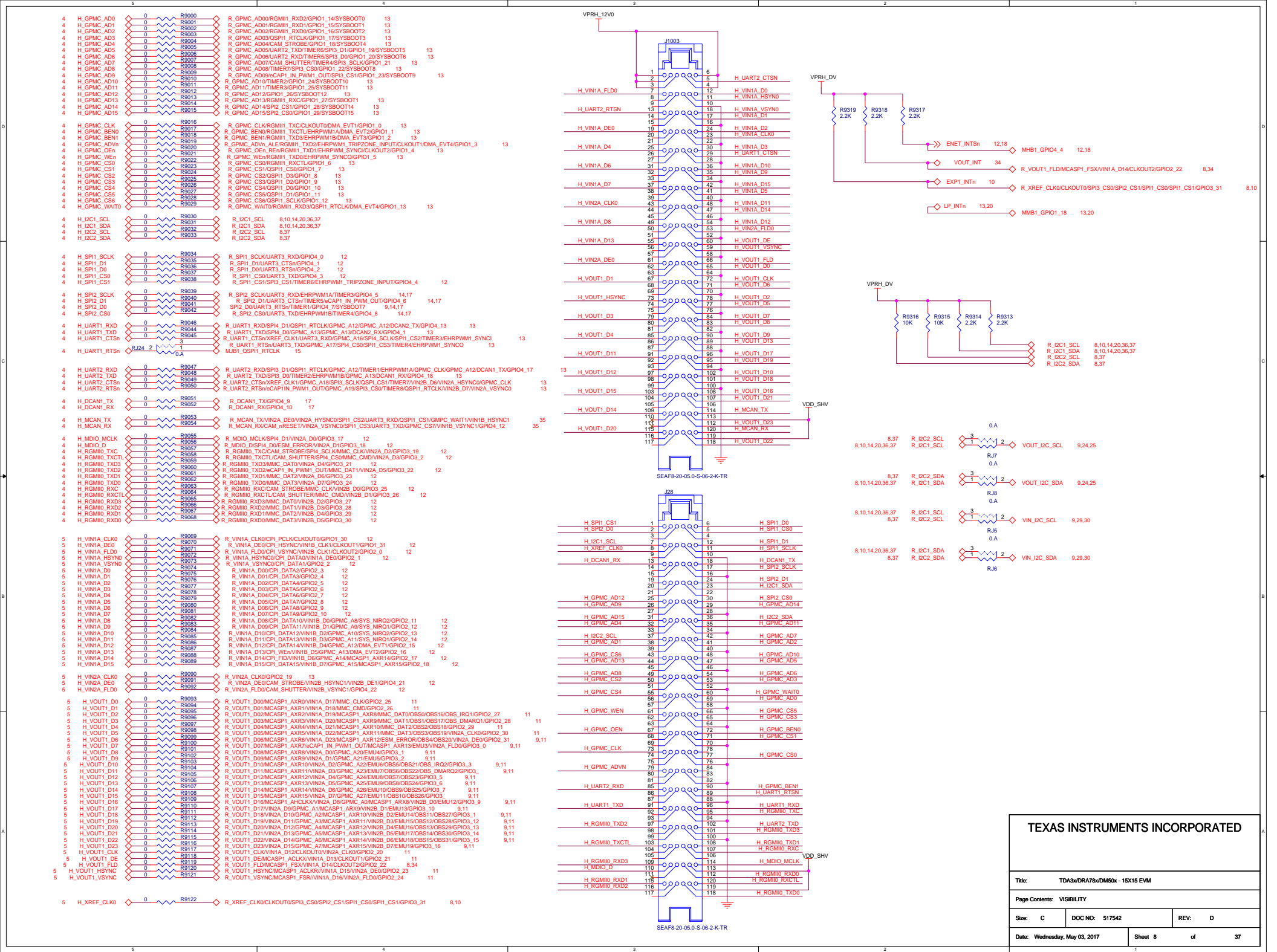
Title: TDA3M/DRA76/DM50x - 15X15 EVM

Page Contents: DDR3

Size: C DOC NO: 517542 REV: E

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Title: TDA80DRA76bDM50x - 15X15 EVM

Page Contents: VISIBILITY

Size: C	DOC NO: 517542	REV: D
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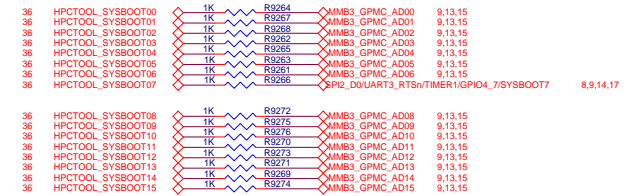
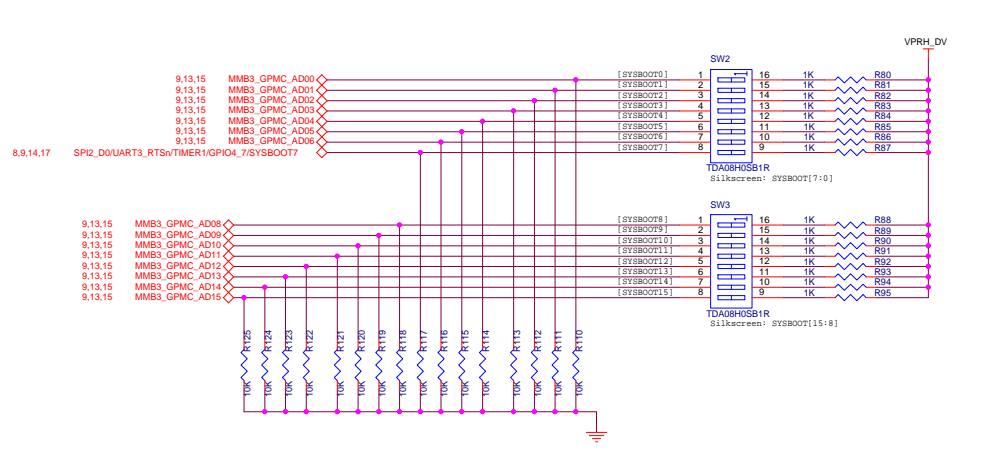
Date: Wednesday, May 03, 2017

Sheet 8	of	37
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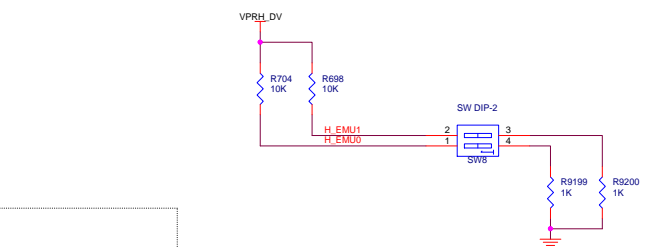
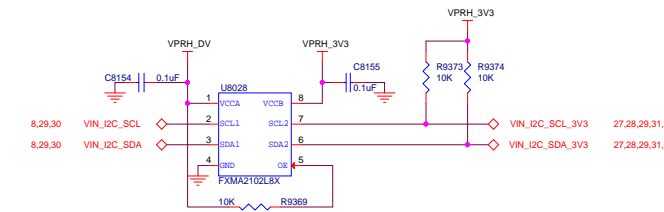
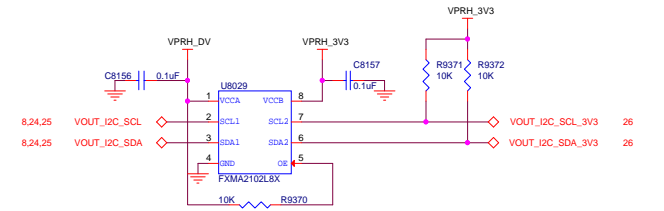


# SYBOOT Control

Note: Switch OFF is logic '0', ON is logic '1'.

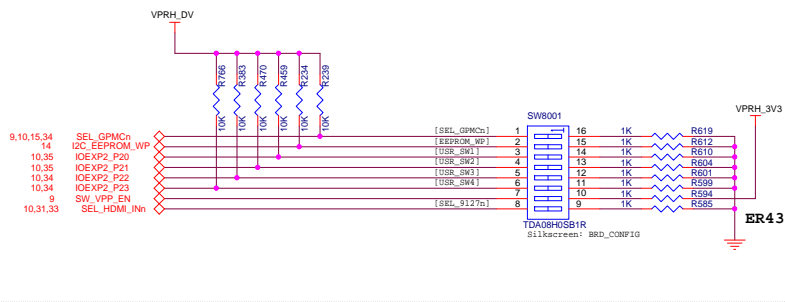


PLACE THESE RESISTORS NEAR THE BOOT SWITCHES, NO-POP TO REMOVE HPC STUBS, THESE RES NEED TO BE 1K OR HIGHER. THE I2C EXPANDER IS A PET TO VCC RAIL AND OR GROUND.

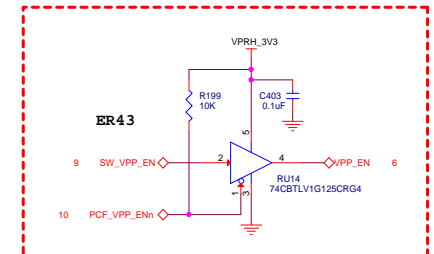
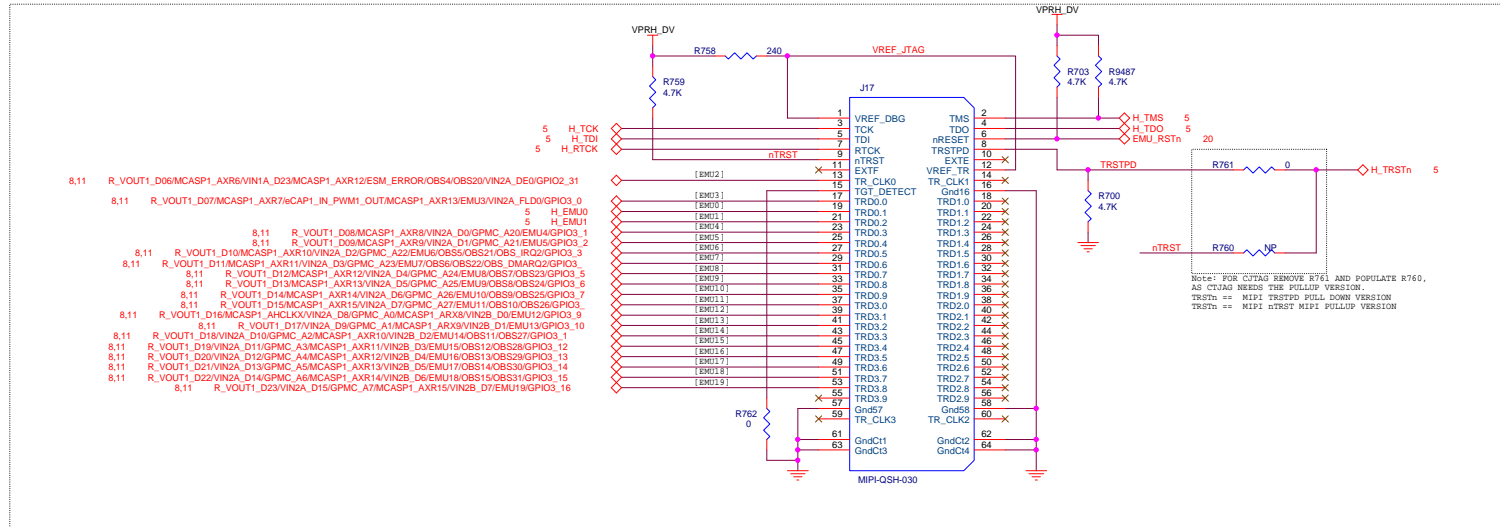


# Board Configuration

Note: Switch OFF is logic '0', ON is logic '1'.



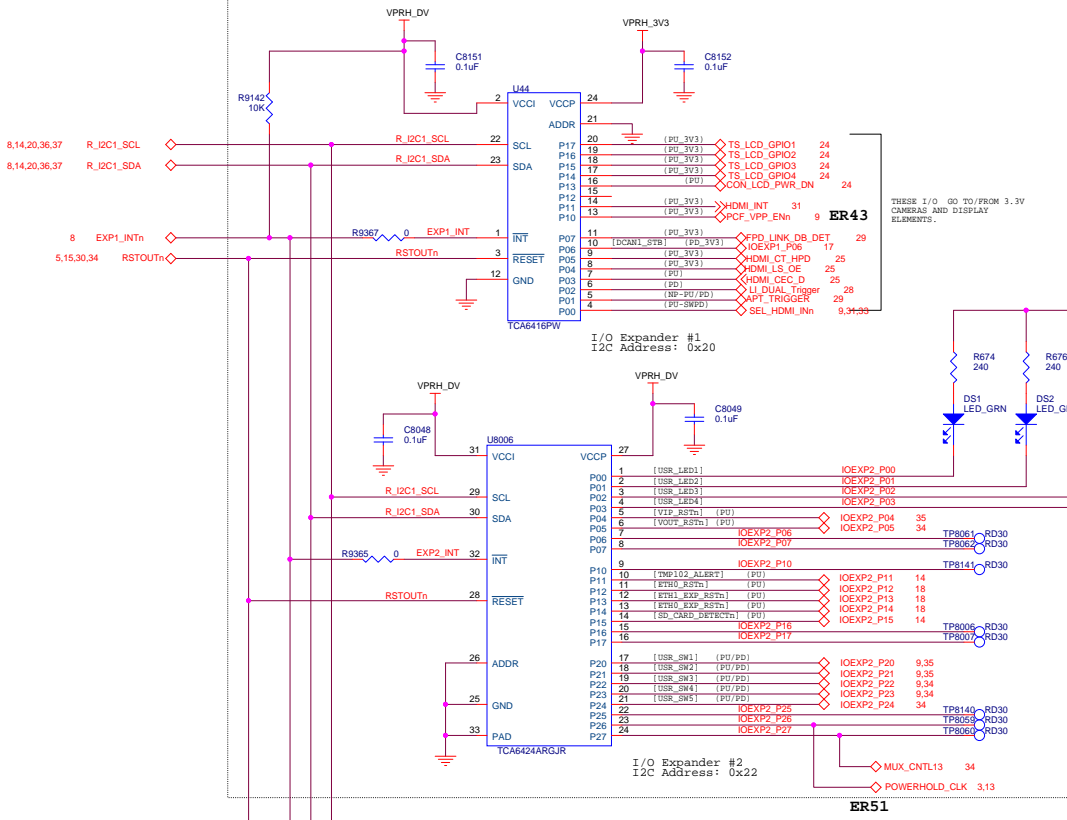
# MIPI-60 JTAG/Emulation Interface



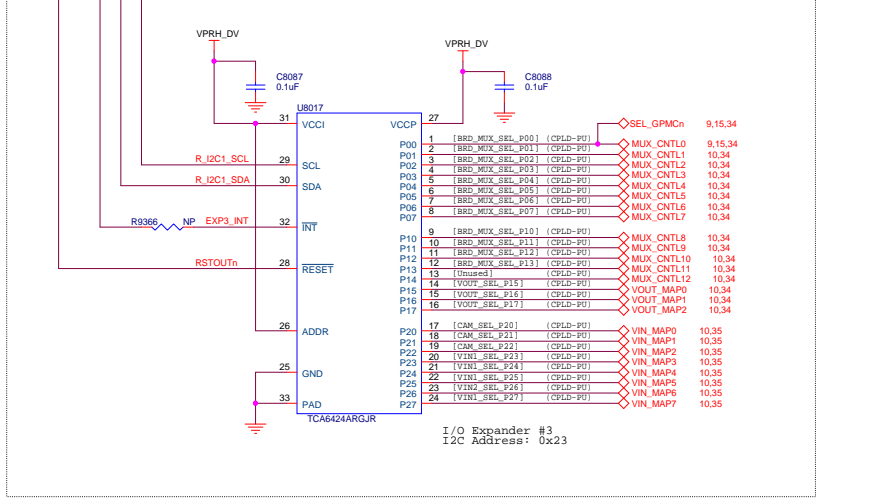
## TEXAS INSTRUMENTS INCORPORATED

Title:	TDA3xDRA76xDMS0x - 15X15 EVM		
Page Contents:	BOOT/JTAG		
Size:	C	DOC NO: 517542	REV: D
Date:	Wednesday, May 03, 2017	Sheet 9	of 37

# Peripheral I/O Control



# Board/CPLD Mux Configuration



ADAS MUX SELECTION P0[7:0] P1[13:10]											
MUX A											
11	10	9	8	7	6	5	4	3	2	1	0
L	H	B1	VOUT1								
H	H	B2	VIN1								
H	L	B3	NA								
L	L	Z	Z	Z Needed for emu-19 isolation (Default)							
MUX C											
11	10	9	8	7	6	5	4	3	2	1	0
L	H	H	B1	VOUT1							
H	H	H	B2	VIN2A							
H	L	L	B3	GPIC/BOOT							
L	L	L	Z	Z	Z Needed for emu-19 isolation (Default)						
MUX D/E											
11	10	9	8	7	6	5	4	3	2	1	0
L	L	H	B1	VIN1A/2A/2B (Default)							
H	H	B2	CPI								
H	L	L	B3	GPIC/BOOT							
L	L	L	Z	Z							
MUX F											
11	10	9	8	7	6	5	4	3	2	1	0
L	H	H	B1	EMACOPHY (Default)							
H	H	B2	EMAC0-EXPANSION								
H	L	L	B3	MMC1							
L	L	L	Z	Z							
MUX H											
11	10	9	8	7	6	5	4	3	2	1	0
L	L	H	B1	UART3 (Default)							
H	H	B2	SP1								
L	L	L	Z	Z							
MUX J											
11	10	9	8	7	6	5	4	3	2	1	0
L	L	H	B1	DCAN2/VIN2A/QSPI (Default)							
H	H	B2	UART1/SP4								
H	L	B3	GPIC/BOOT								
L	L	L	B1	L							
MUX K											
11	10	9	8	7	6	5	4	3	2	1	0
L	L	H	B1	UART1 (Default)							
H	H	B2	SP4								
L	L	L	Z	Z							
MUX M											
11	10	9	8	7	6	5	4	3	2	1	0
L	L	H	B1	EMAC1/GPIO/SP3 (Default)							
H	H	B1	NA								
H	L	B3	GPIC/BOOT								
L	L	L	B1	L							

**VIN MUX SELECTOR - P[27:20]**

P27	P26	P25	P24	P23	P22	P21	P20
7	6	5	4	3	2	1	0
L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H

**INPUT MODE SELECTION**

P27	P26	P25	P24	P23	P22	P21	P20
7	6	5	4	3	2	1	0
L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H

**IMAGER SELECTION**

P27	P26	P25	P24	P23	P22	P21	P20
7	6	5	4	3	2	1	0
L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H

**VIN1 SELECTION**

P27	P26	P25	P24	P23	P22	P21	P20
7	6	5	4	3	2	1	0
L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H

**VIN2 SELECTION**

P27	P26	P25	P24	P23	P22	P21	P20
7	6	5	4	3	2	1	0
L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H

**VOUT MUX SELECTOR - P[17:15]**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

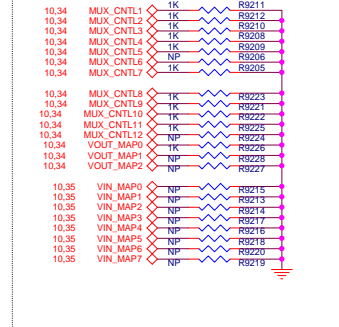
**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

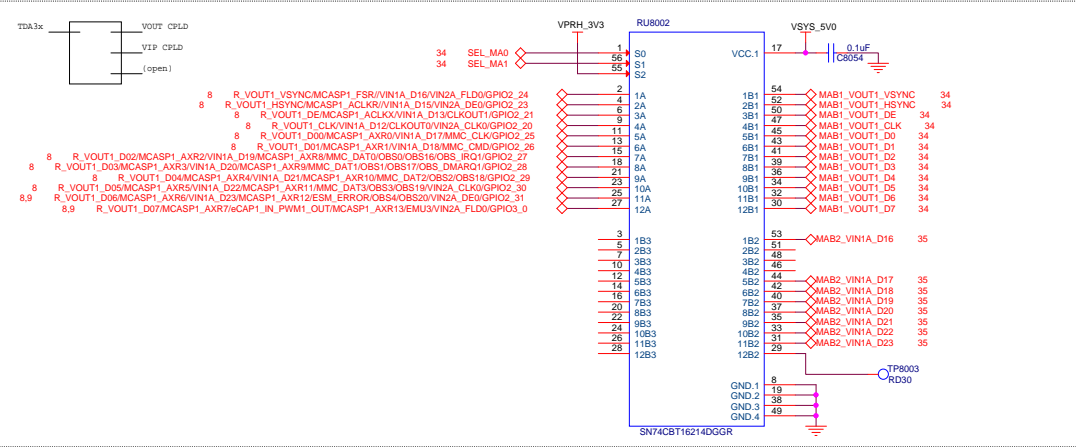
**VOUT MODE SELECTION**

P17	P16	P15
15	14	13
L	L	L
H	H	H

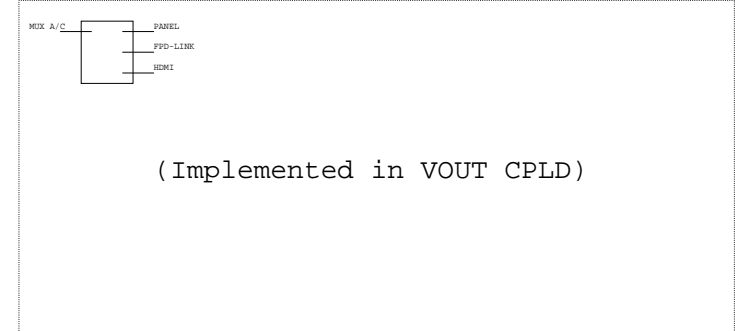
Note: Mux selection population options for default select. Over-rides CPLD internal Pullups. (Value = 1K)



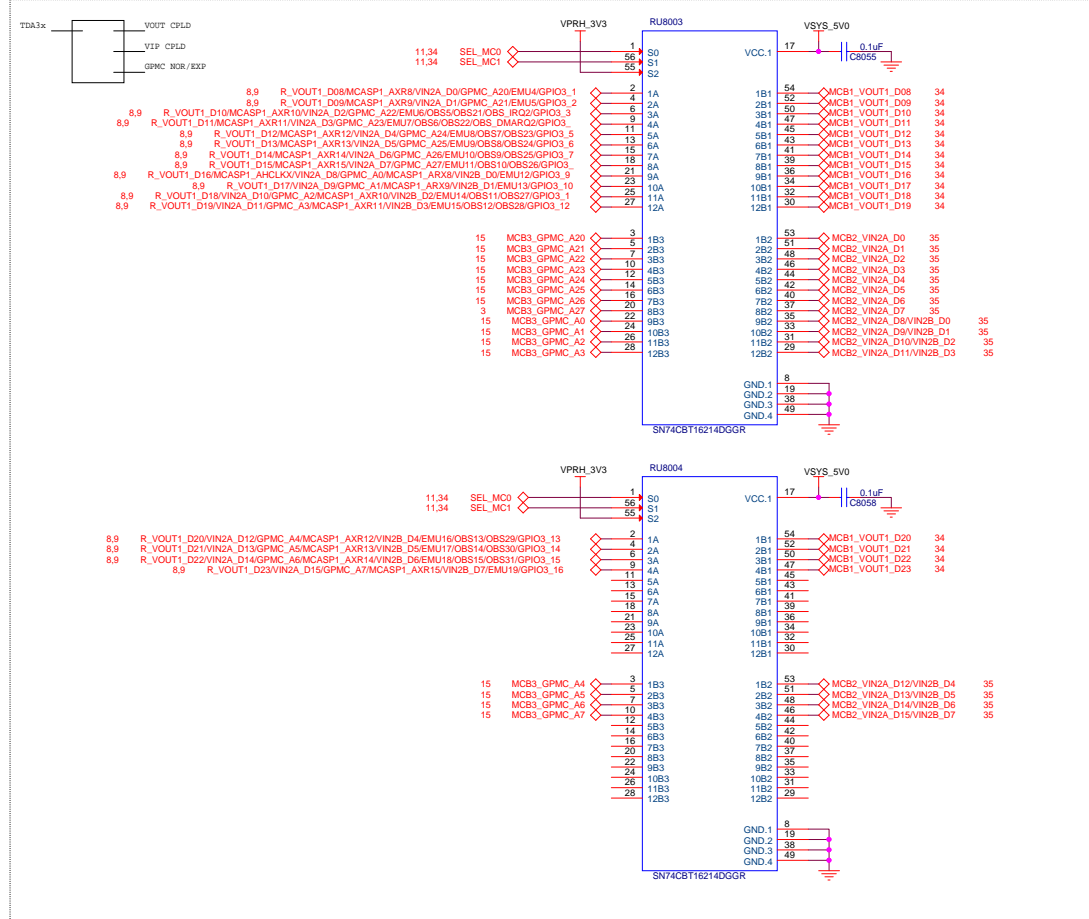
### Board Mux A



### Board Mux B



### Board Mux C



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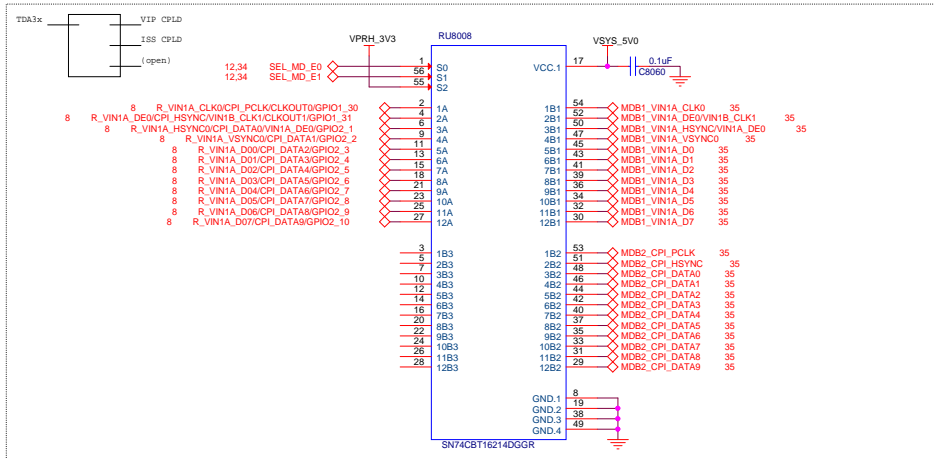
Title: TDA3x/DRA7x/DM50x - 15X15 EVM

Page Contents: MUX A/B/C

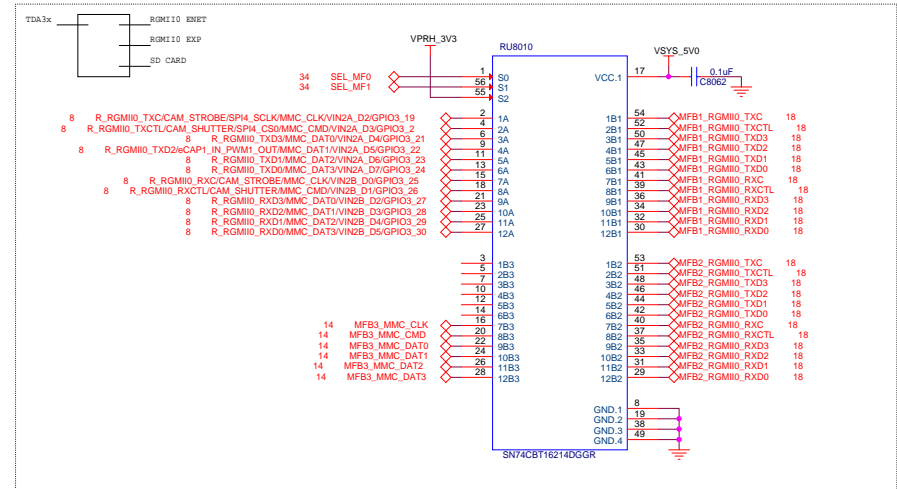
Size: C DOC NO: 517542 REV: A

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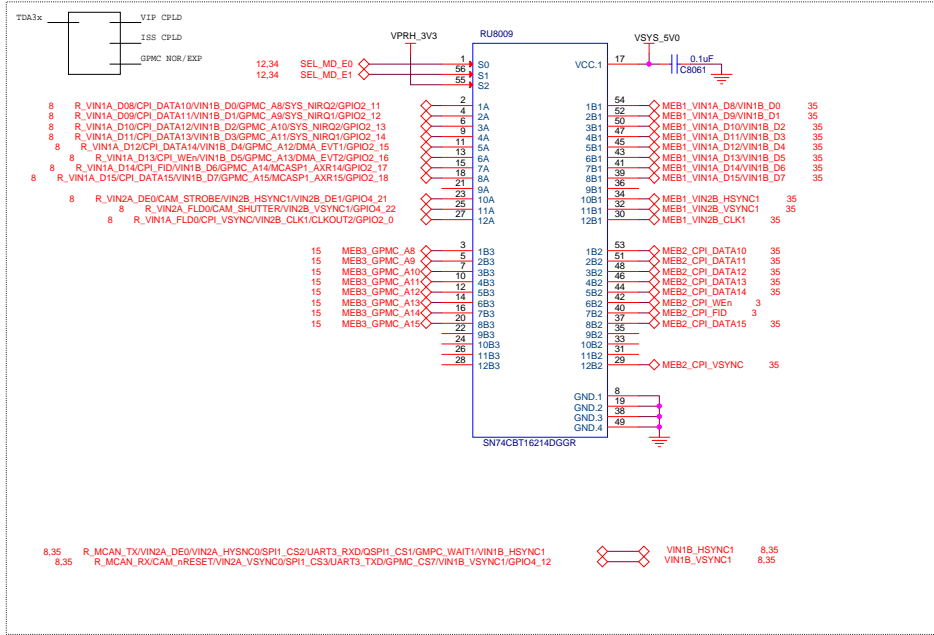
### Board Mux D



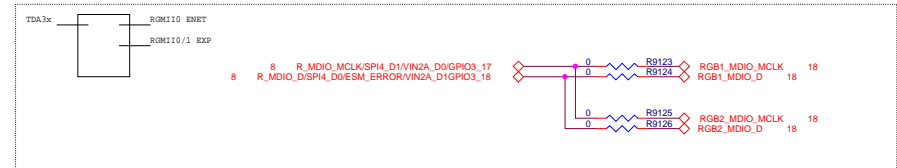
### Board Mux F



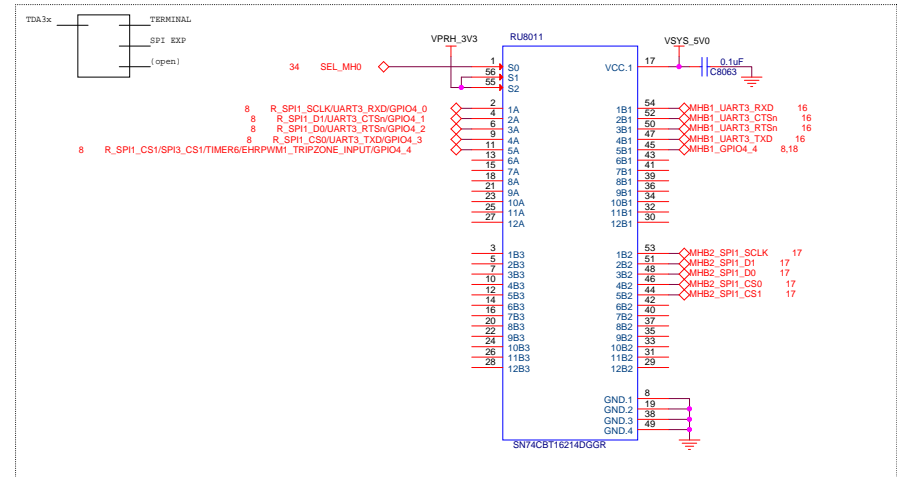
### Board Mux E



### Board Mux G



### Board Mux H



TEXAS INSTRUMENTS INCORPORATED

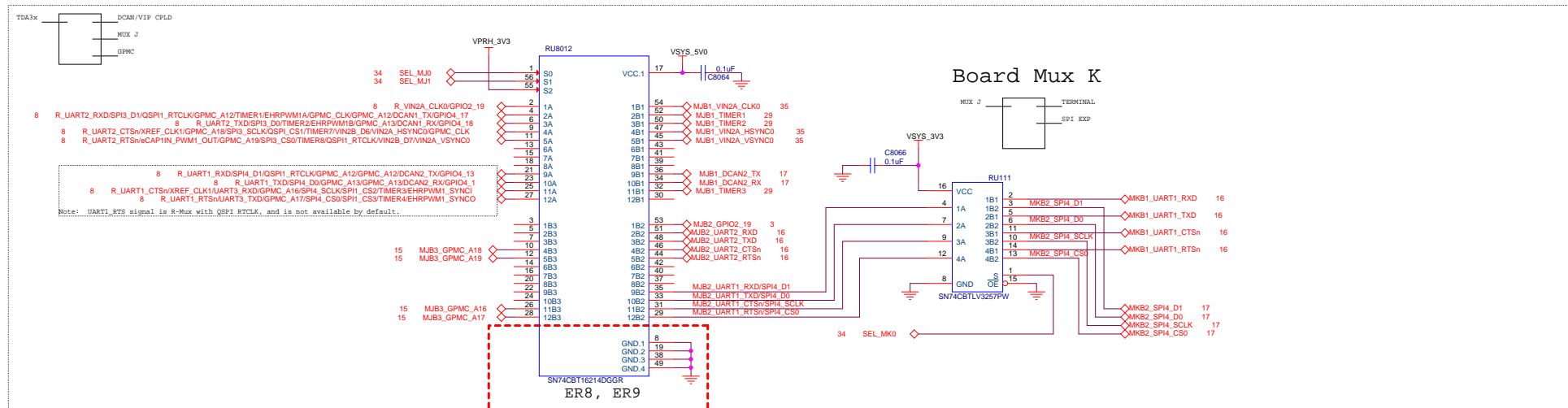
Title: TDA3N/DRA76x/DMS6x - 15X15 EVM

Page Contents: MUX D/E/F/G/H

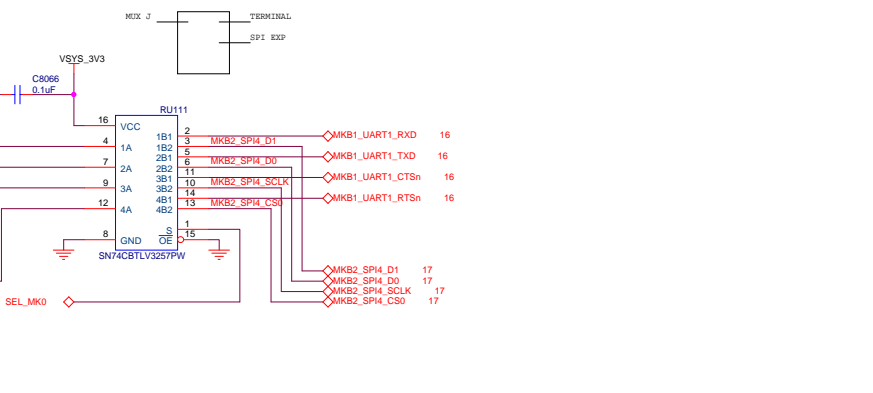
Size: C DOC NO: 517542 REV: A

Date: Wednesday, May 03, 2017 Sheet 12 of 37

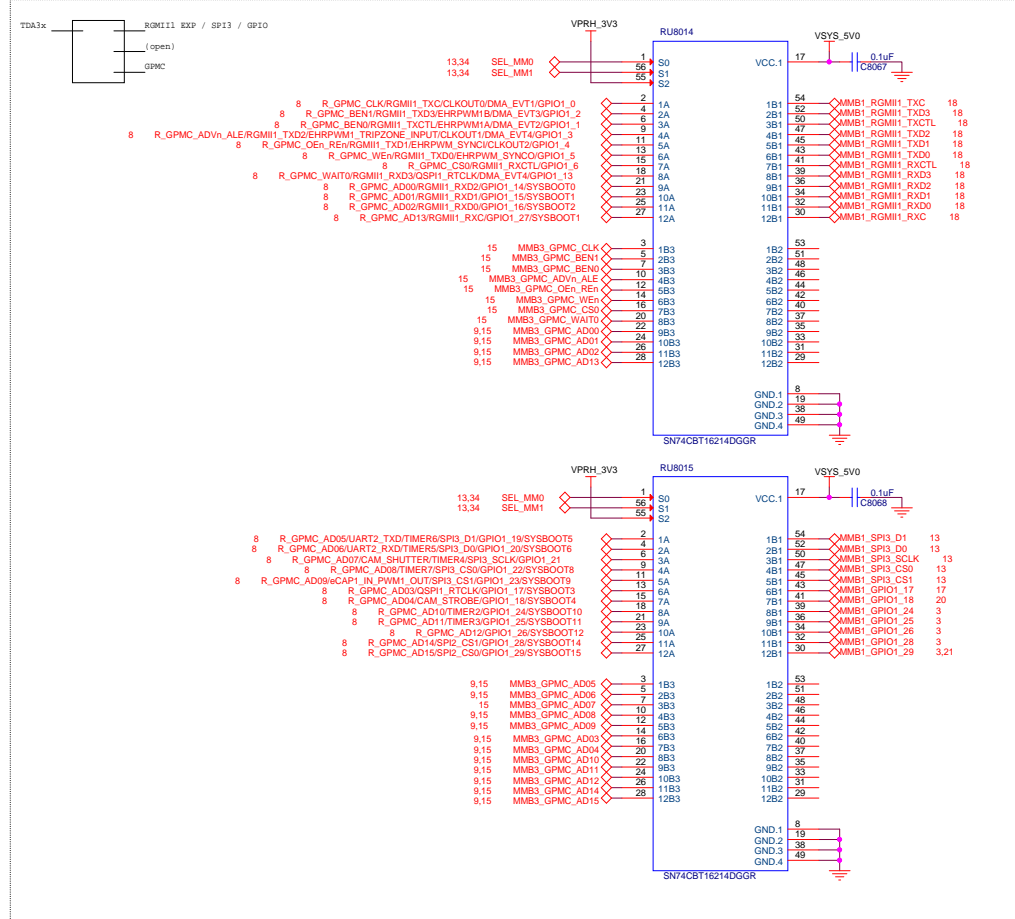
# Board Mux J



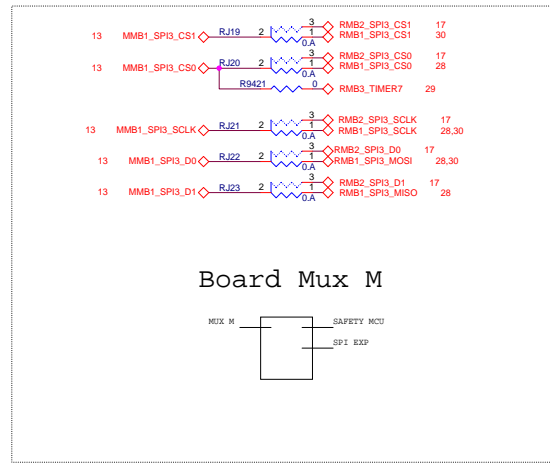
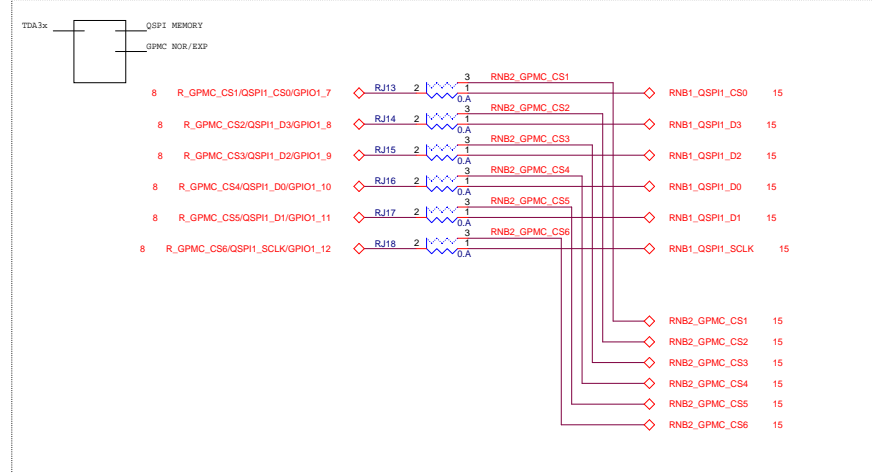
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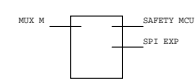
# Board Mux M



# Board Mux N



# Board Mux W



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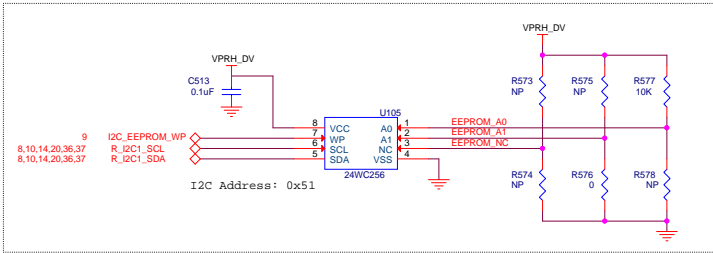
Title: TDA3x/DRA76xD/DM50x - 15X15 EVM

Page Contents: MUX H/J/K/M/N

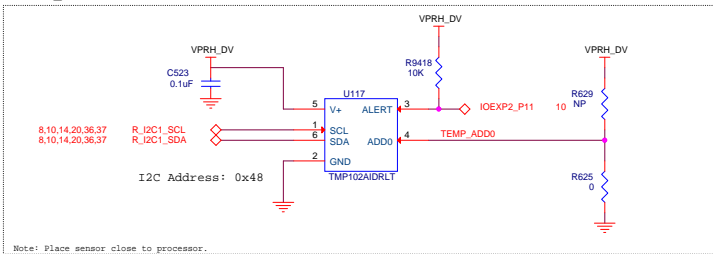
Size: C DOC NO: 517542 REV: B

Date: Wednesday, May 03, 2017 Sheet 13 of 37

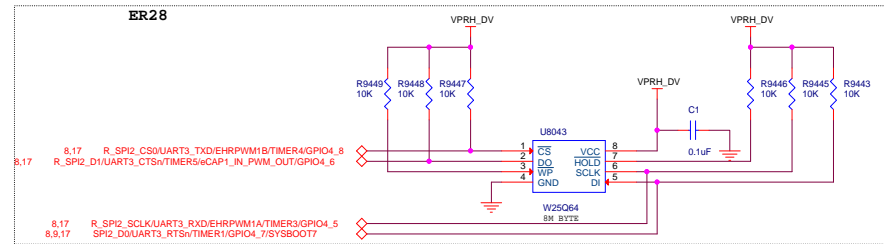
## Board EEPROM



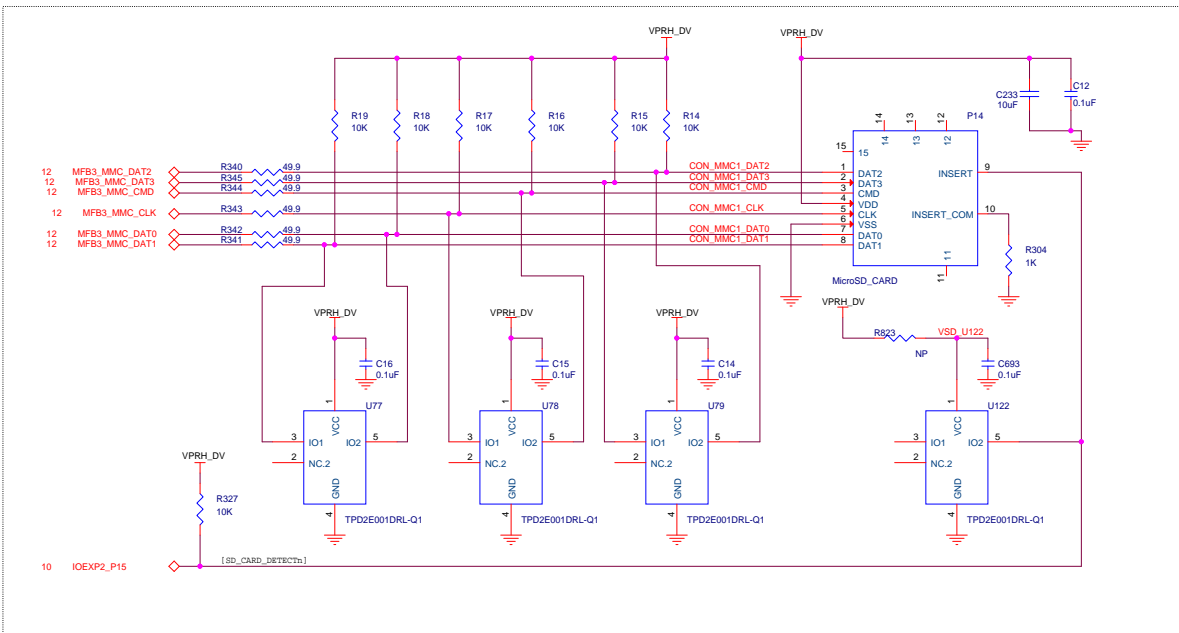
## Temperature Sensor



## SPI MEMORY 8M BYTE



## SD CARD



TEXAS INSTRUMENTS INCORPORATED

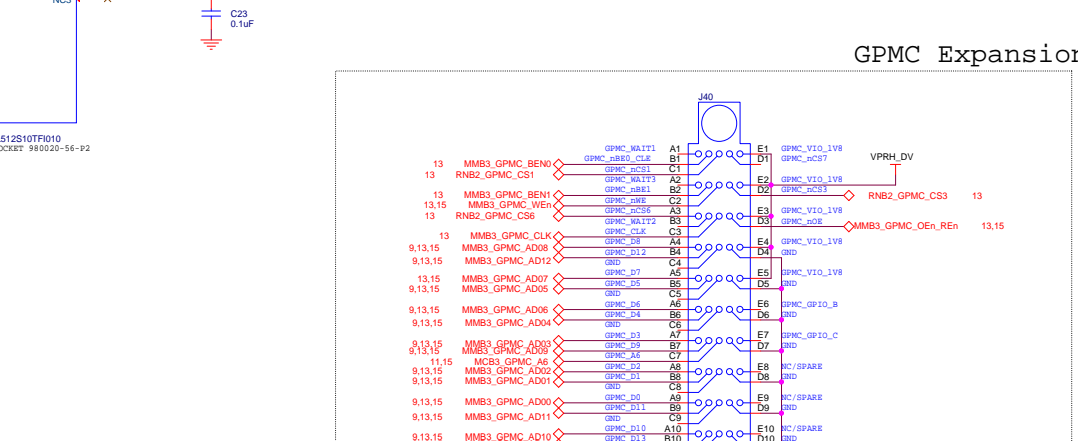
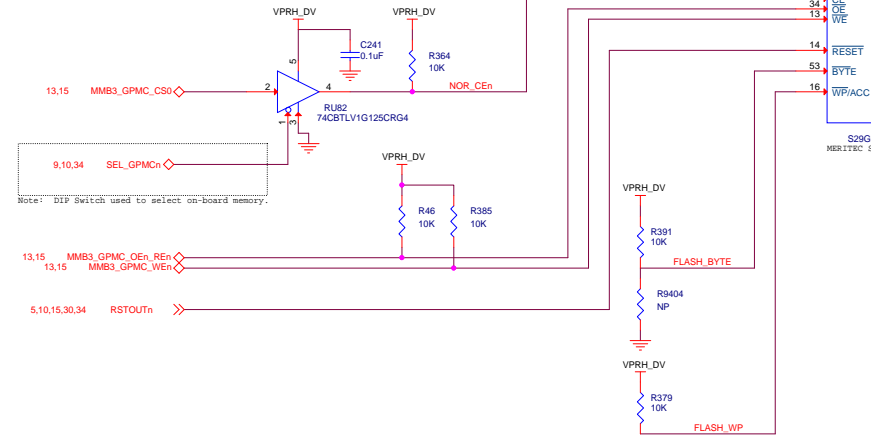
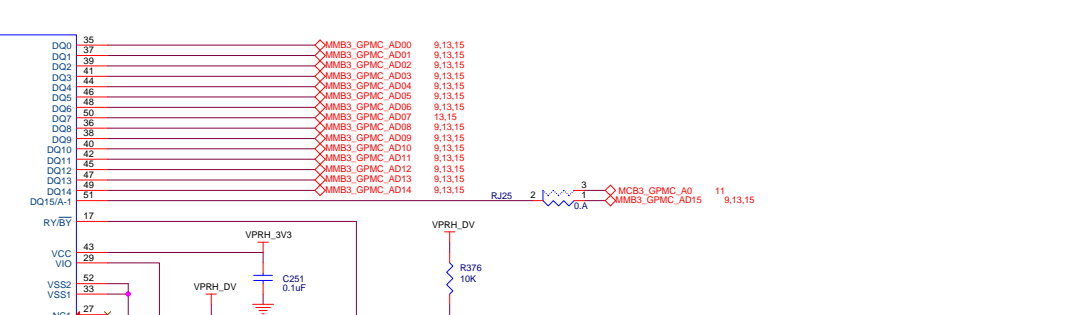
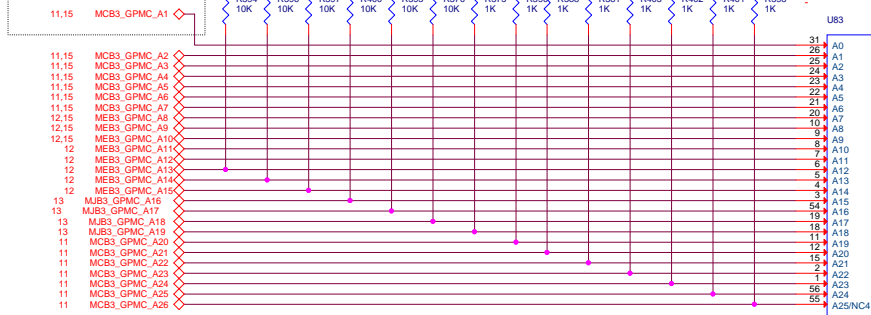
Title: TDA3x/DRA7x/DM50x - 15x15 EVM

Page Contents: SD CARD/EEPROM/TMP

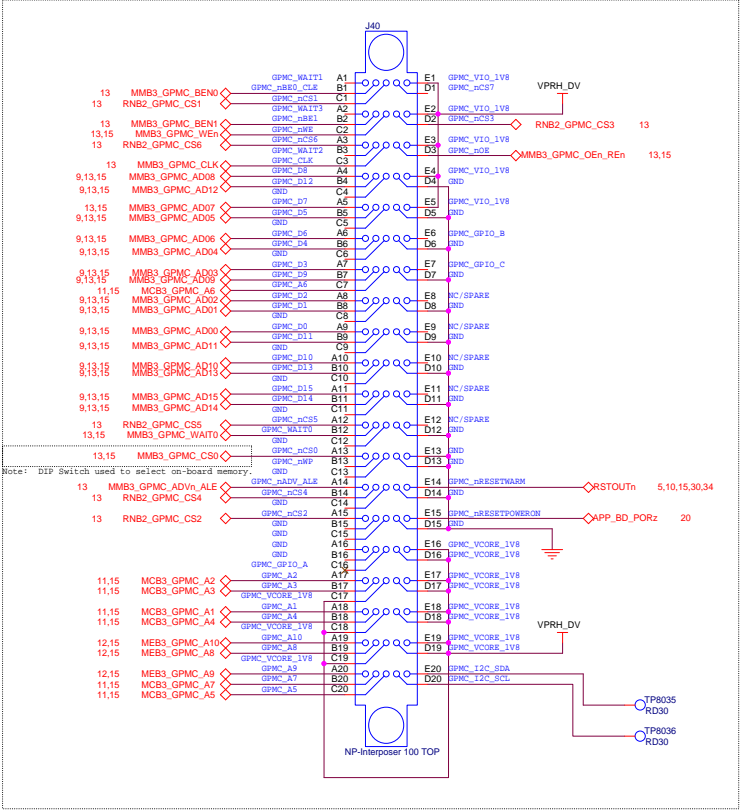
Size: C DOC NO: 517542 REV: D

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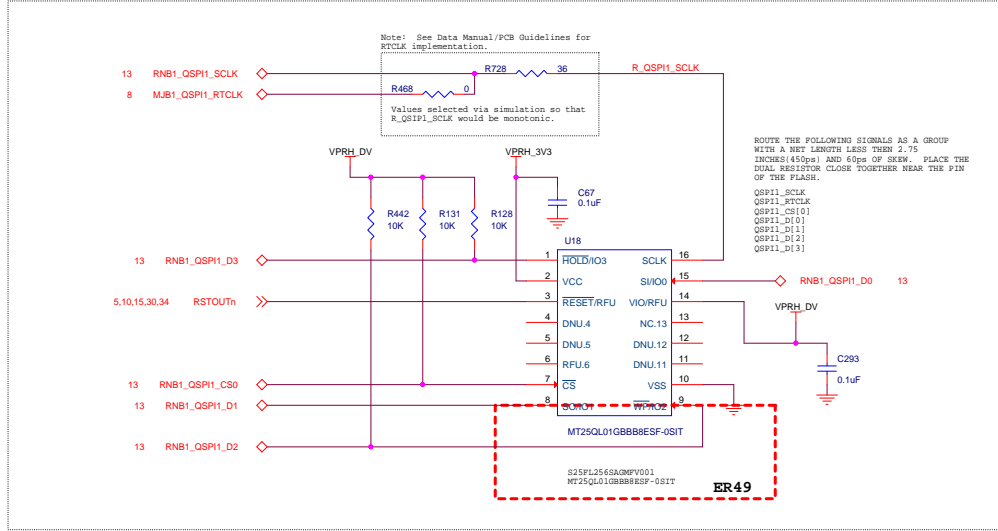
Note: GPMC A1 maps to memory A0 because 16b device.



### GPMC Expansion



### QSPI Memory

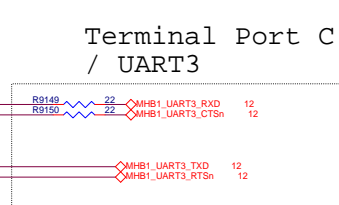
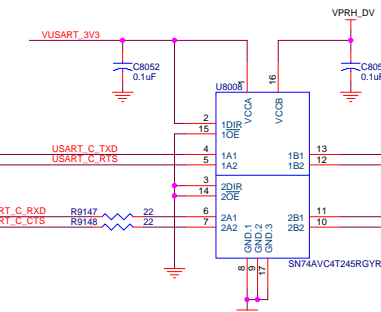
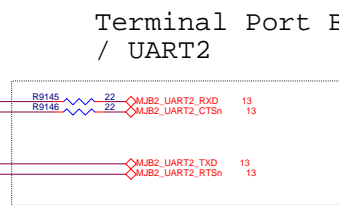
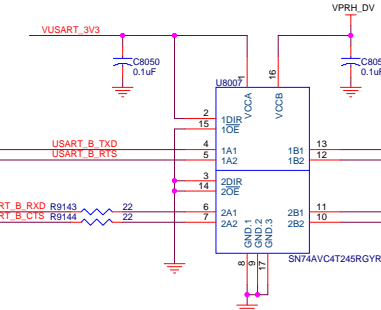
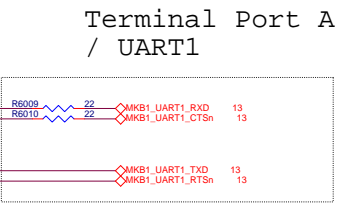
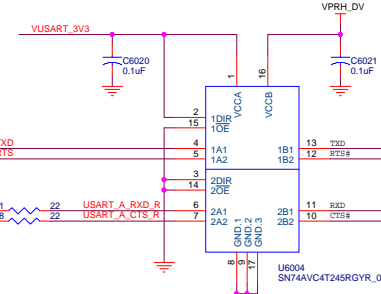
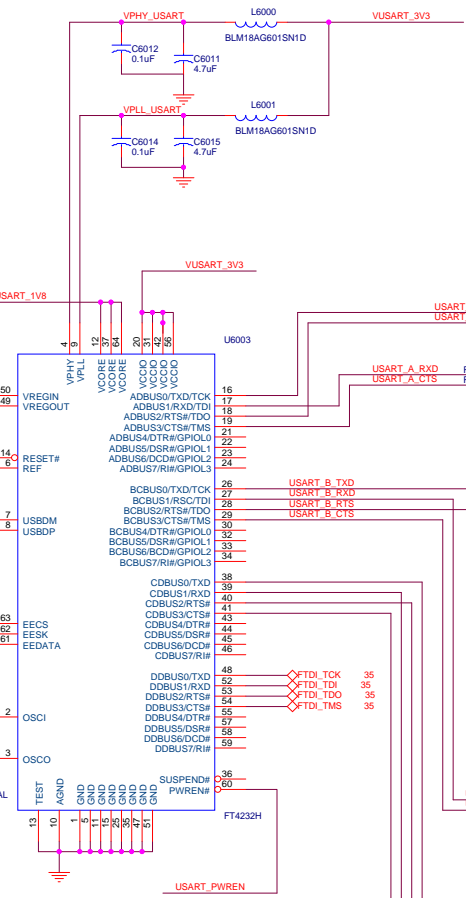
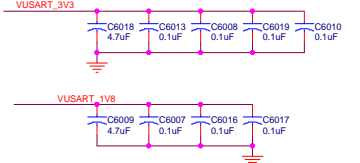
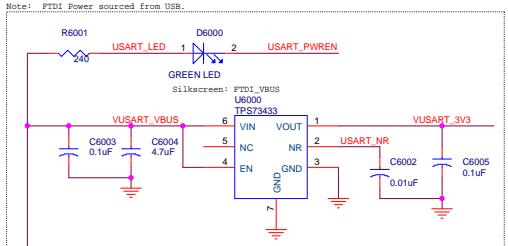
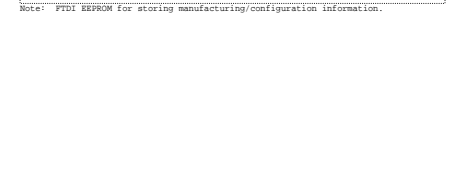
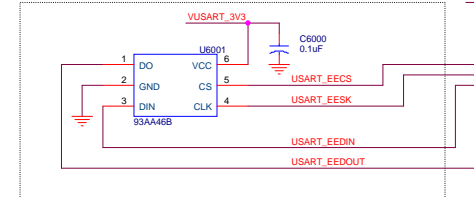
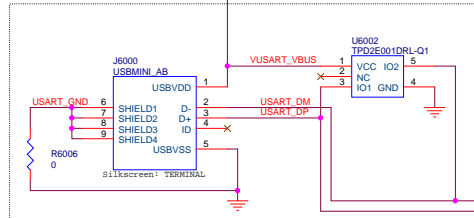


### TEXAS INSTRUMENTS INCORPORATED

Title: TDA3M/DRA76vDM50x - 15K15 EVM			
Page Contents: MEM NONVOLATILE			
Size: C	DOC NO: 517542	REV: D	
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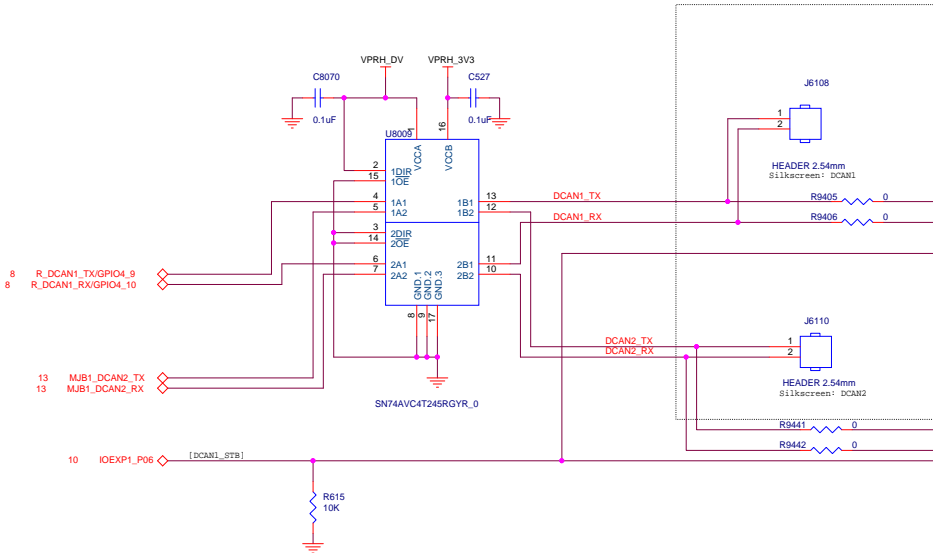


# Terminal Connector

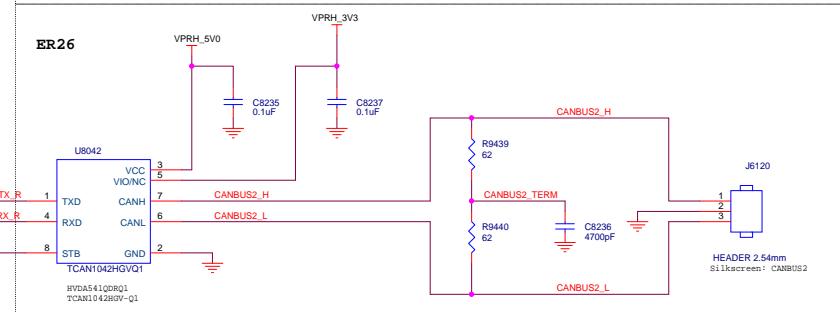
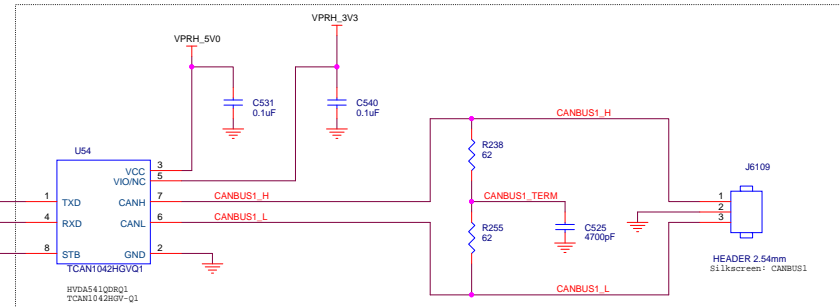


<b>TEXAS INSTRUMENTS INCORPORATED</b>			
Title: TDA3x/DRA7x/DM50x - 15X15 EVM			
Page Contents: USB FTDI UART			
Size: C	DOC NO: 517542	REV: A	
Date: Wednesday, May 03, 2017	Sheet 16	of	37

### DCAN1/2 Headers

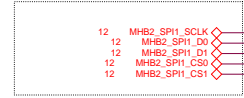


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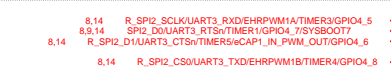


### CAN2 Transceiver/Header

### SPI1



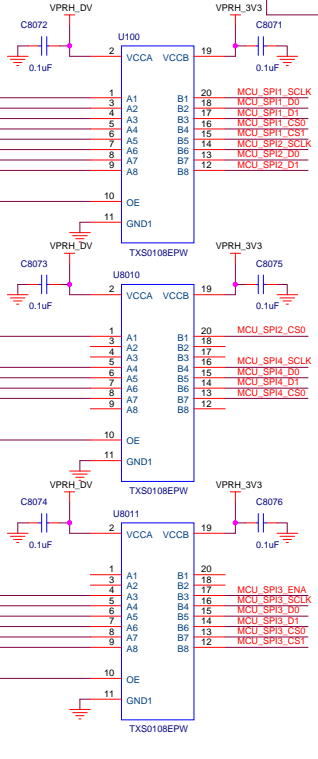
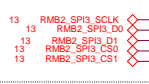
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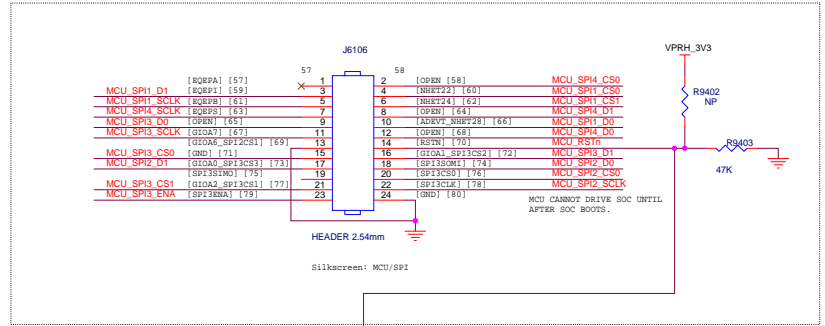
### SPI4



### SPI3



### Safety MCU/SPI Interface



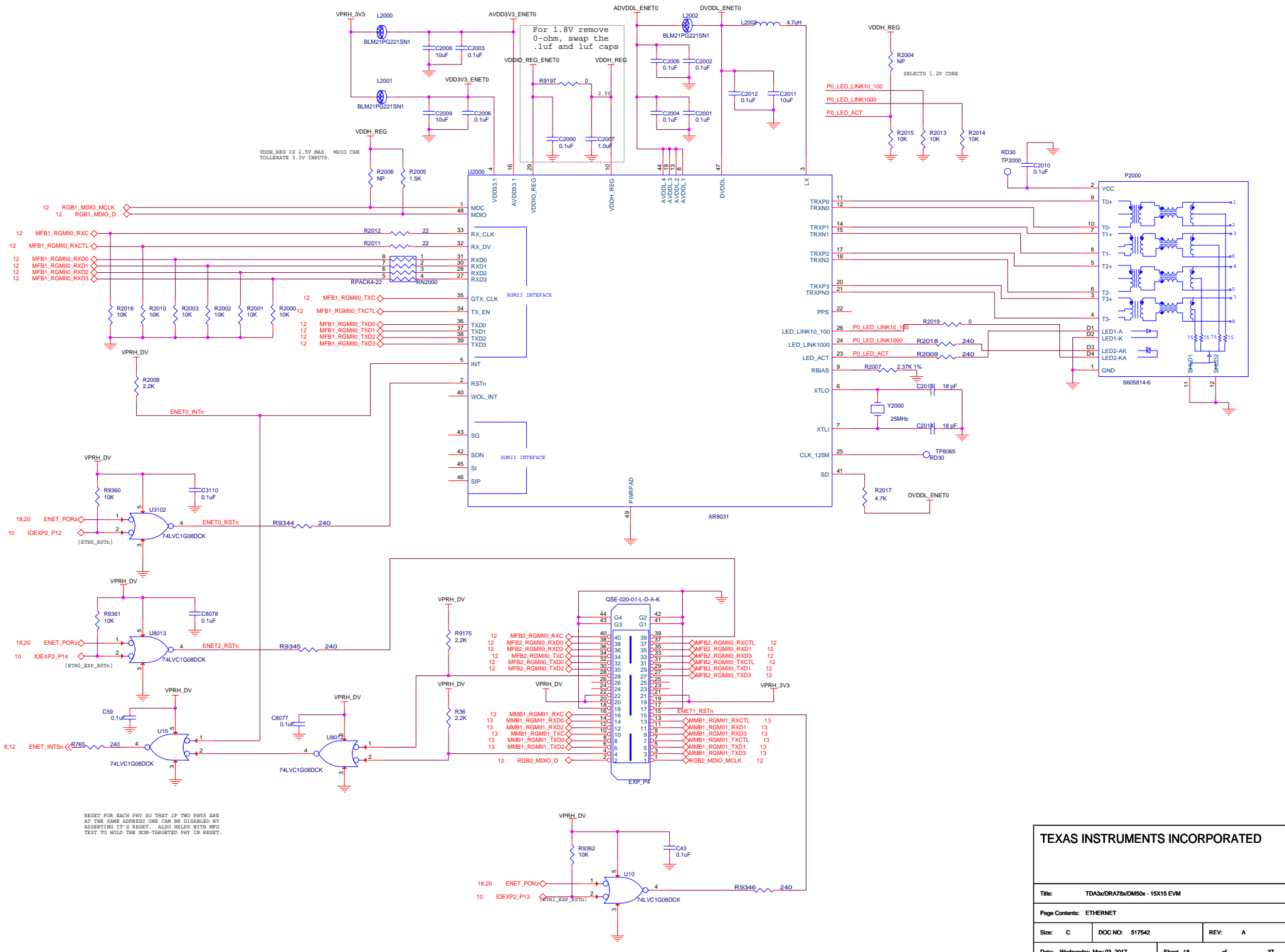
**TEXAS INSTRUMENTS INCORPORATED**

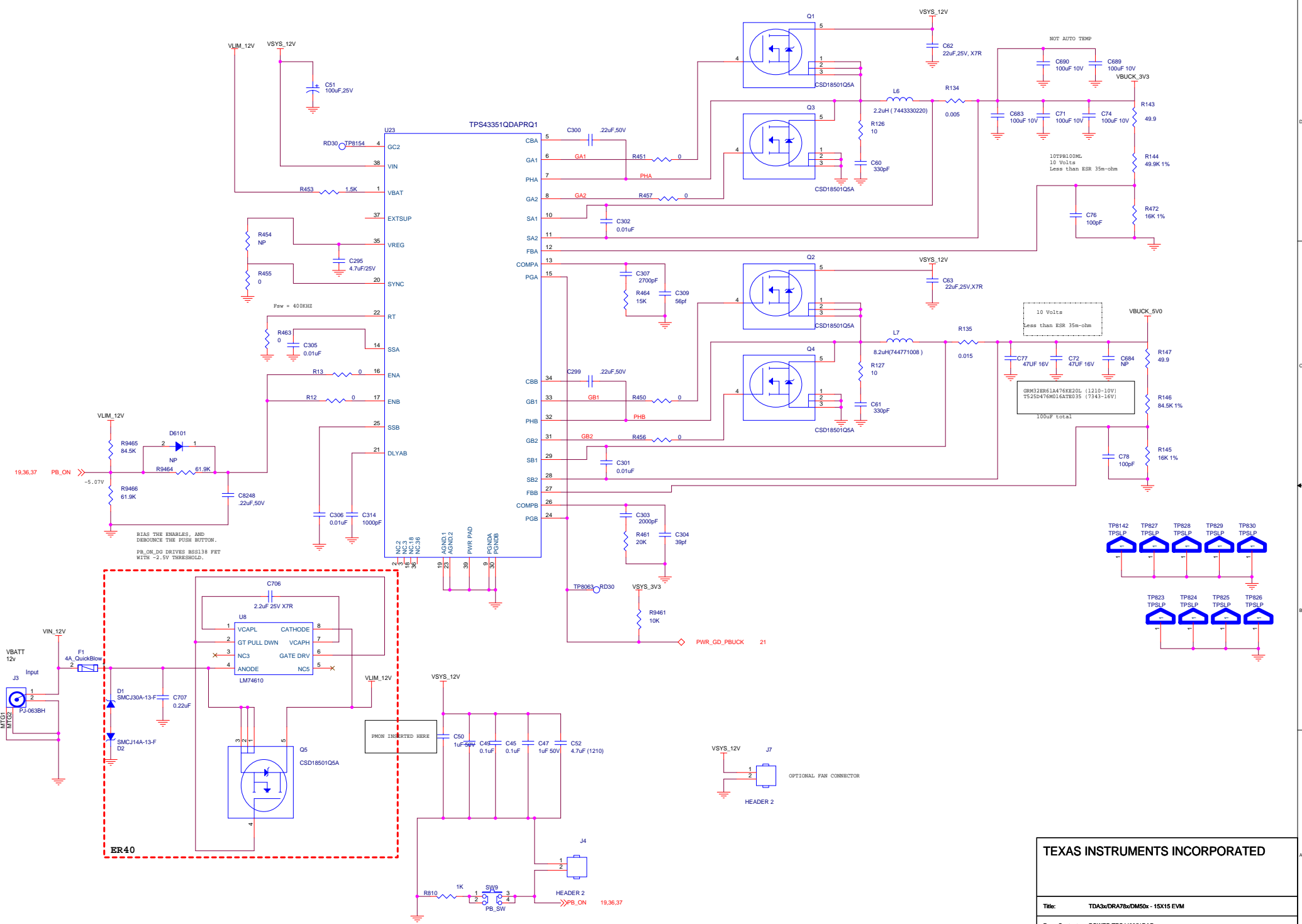
Title: TDA3M/DRA76vDM50x - 15X15 EVM

Page Contents: CANSAFETY MCU

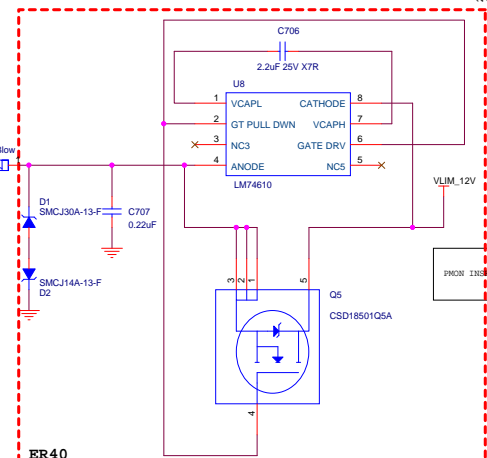
Size: C    DOC NO: 517542    REV: D

Date: Wednesday, May 03, 2017    Sheet 17    of    37

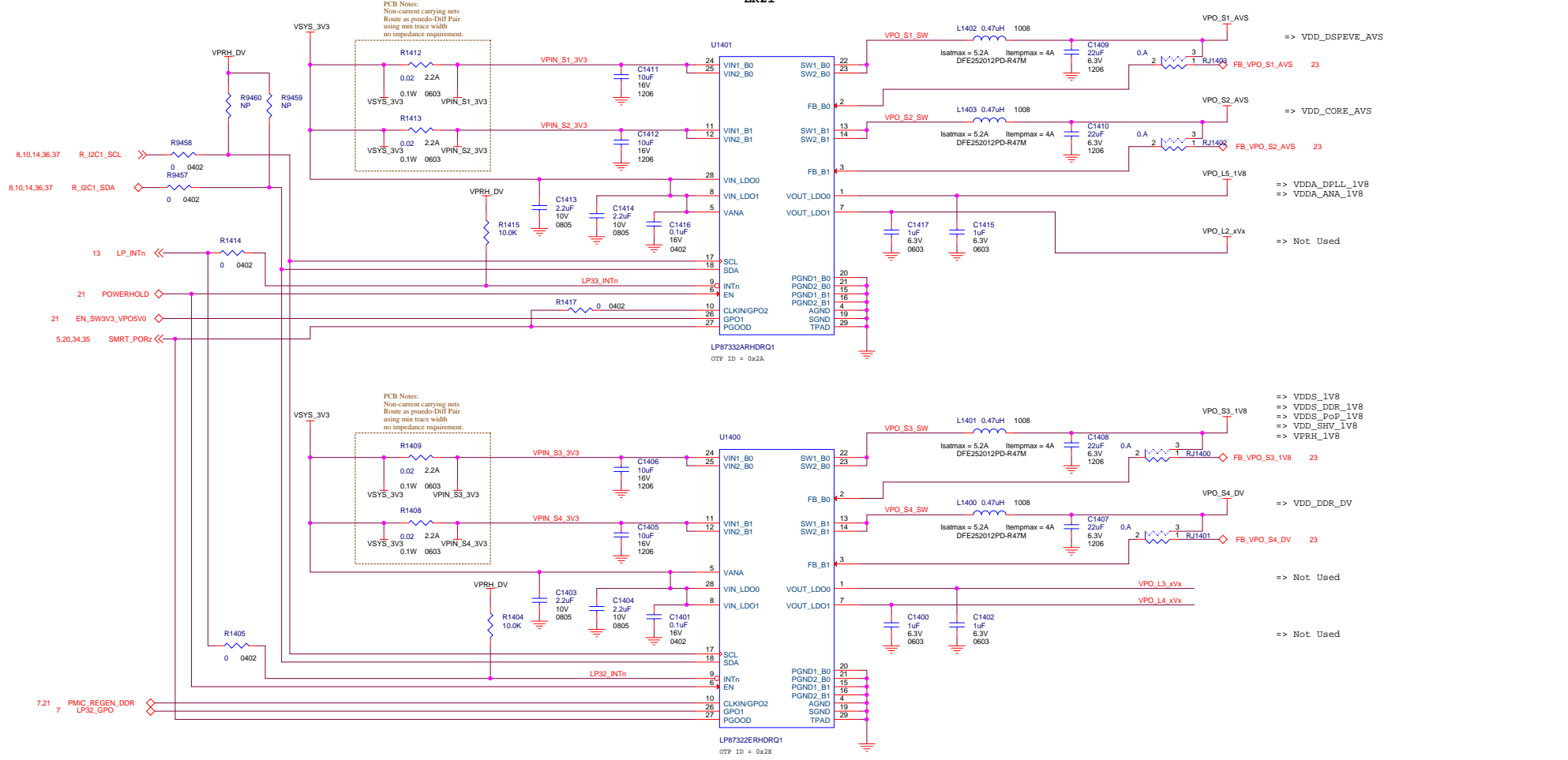




BLAS THE ENABLES, AND DEBOUNCE THE PUSH BUTTON.  
 PB\_ON\_DG DRIVES BS1138 FET WITH -2.5V THRESHOLD.



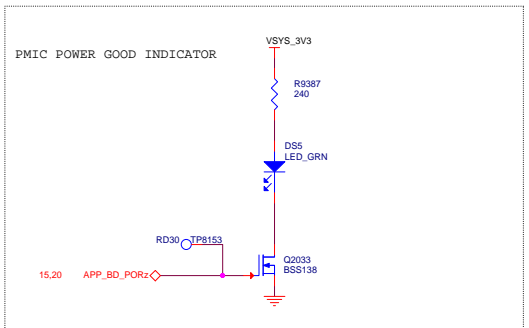
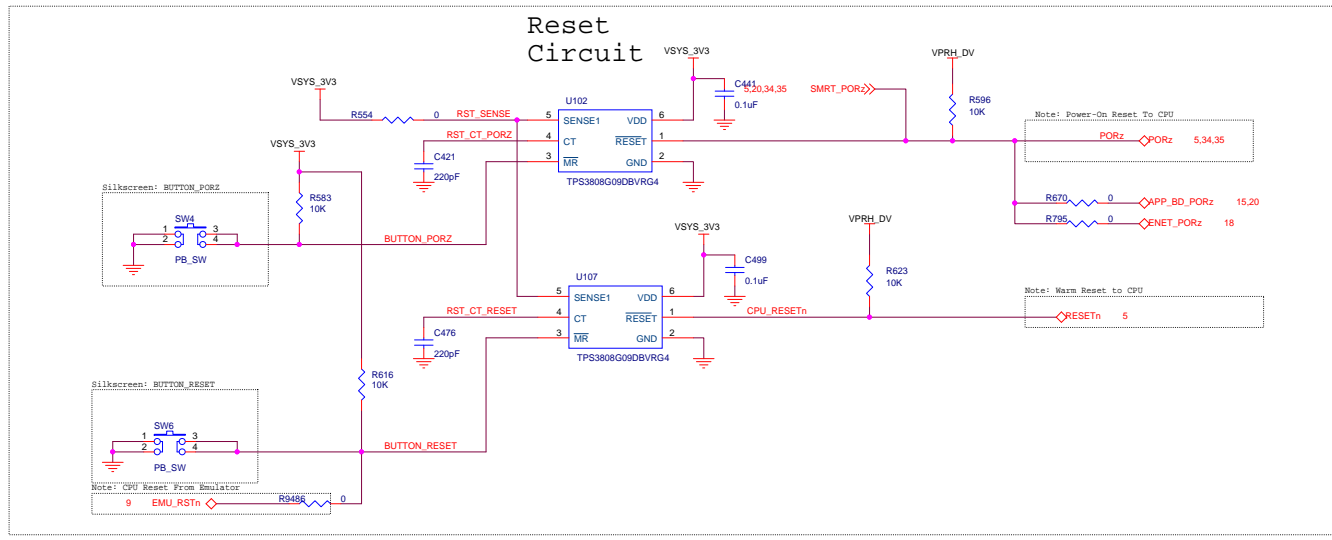
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Title: TDA3w/DRA76w/DM50x - 15X15 EVM			
Page Contents: POWER TPS443351DAP			
Size: C	DOC NO: 517542	REV: D	
Date: Wednesday, May 03, 2017	Sheet 19	of	37



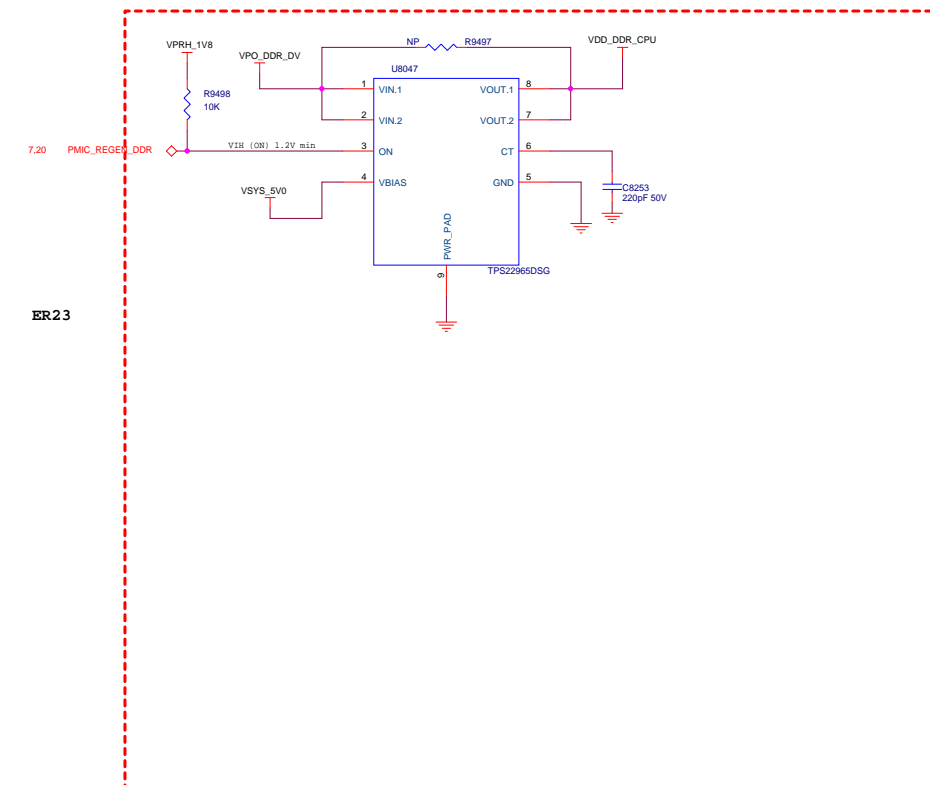
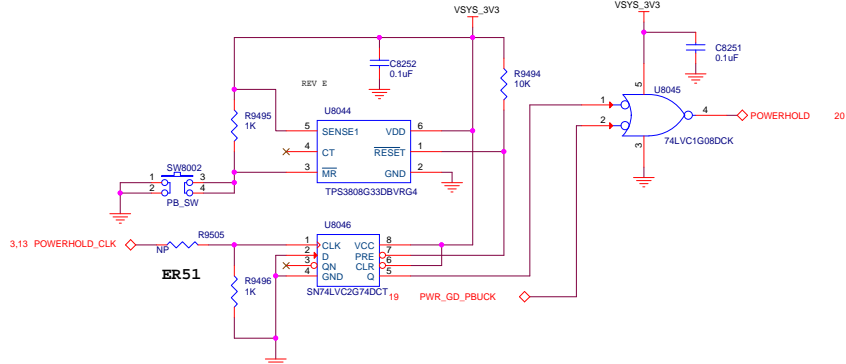
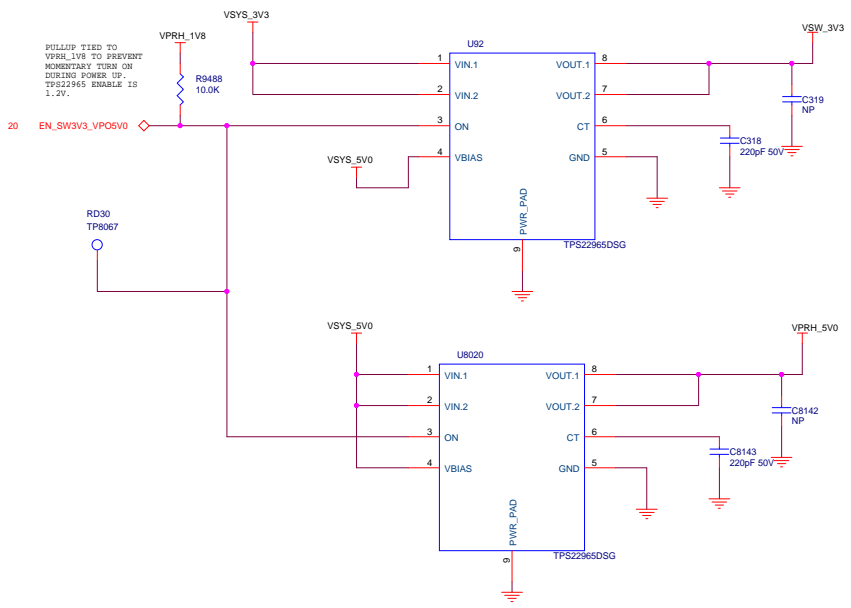
PCB Notes:  
 Non-current carrying nets  
 Route as pseudo-Diff Pair  
 using min trace width  
 no impedance requirement.

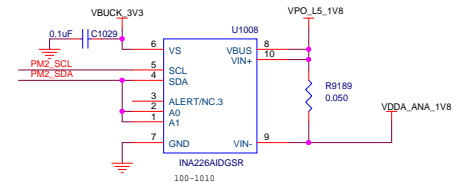
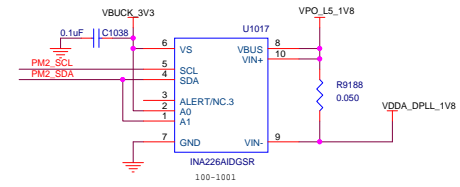
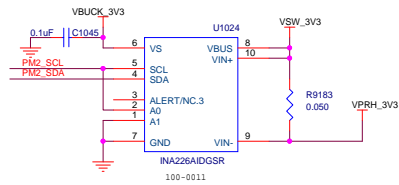
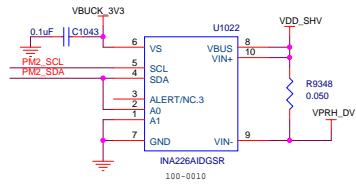
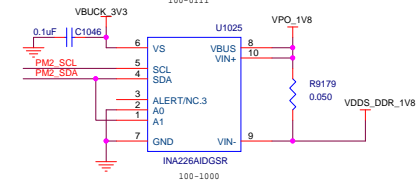
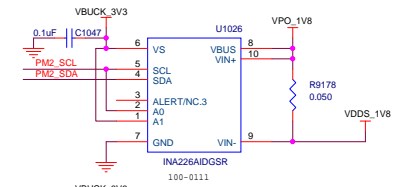
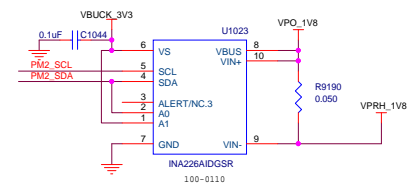
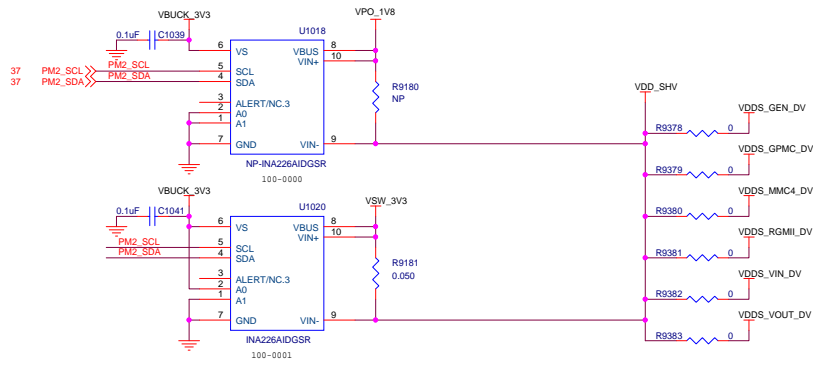
PCB Notes:  
 Non-current carrying nets  
 Route as pseudo-Diff Pair  
 using min trace width  
 no impedance requirement.

### Reset Circuit



<b>TEXAS INSTRUMENTS INCORPORATED</b>			
Title: TDA3x/DRA7x/DM50x - 15x15 EVM			
Page Contents: POWER PMIC			
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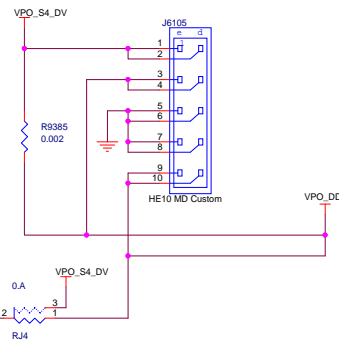
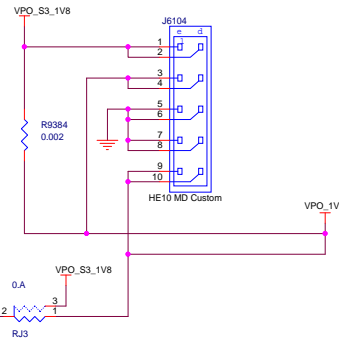
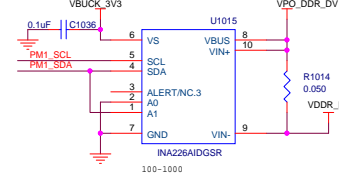
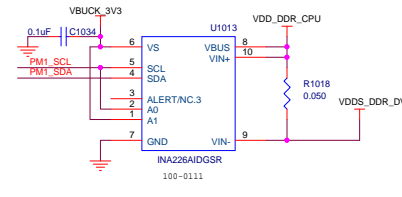
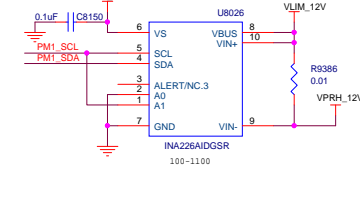
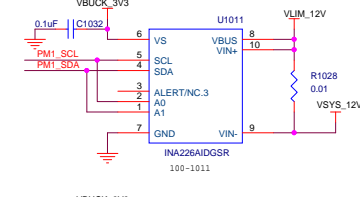
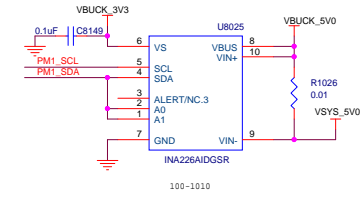
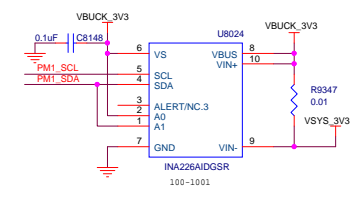
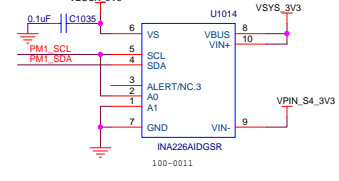
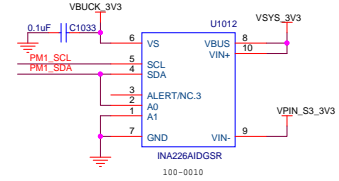
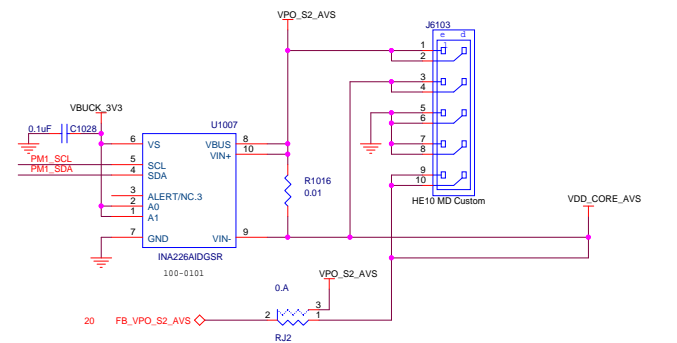
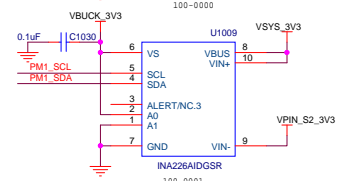
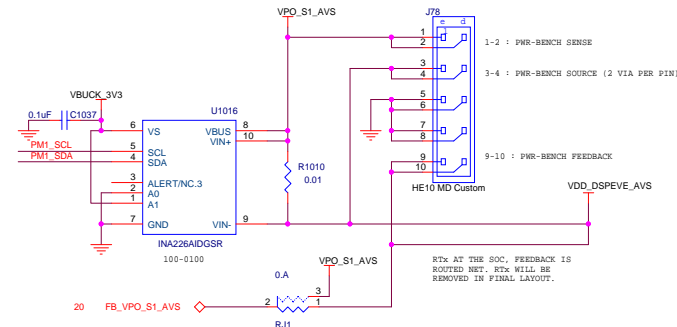
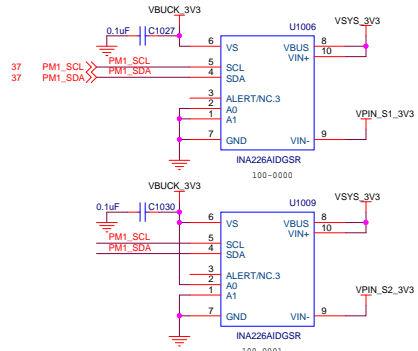
Title: TDA3x/DRA76x/DM50x - 15X15 EVM

Page Contents: POWER MONITORS

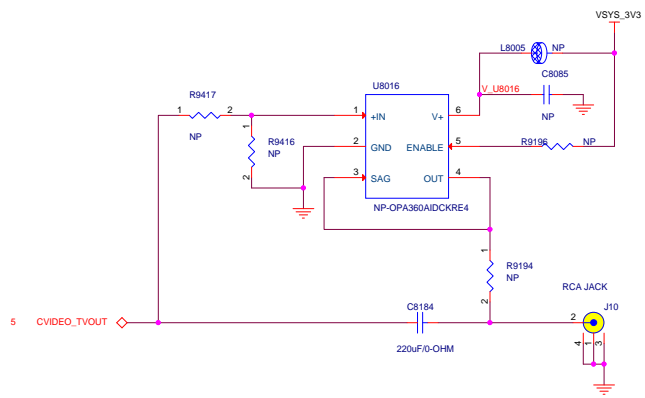
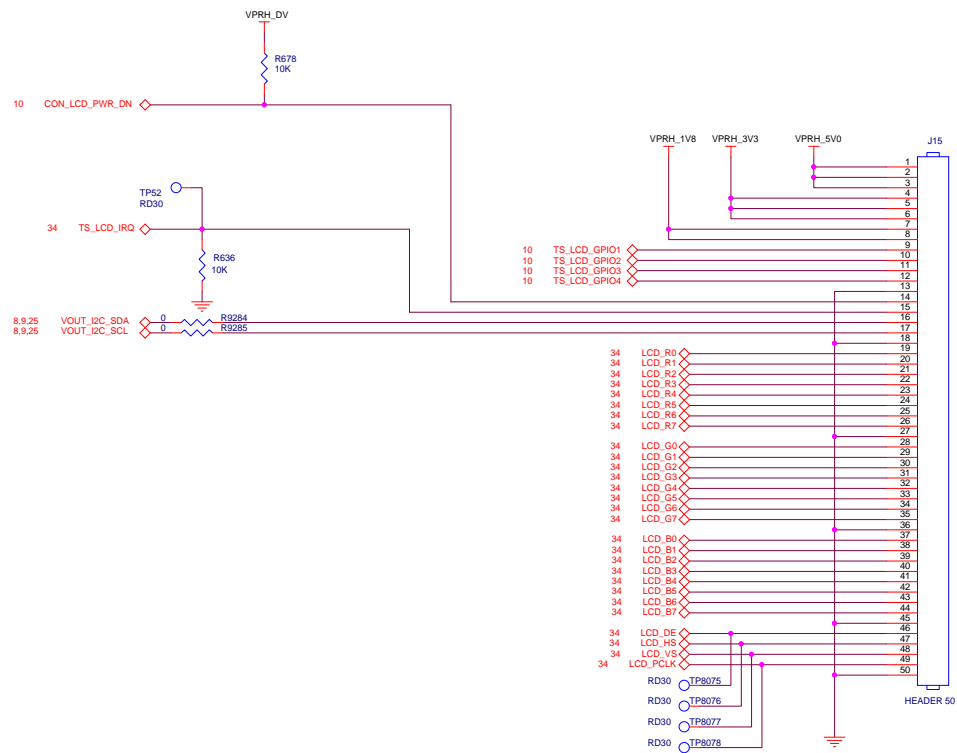
Size: C DOC NO: 517542 REV: B

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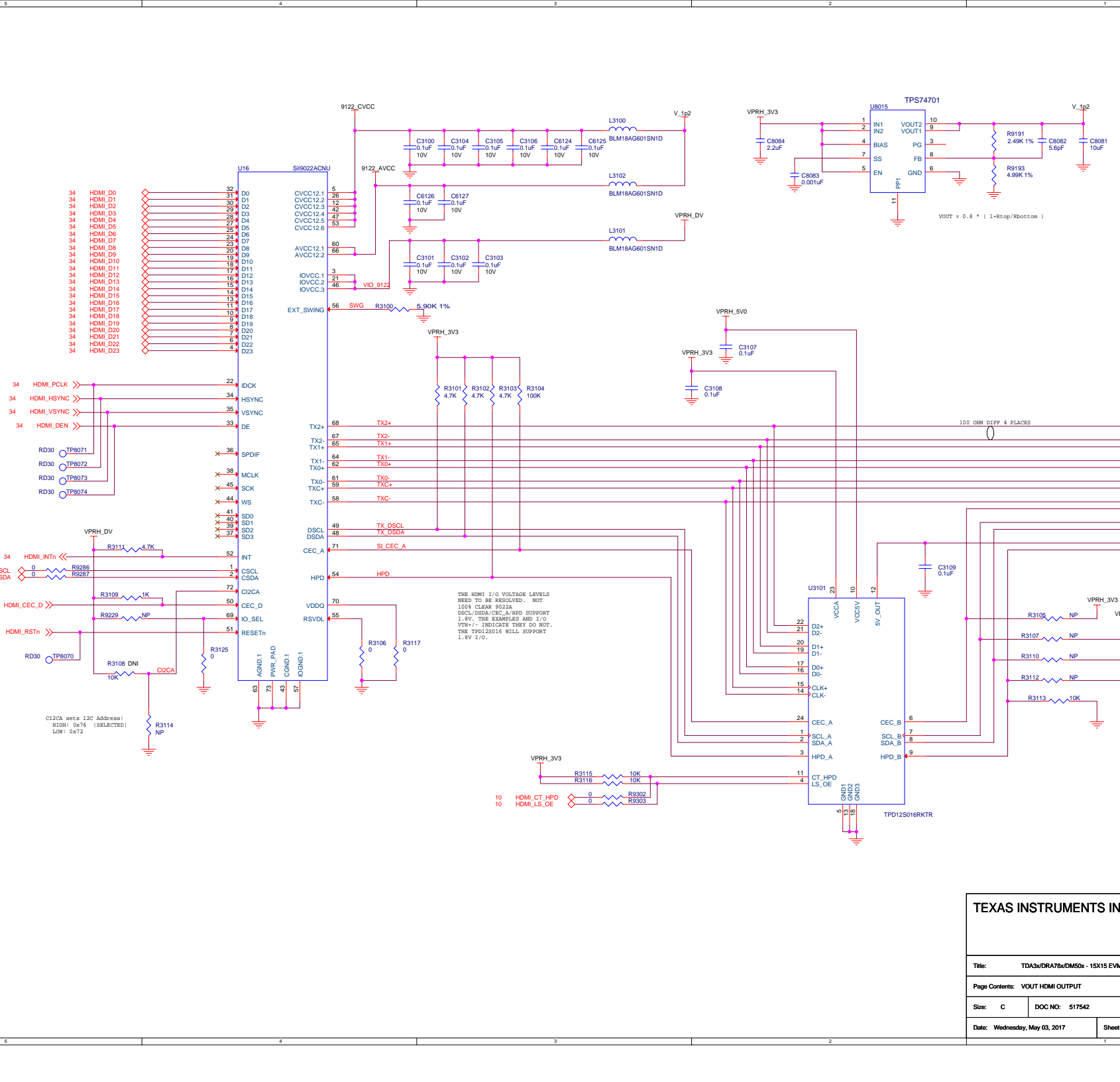


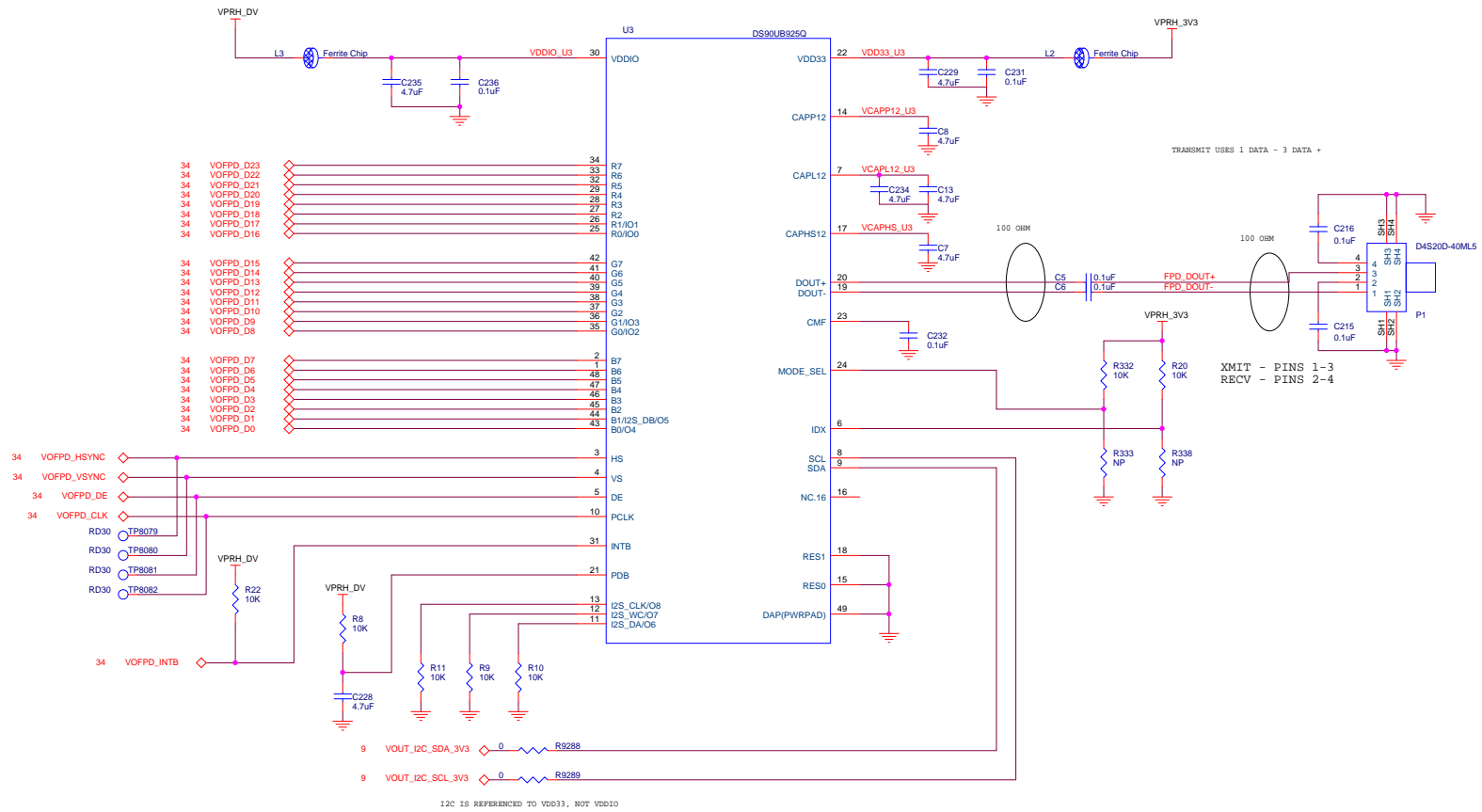


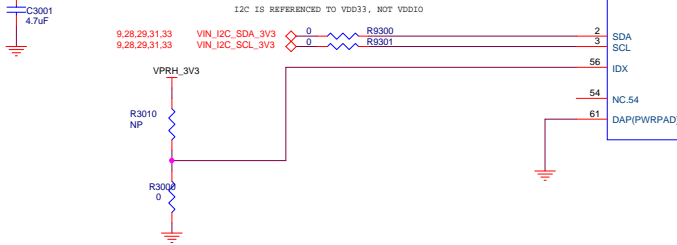
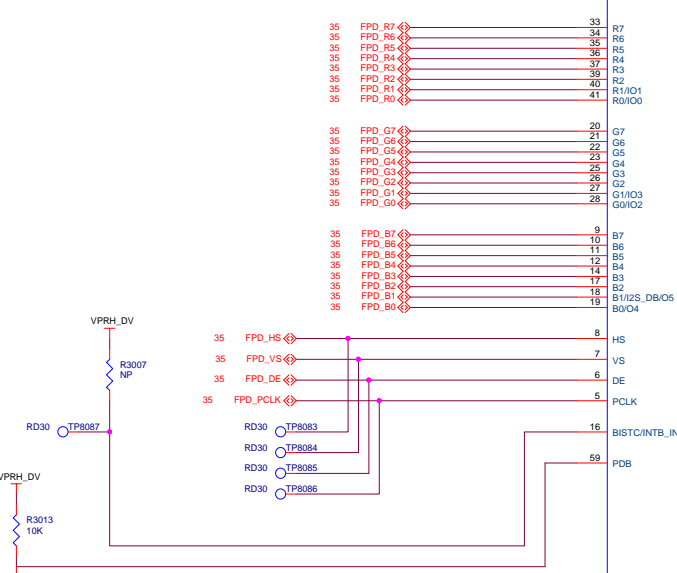
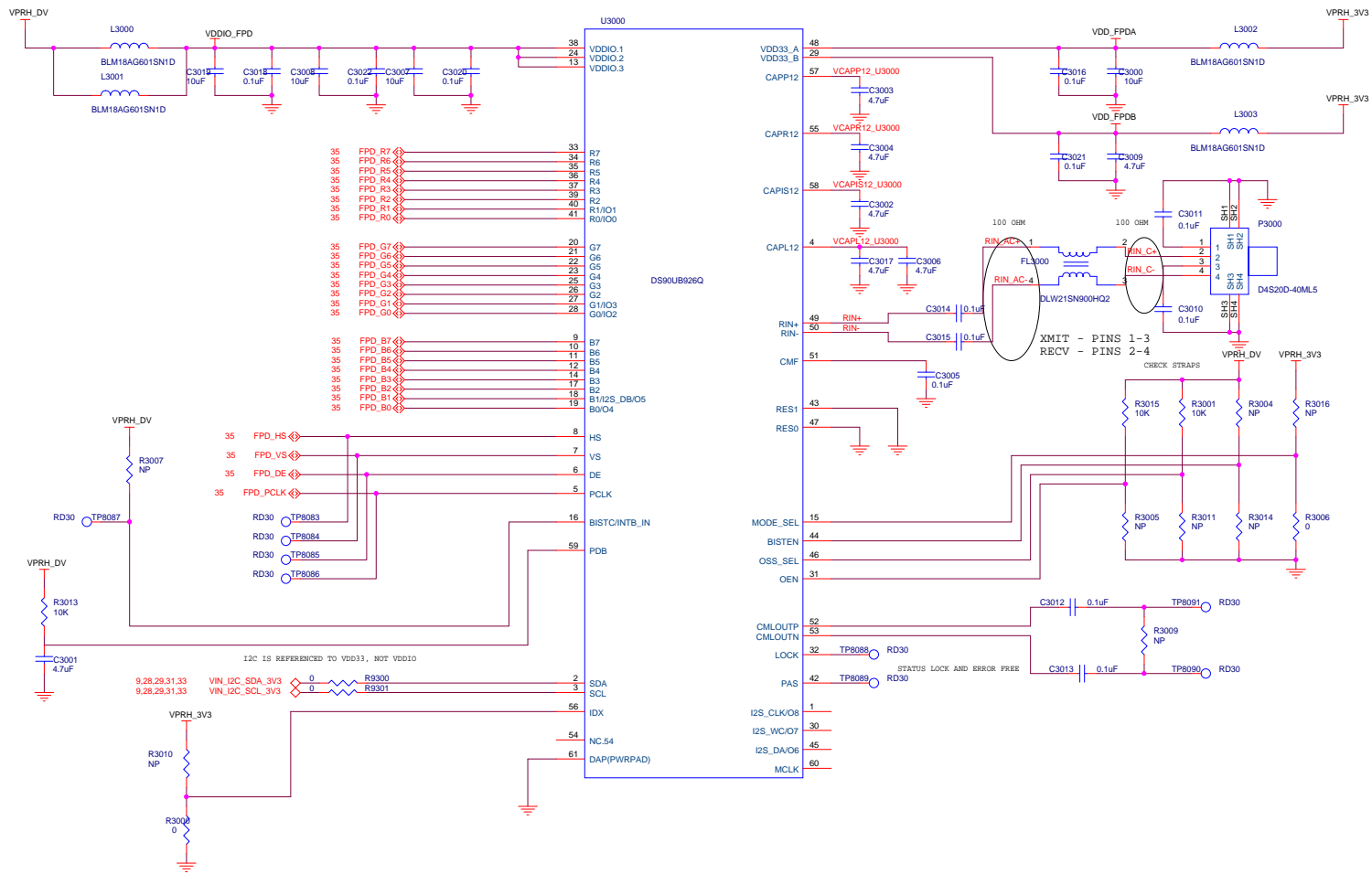
<b>TEXAS INSTRUMENTS INCORPORATED</b>			
Title: TDA3x/DRA76x/DM50x - 15X15 EVM			
Page Contents: POWER BENCHMONITORS			
Size: C	DOC NO: 517542	REV: A	
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<b>TEXAS INSTRUMENTS INCORPORATED</b>			
Title: TDA3x/DRA76x/DM50x - 15X15 EVM			
Page Contents: VOUT LCD CONNECTOR			
Size: C	DOC NO: 517542	REV: A	
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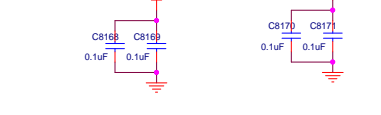
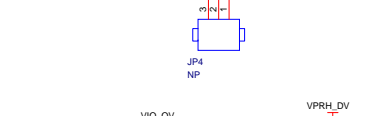
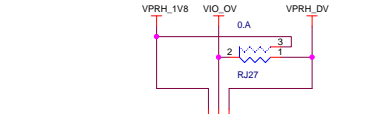
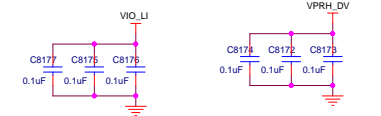
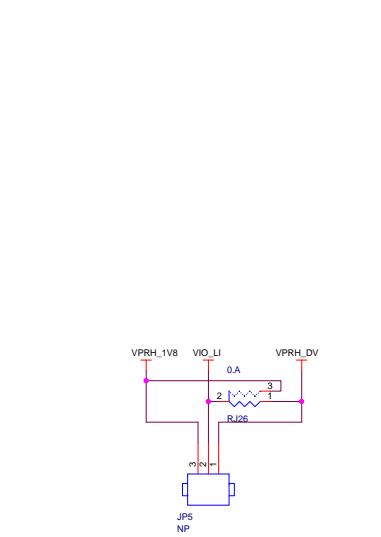
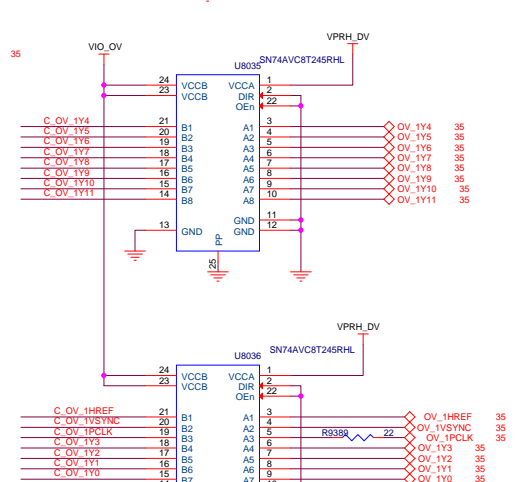
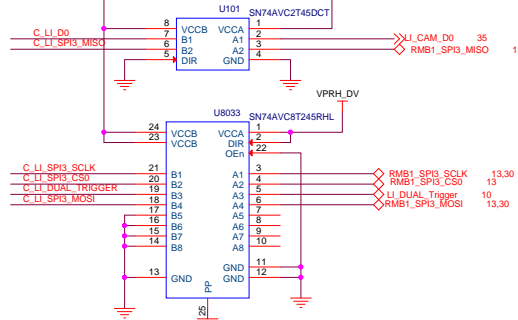
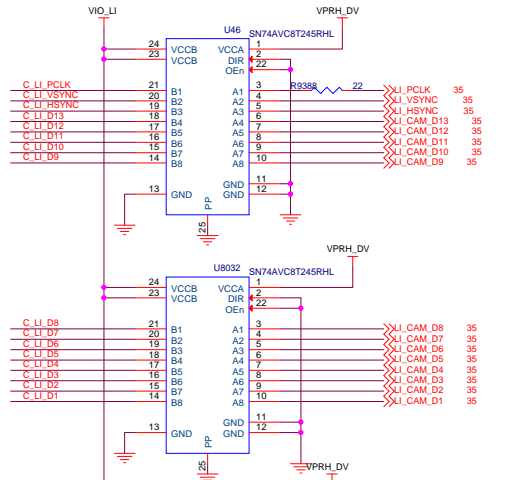
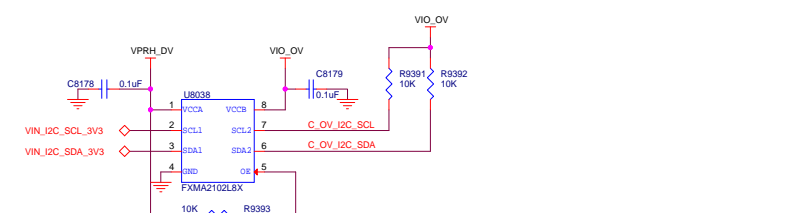
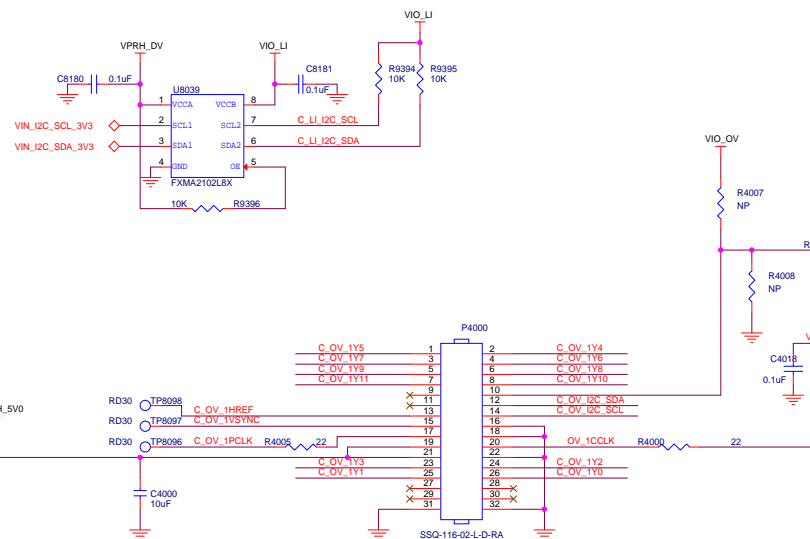
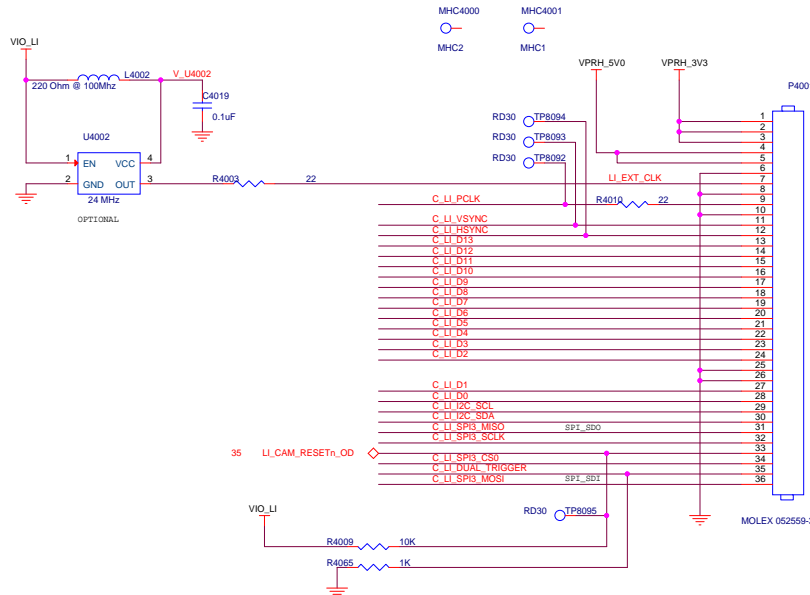






TEXAS INSTRUMENTS INCORPORATED

Title: TDA3xDRA76xDM50x - 15X15 EVM			
Page Contents: VIN DS90UH26Q			
Size: C	DOC NO: 517542	REV: A	
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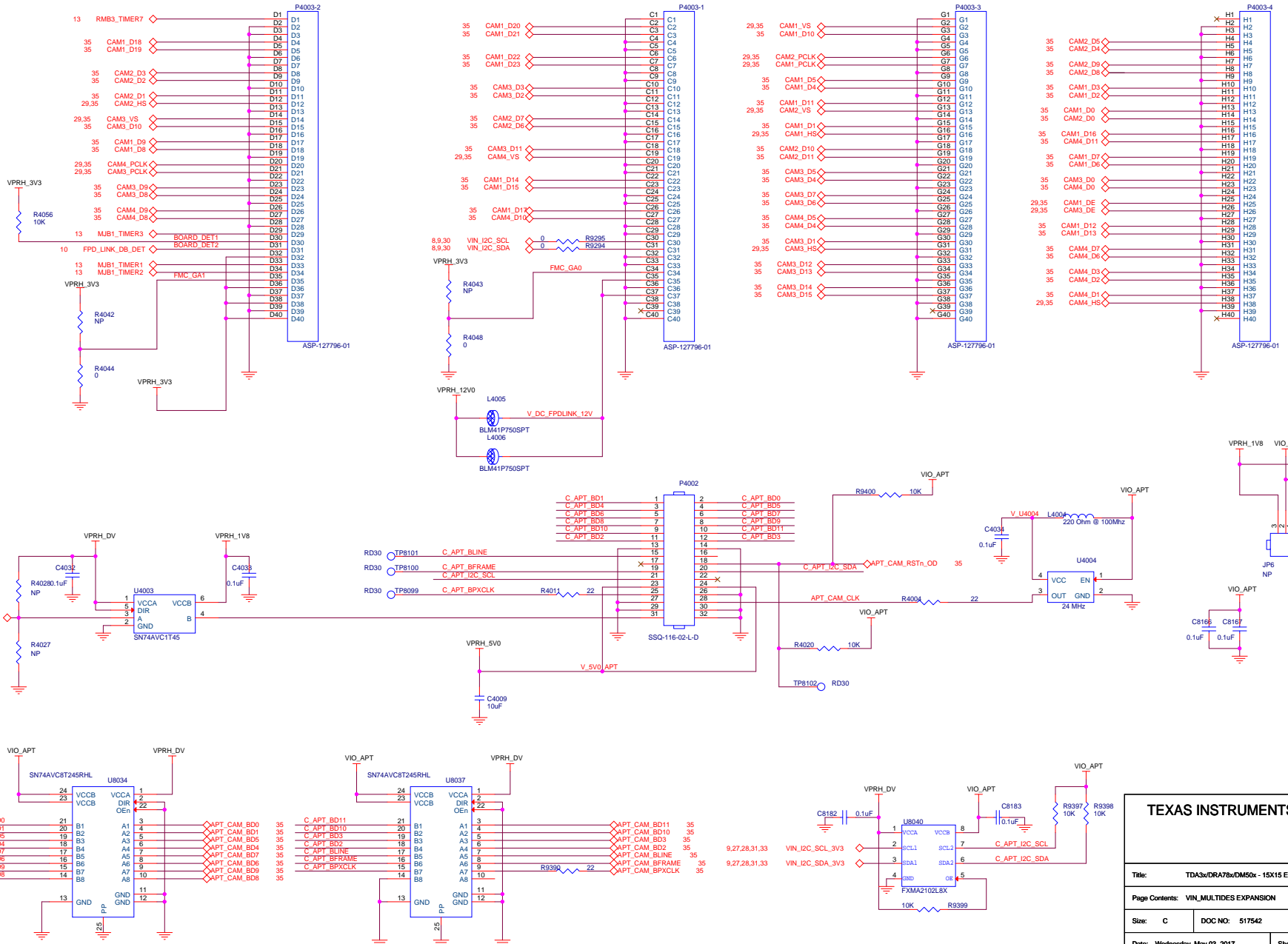


**TEXAS INSTRUMENTS INCORPORATED**

Title: TDA3xDRA76xDMS0x - 15X15 EVM			
Page Contents: VIN CAMERA SENSORS			
Size: C	DOC NO: 517542	REV: C1	
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THE SAMTEC CONNECTOR PINNING IS H-G-D-C BOTTOM VIEW. THE FOLLOWING ARRANGEMENT IS PER THE TI SPECIFICATION. THE PINNING DOES MATCH THE FMC TABLE 2.2 AND 2.3.



**TEXAS INSTRUMENTS INCORPORATED**

Title: TDA3M/DRA760/DMS0x - 15X15 EVM

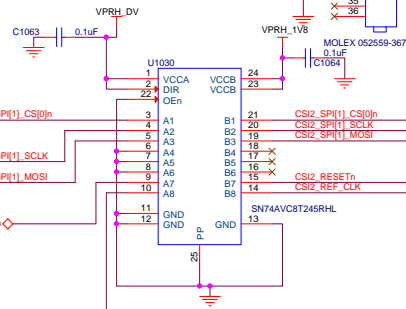
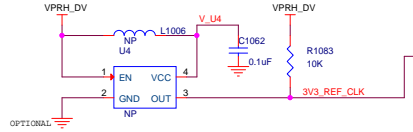
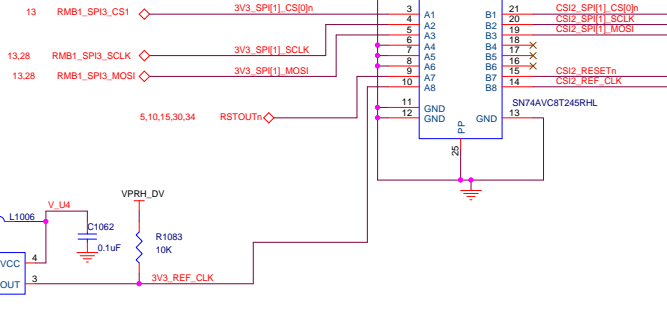
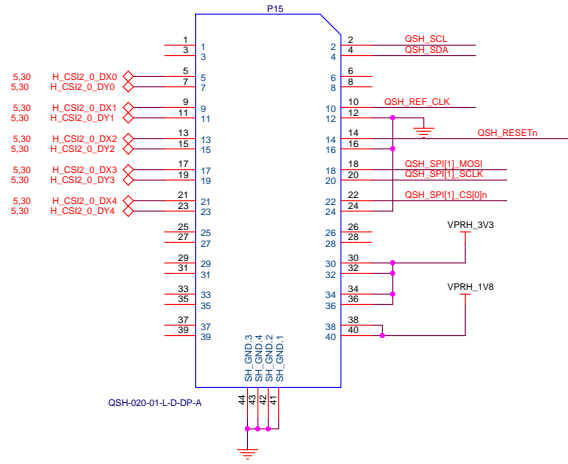
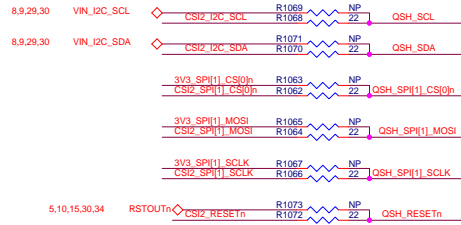
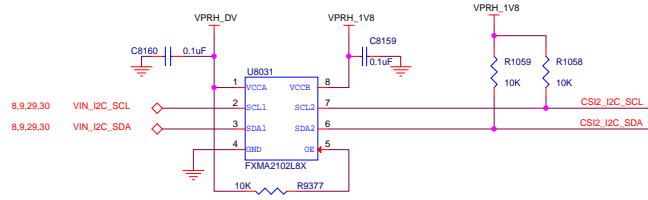
Page Contents: VIN\_MULTIDES EXPANSION

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MHC1  
MHC1  
MHC2  
MHC2



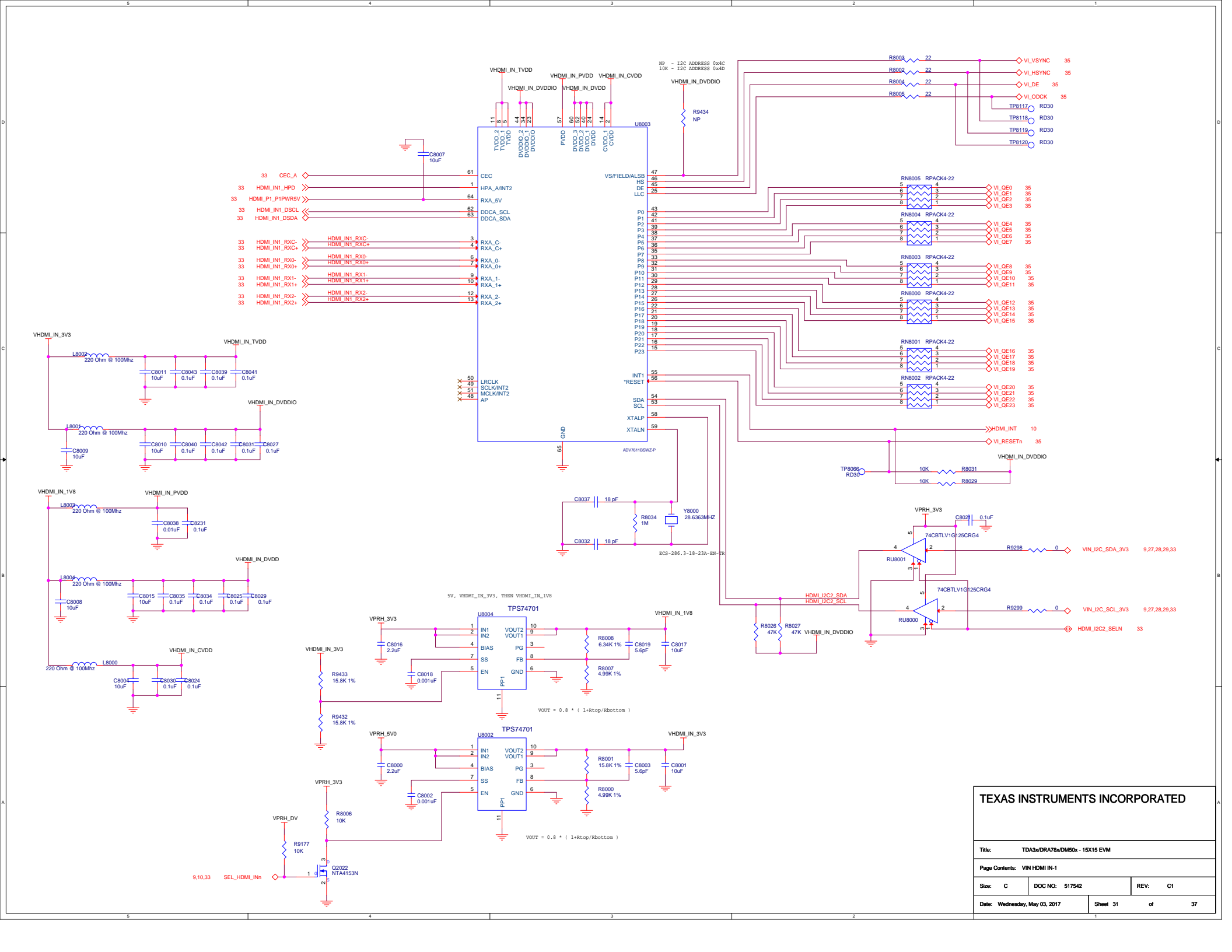
TEXAS INSTRUMENTS INCORPORATED

Title: TDA3x/DRA7x/DM50x - 15X15 EVM

Page Contents: VIN CS12

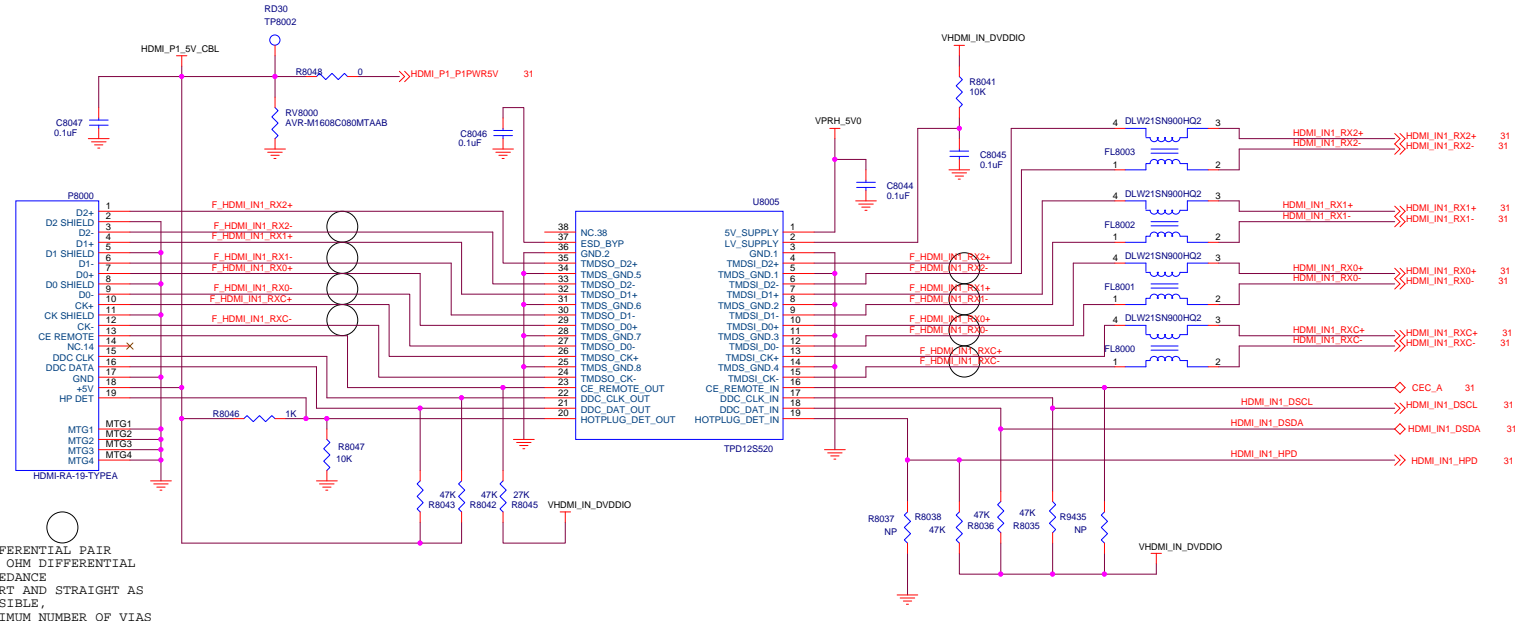
Size: C DOC NO: 517542 REV: C1

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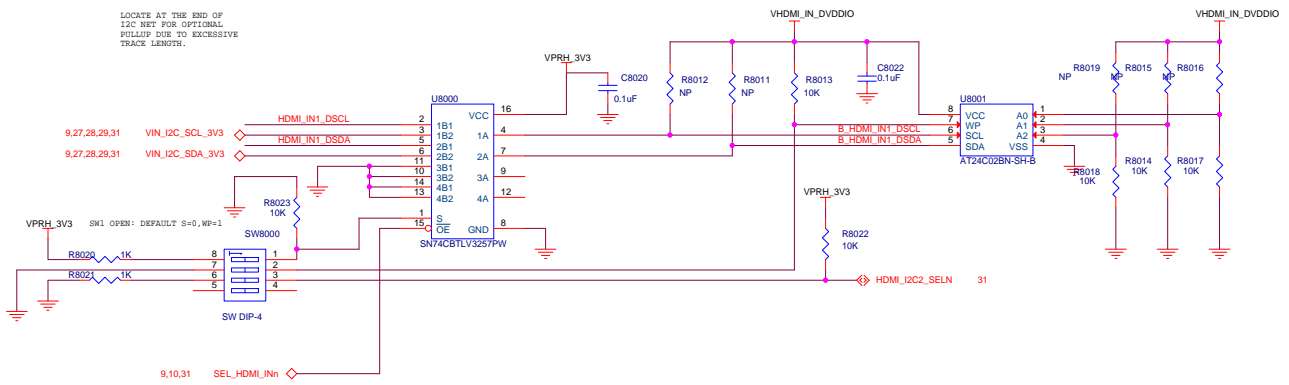
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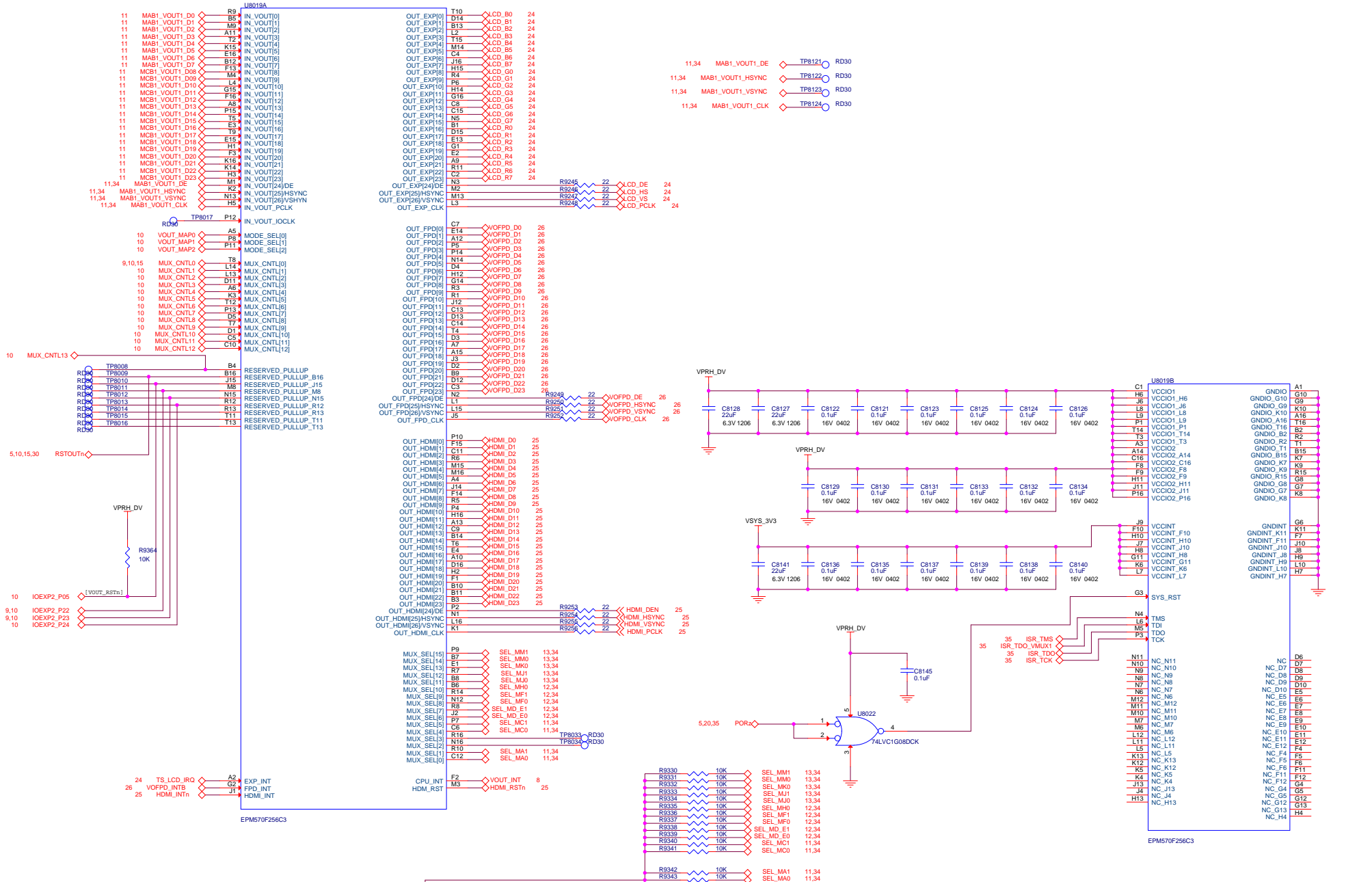
<b>TEXAS INSTRUMENTS INCORPORATED</b>		
Title: TDA3x/DRA76x/DM50x - 15X15 EVM		
Page Contents: VIN HDMI IN-2		
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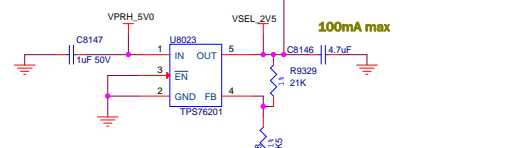
DIFFERENTIAL PAIR  
100 OHM DIFFERENTIAL  
IMPEDANCE  
SHORT AND STRAIGHT AS  
POSSIBLE,  
MINIMUM NUMBER OF VIAS

LOCATE AT THE END OF  
I2C NET FOR OPTIONAL  
PULLUP DUE TO EXCESSIVE  
TRACE LENGTH.





MUX SELECTS OPERATE AS OPEN DRAIN WITH 2.5V PULLUP. THIS SUPPORTS VINMIN WITH VOSYSV AT 1.8V. CPU I/O CAN HANDLE 2.5V WITH 1.8V I/O VOLTAGE.



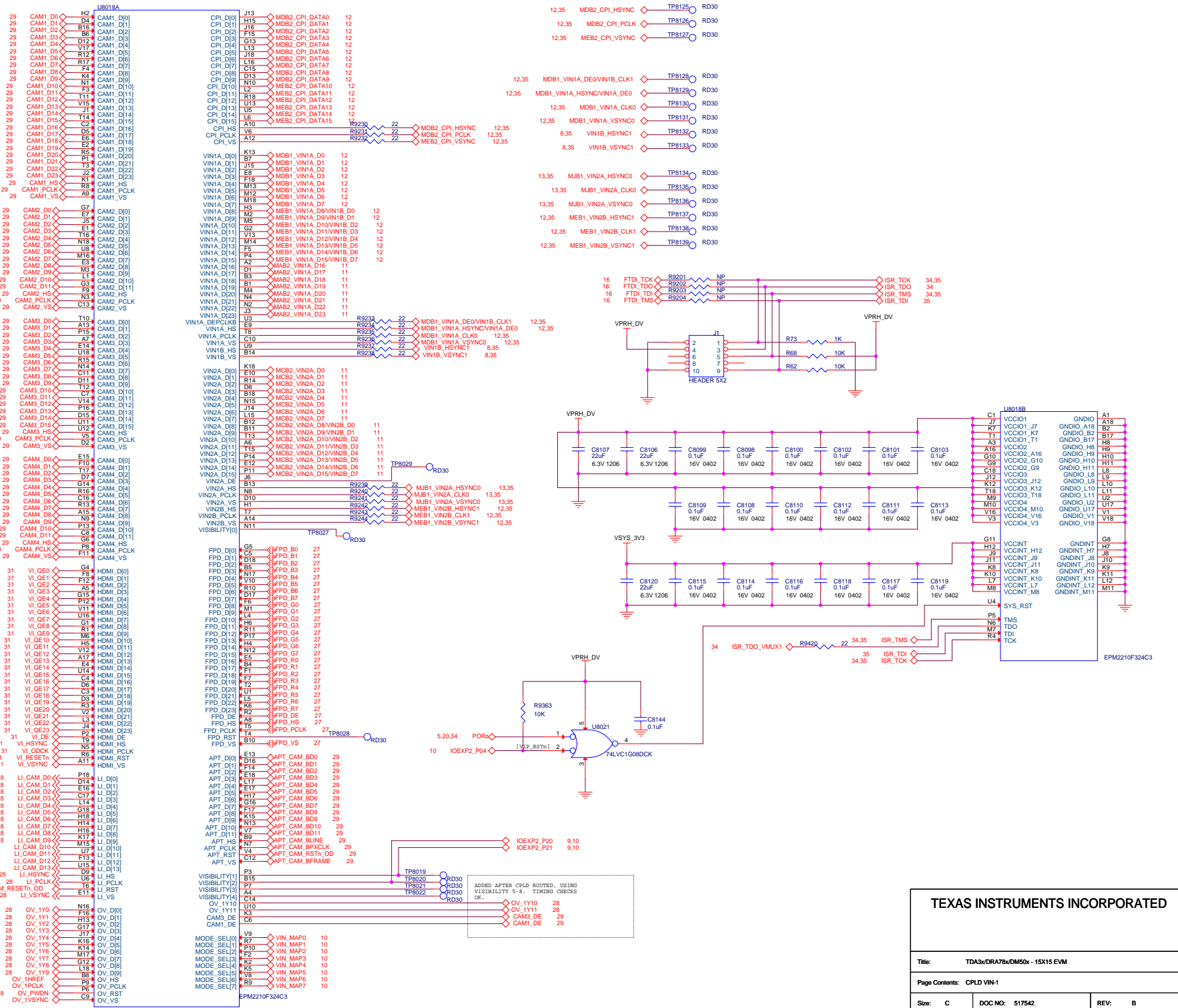
**TEXAS INSTRUMENTS INCORPORATED**

Title: TDA3N/DRA76xDMM50x - 15X15 EVM

Page Contents: CPLD VOUT-1

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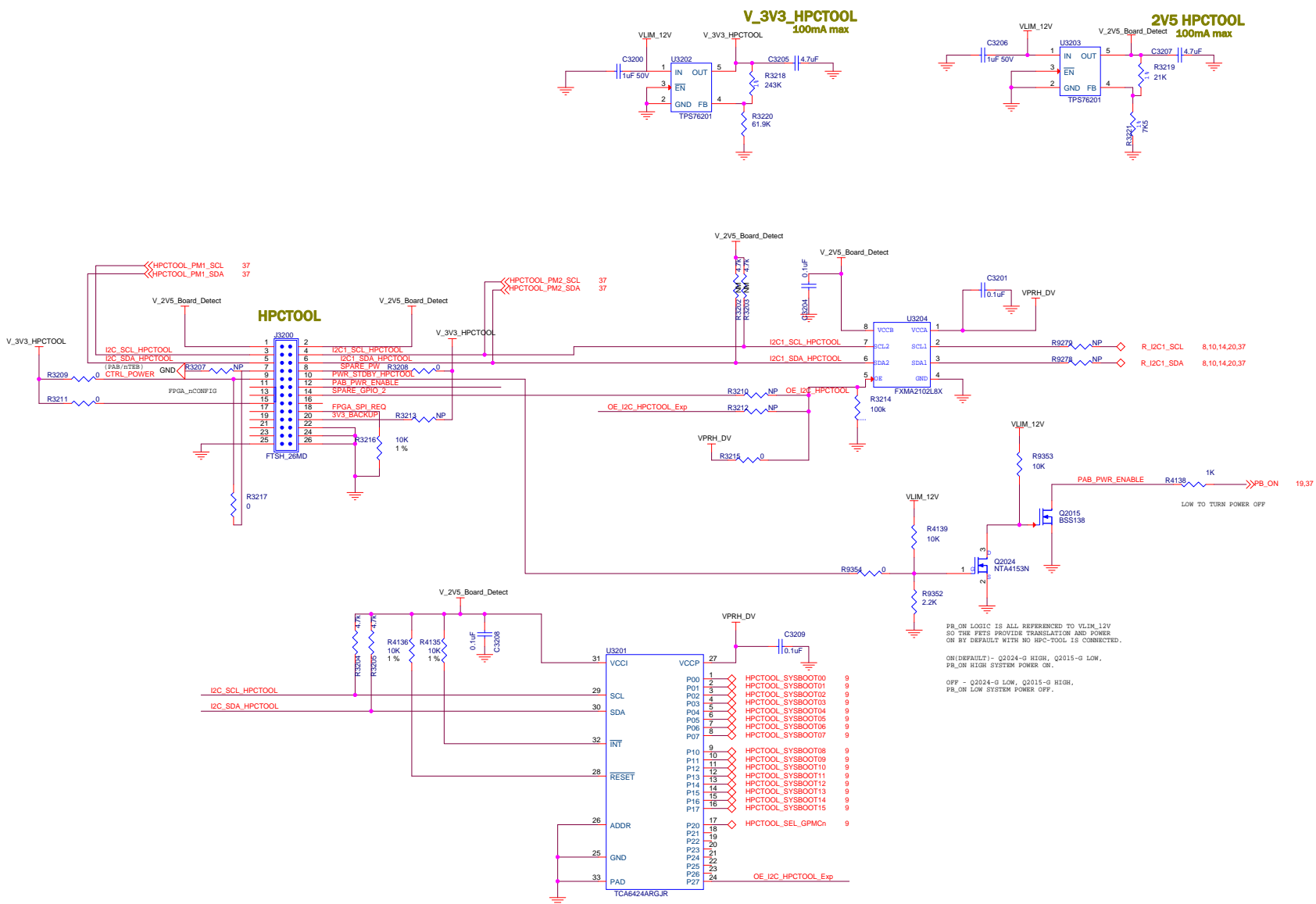


**TEXAS INSTRUMENTS INCORPORATED**

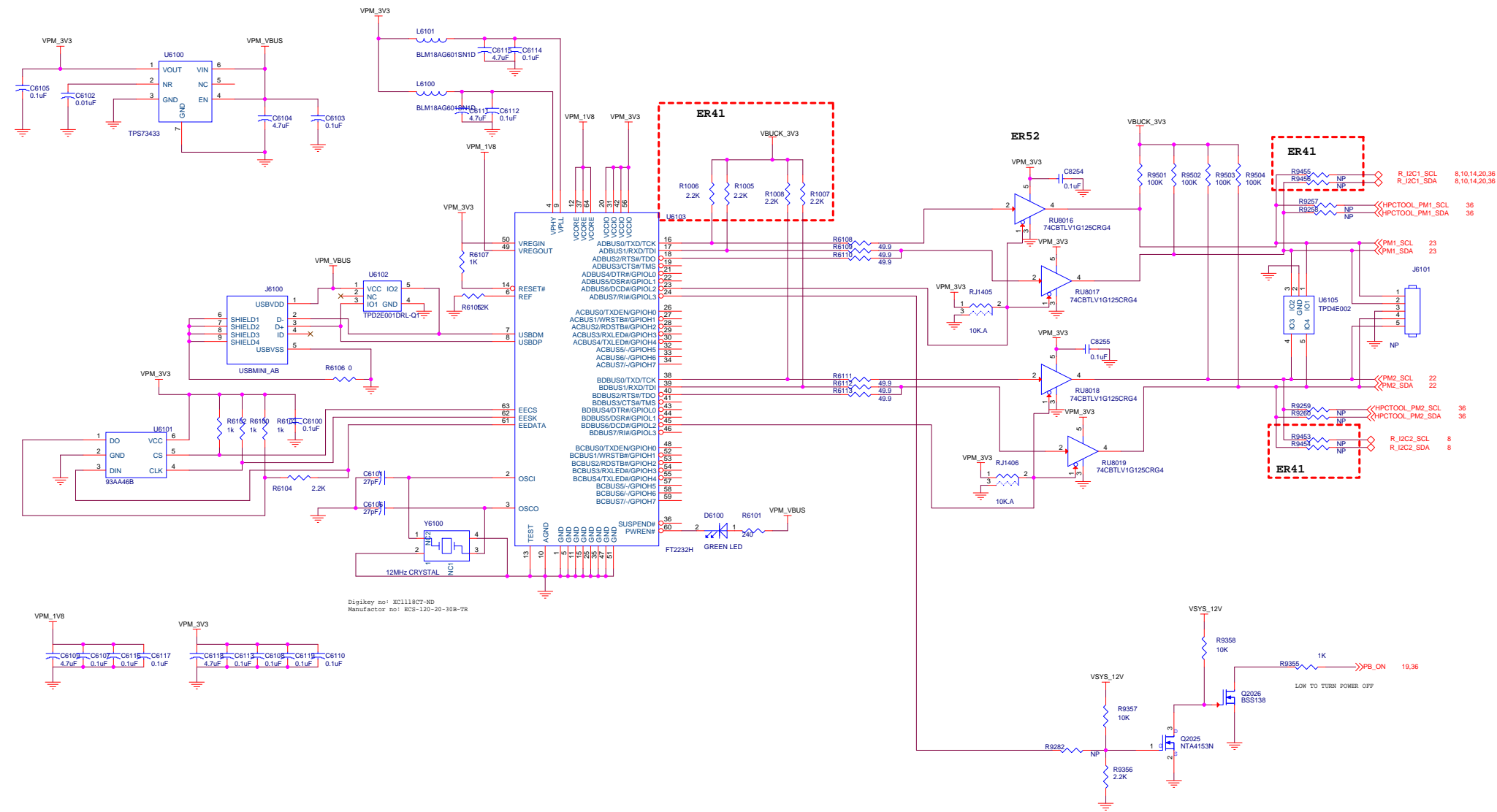
Title: TDA3M07A760DM50x - 15X15 EVM

Page Contents: CPLD VIN-1

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Digikey no: XC1118C7-ND  
 Manufacturer no: ECS-120-20-30B-TR

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