Application Report
SPRACH3–July 2018

TMS320VC5502 to TMS320C5517 Hardware Migration Guide

ABSTRACT

This application report discusses the differences between the Texas Instruments TMS320VC5502 processor and the TMS320C5517 processor.

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Trademarks

1 Introduction

Texas Instruments recommends using the TMS320C5517 Digital Signal Processor (DSP) as an alternative part to replace the TMS320VC5502 DSP. This alternative part that has similar functionality but is not functionally equivalent to the TMS320VC5502 device. While the maximum system clock is changed from 300 MHz to 200 MHz with the TMS320C5517, it offers improvements like substantially more on-chip memory, a hardware-accelerated FFT coprocessor, and an improved C55x core to handle similar workloads. The TMS320C5517 includes many of the same peripherals as the TMS320VC5502 device for backwards compatibility, but also offers newer, faster peripherals for todays needs. Additionally, the newer TMS320C5517 device comes with better support from TI like an improved Chip Support Library with more examples, better Code Composer Studio™ integration, easier to use EVMs with newer components, and better support on the E2E forum.

All of the documentation referenced in this migration guide can be found in the two product folders [1] [2] shown in Section 7. The descriptions of the behavior and functions of the devices are explained only to the extent to illustrate the differences. This document does not cover the silicon exceptions that may be present on the device. For the list of silicon exceptions and the suggested workarounds, consult the device-specific Silicon Errata [5] [6]. All references in this document to VC5502 refer to the TMS320VC5502 device, unless otherwise specified. All references in this document to C5517 refer to the TMS320C5517 device, unless otherwise specified.

2 Basic Feature comparison

Figure 1 and Table 1 show a comparison of the basic features of the VC5502 and the C5517. The remainder of this document presents a comparison of these features in greater detail, and also provides references to the appropriate documentation for further information.

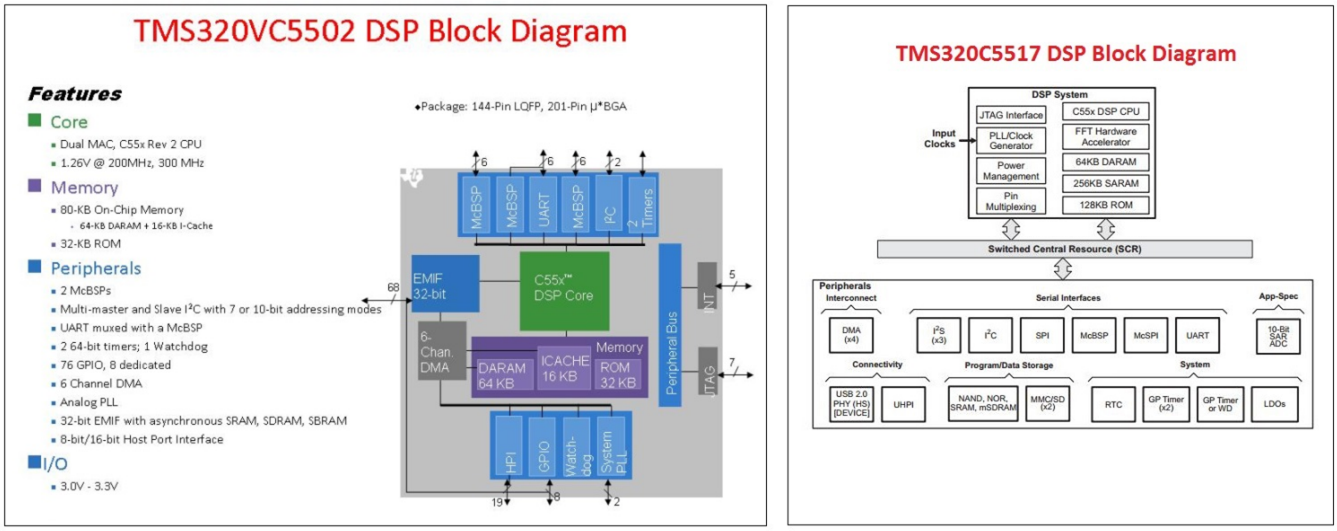

Figure 1. TMS320VC5502 and TMS320C5517 DSP Block Diagrams

Table 1. Basic Feature Comparison

Device	VC5502	C5517
Processor		
Device Family	Fixed-Point TMS320C55x Digital Signal Processor	Fixed-Point TMS320C55x Digital Signal Processor
DSP Core	TMS320C55x DSP up to 300MHz	TMS320C55x DSP up to 200MHz
Silicon Revision	1.0	2.1
CPU Revision	2.2 (refer to C55x_CPU_revision)	3.3 (refer to C55x_CPU_revision)
Operating Frequency	200 MHz, 300 MHz	75 MHz, 175 MHz, 200 MHz
Operating Voltage	Core Voltage: 1.26 V	Core Voltage: 1.05 V, 1.3 V, 1.4 V
FFT Hardware Accelerator	No	Yes – one tightly coupled FFT hardware accelerator that supports 8- to 1024-point (by power of 2) real- and complex-valued FFTs.
Memory		
Internal Memory	64KB Dual Access RAM (support two reads in one cycle) + 16KB Instruction Cache; 32KB ROM	64KB Dual Access RAM (support two reads in one cycle) + 256KB Single Access RAM (zero-wait state); 128KB ROM
DMA Controller	1 (6 channels)	4 DMA controllers each with 4 channels (16 channels)

Table 1. Basic Feature Comparison (continued)

Device	VC5502	C5517
EMIF Controller	Asynchronous Static RAM (SRAM) Asynchronous EPROM Synchronous DRAM (SDRAM) Synchronous Burst RAM (SBRAM)	8-Bit or 16-Bit NAND Flash 1-Bit or 4-Bit ECC 8-Bit and 16-Bit NOR Flash Asynchronous Static RAM (SRAM) SDRAM or Mobile SDRAM (1.8, 2.75, and 3.3 V)
Peripherals		
USB	No	USB 2.0 High- and Full-Speed Device (device mode only)
McBSP	3 – full-duplex, 128 separately enabled channels, supports CLKSTP (SPI master/slave), multiplexed with UART	1
UART	1 - multiplexed with McBSP2	1 - programmable baud rates, even, odd, or no PARITY bit generation and detection
McSPI	0	1 – master and slave, full-duplex, synchronous, serial communication to SPI-compliant external devices (slaves and masters), 128-bytes built-in FIFO
SPI	0	1 – master mode only
I2C	1 - fast mode - upto 400 Kbps, supports seven bit or ten bit addressing mode, master and slave	1 - fast mode - upto 400 Kbps, supports seven bit or ten bit addressing mode, master and slave
I2S	0	3 - full-duplex, I2S and DSP modes, word-lengths of 8, 10, 12, 14, 16, 18, 20, 24, or 32 bits
GPIO	8	26
HPI	8-bit or 16-bit HPU	16-bit UHPI
ADC	No	10-bit 4-Input Successive Approximation (SAR) ADC, one 3.6V tolerant input
MMC/SD/SDIO	No	2 - MMC v3.31, SD Phys Layer v2.0, SDIO v2.0, 4-bit data width
RTC	No	Yes
GP Timer	2	3 32-Bit General-Purpose (GP) Timers, Timer2 shared with Watchdog Timer
Watchdog Timer	1	1, shared with GP Timer 2
JTAG	Yes	Yes
Package		
Package Options	176-Terminal LQFP (Low-Profile Quad Flatpack) (PGF Suffix) 201-Terminal MicroStar BGA (Ball Grid Array) (GZZ and ZZZ Suffixes)	196-Terminal Pb-Free Plastic BGA (Ball Grid Array) (ZCH Suffix), 0.65-mm Pitch

3 Power, Input Clocks, and PLL

3.1 Voltage Rails

Table 2 and Table 3 compare the power supplies for C5502 and C5517.

Table 2. VC5502 Voltage Rails

Supply	Description	Value
CVDD	Device Supply Voltage	1.26 V
DVDD	Device supply voltage, I/O (except DP, DN, PU, SDA, SCL)	3.3 V
PVDD	Device supply voltage, PLL	3.3 V

Table 3. C5517 Voltage Rails

Supply	Description	Value
CVDD	Digital Core supply voltage	1.05 V (75 MHz) 1.3 V (175 MHz) 1.4 V (200 MHz)
DVDDIO	I/O power supply for non-EMIF and non-RTC I/Os	1.8 V, 2.75 V, or 3.3 V
DVDDEMIF	EMIF I/O power supply	1.8 V, 2.75 V, or 3.3 V
LDOI	Analog Pwr Mgmt and LDO Inputs	1.8 V to 3.6 V
CVDDDRTC	RTC digital core and RTC oscillator power supply	1.05 V, 1.3 V, 1.4 V
DVDDRTC	RTC I/O power supply	1.8 V, 2.75 V, or 3.3 V
VDDA_PLL	Analog PLL power supply for the system clock generator	1.3 V
USB_VDDPLL	USB Analog PLL power supply.	3.3 V
USB_VDD1P3	Digital core power supply for USB PHY	1.3 V
USB_VDDA1P3	Analog 1.3V power supply for USB PHY	1.3 V
USB_VDDA3P3	Analog 3.3V power supply for USB PHY	3.3 V
USB_VDDOSC	Power supply for USB oscillator	3.3 V
VDDA_ANA	Supply for power management and 10-bit SAR ADC	1.3 V

3.2 Power Management

The C5502 does not have power management built in to the device.

The C5517 supports power management and has the following features:

- PLL Power Down
- Peripheral Clock Idling
- Core Voltage Scaling
- RTC-only mode (CORE Voltage off)
- DARAM/SARAM Low Power Modes
- Independent Power Domains
- I/O Voltage Selection
- USB Power Down
- RTC Power Down

3.3 Input Clocks

The following tables compare the input clocks for C5502 and C5517.

Table 4. VC5502 Input Clocks

Clock Name	Source	Value
X2/CLKIN	Master Oscillator	5 to 20 MHz

Table 5. C5517 Input Clocks

Clock Name	Source	Value
CLKIN	Input clock System clock generator input when CLK_SEL pin = 1	11.2896, 12.0, 12.288, 16.8, or 19.2 MHz
USB_MXI	12-MHz on-chip USB oscillator System clock generator input when CLK_SEL pin = 0	12 MHz
RTC_XI	Real-time clock oscillator input. (RTC clock only)	32.768 kHz

3.4 PLLs

Both C5502 and C5517 have the following PLLs, driven by an input crystal (X2/CLKIN):

- VC5502

  The GPIO4 pin determines the source of the input clock for the PLL. If GPIO4 is low at reset, the internal oscillator and the external crystal will generate an input clock (OSCOUT) for the DSP. If GPIO4 is high, the CLKMD0 bit will be set to '1' and the input clock will be taken directly from the X2/CLKIN pin.

- C5517

  The CLK_SEL pin determines whether the input clock to the PLL comes from the USB oscillator (CLK_SEL = 0) or the CLKIN pin (CLK_SEL = 1).

4 Boot Modes

Table 6 compares the support for various boot modes on the VC5502 and C5517.

Table 6. Comparison of Boot Modes on the VC5502 and C5517

C5502	C5517	Boot Type	Description
N	Y	NOR	This mode allows booting from NOR flash memories. The C5502 does not support NOR flash boot. For C5517, 16-bit NOR flash boots from all asynchronous CS spaces, system clock generator is in bypass mode.
N	Y	NAND	This mode starts downloading code from an NAND memory. The C5502 does not support NAND flash boot. For C5517, 16-bit or 8-bit NAND flash data boot, system clock generator is in bypass mode.
Y	N	Asynchronous Memory	This mode starts downloading code from an asynchronous memory. The C5502 supports external asynchronous memory boot (via the EMIF) from 16-bit-wide memory. The C5517 does not support this boot mode.
Y	N	Direct Execution-Asynchronous Memory	This mode executes code directly from an asynchronous memory The C5502 supports direct execution (no boot) from external asynchronous memory (via the EMIF) - 32-bit-wide or 16-bit-wide memory. The C5517 does not support this boot mode.
Y	N	Serial Port Boot (from McBSP)	This mode starts booting from the McBSP serial port The C5502 supports serial port boot from the McBSP0 serial port with 16-bit element length. The C5517 does not support this boot mode.
Y	Y	SPI	This mode starts downloading code from an SPI EEPROM or SPI Flash. For C5502, Serial (SPI) EPROM Boot (24-bit/16-bit address) via McBSP0. For C5517, SPI 16-bit or 24-bit address Boot (SPI_CLK < 1 MHz or 10 MHz), system clock generator output = input clock x 3.
N	Y	McSPI	This mode starts downloading code from EEPROM/ Serial Flash through McSPI. The C5502 does not support McSPI boot. For C5517, McSPI 24-bit address serial flash at 10 MHz or 40 MHz mode.
Y	Y	I2C	This mode starts downloading code from an I2C EEPROM. For C5502, I2C EEPROM (7-bit address). For C5517, I2C 16-bit address Boot, 400 kHz, system clock generator is in bypass mode.
Y	Y	UART	In this mode, the UART sends a BOOTME request to the UART peripheral and waits for a response along with code from a host processor. For C5502, standard UART boot. For C5517, UART 9600, 57600, 115200 baud boot, system clock generator output = input clock x 3.

Table 6. Comparison of Boot Modes on the VC5502 and C5517 (continued)

C5502	C5517	Boot Type	Description
N	Y	MMC/SD	This mode starts booting code from an MMC/SD Controller. The C5502 does not support MMC/SD boot. For C5517, SD or SDHC, MMC, or eMMC Controller 0/1 card boot, system clock generator is in bypass mode.
Y	Y	HPI	This mode starts booting code from the HPI. The C5502 supports HPI boot (multiplexed and non-multiplexed) For C5517, UHPI 16-bit multiplexed mode boot, system clock generator output = input clock x 3.
N	Y	USB	This mode starts booting code from the USB device. The C5502 does not support USB boot. For C5517, USB boot, system clock generator output = input clock x 3.

The C5502 device supports the following boot modes:

- Host-port interface (HPI) boot, both in multiplexed and non-multiplexed modes
- External memory boot (via EMIF) from 16-bit asynchronous memory
- Serial port boot (from McBSP0) with 16-bit element length
- SPI EPROM boot (from McBSP0) supporting EPROMs with 24-bit addresses
- I2C EPROM boot (from I2C) supporting EPROMs larger than 512K bits
- UART boot
- Direct execution (no boot) from 16- or 32-bit external asynchronous memory

The C5517 device supports the following boot modes:

- 16-bit NOR flash data boot, system clock generator is in bypass mode.
- 16-bit or 8-bit NAND flash data boot, system clock generator is in bypass mode.
- UART 9600 baud boot, system clock generator output = input clock x 3
- UART 57600 baud boot, system clock generator output = input clock x 3
- UART 115200 baud boot, system clock generator output = input clock x 3
- SPI 16-bit or 24-bit address Boot (SPI_CLK < 1 MHz), system clock generator output = input clock x 3
- SPI 16-bit or 24-bit address Boot (SPI_CLK < 10 MHz), sD or SDHC, MMC, or eMMC Controller 0 card boot, system clock generator is in bypass modeystem clock generator output = input clock x 3
- Polling Mode: Check for valid boot image from peripherals in the following order: NOR, NAND, SPI, I2C, SD/SDHC/MMC/eMMC Controller 0, McSPI, and UART/USB (infinite retry).
- I2C 16-bit address Boot, 400 kHz, system clock generator is in bypass mode.
- SSD or SDHC, MMC, or eMMC Controller 1 card boot, system clock generator is in bypass mode
- Polling Mode: Check for valid boot image from peripherals in the following order: NOR, NAND, SPI, I2C, SD/SDHC/MMC/eMMC Controller 0, SD/SDHC/MMC/eMMC Controller 1, and UART/USB (infinite retry).(2)
- UHPI 16-bit multiplexed mode boot, system clock generator output = input clock x 3
- McSPI 24-bit address serial flash at 10-MHz mode
- McSPI 24-bit address serial flash at 40-MHz mode
- USB boot, system clock generator output = input clock x 3

5 Pin Multiplexing

5.1 VC5502

The GPIO6 and GPIO7 pins are latched upon the release of reset to configure the pin multiplexing of the VC5502 device. Once set at reset, the pin multiplexing cannot be modified.

The GPIO6 pin is used to select the function of the multiplexed signals in the Parallel Port and the Host Port. The EMIF will be disabled and the HPI will operate in non-multiplexed mode when the GPIO6pin is low during reset. The EMIF will be enabled and the HPI will operate in multiplexed mode when the GPIO6 pin is high during reset.

The GPIO7 pin is used to select the function of the multiplexed signals of Serial Port 2. The UART will be enabled and McBSP2 will be disabled when GPIO7 is low during reset. McBSP2 will be enabled and the UART will be disabled when GPIO7 is high during reset.

5.2 C5517

The C5517 pin multiplexing configuration is controlled by software with the EBSR Register.

The EBSR Parallel Port Mode (PPMODE) control bits control the pin multiplexing of the UHPI, SPI, UART, I2S2, I2S3, and GP[31:27, 20:12] pins on the parallel port. Allowable combinations of these peripherals are listed below:

- Mode 0 (16-bit UHPI bus). All 28 signals of the UHPI bus module are routed to the 28 external signals of the parallel port. Note: SDRAM control signals are multiplexed with UHPI bus control signals. In this mode, UHPI bus signals are routed to the control ports, so SDRAM cannot be accessible.
- Mode 1 (SPI, GPIO, UART, I2S2, and SDRAM). 7 signals of the SPI module, 6 GPIO signals, 4 signals of the UART module, 4 signals of the I2S2 module, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port.
- Mode 2 (GPIO and SDRAM). 8 GPIO and 7 SDRAM control signals are routed to the 28 external signals of the parallel port.
- Mode 3 (SPI, I2S3, and SDRAM). 4 signals of the SPI module, 4 signals of the I2S3 module, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port.
- Mode 4 (I2S2, UART, and SDRAM). 4 signals of the I2S2 module, 4 signals of the UART module, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port.
- Mode 5 (SPI, UART, and SDRAM). 4 signals of the SPI module, 4 signals of the UART module, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port.
- Mode 6 (SPI, I2S2, I2S3, GPIO, and SDRAM). 7 signals of the SPI module, 4 signals of the I2S2 module, 4 signals of the I2S3 module, 6 GPIO, and 7 SDRAM control signals are routed to the 28 external signals of the parallel port.

The two serial port pin mux configurations are controlled by the EBSR Serial Port 1 Mode (SP1MODE) Control Bits and the Serial Port 0 Mode (SP0MODE) Control Bits. Pin multiplexing options for each serial port are listed below.

- Serial Port 1 Mode Control Bits control the pin multiplexing of the MMC/SD1, McSPI, and GPIO signals:
  - Mode 0 (MMC1 and SD1). All 6 signals of the MMC1 and SD1 module are routed to the 6 external signals of the serial port 1.
  - Mode 1 (McSPI). 6 signals of the McSPI module signals are routed to the 6 external signals of the serial port 1.
  - Mode 2 (GP[11:6]). 6 GPIO signals (GP[11:6]) are routed to the 6 external signals of the serial port 1.

- Serial Port 0 Mode Control Bits control the pin multiplexing of the MMC/SD0, I2S0, McBSP, and GPIO signals
  - Mode 0 (MMC0 and SD0). All 6 signals of the MMC0 and SD0 module are routed to the 6 external signals of the serial port 0.
  - Mode 1 (I2S0 and GP[5:4]). 4 signals of the I2S0 module and 2 GP[5:4] signals are routed to the 6 external signals of the serial port 0.
  - Mode 2 (GP[5:0]). 6 GPIO signals (GP[5:0]) are routed to the 6 external signals of the serial port 0.
  - Mode 3 (McBSP). 6 signals of the McBSP module are routed to the 6 external signal port 0.

6 Compiler Options

The CC55x Gode Gen Tools require the following compiler target options in order to build object code compatible with the respective CPU revision.

6.1 C5502

- Silicon Revision: 1.0
- CPU Revision: 2.2
- Available Equivalent Compiler Target Options:
  - vcore:2.2
  - vcpu:2.2
  - v5502
  - v5502:1.0

6.2 C5517

- Silicon Revision: 2.1
- CPU Revision: 3.3
- Available Equivalent Compiler Target Options:
  - vcore:3.3
  - vcpu:3.3
  - v5515
  - v5515:1.0

7 References

1. VC5502 Product Page
2. C5517 Product Page
3. *TMS320VC5502 Fixed-Point Digital Signal Processor Data Manual*
4. *TMS320C5517 Fixed-Point Digital Signal Processor*
5. *TMS320VC5502 and TMS320VC5501 Digital Signal Processors Silicon Errata*
6. *TMS320C5517 Fixed-Point Digital Signal Processor Silicon Revision 1.0, 2.0, and 2.1 Silicon Errata*

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