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ABSTRACT

As C2000™ devices have advanced in terms of available peripherals, larger memories, pin count and other options, the startup boot code has also been enhanced along with it. When it comes to the boot options available on a device, they always have to be designed to balance flexibility in terms of customization as well as the ease of use by the developer. From C2000 device-to-device, these new features and options are not always clearly highlighted in comparison to older devices. Any new boot features are developed with an intended purpose in mind that may not be clear when coming from an older device. This application report includes details beyond what boot code does but actually how these features have been enhanced device-to-device and how to best take advantage of them in an application.

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1 Introduction

With devices growing in available memory, peripherals, and pin options, the need to enhance and allow further boot configurations is critical to developers. The boot mode options provided on the device drives the development strategy used to guarantee the device has the flexibility needed for all stages of development. Although code could be placed in flash to run custom kernels, this uses valuable flash memory space and adds additional delay before running the main application. C2000 devices over the years have strived toward a more configurable, less demanding boot flow by reducing the number of boot mode selection pins from 4 to 2 as well as adding some additional peripheral bootloader general-purpose input/output (GPIO) pin mux options. This application report is here to not only detail how these customizable options have changed on various C2000 devices, but also explain how the new boot options on F28004x device onwards lead to a much more customizable, flexible device. The following sections will cover several aspects of boot customizations now possible. One being the customization of how many boot mode select pins are allocated on the device, which allows for such scenarios where 0 boot mode select pins are used, if desired. Additionally, the boot mode select pin GPIOs are configurable and it is possible to create a fully user defined default boot mode selection table using a greater defined set of available boot modes.

For more details regarding boot up flow and the referenced configurable boot memory locations, see the device-specific reference guides and technical reference manuals (TRM):

- [TMS320x2833x, 2823x Boot ROM Reference Guide](#)
- [TMS320x2802x Piccolo Boot ROM Reference Guide](#)
- [TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual](#)
- [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#)
- [TMS320F2807x Piccolo Microcontrollers Technical Reference Manual](#)
- [TMS320F28004x Piccolo Microcontrollers Technical Reference Manual](#)
- [TMS320F2838x Real-Time Microcontrollers With Connectivity Manager TRM](#)
- [TMS320F28002x Real-Time Microcontrollers Technical Reference Manual](#)
- [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#)

2 Features and Configurations

The complexity and flexibility of C2000 boot configurations have scaled as devices evolved. The latest enhanced features and options for specific boot configurations starting on F28004x devices now bring C2000 to a whole new level of customization and flexibility. The following sections highlight and describe these new options. Additionally, a comparison is provided to show how such customizations were handled on past C2000 devices.

2.1 Selecting Boot Mode Select Pins (BMSP) and GPIOs

All the latest C2000 devices use a defined set of GPIOs to allow for boot mode selection upon device power-on or reset. This is accomplished by the boot code decoding the state, whether pulled high or low, of the GPIOs. Once decoded, the interpreted value is used as an index to select which boot mode from the boot mode selection table should be run. The GPIOs used as boot mode select pins have typically been locked to their default GPIO. Starting with the Delfino F2837xD devices and carried over to future devices, the GPIOs used as boot mode select pins are now configurable. On F28004x onwards, writing to the BOOTPIN_CONFIG memory location in user-configurable dual code security module (DCSM) OTP allows for all three of the possible boot mode select pins to be set to almost any GPIO available on the device. Devices are no longer locked to the factory default GPIOs, which allows for a greater flexibility in terms of pin usage.

C2000 devices have not only required a certain set of GPIOs to use as boot mode select pins, but a specified number of pins themselves. The number of boot mode select pins used either expands or restricts the available boot modes selectable in the boot table. If there are four boot mode select pins used, there can be up to 16 boot options selectable, but if only two boot mode select pins are used then only four boot options are selectable. On F28004x device onwards, the factory default setting is two boot mode select pins but the number of pins can be customized to support as many as three pins and as few as 0 pins. Using options such as 0 boot mode select pins, provides only a single boot mode to be selected but also frees up the other pins to be repurposed. If many boot modes are required for various scenarios, then using three pins will allow for selecting between eight possible boot choices. Disabling any particular boot mode selection pin uses the same BOOTPIN_CONFIG memory location as when changing the GPIO number used except now a value of "0xFF" is written to disable that specified pin.

Table 2-1. Boot Pin GPIO Selection Comparison

Device	Boot Pin GPIO Custom Selection	Number of Boot Pins	Factory Default Boot Pins
F2833x	Number of boot mode select pins (BMSP) and GPIOs assigned are fixed	4	BMSP3: GPIO87 BMSP2: GPIO86 BMSP1: GPIO85 BMSP0: GPIO84
F2802x		2	BMSP1: GPIO37 BMSP0: GPIO34
F2806x		2	BMSP1: GPIO37 BMSP0: GPIO34
F2837xD/F2837xS/F2807x	Number of BMSPs fixed at 2 and GPIOs assigned are customizable. It is also possible to assign same GPIO to both BMSP thus allowing a single pin use case	2	BMSP1: GPIO72 BMSP0: GPIO84
F28004x	Number of BMSPs and GPIOs assigned are customizable	0,1,2 or 3	BMSP1: GPIO24 BMSP0: GPIO32
F2838xD/F2838xS			BMSP1: GPIO72 BMSP0: GPIO84
F28002x			BMSP1: GPIO24 BMSP0: GPIO32
F28003x			BMSP1: GPIO24 BMSP0: GPIO32

2.2 Customizing the Boot Selection Table

Each C2000 device has a factory set default boot selection table that contains boot mode options available on an unprogrammed device. The default number of boot mode selection pins determines how many options are available in the default table. The latest devices use two boot mode selection pins and hence have four default boot modes selectable in [Table 2-2](#).

Table 2-2. Default Boot Options Table Comparison

Device	Default Boot Table Options (unprogrammed device)	All Available Boot Modes	Comments
F2833x	<ul style="list-style-type: none"> 0. SCI boot (No ADC calibration) 1. RAM boot (No ADC calibration) 2. Flash boot (No ADC calibration) 3. Check boot (loop) mode 4. RAM boot 5. Parallel XINTF boot 6. Parallel boot 7. OTP boot 8. XINTF x32 boot 9. XINTF x16 boot 10. McBSP boot 11. CAN boot 12. I2C boot 13. SPI boot 14. SCI boot 15. Flash boot 	All available boot modes are same as in default boot table	All boot modes accessed through BMSP
F2802x	<ul style="list-style-type: none"> 0. Parallel boot 1. SCI boot 2. Wait boot 3. Get boot/flash 	<ul style="list-style-type: none"> Parallel boot SCI boot Wait boot Get boot SPI boot I2C boot OTP boot Flash boot RAM boot 	Boot modes other than those in default table can be accessed either through emulation boot mode or standalone boot mode. In standalone mode get boot mode is first selected using BMSP and get boot reads the boot mode selection programmed in OTP
F2806x	<ul style="list-style-type: none"> 0. Parallel boot 1. SCI boot 2. Wait boot 3. Get boot/flash 	<ul style="list-style-type: none"> Parallel boot SCI boot Wait boot Get boot SPI boot I2C boot OTP boot CAN boot Flash boot RAM boot 	Boot modes other than those in default table can be accessed either through emulation boot mode or standalone boot mode. In standalone mode get boot mode is first selected using BMSP and get boot reads the boot mode selection programmed in OTP

Table 2-2. Default Boot Options Table Comparison (continued)

Device	Default Boot Table Options (unprogrammed device)	All Available Boot Modes	Comments
F2837xD/F2837xS/ F2807x	<ul style="list-style-type: none"> 0. Parallel boot 1. SCI boot 2. Wait boot 3. Get boot/flash 	<ul style="list-style-type: none"> Parallel boot SCI boot Wait boot Get boot SPI boot I2C boot CAN boot Flash boot RAM boot USB boot 	<p>Boot modes other than those in default table can be accessed either through emulation boot mode or standalone boot mode. In standalone mode get boot mode is first selected using BMSP and get boot reads the boot mode selection programmed in OTP. For dual core devices all boot modes are available on both CPU1 and CPU2 except USB boot which is available only on CPU1</p>
F28004x	<ul style="list-style-type: none"> 0. Parallel boot 1. SCI/wait boot 2. CAN boot 3. Flash boot 	<ul style="list-style-type: none"> Parallel boot SCI/wait boot Wait boot SPI boot I2C boot CAN boot Flash boot RAM boot 	<p>Boot modes other than those in default table can be accessed either through emulation boot mode or standalone boot mode. In standalone mode a custom boot mode table has to be programmed in OTP</p>
F2838xD/F2838xS	<ul style="list-style-type: none"> 0. Parallel boot 1. SCI/wait boot 2. CAN boot 3. Flash/USB boot 	<ul style="list-style-type: none"> Parallel boot SCI/wait boot Wait boot SPI boot I2C boot OTP boot CAN boot Flash boot RAM boot USB boot Secure flash boot IPC message copy to RAM 	<p>Boot modes other than those in default table can be accessed either through emulation boot mode or standalone boot mode. In standalone mode a custom boot mode table has to be programmed in OTP. For dual core devices C28x CPU2 and CM core are booted through IPC boot command from C28x CPU1. CPU2 and CM core only support flash, wait, RAM, secure flash, user OTP and IPC message copy boot modes. CPU1 does not support User OTP and IPC message copy boot modes</p>
F28002x	<ul style="list-style-type: none"> 0. Parallel boot 1. SCI/wait boot 2. CAN boot 3. Flash boot 	<ul style="list-style-type: none"> Parallel boot SCI/wait boot Wait boot SPI boot I2C boot CAN boot Flash boot RAM boot 	<p>Boot modes other than those in default table can be accessed either through emulation boot mode or standalone boot mode. In standalone mode a custom boot mode table has to be programmed in OTP</p>

Table 2-2. Default Boot Options Table Comparison (continued)

Device	Default Boot Table Options (unprogrammed device)	All Available Boot Modes	Comments
F28003x	0. Parallel boot 1. SCI/wait boot 2. CAN boot 3. Flash boot	Parallel boot SCI/wait boot Wait boot SPI boot I2C boot CAN boot Flash boot RAM boot Secure flash boot Live firmware update (LFU) flash boot Secure LFU flash boot	Boot modes other than those in default table can be accessed either through emulation boot mode or standalone boot mode. In standalone mode a custom boot mode table has to be programmed in OTP

Previous to F28004x devices, the 4th boot mode entry in the default boot table was get boot mode. The get boot mode read a programmable OTP value which decided the boot mode selected. After F28004x, when programmed, the whole boot mode selection table is customizable. Depending on the number of boot mode selection pins (0, 1, 2 or 3) enabled on the device, the custom boot selection table can have 1, 2, 4, or 8 boot mode options available. This custom table replaces the default factory table, so instead of parallel boot, for example, tied to boot option 0, this can now be set to any boot mode such as flash or CAN boot. This table is setup by configuring the 64-bit BOOTDEF memory location in user-configurable DCSM OTP. Each byte represents a specified boot mode.

Table 2-3. Boot Selection Table Comparison

Device	Boot table customization
F2833x	Not customizable, the table is locked to the factory default.
F2802x	Semi-customizable, the 4th entry in the boot table (Get mode) can be programmed to a specific boot mode using OTP memory
F2806x	
F2837xD/F2837xS/F2807x	
F28004x	Fully customizable, all boot options in the boot table can be programmed to any boot mode using OTP memory
F2838xD/F2838xS	
F28002x	
F28003x	

2.3 Using Expanded Boot Options

The memory address to branch upon booting on selecting flash boot mode or GPIOs used as part of a peripheral bootloader are predefined in ROM. This places constraints on hardware design while selecting pin functions if any specific pins are already used for peripheral bootloaders. Beginning with F2837xD devices, some additional peripheral GPIO mux options were provided to add more flexibility to the GPIOs used as part of the application. F28004x onwards, more of these expanded boot options have been added versus any other previous device. This includes multiple entry address options when booting to flash and multiple GPIO mux combinations for bootloader peripherals such as SCI, CAN, SPI, parallel and I2C. Using the expanded boot options is no different than setting any other boot mode in the custom table. First find the boot mode option with the associated value in the GPIO assignments section of the TRM and then set it in the 64-bit BOOTDEF memory location in user-configurable DCSM OTP.

Table 2-4. Expanded Boot Mode Options Comparison

Device	Peripheral bootloader GPIO options	Flash entry point options
F2833x	Single factory default pinout for peripheral bootloaders	Single flash entry point
F2802x		
F2806x		
F2837xD/F2837xS/F2807x	Two pinout options for most of peripheral bootloaders. Each pinout option has its own boot mode identifier and can be selected through get boot mode	
F28004x	Multiple pinout options for most of peripheral bootloaders. Each pinout option has its own boot mode identifier and can be programmed into custom boot table	Multiple flash entry point options
F2838xD/F2838xS		
F28002x		
F28003x		

3 Recommended Boot Configurations

With the latest boot enhancements on F28004x onwards, the customizations now available allow for some specific boot scenarios to be setup. These range from using no boot mode select pins to using all 3 pins.

Table 3-1. Recommended Example Boot Configurations

Scenario	Number of Pins Used	Boot Mode Table Options
Zero boot pins	0	0. Flash Boot
Firmware upgrade	1	0. Flash Boot 1. SCI/Any bootloader
Multi-function/flexible Device	3	0. Flash Boot
		1. Flash Boot (alternate address)
		2. Flash Boot (alternate address)
		3. Flash Boot (alternate address)
		4. SCI/Any bootloader
		5. CAN/Any bootloader
		6. I2C/Any bootloader
7. SCI Alternative/Any bootloader		

4 How to Configure Boot Options

For more details on how to configure these custom boot options, see *Device boot modes* section of *ROM Code and Peripheral Booting* chapter of the device-specific TRMs.

For an example on how to configure boot pins, a custom boot table, and use expanded boot options, see the *boot_ex2_customBootConfig* project under F28004x in [C2000Ware](#).

5 References

- [TMS320x2833x, 2823x Boot ROM Reference Guide](#)
- [TMS320x2802x Piccolo Boot ROM Reference Guide](#)
- [TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual](#)
- [TMS320F2837xS Delfino Microcontrollers Technical Reference Manual](#)
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- [TMS320F28002x Real-Time Microcontrollers Technical Reference Manual](#)
- [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#)

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2017) to Revision A (March 2022)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document.....	2
• Document updated with information on F2838xD/F2838xS, F28002x and F28003x devices.....	2
• Changed the title of the document.....	2
• Updated Section 2.1	2
• Updated Section 2.2	4
• Updated Section 2.3	6
• Updated Section 5	7

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