Application Report
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# 66AK2G0x General-Purpose EVM Power Distribution Network Analysis

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**ABSTRACT**

The purpose of this application report is to present the flow, the environment settings and methodology used for a performance analysis of critical power nets of a platform using the 66AK2G0x System-on-Chip (SoC) application processor.

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## Trademarks

# 1 Power Distribution Network Requirements (PDN)

The purpose of a power distribution network (PDN) is primarily to provide clean and reliable power to the active devices on the system. The printed circuit board (PCB) is a critical component of the system-level PDN delivery network. As such, optimal design of the PCB power distribution network is of utmost importance for high performance/low power microprocessors.

TI strongly believes that simulating a PCB's proposed PDN is required for first pass PCB design success. PDN performance must be modeled early in the PCB design process and then optimized in an iterative manner to meet specified device requirements.

Figure 1 presents a break-down model of a complete PDN network from the Voltage Resource Manager (VRM) to the SoC.

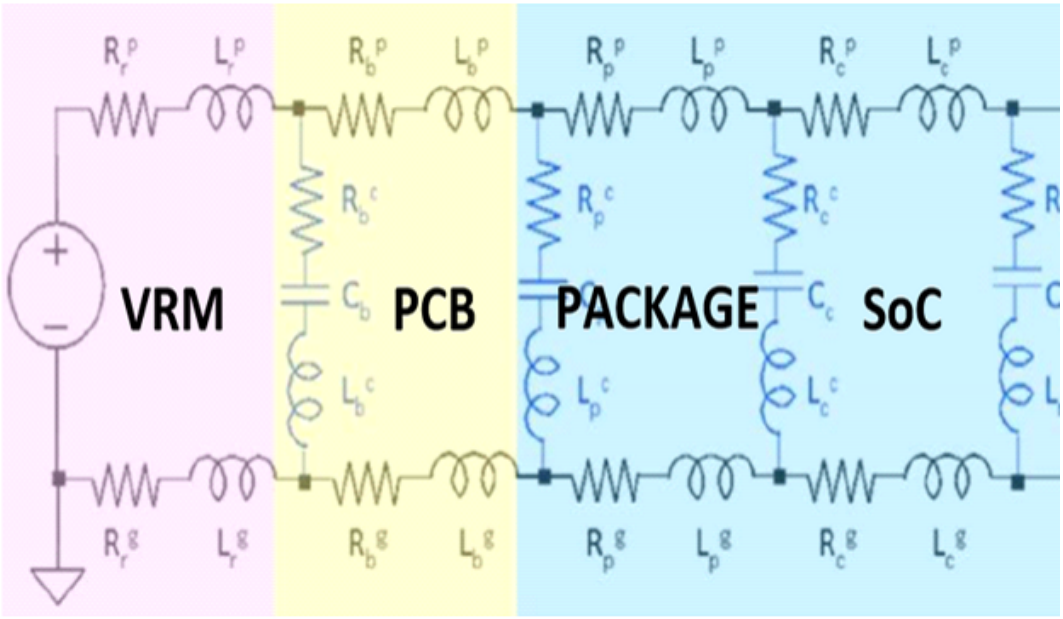


**Figure 1. PDN Model**

Factors such as component selection, board manufacturing, assembly issues, ambient temperature, and other variables, can also cause power supply issues, but not all possible issues are discussed in this document. Nonetheless, every new board design should carefully consider the layout of each of the power supplies since some may be stressed more than others depending on the specific needs of each application.

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## *1.1 General PCB "Best Practices" for PDN*

Although this list is not inclusive of every parameter that must be considered when designing a PCB, a PDN-optimized PCB design will implement these guidelines:

- Power and ground plane pairs (or "islands") should be closely coupled together. The capacitance formed between the planes can be used to decouple the power supply at lower frequencies.
- Whenever possible, the power and ground planes should be solid as this provides a continuous return path for return current.
- Use a thin dielectric thickness between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair so minimizing the separation distance (i.e. the dielectric thickness) will maximize the resulting capacitance.

- The placement of power and ground planes in the PCB stack-up (determined by layer assignment) has a significant impact on the parasitic inductances of power current path. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, placing high priority supplies in the upper-half of the stack-up and low priority supplies in the lower half of the stack-up. This helps to minimize the loop inductance caused by decoupling capacitors and their associated vias.
- External power trace routing between components should be as wide as possible as wider traces result in reduced inductance, increased capacitance, reduced DC resistance and consequently a lower static IR drop.
- Whenever possible, attempt to achieve a ratio of 1:1 (or better) for component pins and associated vias. Do not share vias among multiple capacitors.
- Placement of decoupling capacitors should be as close to the SoC ball as possible.
- Use of short and wide surface traces to connect capacitor pads to the vias connected to the planes below is preferred.
- Use of large diameter vias is preferred for reduced inductance/resistance.

# 2 Simulation Environment

## *2.1 Methodology*

Simulations were run to determine the electrical characteristics of the 66AK2G0x GP EVM processor board. These simulations verify the basic electrical characteristics of the power delivery networks of these critical power supplies to the processor. For the details and requirements for each of these power supplies to the 66AK2G0x, see the *66AK2G0x Multicore DSP+ARM KeyStone II System-on-Chip (SoC) Data Manual* (SPRS932).

Note that only the main power rails are discussed in this analysis. These are:

- CVDD
- CVDD1
- PMIC_VDD1
- PMIC_VDD_CTRL

Figure 2 describes the flow used by most simulation tools to extract DC resistance. In TI PDN analysis, the lumped methodology is preferred where each of the power and GND pins of the VRM and SoC are grouped to shorten the simulation run time.

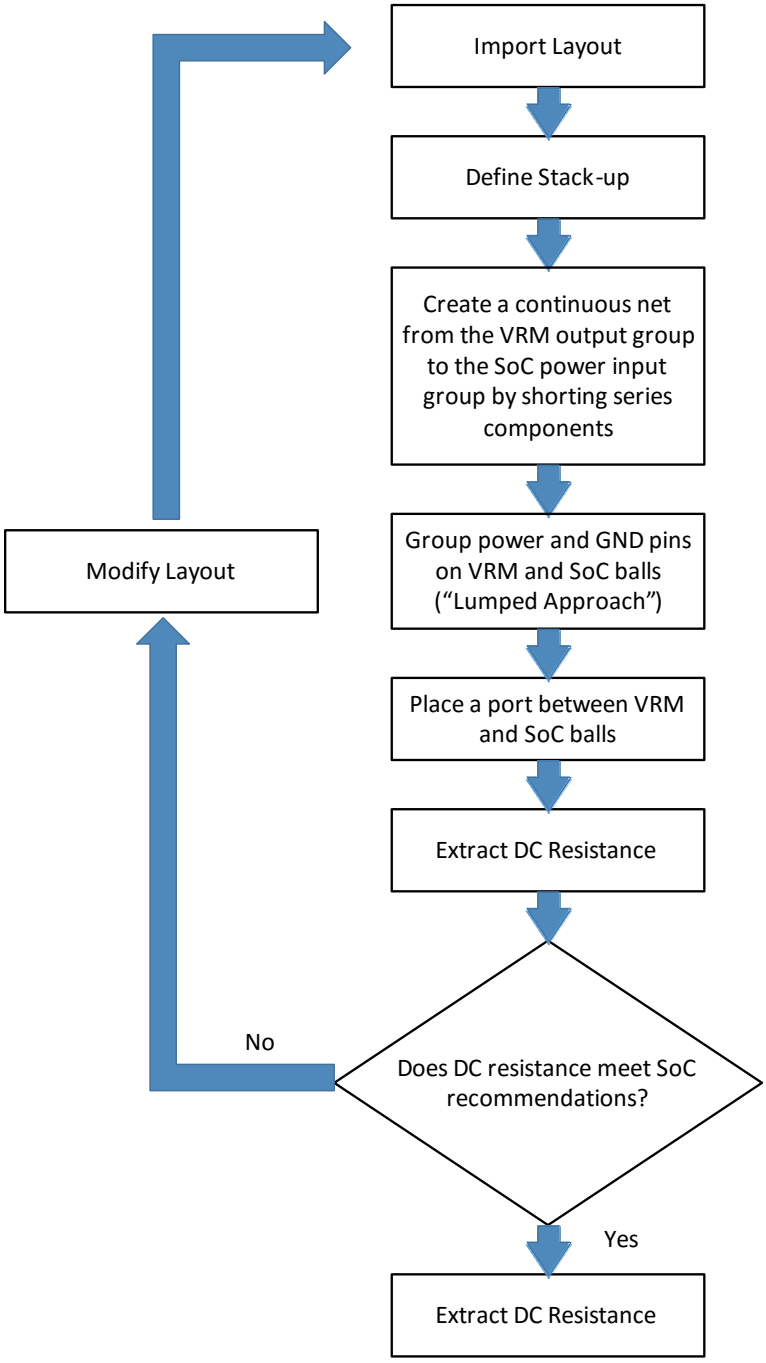


**Figure 2. DC Resistance Extraction Flow**

## 2.2 Software

The simulation results in this document were provided by Ansys Sentinel-PSI v14.2.1p3 running on RedHat Enterprise Linux v6.

### 2.2.1 66AK2G0x GP EVM Stackup

The 66AK2G0x GP EVM implements a 10-layer printed circuit board (PCB). The stack-up utilized for the GP EVM was reproduced in simulation and is presented in Figure 3.

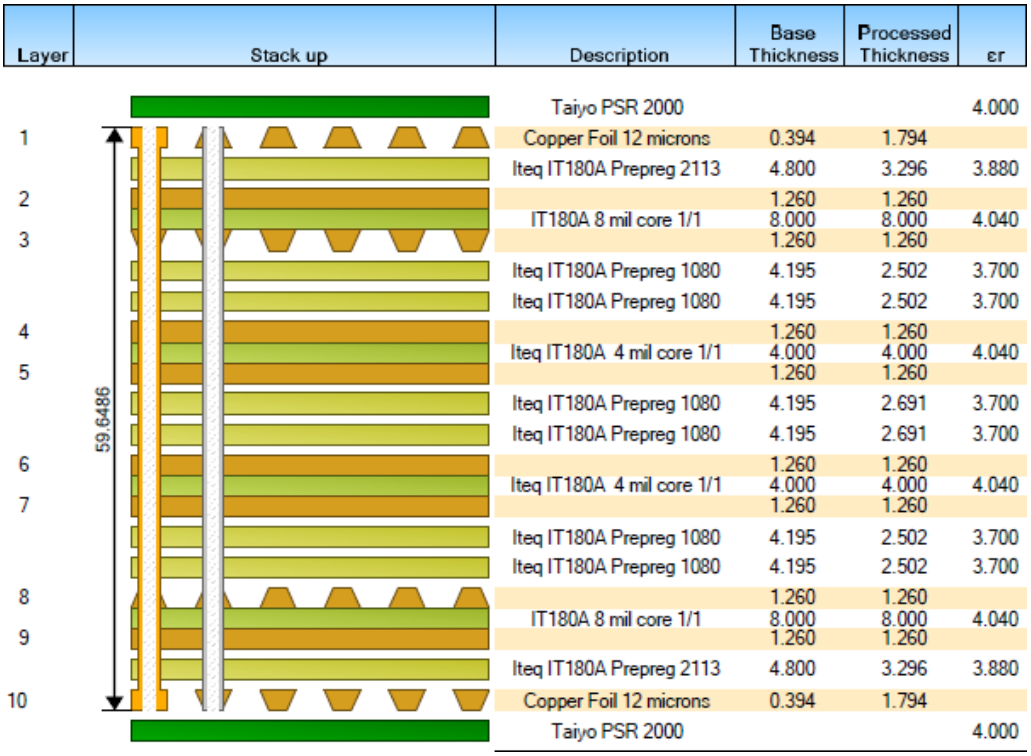


**Figure 3. GP EVM PCB Stack Up**

### 2.2.2 Decoupling Capacitor Count

The GP EVM power supply decoupling capacitor count (broken down by power rail) is provided in Table 1.

**Table 1. GP EVM Decoupling Capacitor Count**

| | Number of Capacitors | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Rail Name** | **0.01 µF** | **0.1 µF** | **0.33 µF** | **1.0 µF** | **3.3 µF** | **4.7 µF** | **10 µF** | **100 µF** | **330 µF** |
| PMIC_VDD_CTRL | | 2 | | | | | | | 1 |
| PMIC_VDD1 | | 3 | | | | | 1 | | |
| CVDD | | 37 | 1 | 1 | 1 | 1 | | 1 | |
| CVDD1 | 1 | 5 | | | | | | 1 | |

### 2.2.3 Decoupling Capacitor Characteristics

The power supply decoupling capacitor main characteristics for capacitors used on the GP EVM are provided in Table 2.

**Table 2. GP EVM Decoupling Capacitor Characteristics**

| Value | Voltage | Package | Temperature Coefficient | Tolerance |
|---|---|---|---|---|
| 0.01 µF | 10 V | 0201 | X5R | 10% |
| 0.1 µF | 10 V | 0201 | X5R | 10% |
| 0.1 µF | 25 V | 0402 | Y5V | 20% |
| 0.33 µF | 6.3 V | 0201 | JB | 20% |
| 1 µF | 10 V | 0402 | X5R | 10% |
| 3.3 µF | 6.3 V | 0402 | X5R | 20% |
| 4.7 µF | 6.3 V | 0603 | X5R | 10% |
| 10 µF | 16 V | 0805 | X5R | 10% |
| 100 µF | 10 V | 1210 | X5R | 20% |

## 3 Simulation Results

### *3.1 IR Drop – Power*

The simulated IR drop for the GP EVM power rails are presented in Figure 4 through Figure 7.

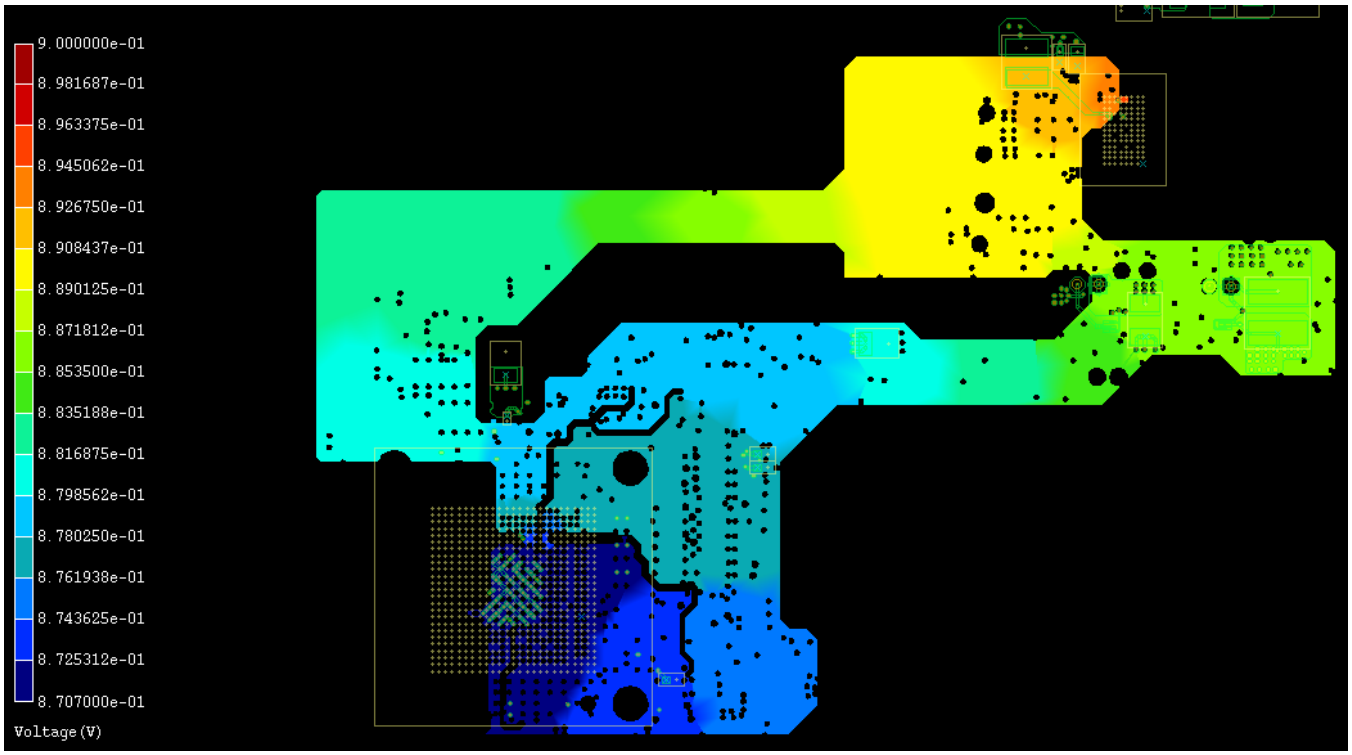


**Figure 4. Voltage Map – CVDD**

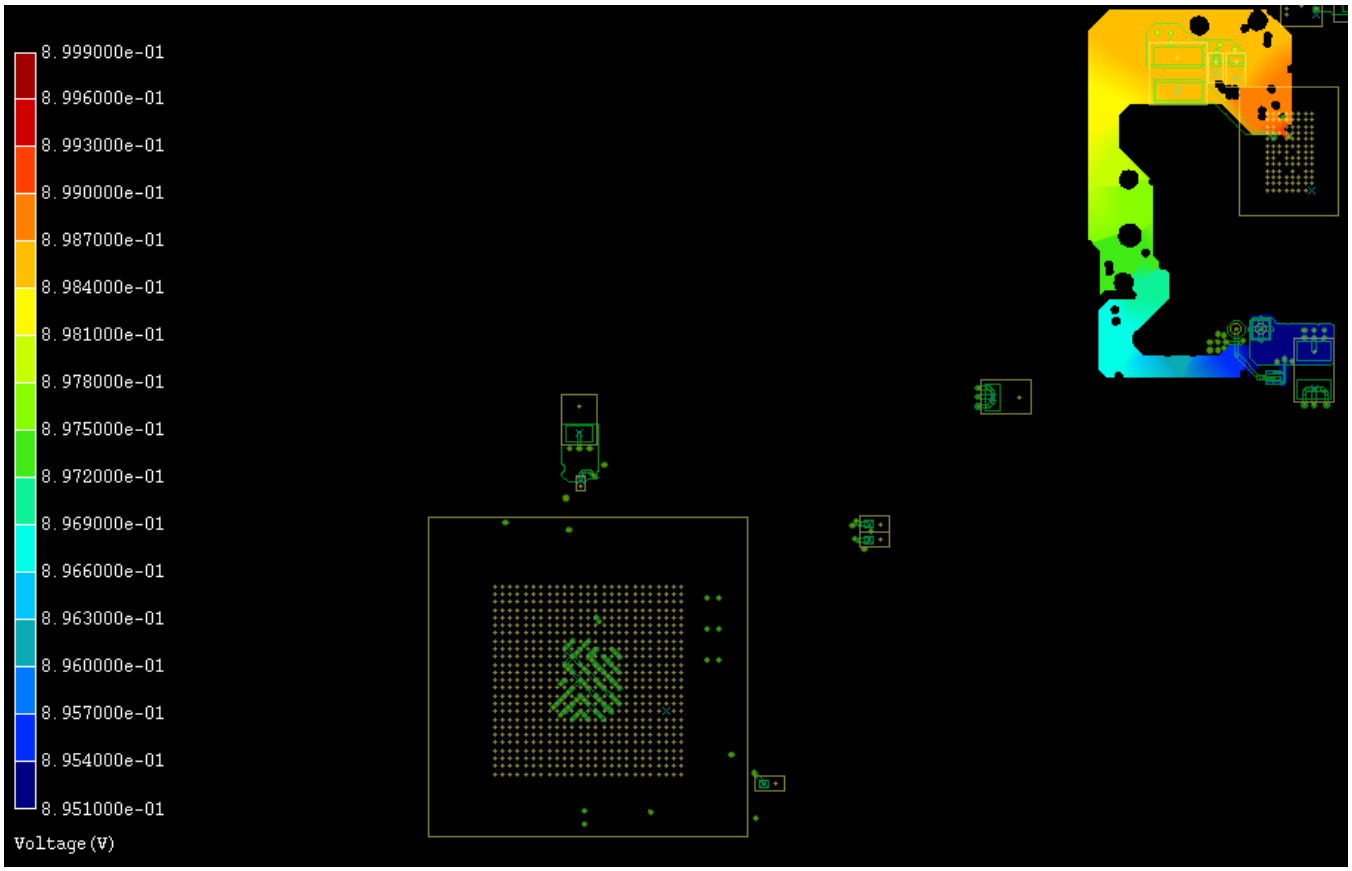


**Figure 5. Voltage Map – PMIC_VDD1**

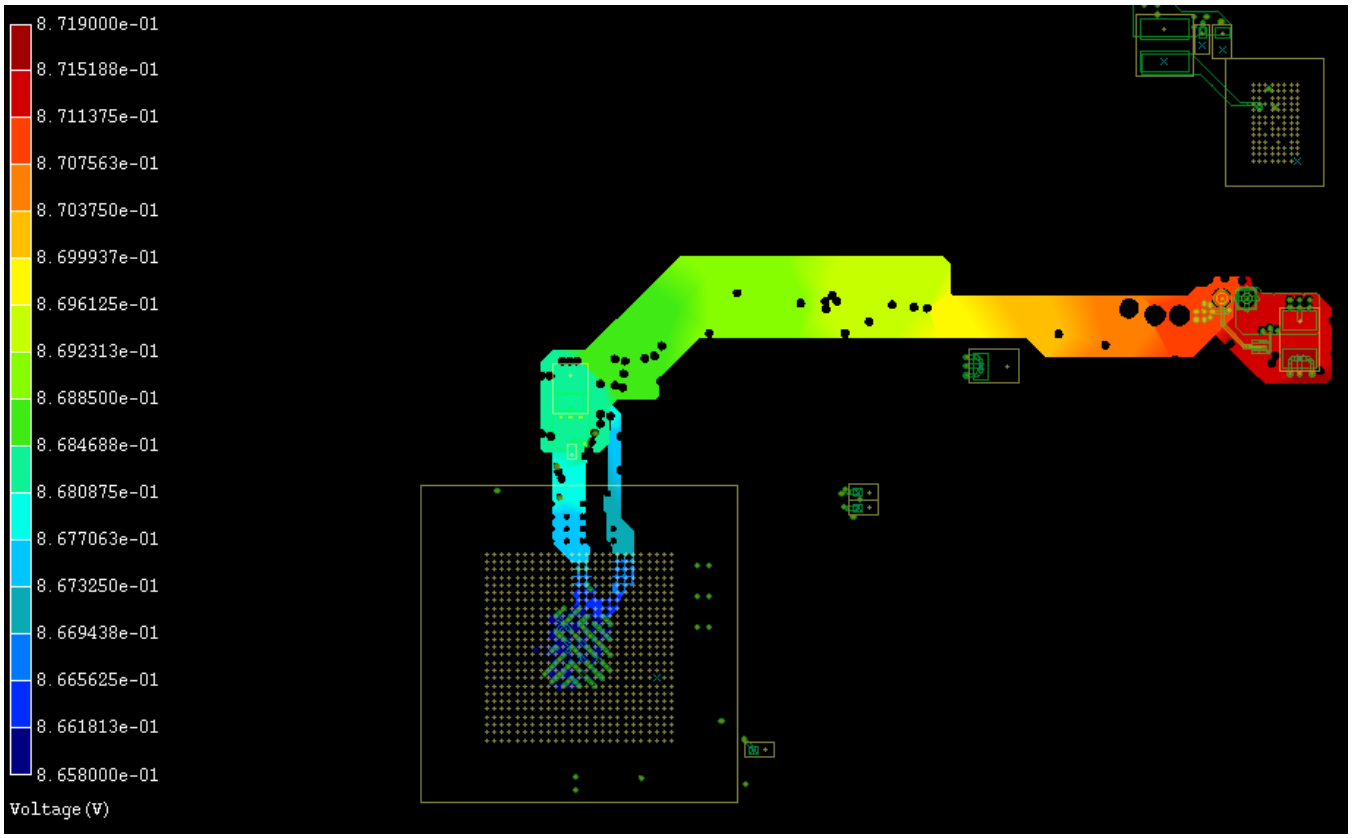


**Figure 6. Voltage Map – CVDD1**


**Figure 7. Voltage Map - PMIC_VDD_CTRL**

The detailed IR drop values for all four power rails are presented in Table 3.

**Table 3. IR Drop – Power (Details)**

| Power Rail | Voltage at Source (V) | Voltage at SoC (V) | IR Drop (mV) |
|---|---|---|---|
| CVDD | 0.9 | 0.871 | 29 |
| PMIC_VDD1/CVDD1 (1) | 0.9 | 0.866 | 34 |
| PMIC_VDD_CTRL | 0.9 | 0.886 | 14 |

(1) PMIC_VDD1 and CVDD1 are linked in series for purposes of simulation.

## 3.2 IR Drop - GND

The simulated IR drop for the GP EVM power rails are presented in Figure 8.

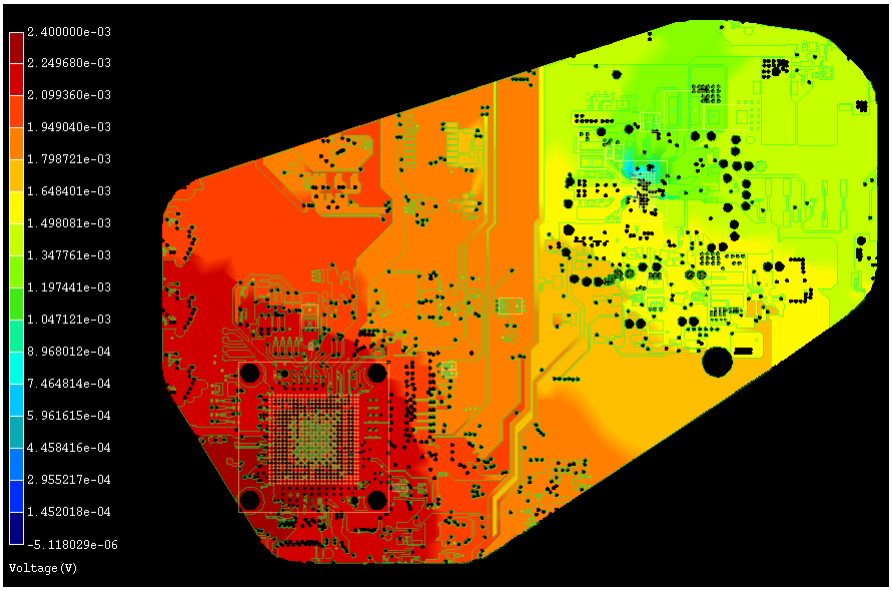


**Figure 8. Voltage Map – DGND**

The detailed IR drop value for the GND rail is presented in Table 4.

**Table 4. IR Drop – GND (Details)**

| Power Rail | Voltage at Source (V) | Voltage at SoC (V) | GND IR Drop (mV) |
|---|---|---|---|
| DGND | 0 | -2.4 | 2.4 |

### 3.3 IR Drop – Total

Because total IR drop is a function of both GND and the power rail in question, both values must be considered when determining if a particular board design meets the overall SoC power delivery requirements.

**Table 5. Combined IR Drop Results**

| Power Rail | Voltage at Source (V) | Voltage at SoC (V) | GND IR Drop (mV) | IR Drop (mV) | Total IR Drop (mV) (1) | IR Drop Limit (mV) | Simulation Results |
|---|---|---|---|---|---|---|---|
| CVDD | 0.9 | 0.871 | 2.4 | 29 | 31.4 | 45 | PASS |
| PMIC_VDD1/CVDD1 (2) | 0.9 | 0.866 | 2.4 | 34 | 36.4 | 45 | PASS |
| PMIC_VDD_CTRL | 0.9 | 0.886 | 2.4 | 14 | 16.4 | 45 | PASS |

(1) Represents the cumulative IR drop of both GND and the respective power rail.

(2) PMIC_VDD1 and CVDD1 are linked in series for purposes of simulation.

## 4 Conclusion

All power rails of the 66AK2G0x GP EVM meet the SoC power delivery requirements. Note that there also exists sufficient margin to support power supply delivery transients, which depending on the power supply chosen, could be substantial.

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