Application Report
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Migrating from TMS320VC5510 to TMS320VC5502

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ABSTRACT

This document describes issues of interest related to migration from the TMS320VC5510 to the TMS320VC5502. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the following data manuals and reference guides: the *TMS320VC5510 Fixed-Point Digital Signal Processor Data Manual* (SPRS076), the *TMS320VC5502 Fixed-Point Digital Signal Processor Data Manual* (SPRS166), the *TMS320C55x DSP CPU Reference Guide* (SPRU371) and the *TMS320C55x DSP Peripherals Reference Guide* (SPRU317).

Migration issues from the TMS320VC5510 to TMS320VC5502 are indicated with the following symbols:

- [S] means software modification is required.
- [H] means hardware modification is required.
- [D] means the VC5510 and VC5502 are different but no modification is necessary for migration (i.e., different but compatible).
- [N] means the VC5502 adds new features that are not available on the VC5510

These symbols are included at the beginning of each section.

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1 Pin and Package Compatibility [H]

Table 1. VC5510, VC5502 Package Types

Device	Package Type(s)	Pin Count
VC5510	MicroStar (Ball Grid Array) (GGW Suffix)	240
VC5502	MicroStar (Ball Grid Array) (GGW Suffix)	176
	Low Profile Quad Flatpack (PGF)	176

NOTE: The VC5502 PSENSE pin, which is a supply pin used for test purposes only, must be left unconnected.

2 Power Supply [H]

Table 2. Power Supply Differences

	Core Supply Voltage (CV_{DD})			I/O Supply Voltage (DV_{DD})			PLL Supply Voltage (PV_{DD})		
Device	**MIN**	***NOM***	**MAX**	**MIN**	***NOM***	**MAX**	**MIN**	***NOM***	**MAX**
VC5510	1.55V	1.6V	1.65V	2.7V	3.3V	3.6V	N/A	N/A	N/A
VC5502	1.20V	1.26V	1.32V	2.7V	3.3V	3.6V	2.7V	3.3V	3.6V

The VC5502 contains an additional supply voltage, PV_{DD}, dedicated for the PLL module only. On the VC5510, the PLL runs on the core supply voltage (CV_{DD}).

NOTE: TI 55x™ DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to insure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long-term reliability of the device. Please refer to the *Power Supply Sequencing Solutions for Dual Supply Voltage DSPs* application report (SLVA073) for more information.

3 Phase-Locked Loop (PLL) and Clock Mode Settings at Reset [S]

Table 3. PLL and Clock Mode Setting Differences

Device	PLL Type	On-Chip Oscillator	Clock Input Source
VC5502	Analog PLL	Yes	Externally generated clock input, or on-chip oscillator with external crystal
VC5510	Digital PLL	No	Externally generated clock input only

The clock input of VC5502 may be sourced either from an externally generated 3.3-V clock input on the X2/CLKIN pin, or from the on-chip oscillator (OSCIN) if an external crystal circuit is attached to the device. The oscillator supports fundamental mode crystals up to 25 MHz. Please refer to the *TMS320VC5502 Fixed-Point Digital Signal Processor Data Manual* (SPRS166) for more details.

The VC5510 has a clock mode select (CLKMD) input pin that selects the mode of the clock generator after reset. Depending on the state of CLKMD, the clock generator will run at either the same frequency as CLKIN or one-half the frequency of the CLKIN. The clock generator can later be programmed in software. Please refer to the *TMS320VC5510 Fixed-Point Digital Signal Processor Data Manual* (SPRS076) for more details.

Unlike the VC5510, the VC5502 does not support the CLKMD input pin. The state of the GPIO4 pin at reset determines whether the internal oscillator will be enabled or disabled. If GPIO4 is low, the internal oscillator will be enabled and the internal oscillator and an external crystal will generate the input clock. If GPIO4 is high, the internal oscillator will be set to power-down mode and the input clock will be taken from the X2/CLKIN pin. Please note that after reset, the GPIO4 pin may become active depending on the boot mode selected through the GPIO[2:0] pins. Refer to section 3.9, *System Clock Generator*, of the *TMS320VC5502 Fixed-Point Digital Signal Processor Data Manual* (SPRS166) for more details.

When the VC5510 is in lock mode (DPLL synthesis enabled), the frequency of the reference clock provided at the CLKIN pin can be multiplied by a synthesis factor of *N* to generate the internal CPU clock cycle. The synthesis factor is determined by:

$$N = M/D_L$$

Where:

M = the multiply factor set in the PLL_MULT field of the clock mode register
D_L = the divide factor set in the PLL_DIV field of the clock mode register

Valid values for *M* are (multiply by) 2 to 31. Valid values for D_L are (divide by) 1, 2, 3, and 4.

For detailed information on clock generation configuration, see the *TMS320C55x DSP Peripherals Reference Guide* (SPRU317).

When the VC5502 is not in bypass mode (PLL mode enabled) the frequency of the input clock can be divided down by a programmable divider (D0) by any factor from 1 to 32. The output clock of the divider can be multiplied by any factor from 1 to 16 through a programmable multiplier (M1). The divider factor can be set through the PLLDIV0 bit of the PLL Divider 0 Register. The multiplier factor can be set through the PLLM bits of the PLL Multiplier Control Register. After reset the divider and multiplier factors are set to 1.

4 Memory [D]

Table 4. Memory Differences

Device	Total On-Chip Memory	SARAM	DARAM	ROM	Max. Addressable External Memory
VC5510	176K words (352K bytes)	128KW	32KW	16kW	8M word
VC5502	48K words (96K bytes)	None	32KW	16kW	8M word

There is a 32-bit EMIF interface on both devices; however, the VC5502 has additional GPIO capabilities. The VC5502 host port interface (HPI) can only access the on-chip DARAM memory.

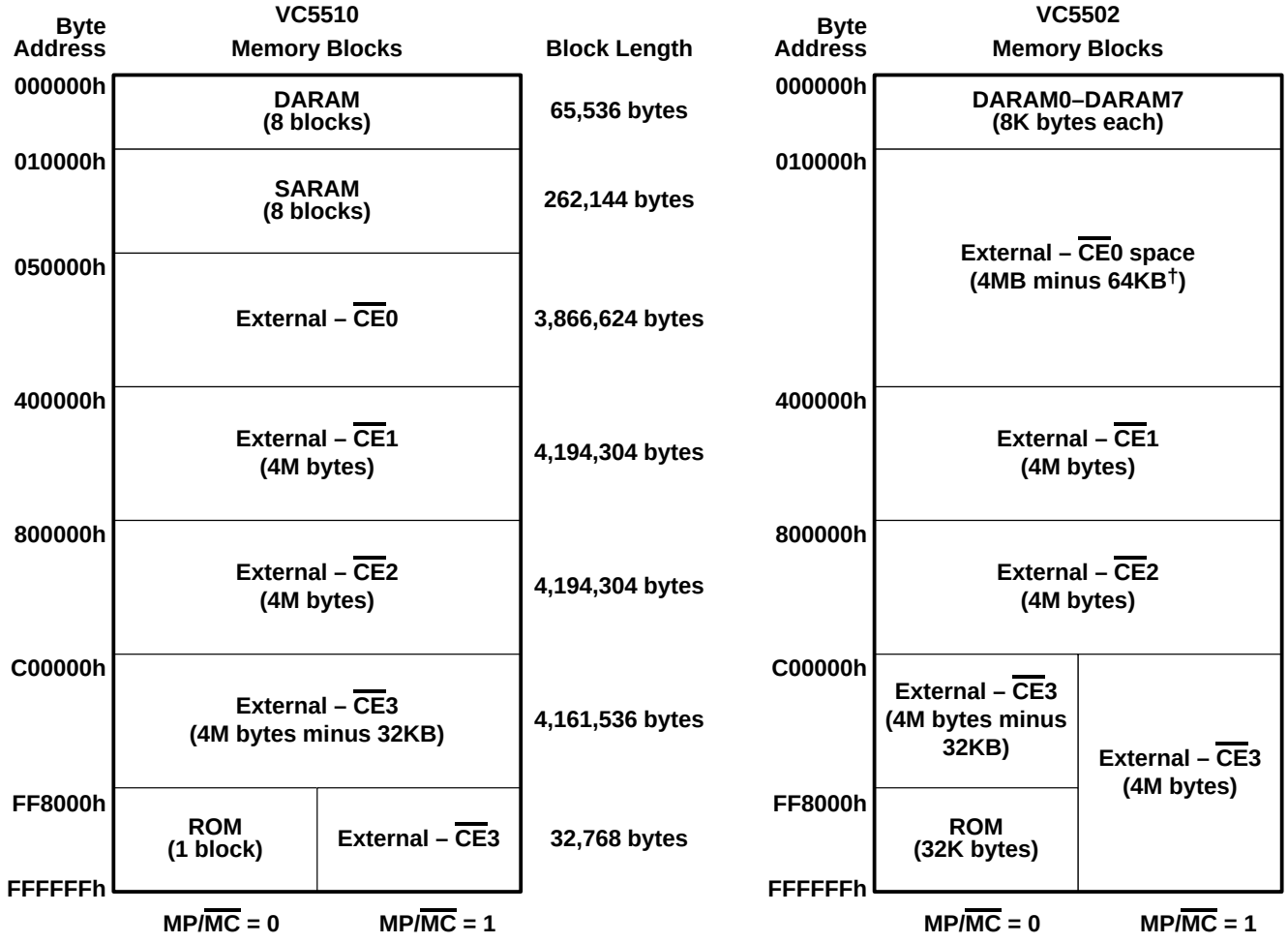
4.1 Instruction Cache (I-Cache) [D]

Table 5. Instruction–Cache Differences

Device	I-Cache Size	Line Flush Support	Miss Counter Register Function Support	RAMSET Block Configuration Support
VC5510	24K Byte	No	No	Yes
VC5502	16K Byte	Yes	Yes	No

The VC5502 supports line flush. A line flush will invalidate the line valid (LV) bit for a specific line in the cache. As a result, the instruction cache registers are different. The VC5502 also supports the miss counter register (ICWMC) function. Refer to the *VC5502 Instruction Cache Reference Guide* (SPRU630) and the *VC5510 Instruction Guide Reference Guide* (SPRU576).

4.2 Memory Map [D]



† The 64K bytes are the on-chip DARAM block.

Figure 1. VC5510, VC5502 Memory Maps

5 Multichannel Buffered Serial Port (McBSP) [H/S]

Some McBSP memory-mapped register addresses are different between the VC5510 and VC5502. Table 6 shows McBSP memory-mapped register differences for Port#0. The same differences also apply to the other McBSP ports. Please refer to the *TMS320VC5510 Fixed-Point Digital Signal Processor Data Manual* (SPRS076) and the *TMS320VC5502 Fixed-Point Digital Signal Processor Data Manual* (SPRS166) for a complete listing of all McBSP registers.

The VC5502 serial port0 (McBSP0) and serial port1 (McBSP1) consist of six signals each routed to the six external signals of each of the serial ports. Four of the six signals of the third serial port (McBSP2) are multiplexed with two pins of the on-chip UART and two pins of the GPIO. In contrast, each McBSP on the VC5510 consists of six signals that are dedicated to that serial port with no pin multiplexing on any McBSP port.

Table 6. VC5510, VC5502 McBSP Port#0 Registers

McBSP Port#0 Registers	VC5510 Word Address	VC5502 Word Address
DRR1_0 (Data Receive Register 1)	0x2801	0x2800
DRR2_0 (Data Receive Register 2)	0x2800	0x2801
DXR1_0 (Data Transmit Register 1)	0x2803	0x2802
DXR2_0 (Data Transmit Register 2)	0x2802	0x2803
SPCR1_0 (Serial Port Control Register 1)	0x2805	0x2804
SPCR2_0 (Serial Port Control Register 2)	0x2804	0x2805
RCR1_0 (Receive Control Register 1)	0x2807	0x2806
RCR2_0 (Receive Control Register 2)	0x2806	0x2807
XCR1_0 (Transmit Control Register 1)	0x2809	0x2808
XCR2_0 (Transmit Control Register 2)	0x2808	0x2809
SRGR1_0 (Sample Rate Generator Register 1)	0x280B	0x280A
SRGR2_0 (Sample Rate Generator Register 1)	0x280A	0x280B
MCR1_0 (Multichannel Control Register 1)	0x280D	0x280C
MCR2_0 (Multichannel Control Register 2)	0x280C	0x280D
RCERC_0 (Receive Channel Enable Register Partition C)	0x2813†	0x2814
RCERD_0 (Receive Channel Enable Register Partition D)	0x2814	0x2815
XCERC_0 (Transmit Channel Enable Register Partition C)	0x2815	0x2816
XCERD_0 (Transmit Channel Enable Register Partition D)	0x2816	0x2817
RCERE_0 (Receive Channel Enable Register Partition E)	0x2817	0x2818
RCERF_0 (Receive Channel Enable Register Partition F)	0x2818	0x2819
XCERE_0 (Transmit Channel Enable Register Partition E)	0x2819	0x281A
XCERF_0 (Transmit Channel Enable Register Partition F)	0x281A	0x281B
RCERG_0 (Receive Channel Enable Register Partition G)	0x281B	0x281C
RCERH_0 (Receive Channel Enable Register Partition H)	0x281C	0x281D
XCERG_0 (Transmit Channel Enable Register Partition G)	0x281D	0x281E
XCERH_0 (Transmit Channel Enable Register Partition H)	0x281E	0x281F

† Word address 0x2813 is a reserved field in the VC5502.

Both the VC5502 and the VC5510 support bootloading via the McBSP0 port in 16-bit serial-slave mode or 8-bit serial EEPROM mode. The VC5510 also supports bootloading from the McBSP0 port in 8-bit serial-slave mode. In both devices, GPIO4 can be used as a handshaking signal when using the McBSP serial-slave boot mode. On both the VC5510 and the VC5502, GPIO4 will go low to signal the host that the device is ready to receive new data. However, on the VC5502 the GPIO4 signal will toggle between every 16-bit word transaction whereas on the VC5510 the GPIO4 signal will go low only after it has received the number of bits it is expecting as dictated by the boot table format (i.e., 32-bits for the entry point address, 16-bits for register contents, etc.). Please refer to the *Using the TMS320VC5510 Bootloader* (SPRA763) and the *TMS320VC5502 Fixed-Point Digital Signal Processor Data Manual* (SPRS166) for more details.

6 Pin Muxing [N]

A number of pins on the VC5502 have two functions, a feature that allows system designers to choose an appropriate media interface for their application without the need for a large pin-count package. Three muxes are included in the VC5502 (see Figure 2) to control the configuration of these dual-function pins: the parallel port mux, the host port mux, and the serial port mux. The state of these muxes is set at reset based on the state of the GPIO6 and GPIO7 pins. The external bus selection register (XBSR) shows the configuration of these muxes after the VC5502 comes out of reset. These muxes represent a significant change from the VC5510 architecture which does not have any muxing for these pins; instead it has dedicated and independent EMIF, EHPI, and serial ports.

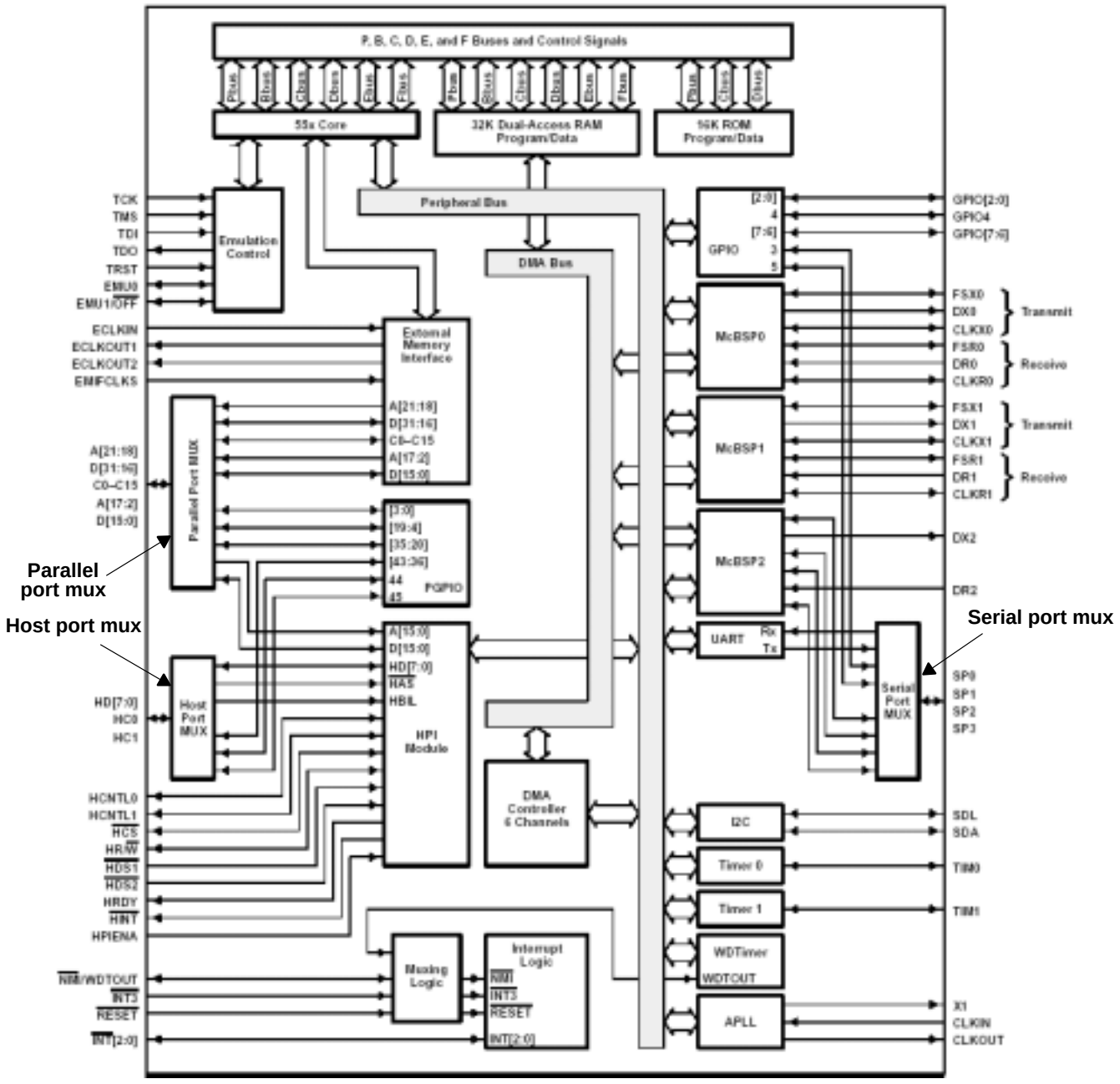


Figure 2. VC5502 Functional Diagram

NOTE: The designation enhanced host port interface (EHPI) on the VC5510 is no longer used for newer C55x devices such as the VC5502. The new name is just host port interface (HPI).

6.1 Parallel Port Mux

The parallel port mux of the VC5502 consists of 20 address signals, 32 data signals, and 16 control signals. The parallel bus supports two different modes (determined by the state of the GPIO6 pin at reset):

- Full EMIF mode: The EMIF's 20 address, 32 data, and 16 control signals are routed to the corresponding external parallel bus address, data, and control signals. HPI 8-bit multiplexed mode can also be selected in parallel with the full-EMIF mode
- Non-multiplexed HPI mode: The HPI is enabled with its 16 address, 16 data, and 9 control signals routed to the corresponding address, data, and control signals of the external parallel bus. Moreover, 16 control signals, 4 address signals, and 16 data signals of the external parallel bus that are not needed for HPI operation are set to general-purpose I/O. EMIF is not available in this mode.

6.2 Host Port Mux

The VC5502 host port mux controls the function of 8 data signals (pins HD[7:0]) and 2 control signals (pins HC0 and HC1). The host port mux supports two different modes (determined by the state of the GPIO6 pin at reset):

- 8-bit multiplexed mode: The HPI's 8 data and 2 control signals are routed to their corresponding pins on the host-port mux.
- Parallel general-purpose I/O mode: All pins on the host-port mux are routed to the PGPIO. The HPI is enabled to 16-bit (non-multiplexed) mode, but communicates through the parallel-port mux.

Additional HPI features available on the VC5502:

- The VC5502 HPI has its own register set, therefore the HINT bit of CPU register ST3_55 is not used for DSP-to-host interrupts. The HINT bit in the host port control register (HPIC) should be used for DSP-to-host interrupts.
- The host port interface ENAble pin (HPIENA) does not exist on the VC5510
- HPI can access the DARAM memory space including the memory-mapped registers.

NOTE: The HPI does not have access to external memory or the peripheral I/O space. The HPI cannot access internal DARAM space when the device is in reset.

The enhanced host port interface (EHPI) on the VC5510 is a dedicated 16-bit parallel interface for interfacing with host processors only. The interface has a 20-bit host address bus and a 16-bit host data bus allowing host accesses to on-chip SARAM, on-chip DARAM, and a portion of external memory. However, the EHPI cannot directly access the on-chip peripherals and cannot access the memory-mapped registers below word address 000030h (byte address 000060h) in DARAM. The signals/pins on the EHPI are not shared/multiplexed with any other external ports.

6.3 Serial Port Mux

On the VC5502, four of the McBSP2 pins are multiplexed with two pins of the on-chip UART and two pins of the GPIO (see Figure 3). The mode of the serial-port mux (determined by the state of the GPIO7 pin at reset) selects which signals are routed to the VC5502 pins.

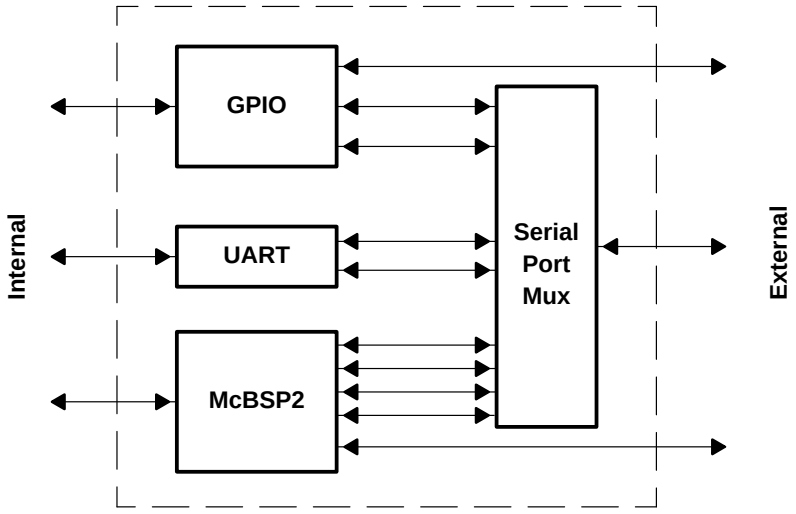


Figure 3. Serial Port Functional Diagram

7 External Memory Interface (EMIF) [H/S]

The VC5502 has an external memory interface (EMIF) supporting a 32-bit interface with general-purpose input/out (GPIO) capabilities and glueless interface to:

- asynchronous static RAM (SRAM)
- asynchronous EPROM
- synchronous DRAM (SDRAM)
- synchronous burst RAM (SBRAM)

The EMIF may be clocked from an external asynchronous clock source through the ECLKIN pin if a specific EMIF frequency is needed. The source for the EMIF clock can be specified at reset through the EMIFCLKS pin. The data throughput performance may be affected due to synchronization issues when an external clock source is used for the EMIF.

The EMIF timings on the VC5502 EMIF are different from the VC5510. For detailed information on EMIF timings, see the device-specific data manuals.

NOTE: The VC5502 EMIF software programming/configuration is different than the VC5510. Please refer to the peripheral guides for more information.

8 Timers [S]

Table 7. Timer Differences

Device	Total Number of Timers	Number of Bits	Type
VC5510	2	20	General purpose (GP)
VC5502	4	64	2 GP, 1 watchdog, 1 DSP/BIOS counter

The VC5502 has four 64-bit timers: Timer 0, Timer 1, Watchdog Timer (WDT), and Timer 3. The first two timers, Timer 0 and Timer 1, are mainly used as general-purpose timers. The watchdog timer can be used as either a general-purpose timer or a watchdog timer. The output pin of the watchdog timer, WDTOUT, is multiplexed with the NMI input pin; its function can be controlled via the NMI/WDTOUT_CFG bit of the TSSR register. The watchdog timer output can also be internally connected to the NMI, RESET, and INT3 signals of the VC5502 via the IWCON bits of the TSSR. The fourth timer, Timer 3, is reserved as a DSP/BIOS counter. This timer has no input or output pin. No interrupts are needed from this timer; therefore, the timer output is not internally connected to the CPU interrupt logic.

NOTE: The VC5502 timer software programming/configuration is different than the VC5510. Please refer to the peripheral guides for more information.

9 UART [N]

The VC5502 adds a universal asynchronous receiver/transmitter (UART) on-chip peripheral. The UART performs serial-to-parallel conversions on data received from a peripheral device or modem and parallel-to-serial conversion on data received from the CPU. The CPU can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be configured to minimize software management of the communications link. It also includes a programmable baud rate generator capable of dividing the CPU clock by divisors from 1 to 65535 and producing a 16y-reference clock for the internal transmitter and receiver logic.

UART bootload is also supported on the VC5502. The boot load mode selection is determined by the logic level on the GPIO[2:0] pins when sampled at reset.

10 Inter-Integrated Circuit (I^2C) [N]

The VC5502 adds an Inter-integrated circuit (I2C) multi-master and slave interface. The I2C serial port offers compatibility with Philips. I2C-Bus. Specification, Version 2.1 (January 2000). Some features of this port include:

- Up to 400 Kbps (no fail-safe I/O buffers)
- 7-bit and 10-bit device addressing modes
- Master (transmit/receive) and slave (transmit/receive) functionality

I^2C boot load in master mode is supported on the VC5502.

11 DMA [S]

The VC5502 DMA provides four standard ports: two for DARAM, one for peripherals, and one for external memory. The VC5510 DMA differs in that it has one standard port for SARAM and one for DARAM while the rest of the ports are the same.

The VC5502 DMA controller allows transfers to be synchronized to selected events. The VC5502 supports 16 separate sync events and each channel can be tied to separate sync events independent of the other channels. The VC5510 supports only 14 separate sync events. The setting of the SYNC field in the DMA_CCR register determines the synchronization mode. Please refer to Table 8.

Table 8. VC5510, VC5502 DMA Synchronization Events

DMA_CCR Sync Field	VC5510 Sync Event	VC5502 Sync Event
00000b	No sync event	No sync event
00001b	McBSP0 receive event (REVT0)	McBSP0 receive event (REVT0)
00010b	McBSP0 transmit event (XEVT0)	McBSP0 transmit event (XEVT0)
00101b	McBSP1 receive event (REVT1)	McBSP1 receive event (REVT1)
00110b	McBSP1 transmit event (XEVT1)	McBSP1 transmit event (XEVT1)
01001b	McBSP2 receive event (REVT2)	Reserved/McBSP event Serial port mux mode = 0: reserved Serial port mux mode = 1: McBSP2 receive event (REVT2)
01010b	McBSP2 transmit event (XEVT2)	Reserved/McBSP event Serial port mux mode = 0: reserved Serial port mux mode = 1: McBSP2 transmit event (XEVT2)
01011b	Reserved (do not use this value)	Reserved/UART event Serial port mux mode = 0: UART receive event (UARTREVT) Serial port mux mode = 1: reserved
01100b	Reserved (do not use this value)	Reserved/UART event Serial port mux mode = 0: UART transmit event (UARTXEVT) Serial port mux mode = 1: reserved
01101b	Timer 0 event	Timer 0 event
01110b	Timer 1 event	Timer 1 event
01111b	External Interrupt 0	External interrupt 0
10000b	External Interrupt 1	External interrupt 1
10001b	External Interrupt 2	External interrupt 2
10010b	External Interrupt 3	External interrupt 3
10011b	External Interrupt 4	I^2C receive event
10100b	External Interrupt 5	I^2C transmit event
Other values	Reserved (do not use these values)	Reserved (do not use these values)

The reset values of the DMA registers are different between the two devices. Please refer to Table 9.

Table 9. VC5510, VC5502 DMA Register Reset Values

DMA Register	VC5510 Reset Value	VC5502 Reset Value
DMA_GCR†	0008h	0000h
DMA_CCR	0000h	0000h
DMA_CICR	0003h	0183h
DMA_CSR	0000h	0000h
DMA_CSDP	0000h	0000h
DMA_CSSA_L	Undefined	0000h
DMA_CSSA_U	Undefined	0000h
DMA_CDSA_L	Undefined	0000h
DMA_CDSA_U	Undefined	0000h
DMA_CEN	Undefined	0001h
DMA_CFN	Undefined	0001h
DMA_CEI	Undefined	Does not exist
DMA_CSEI	Undefined	0000h
DMA_CDEI	Undefined	0000h
DMA_CFI	Undefined	Does not exist
DMA_CSFI	Undefined	0000h
DMA_CDFI	Undefined	0000h
DMA_GTCR	0000h	0000h
DMA_GSCR	0000h	Does not exist
DMA_CSAC	Undefined	Does not exist
DMA_CDAC	Undefined	Does not exist

† The EHPI_EXCL and EHPI_PRIO bits are reserved bits on the VC5502

NOTE: The DMA software compatibility register (DMA_GSCR) is not available on the VC5502. Please refer to the *TMS320C55x DSP Peripherals Reference Guide* (SPRU317) for a complete description of all DMA register functions.

12 Bootloader [H]

Both the VC5502 and VC5510 offer several options to download code into the DSP on-chip RAM. Refer to Table 10.

In both devices, GPIO4 can be used as a handshaking signal when using the McBSP serial-slave boot mode. GPIO4 will go low to signal the host that the device is ready to receive new data. However, on the VC5502 the GPIO4 signal will toggle between every 16-bit word transaction whereas on the VC5510 the GPIO4 signal will go low only after it has received the number of bits it is expecting as dictated by the boot table format (i.e., 32-bits for the entry point address, 16-bits for register contents, etc.). Please refer to the *Using the TMS320VC5510 Bootloader* (SPRA763) and *TMS320VC5502 Fixed-Point Digital Signal Processor Data Manual* (SPRS166) for more details.

On the VC5502 external pins BOOTM2, BOOTM1, and BOOTM0 select the boot configuration. The values of BOOTM[2:0] are latched with the rising edge of the RESET input. BOOTM2 is shared with GPIO2, BOOTM1 is shared with GPIO1, and BOOTM0 is shared with GPIO0. However, on the VC5510, external pins BOOTM3, BOOTM2, BOOTM1, and BOOTM0 select the boot configuration. The values of BOOTM[2:0] are latched with the rising edge of the RESET input. BOOTM[0] is shared with general-purpose IO1. BOOTM[1] is shared with general-purpose IO2. BOOTM[2] is shared with general-purpose IO3.

Table 10. VC5510, VC5502 Bootloader Modes

	VC5510		VC5502	
Boot Mode Source	**Support**	**BOOTM[3:0]**	**Support**	**BOOTM[2:0]**
Standard serial boot from McBSP0 (16-bit)	Yes	1110	Yes	010
Standard serial boot from McBSP0 (8-bit)	Yes	1111	No	–
SPI EEPROM boot (16-bit address EEPROM) using McBSP0	Yes	1001	No	–
SPI EEPROM boot (24-bit address EEPROM) using McBSP0	Yes	0001	Yes	001
HPI boot, both in multiplexed and non-multiplexed modes†	Yes	1101	Yes	101
Parallel EMIF boot from 8-bit external asynchronous memory	Yes	1010	No	-
Parallel EMIF boot from 16-bit external asynchronous memory	Yes	1011	Yes	011
Parallel EMIF boot from 32-bit external asynchronous memory	Yes	1100	No	–
Direct execution (no boot) from 32-bit external asynchronous memory	Yes	0000, 1000	Yes	100
Direct execution (no boot) from 16-bit external asynchronous memory	No	–	Yes	000
I^2C EPROM‡ boot	No	–	Yes	110
UART boot	No	–	Yes	111

† This is called the EHPI mode on the VC5510.
‡ Supporting EPROMs up to 512K bits.

13 IDLE Domain Configuration [S]

The IDLE_EN bits control whether or not a peripheral responds to an idle request from the peripheral domain. On the VC5510, these bits reside in the control registers for each peripheral. On the VC5502, however, these bits are all consolidated into the peripheral idle control register (PICR) and the master idle control register (MICR). As a result, the software configuration for idle modes is different between the two devices.

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