TMS320C6000 HPI to PCI Interfacing Using the PLX PCI9050

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ABSTRACT

This application report describes an interface between the Texas Instruments TMS320C6000™ DSP host port and the PLX Technology PCI9050 (PCI9052), the PCI interface chip. The PCI9052 is functionally the same as the PCI9050. The only difference between these two devices is that the PCI9052 is somewhat faster than the PCI9050.

This application report includes a diagram showing connections between the two devices, PAL equations, and verification that timing requirements are met for each device (using tables and timing diagrams).

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1 Host Port Interface to the PCI Bus

The PCI9050 provides a compact high-performance PCI bus target (slave) interface for adapter boards. The PCI9050 is designed to connect a wide variety of local bus designs to the PCI bus. The PCI9050 can be programmed to connect directly to the multiplexed or nonmultiplexed 8-bit, 16-bit, or 32-bit local bus. The 8-bit and 16-bit modes enable easy conversion of ISA designs to the PCI. The PCI9050 contains a bidirectional FIFO to speed match the 32-bit wide, 33-MHz PCI bus to a local bus, which may be narrower or slower. Up to five local address spaces and up to four chip selects are supported.

2 PCI9050 Interface

Voltage conversion is required between the PCI9050 and TMS320C6000 DSP because the PCI9050 requires 5 V to operate and the C6000™ DSP is a 3–V device. Voltage conversion can be accomplished using the TI SN74CBTD3384 bus switch. The SN74CBTD3384 is a 10-bit straight-through switch with inputs on one side and outputs on the opposite side of the package. The basic bus switch is an NMOS device with the substrate connected to ground, thus allowing bidirectional data flow through the channel. To make this device into a voltage translator, the 5-V Vcc is lowered to 4.3 V through an internal diode. The 3.3-V bus is established because the NMOS bus switch requires a gate-to-source voltage of 1 V to conduct.

The PCI9050 has no direct master capability on the PCI bus. The internal registers are accessible from the host CPU on the PCI bus or from the serial EEPROM.

Figure 1 is a diagram and Table 1 is a list of the PCI9050-to-HPI connections. The PCI9050 local bus is programmed to be nonmultiplexed (MODE pin is low).

The configuration shown does not support the PCI9050 burst mode.

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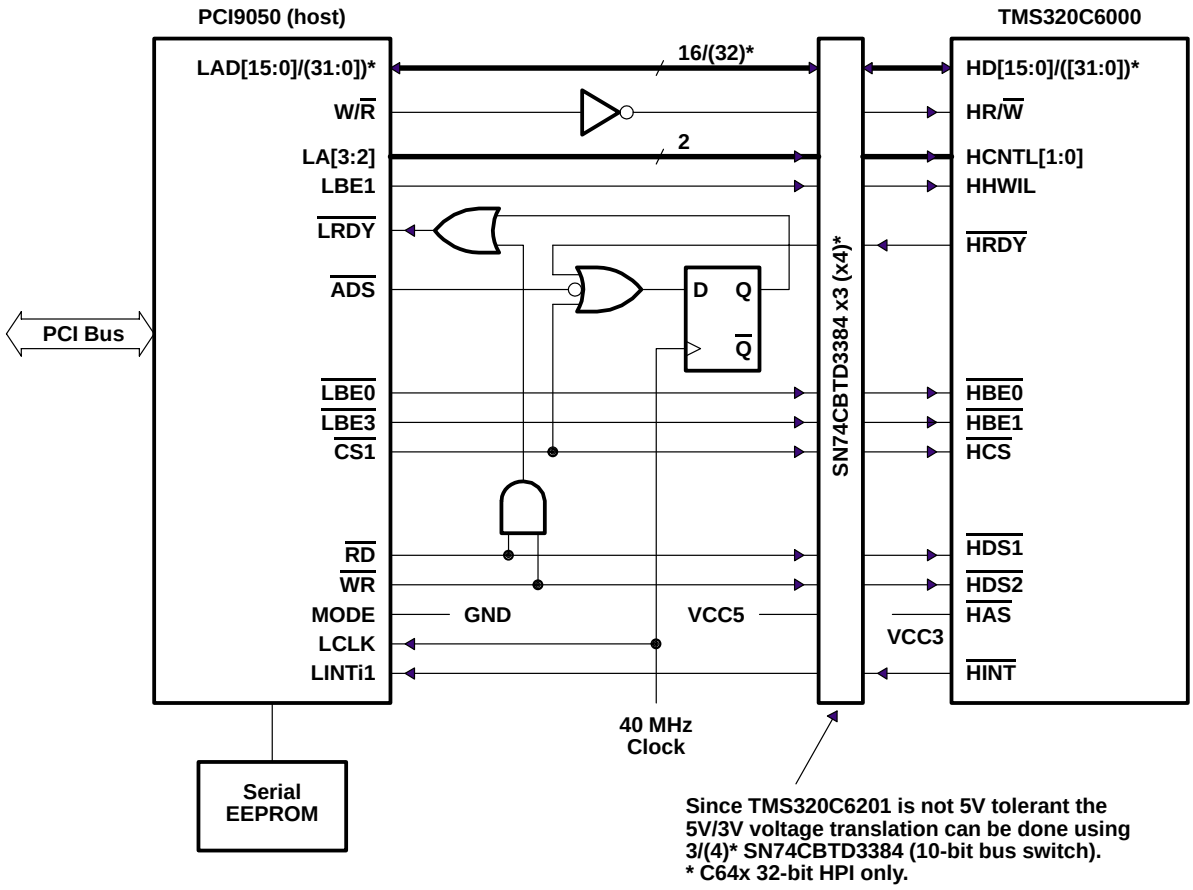


Figure 1. PCI9050-to-HPI Interface Block Diagram

Table 1. PCI9050-to-HPI Pin Connections

HPI Pin	PCI9050 Pin	Function
HCNTL[1:0]	LA[3:2]	Address bits of PCI9050 are used as control signals.
HHWIL	LBE1	LBE1 identifies the first or second half-word of transfer. This signal is absent on the TMS320C64x 32-bit HPI.
HR/$\overline{W}$	Inverted W/$\overline{R}$	Indicates a read or write access. Because the C6000 HPI port has a read–write (HR/$\overline{W}$) line with the opposite polarity of the PCI9050 read–write pin (W/$\overline{R}$), an inverter is used to connect these two lines.
HD[15:0]/[31:0]	LAD[15:0]/[31:0]	16 LSBs of data. 32-bit word for C64x 32-bit HPI.
$\overline{HDS1}$	$\overline{RD}$	$\overline{HDS1}$ is connected to the $\overline{RD}$.
$\overline{HDS2}$	$\overline{WR}$	$\overline{HDS2}$ is connected to the $\overline{WR}$.
$\overline{HAS}$	Vcc	Address latch enable is not used in this interface.
$\overline{HCS}$	$\overline{CS1}$	$\overline{HCS}$ can be connected to any of the PCI9050 $\overline{CS}$ output lines.

Table 1. PCI9050-to-HPI Pin Connections (Continued)

HPI Pin	PCI9050 Pin	Function
$\overline{\text{HBE0}}$	$\overline{\text{LBE0}}$	HPI uses this value on writes only. This signal is absent on the C6211/C6711 and C64x.
$\overline{\text{HBE1}}$	$\overline{\text{LBE3}}$	HPI uses this value on writes only. This signal is absent on the C6211/C6711 and C64x.
$\overline{\text{HRDY}}$	$\overline{\text{LRDY}}$	Asynchronous HPI ready output ($\overline{\text{HRDY}}$) is synchronized and connected to $\overline{\text{LRDY}}$.
$\overline{\text{HINT}}$	$\overline{\text{XINTx}}$	Any external interrupt can be chosen.

3 Configuration

During power up, the PCI $\overline{\text{RST}}$ signal resets the default values of the PCI9050 internal registers. In return, the PCI9050 outputs the local reset signal ($\overline{\text{LRESET}}$) and checks for the existence of the serial EEPROM. If a serial EEPROM is installed and the first 16-bit word is not FFFFh, the PCI9050 loads the internal registers for the serial EEPROM. Otherwise, default values are used. The PCI9050 configuration registers can be written only by the optional serial EEPROM or the PCI host processor.

Five local address spaces (local spaces 0–3 and expansion ROM) are accessible from the PCI bus. In this example, local space 1 is used. A set of four registers defines each space, defining the local bus characteristics:

- PCI base address
- Local range
- Local base address (remap)
- Local bus region descriptor

Local bus address space 1 region descriptor register (LAS1BRD) must be set to:

- Disable burst (LAS1BRD[0] = 0)
- Enable READY input (LAS1BRD[1] = 1)
- Disable BTERM input (LAS1BRD[2] = 0)
- Enable 16-bit bus width (LAS1BRD[23:22] = 01) or enable 32-bit bus width for TMS320C64x™ 32-bit HPI (LAS1BRD[23:22] = 10)
- Little-endian (LAS1BRD[24] = 0)
- The PCI9050 provides a write-cycle hold parameter that should be used to extend the cycle for one clock after the write strobe is deasserted (LAS1BRD[31:30] = 01 to extend a write cycle for one clock). This is done to meet the data hold-time requirement for the C6000 DSP.

The wait states for READ strobe should be cleared to 0.

TMS320C64x is a trademark of Texas Instruments.

4 PCI9050-to-HPI Timing Verification

To verify proper operation, two functions have been examined:

1. a PCI9050 write to the HPI (Table 2, Figure 2, and Figure 3)
2. a PCI9050 read from the HPI (Table 3, Figure 4, and Figure 5)

In each instance, timing requirements were compared for each of the devices.

Note that the write cycle is extended for one clock (by setting LAS1BRD[31:30] = 01) after the write strobe is deasserted (to meet data hold-time requirement of the HPI).

The estimated maximum transfer speed between the 16-bit HPI and the PCI bus is 20 Mbytes/s for reads, and 16 Mbytes/s for writes.

The tables and timing diagrams show that the timing parameters for both devices are met in the interface of the PCI9050 and the HPI. The PCI9050 local bus in this example operates at 40 MHz; the TMS320C6201 DSP operates at any frequency ranging from 100–200 MHz (C6211 or C6701 devices can operate at frequencies up to 167 MHz, and C64x™ devices can operate at frequencies up to 600 MHz).

Table 2. Timing Requirements for PCI9050 Write to TMS320C6000 HPI

HPI Symbol	PCI9050 Symbol†	Parameter	C6x01 HPI Min (ns)	C6x11 HPI Min (ns)	C64x HPI Min (ns)	PCI9050 Min (ns)
tw(HSTBL)	$2Tcyc–td(RD)_{max}+td(RD)_{min}$	Pulse width of HDS low	10	24	24	30
tsu(SEL–HSTBL)	Tcyc–td(LBE)+td(WR)	Setup time, select signals valid before HDS	4	5	5	14
th(HSTBL–SEL)	2Tcyc–td(RD)+ td(LBE)	Hold time, select signals valid after HDS low	2	4	2	27
tsu(HDV–HSTBH)	2Tcyc–td(LAD)+td(WR)	Setup time, host data valid before HDS high (WRITE SETUP TIME)	3	5	5	38
th(HSTBH–HDV)	Tcyc–td(WR)+ td(LAD)	Hold time, host data valid after HDS high	2	3	2	17

† Tcyc denotes one clock cycle time of PCI9050 local bus. At 40-MHz operating frequency, Tcyc = 25 ns.

C64x is a trademark of Texas Instruments.

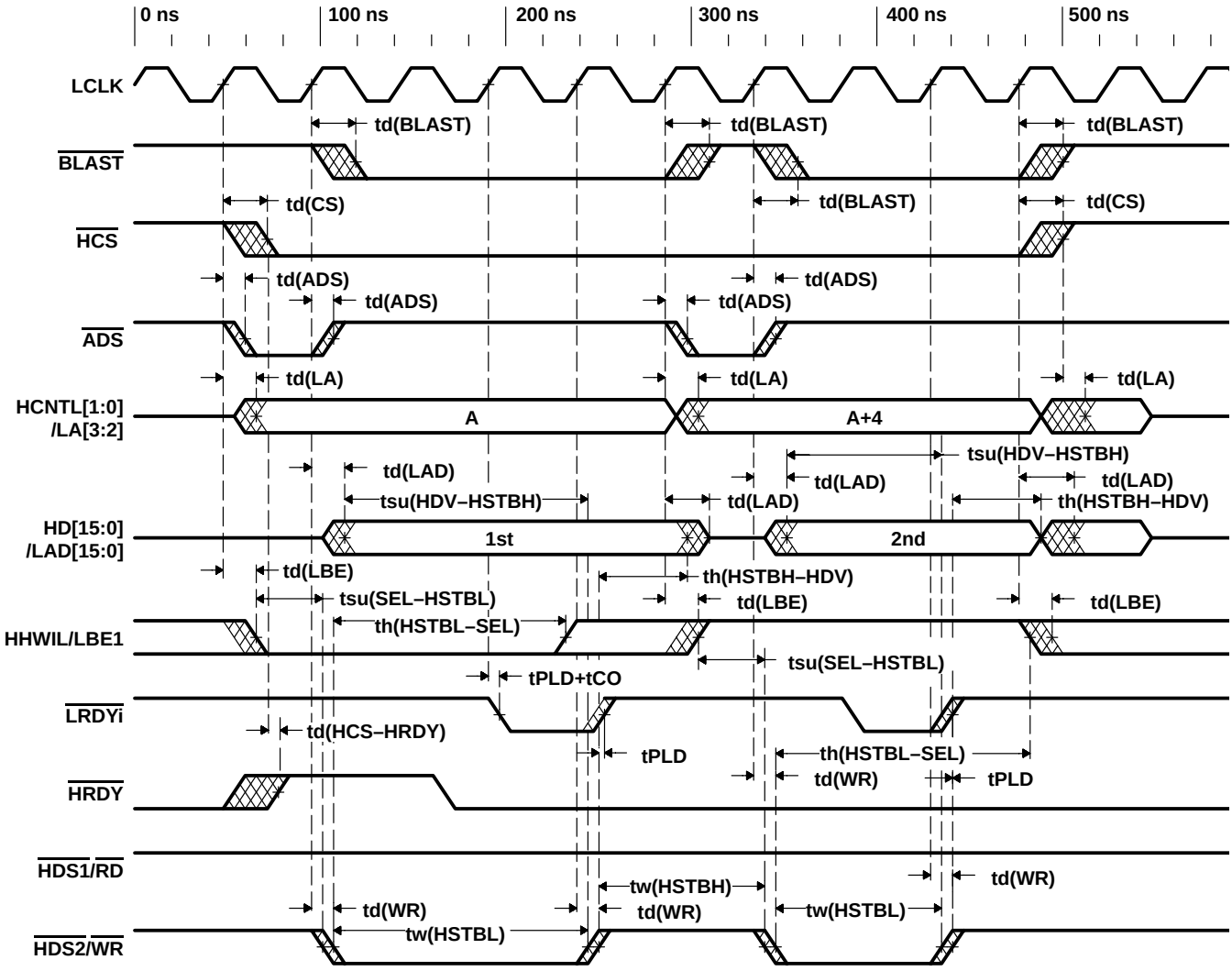


Figure 2. PCI9050 Write to TMS320C6000 DSP Using the HPI (16-Bit)

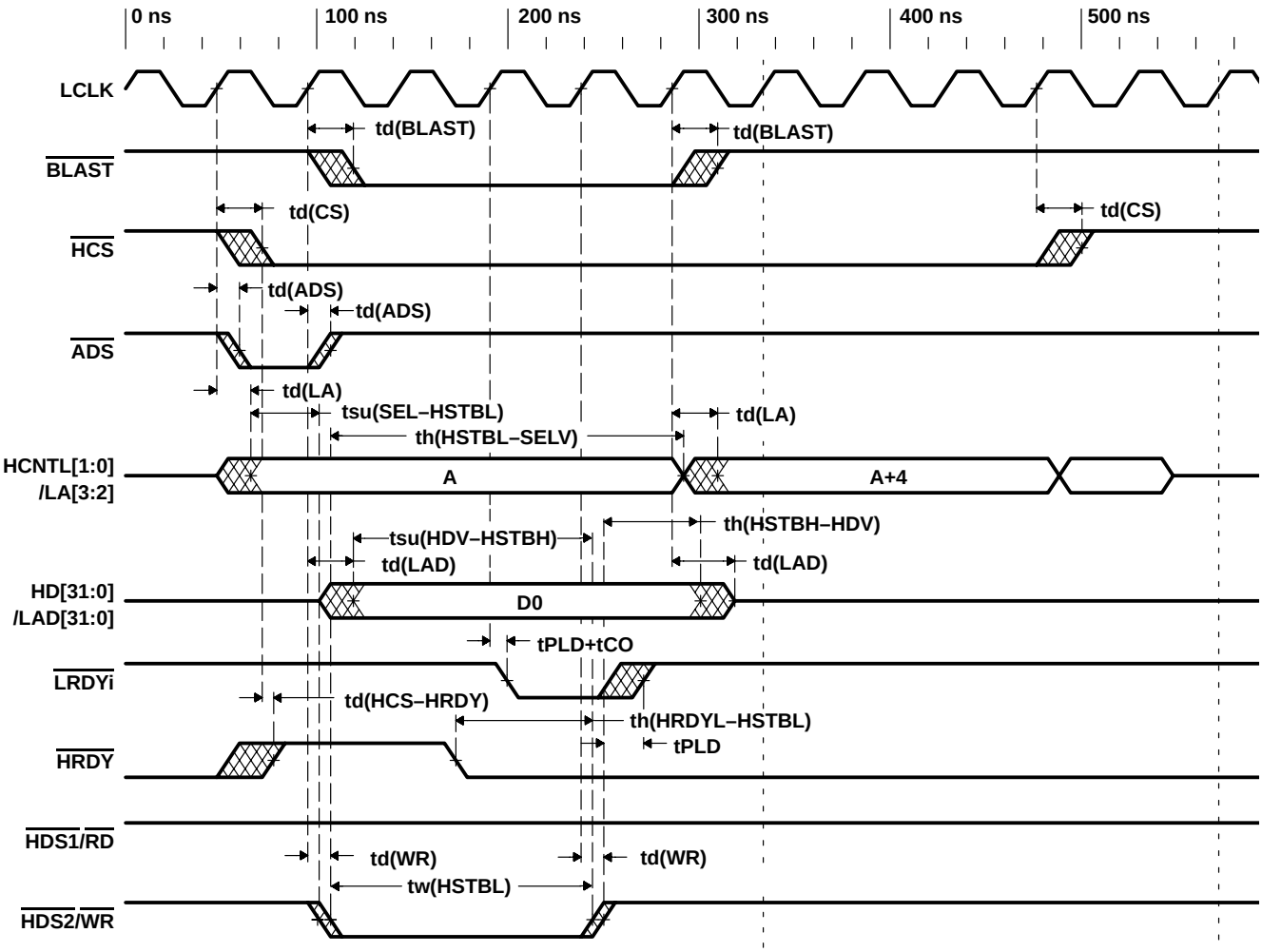


Figure 3. PCI9050 Write to TMS320C64x DSP Using the HPI (32-Bit)

Table 3. Timing Requirements for PCI9050 Read From TMS320C6000 HPI

HPI Symbol†	PCI9050 Symbol	Parameter	C6201 HPI Min (ns)	C6211 HPI Min (ns)	C64x HPI Min (ns)	PCI9050 Min (ns)
2Tcyc–td(RD)–td(HSTBL–HDV)	Tsu	(READ SETUP TIME) Input setup LAD[15:0]/[31:0] – LCLK	11	8	11	8
td(RD)+th(HSTBH–HDV)	Th	Input hold from LCLK – LAD[15:0]/[31:0]	9	10	9	2
Tcyc–tCO–tPLD	Tsu	LRDYi valid to LCLK high–READY setup time	15	15	15	8
Td(RD)+tPLD	Th	LCLK high to LRDYi invalid–READY hold time	12	12	12	2

† Tcyc denotes one clock cycle time of PCI9050 local bus. At 40-MHz operating frequency, Tcyc = 25 ns.

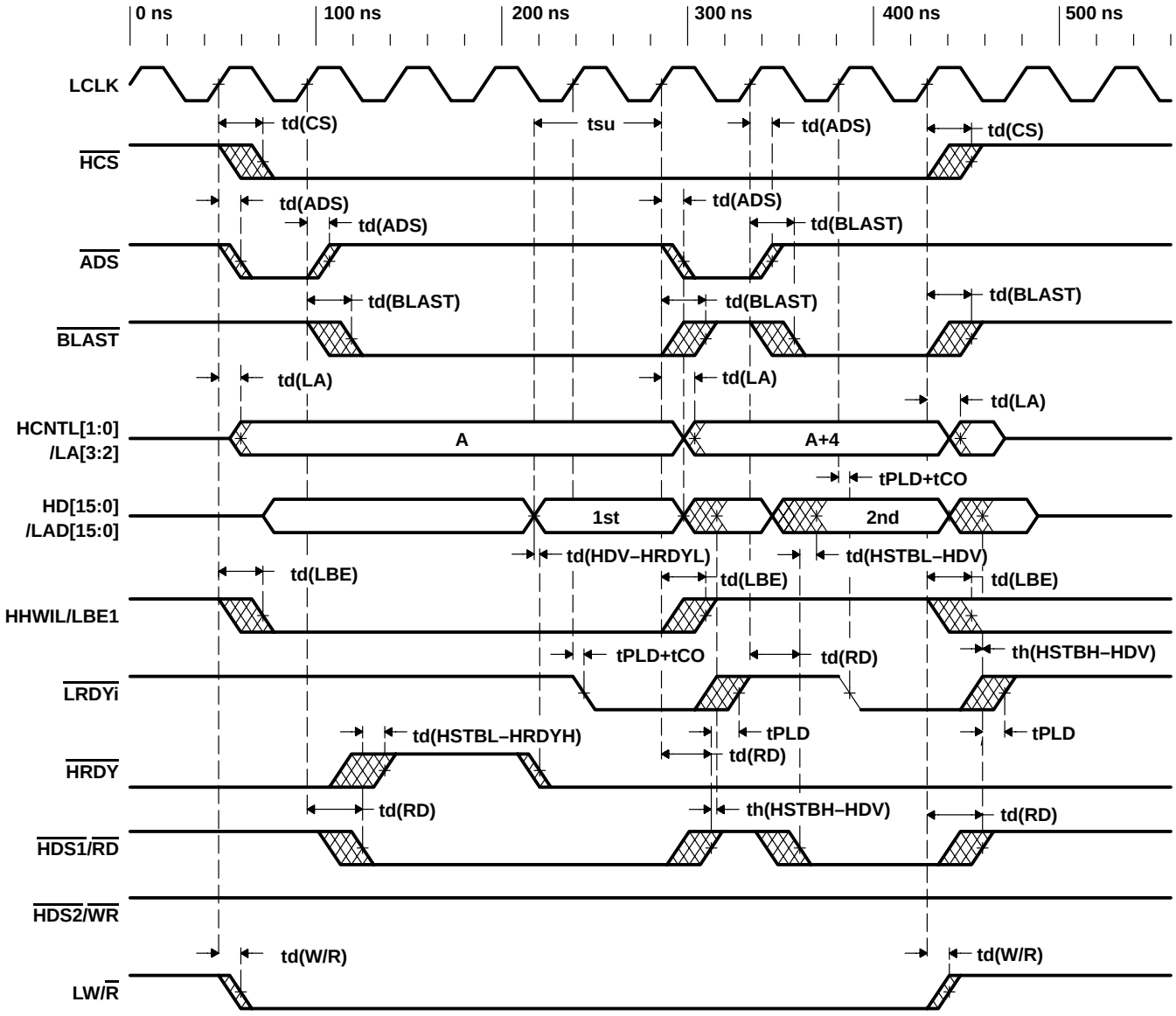


Figure 4. PCI9050 Read From TMS320C6000 DSP Internal Memory Using the HPI (16-Bit)

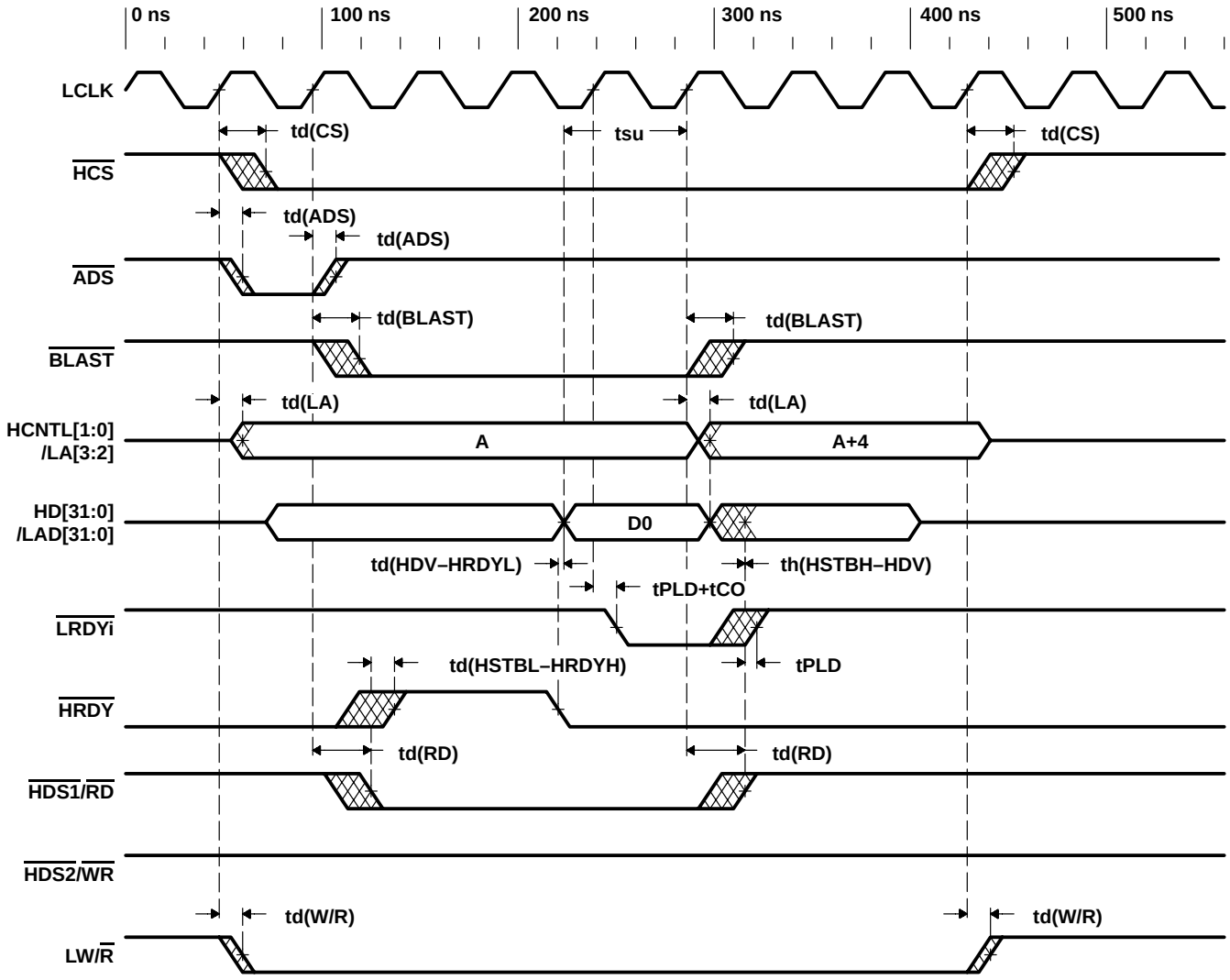


Figure 5. PCI9050 Read From TMS320C64x DSP Internal Memory Using the HPI (32-Bit)

5 References

1. *TMS320C6000 Peripherals Reference Guide*, (SPRU190).
2. See the Texas Instruments web site at www.ti.com for the TMS320C62x™, C64x, and TMS320C67x™ DSP generation devices that have HPI and their respective device-specific data sheets.
3. *TMS320C6201 Fixed-Point Digital Signal Processor* (SPRS051).
4. *TMS320C6211, TMS320C6211B Fixed-Point Digital Signal Processor* (SPRS073).
5. *TMS320C6414 Fixed-Point Digital Signal Processor* (SPRS134).
6. *TMS320C6415 Fixed-Point Digital Signal Processor* (SPRS146).
7. *TMS320C6416 Fixed-Point Digital Signal Processor* (SPRS164).
8. *TMS320C6701 Floating-Point Digital Signal Processor* (SPRS067).
9. *TMS320C6711, TMS320C6711B Floating-Point Digital Signal Processors* (SPRS088).
10. *PLX PCI9050 Datasheet*, PLX Technology, Inc.

Appendix A TMS320C6000 Timing Requirements

The timing requirements in Table A–1 are provided for quick reference only. For detailed descriptions, notes, and restrictions, see the C62x™, C64x, and/or C67x™ DSP generation device-specific data sheets.

Table A–1. Timing Requirements for TMS320C6000 HPI

		C6201 HPI (ns)†		C6211 HPI (ns)†		C64x HPI (ns)†	
Characteristic	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Pulse width of HSTROBE high between consecutive accesses	tw(HSTBH)	2 Tcyc		4 Tcyc		4 Tcyc	
Hold time, HSTROBE low after HRDY low	th(HRDY–HSTBL)	1		2		2	
Pulse width of strobe low	tw(HSTBL)	2 Tcyc		4 Tcyc		4 Tcyc	
Delay time, HCS to HRDY	td(HCS–HRDY)	1	9	1	15	1	7
Setup time, select signals valid before HSTROBE low	tsu(SEL–HSTBL)	4		5		5	
Hold time, select signals valid after HSTROBE low	th(HSTBL–SEL)	2		4		2	
Setup time, select signals valid before HAS low	tsu(SEL–HASL)	4		5		5	
Hold time, select signals valid after HDS low	th(HASL–SEL)	2		3		2	
Setup time, host data valid before HSTROBE high	tsu(HDV–HSTBH)	3		5		5	
Hold time, host data valid after strobe HSTROBE high (write)	th(HSTBH–HDV)	2		3		2	
Hold time, host data valid after HSTROBE high (HPI read)	th(HSTBH–HDV)	2		3		2	
Hold time, host data low impedance after HSTROBE low	th(HSTBL–HDLZ)	4		2		2	
Delay time, HSTROBE high to host data not driven	td(HSTBH–HDHZ)	3	12	3	15		12
Delay time, HSTROBE low to HRDY high	td(HSTBL–HRDYH)	3	12	3	15	3	12
Delay time, host data valid to HRDY low	td(HDV–HRDYL)	Tcyc – 3	Tcyc + 3	2Tcyc – 4	2Tcyc + 4	2Tcyc – 6	
Delay time, host data valid after HSTROBE low	td(HSTBL–HDV)	2	12	3	15		12
Delay time, HSTROBE high to HRDY high	td(HSTBH–HRDYH)	3	12	3	15	3	12

† Tcyc = (1/ DSP clock frequency) [ns]

C62x and C67x are trademarks of Texas Instruments.

Appendix B PCI9050 Timing Requirements

The timing requirements in Table B–1 are provided for quick reference only. For detailed descriptions, notes, and restrictions, see *PLX PCI9050 Datasheet*.

Table B–1. Timing Requirements for PCI9050

Characteristic	Symbol	Min (ns)	Max (ns)
Local bus address strobe	td(ADS)	3	10
Local bus burst last signal	td(BLAST)	5	16
Local bus address	td(LA)	5	14
Local bus data	td(LAD)	5	16
Local bus byte enables	td(LBE)	4	15
Local bus write control signal	td(WR)	4	13
Local bus read control signal	td(RD)	7	27
Local bus W/R_ control signal	td(W/R)	4	12
Local bus input setup time	Tsu		8
Local bus input hold time	Th	2	

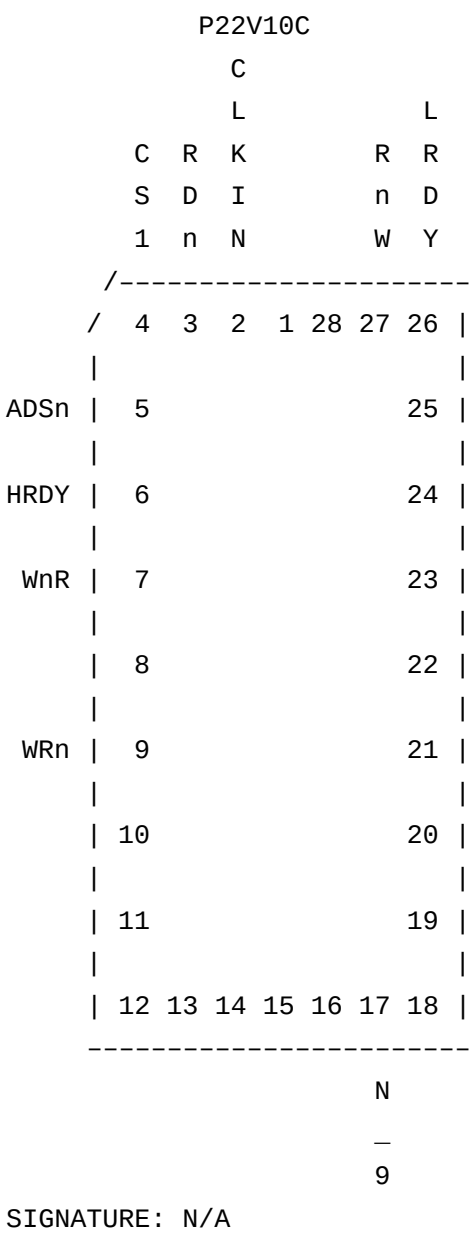
Appendix C PAL Equations

```
                                                                        Page 1
Synario 3.10  –  Device Utilization Chart         Tue May 11 11:43:14 1999
9050.bls
--------------------------------------------------------------------------------
Module                    : 'pci9050'
--------------------------------------------------------------------------------
Input files:
    ABEL PLA file         : pci9050.tt3
    Device library        : P22V10C.dev
Output files:
    Report file           : pci9050.rep
    Programmer load file  : pci9050.jed
--------------------------------------------------------------------------------
```

```
                                                                        Page 2
Synario 3.10  –  Device Utilization Chart         Tue May 11 11:43:14 1999
9050.bls
P22V10C Programmed Logic:
--------------------------------------------------------------------------------
LRDY     = (  N_9.Q
            #   RDn & WRn );
N_9.D    = (  CS1
           #   !ADSn
           #   HRDY ); ” ISTYPE ’INVERT’
N_9.C    = (  CLKIN );
RnW      = (  !WnR );
```

Synario 3.10 – Device Utilization Chart Tue May 11 11:43:14 1999
9050.bls

P22V10C Chip Diagram:



SIGNATURE: N/A

Synario 3.10 – Device Utilization Chart Tue May 11 11:43:14 1999
9050.bls
P22V10C Resource Allocations:

Device Resources	Resource Available	Design Requirement	Unused
Input Pins:			
Input:	12	7	5 (41 %)
Output Pins:			
In/Out:	10	3	7 (70 %)
Output:	–	–	–
Buried Nodes:			
Input Reg:	–	–	–
Pin Reg:	10	1	9 (90 %)
Buried Reg:	–	–	–

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Synario 3.10 – Device Utilization Chart Tue May 11 11:43:14 1999
9050.bls

P22V10C Product Terms Distribution:

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
LRDY	26	2	10	8
N_9.D	17	3	8	5
RnW	27	1	8	7

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
CLKIN	2	CLK/IN
RDn	3	INPUT
CS1	4	INPUT
ADSn	5	INPUT
HRDY	6	INPUT
WnR	7	INPUT
WRn	9	INPUT

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Synario 3.10 – Device Utilization Chart Tue May 11 11:43:14 1999
9050.bls

P22V10C Unused Resources:

Pin Number	Pin Type	Product Terms	Flip–flop Type
10	INPUT	–	–
11	INPUT	–	–
12	INPUT	–	–
13	INPUT	–	–
16	INPUT	–	–
18	BIDIR	NORMAL 10	D
19	BIDIR	NORMAL 12	D
20	BIDIR	NORMAL 14	D
21	BIDIR	NORMAL 16	D
23	BIDIR	NORMAL 16	D
24	BIDIR	NORMAL 14	D
25	BIDIR	NORMAL 12	D

```
                                                                        Page 7
Synario 3.10  –  Device Utilization Chart         Tue May 11 11:43:14 1999
9050.bls
P22V10C Fuse Map:
--------------------------------------------------------------------------------
       0          10         20          30          40
   44: ---------- ---------- ---------- ---------- ----
   88: ---------- ---------- -X-------- ---------- ----
  440: ---------- ---------- ---------- ---------- ----
  484: ---------- ---------- ---------- ---------X ----
  528: ----X----- ---------- ----X----- ---------- ----
 5368: ---------- ---------- ---------- ---------- ----
 5412: --------X- ---------- ---------- ---------- ----
 5456: ---------- ---X------ ---------- ---------- ----
 5500: ---------- ------X--- ---------- ---------- ----
       0          10
 5808: ----XXXXXX XXXXXXXXXX
```

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