Application Report
SPRA536B - September 2003

TMS320C6000 EMIF to TMS320C6000 Host Port Interface

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ABSTRACT

This application report describes the interface between the host port interface (HPI) and the external memory interface (EMIF) of the TMS320C6000™ digital signal processor (DSP). This report examines three possible pairings of the various TMS320C6000 devices: TMS320C6201/C6701 EMIF to TMS320C6201/C6701 HPI, TMS320C6211C/C6711 EMIF to TMS320C6211/C6711 HPI, and TMS320C64x™ EMIF to TMS320C64x HPI.

This document includes schematics showing connections between the two devices for each configuration and verification that timing requirements are met for each device (tables and timing diagrams).

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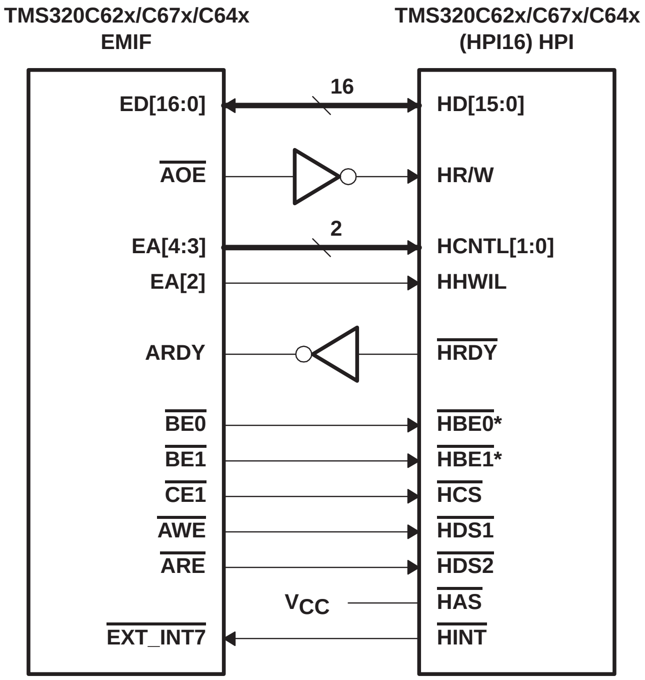
List of Tables

1 Interface Description

Figure 1 and Figure 2 show diagrams of the EMIF interface to the HPI for the TMS320C6201/C6701/C6211/C6711/C64x™ devices. Table 1 describes the pin connections in more detail.

C64x is a trademark of Texas Instruments.



* TMS320C6201/C6701 only

Figure 1. TMS320C62x/C67x/C64x (HPI16) EMIF to HPI Interface Block Diagram

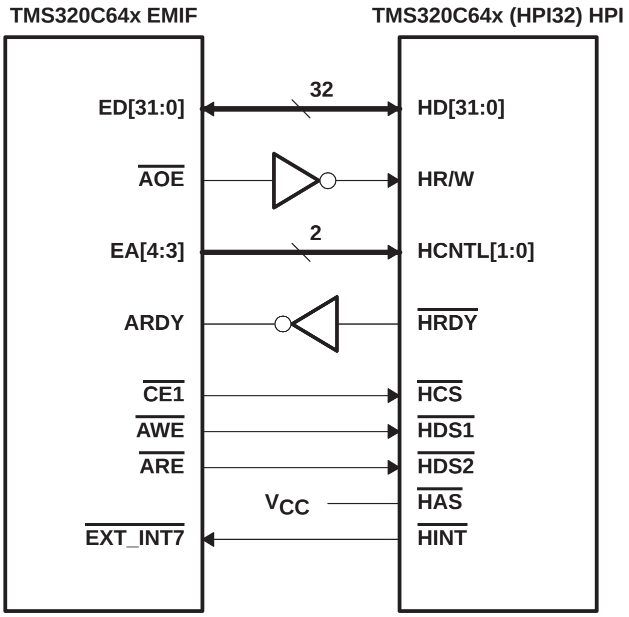


Figure 2. TMS320C64x (HPI32) EMIF to HPI Interface Block Diagram

Table 1. EMIF-to-HPI Pin Connections

HPI Pin	EMIF Pin	Comments
HCNTL[1:0	EA[4:3]	EA[4:3] control HPI access type
HHWIL	EA2	EA2 identifies the first or second half-word of transfer.
HR/$\overline{\text{W}}$	Externally inverted $\overline{\text{AOE}}$	Output-enable ($\overline{\text{AOE}}$) line is inverted and connected to HR/$\overline{\text{W}}$, to decode reads and writes.
HD[15:0]	ED[15:0]	16 LSBs of data
HD[31:16]	ED[31:16]	16 MSBs of data (used only for TMS320C64x HPI32 mode)
$\overline{\text{HDS1}}$	$\overline{\text{AWE}}$	Because the EMIF asynchronous interface has separate read and write strobes that are by nature mutually exclusive, they are tied to HDS1 and HDS2.
$\overline{\text{HDS2}}$	$\overline{\text{ARE}}$	See above.
$\overline{\text{HAS}}$	Vcc	Unused
$\overline{\text{HCS}}$	$\overline{\text{CE1}}$	CE1 is arbitrarily chosen from CE[0:3].
$\overline{\text{HBE0}}$	$\overline{\text{BE1}}$	C6201/C6701 HPI uses this value on writes only. C6211/C6711/C64x does not have this signal.
$\overline{\text{HBE1}}$	$\overline{\text{BE2}}$	C6201/C6701 HPI uses this value on writes only. C6211/C6711/C64x does not have this signal.
$\overline{\text{HRDY}}$	ARDY	Asynchronous ready input.
$\overline{\text{HINT}}$	$\overline{\text{EXT\_INT7}}$	$\overline{\text{EXT\_INT7}}$ is arbitrarily chosen from external interrupts INT7:4

NOTE: The EA2 line is equivalent to logical addresses A2, and the EA[4:3] lines correspond to A[4:3].

2 HPI Configuration

The TMS320C64x HPI supports either a 16-bit or 32-bit external pin interface. The C64x HPI is called the HPI16 when operating as a 16-bit-wide host port, and it is called the HPI32 when operating as a 32-bit-wide host port. HPI16 or HPI32 is selected via the HPI data pin HD5 at reset. HPI16 is selected when this pin is set to 0 at reset, and HPI32 is selected when this pin is set to 1. **If HPI16 is selected, HWOB in the HPIC register must be set to 1. This is because the EMIF performs transfers with the least significant half word first.**

When possible, HPI32 should be selected to increase the throughput of the HPI. All TMS320C62x/C67x HPIs support only 16-bit transfers with the HHWIL input indicating which half-word is currently being transferred. The address mapping for HPI transfers is shown in Table 2.

Table 2. EMIF-to-HPI Interface Host Memory Mapping (CE1 Memory Space of Host is Configured as an Asychronous Memory)

TMS320C6000 Host Address Little-Endian				HPI Action	
Host Address (Map 0)	EA4 (HCNTL1)	EA3 (HCNTL0)	EA2 (HHWIL)	16-bit transfers	HPI32
0100 0000	0	0	0	HPIC read/write 1st half-word	HPIC read/write
0100 0004	0	0	1	HPIC read/write 2nd half-word	
0100 0008	0	1	0	HPIA read/write 1st half-word	HPIA read/write
0100 000c	0	1	1	HPIA read/write 2nd half-word	
0100 0010	1	0	0	HPID read/write 1st half-word with auto-increment	HPID read/write with auto-increment
0100 0014	1	0	1	HPID read/write 2nd half-word with auto-increment	
0100 0018	1	1	0	HPID read/write 1st half-word without auto-increment	HPID read/write without auto-increment
0100 001c	1	1	1	HPID read/write 2nd half-word without auto-increment	

3 Host EMIF Configuration

For the TMS320C64x devices, either EMIFA (64-bit bus) or EMIFB (16-bit bus) may be used to interface with the HPI. For instance, EMIFB may be interfaced with the HPI in HPI16 mode to free the 64-bit EMIFA bus for other uses. For all configurations, the HPI may be mapped to the CE1 memory space of the host. The CE1 Space Control Register contains the EMIF asynchronous timing parameters: Setup, Strobe, and Hold times. Table 3 shows the recommended values for each of the three EMIF-to-HPI configurations.

Table 3. Setup, Strobe, and Hold Settings

Configuration	Read Setup	Read Strobe	Read Hold	Write Setup	Write Strobe	Write Hold
TMS320C6201/C6701 EMIF to TMS320C6201/C6701 HPI	2	6	1	2	3	2
TMS320C6211/C6711 EMIF to TMS320C6211/C6711 HPI	2	4	2	2	4	2
TMS320C64x EMIF to TMS320C64x HPI	2	4	1	1	3	1

Table 4 through Table 7 show how to configure the CE1 space control register to the correct Setup, Strobe, and Hold values. In addition, the CE1 memory space of the host is configured as a 32-bit-wide asynchronous interface for both the TMS320C6201/C6701 and TMS32064x (HPI32 mode) devices by setting the MTYPE field equal to 2. For the TMS 320C6211/C6711 and TMS32064x (HPI16 mode), the CE1 memory space of the host is configured as a 16-bit-wide asynchronous interface by setting the MTYPE field equal to 1. Because the TMS320C6201/C6701 EMIF has its CE1 memory space configured to 32 bits wide, the upper 16 bits of each transfer must be discarded because the TMS320C6201/C6701 HPI supports only a 16-bit interface.

Table 4. TMS320C6201/C6701 EMIF CE1 Space Control Register

Write setup				Write strobe						Write hold		Read setup			
31			28	27					22	21	20	19			16
0	0	1	0	0	0	0	0	1	1	1	0	0	0	1	0

rsv		Read Strobe						rsv	MTYPE			rsv		Read hold	
15	14	13					8	7	6		4	3	2	1	0
X	X	0	0	0	1	1	0	X	0	1	0	X	X	0	1

Table 5. TMS320C6211/C6711 EMIF CE1 Space Control Register

Write setup				Write strobe						Write hold		Read setup			
31			28	27					22	21	20	19			16
0	0	1	0	0	0	0	1	0	0	1	0	0	0	1	0

TA		Read Strobe						MTYPE				rsv		Read hold	
15	14	13					8	7	6		4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	0	1	X	X	1	0

Table 6. TMS320C6211/C64x EMIF CE1 Space Control Register (HPI32)

Write setup				Write strobe						Write hold		Read setup			
31			28	27					22	21	20	19			16
0	0	0	1	0	0	0	0	1	1	0	1	0	0	1	0

rsv		Read Strobe						MTYPE				Write hold MSB		Read hold	
15	14	13					8	7	6		4	3	2	1	0
X	X	0	0	0	1	0	0	0	0	1	0	0	1	0	1

Table 7. TMS320C6211/C64x EMIF CE1 Space Control Register (HPI16)

Write setup				Write strobe						Write hold		Read setup			
31			28	27					22	21	20	19			16
0	0	0	1	0	0	0	0	1	1	0	1	0	0	1	0

rsv		Read Strobe						MTYPE				Write hold MSB		Read hold	
15	14	13					8	7	6		4	3	2	1	0
X	X	0	0	0	1	0	0	0	0	0	1	0	1	0	1

4 Interrupts

Any external interrupt can be connected to the HINT pin of the HPI. In this report, EXT_INT7 is chosen arbitrarily as an example. In addition, the external interrupt polarity register allows you to change the polarity of the four external interrupts (EXT_INT4−EXT_INT7). By setting the related XIP bit in this register to 1, the CPU recognizes a high-to-low transition as signaling an interrupt.

5 EMIF-to-HPI Timing Verification

To verify proper operation of each configuration, two functions have been examined: 1) an EMIF write to HPI and 2) an EMIF read from HPI. In all instances, timing requirements were compared for each of the devices. The results are shown in the following tables and timing diagrams.

The reads and writes presented in Figures 3−10 are parts of burst transfers performed by the DMA channel.

In Figures 3−10, timing parameters are named in the same way as those in the data sheets that are referenced at the end of this document. Actual timing-parameter values are also listed in Appendix A for quick access.

The tables and timing diagrams presented show that the timing parameters for both devices are met in the interface of the EMIF and HPI for each of the configurations.

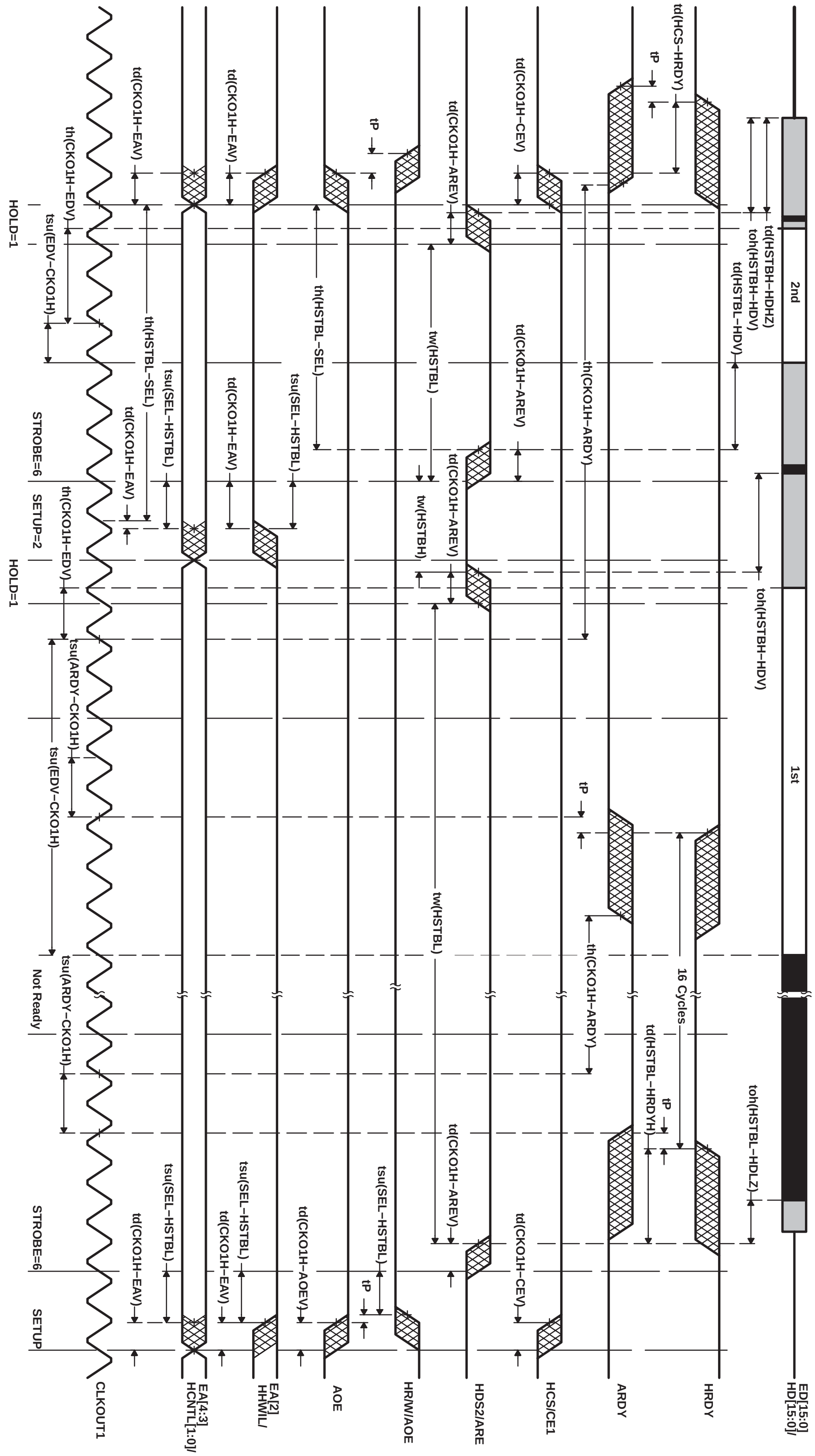


Figure 3. Master TMS320C6201/C6701 EMIF Reads Internal Memory of Slave TMS320C6201/6701 Using HPI (Read Without Auto-Increment)

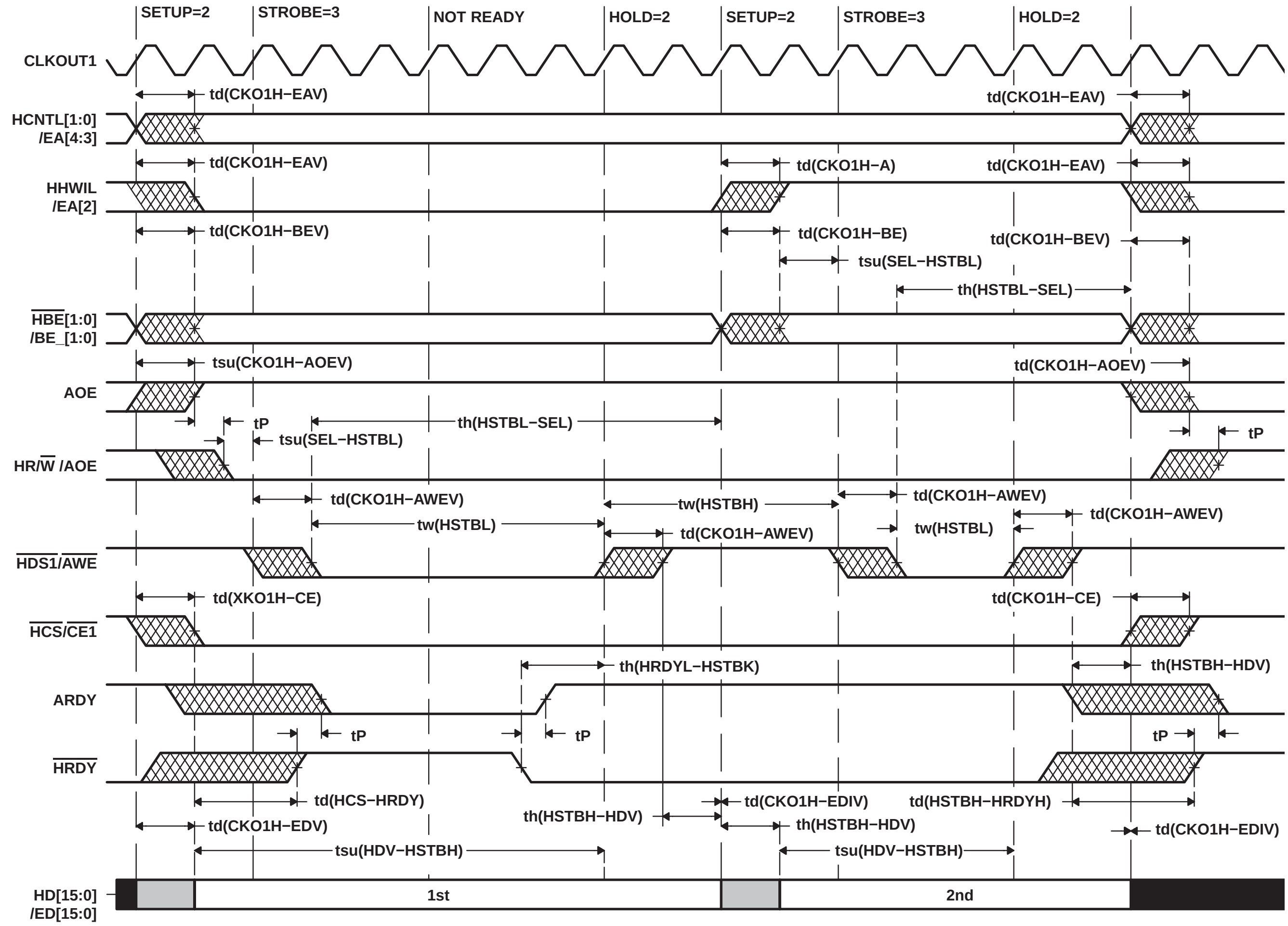


Figure 4. Master TMS320C6201/C6701 EMIF Writes to Internal Memory of Slave TMS320C6201/C6701 Using HPI

Table 8. Timing Requirements for the C6201/C6701 HPI

HPI Symbol	EMIF Symbol	Parameter	Min HPI (ns)	Min EMIF (ns)
t_{su}(SEL−HSTBL)	SETUP*P – Max[t_d(CKO1H−AOEV)] – tP + Min[t_d(CKO1H−AREV)]	Setup time, Select signals valid before HSTROBE low	4	4
t_h(HSTBL−SEL)	(HOLD + STROBE)*P − Max[td(CKO1H−AREV)]	Hold time, select signals valid after HSTROBE low	2	31
t_w(HSTBL)	STROBE*P – Max[t_d(CKO1H−AREV)] + Min[t_d(CKO1H−AREV)]	Pulse Duration, HSTROBE low	2*P=10	10.8
t_w(HSTBH)	(SETUP + HOLD)*P − Max[t_d(CKO1H−AREV)] + Min[t_d(CKO1H−AREV)]	Pulse Duration, HSTROBE high	2*P=10	10.8
t_{su}(HDV−HSTBH)	(STROBE + SETUP)*P − Max[t_d(CKO1H−EDV)] + Min[t_d(CKO1H−AWEV)]	Setup time, host data valid before HSTROBE high	3	20.8
t_h(HSTBH−HDV)	HOLD*P + Min[t_d(CKO1H−EDIV)] − Max[t_d(CKO1H−AWEV)]	Hold time, host data valid after HSTROBE high	2	5.8
t_h(HRDYL−HSTBL)	P + tP	Hold time, HSTROBE low after HRDY low	1	6.8

NOTES: 1. The time required for an edge to propagate through an inverter is represented as tP.
NOTES: 2. P = 5ns @ 200 MHz. P denotes the CPU cycle time.
NOTES: 3. Read: SETUP = 2, STROBE = 6, HOLD = 1 Write: SETUP = 2, STROBE = 3, HOLD = 2

Table 9. Timing Requirements for the C6201/C6701 EMIF

HPI Symbol	EMIF Symbol	Parameter	Min HPI (ns)	Min EMIF (ns)
STROBE*P – t_d(CKO1H−AREV) – t_d(HSTBL−HDV)	t_{su}(EDV−CKO1H)	Setup time, read EDx valid before CLKOUT1 high	14	4
t_d(CKO1H−AREV) + t_{oh}(HSTBH−HDV)	t_h(CKO1H−EDV)	Hold time, read EDx valid after CLKOUT1 high	1.8	0.8
(STROBE + HOLD + SETUP)*P	t_h(CKO1H−ARDY)	Hold time, ARDY valid after CLKOUT1 high	40	1.8

NOTES: 4. P = 5ns @ 200 MHz. P denotes the CPU cycle time.
NOTES: 5. Read: SETUP = 2, STROBE = 6, HOLD = 1 Write: SETUP = 2, STROBE = 3, HOLD = 2

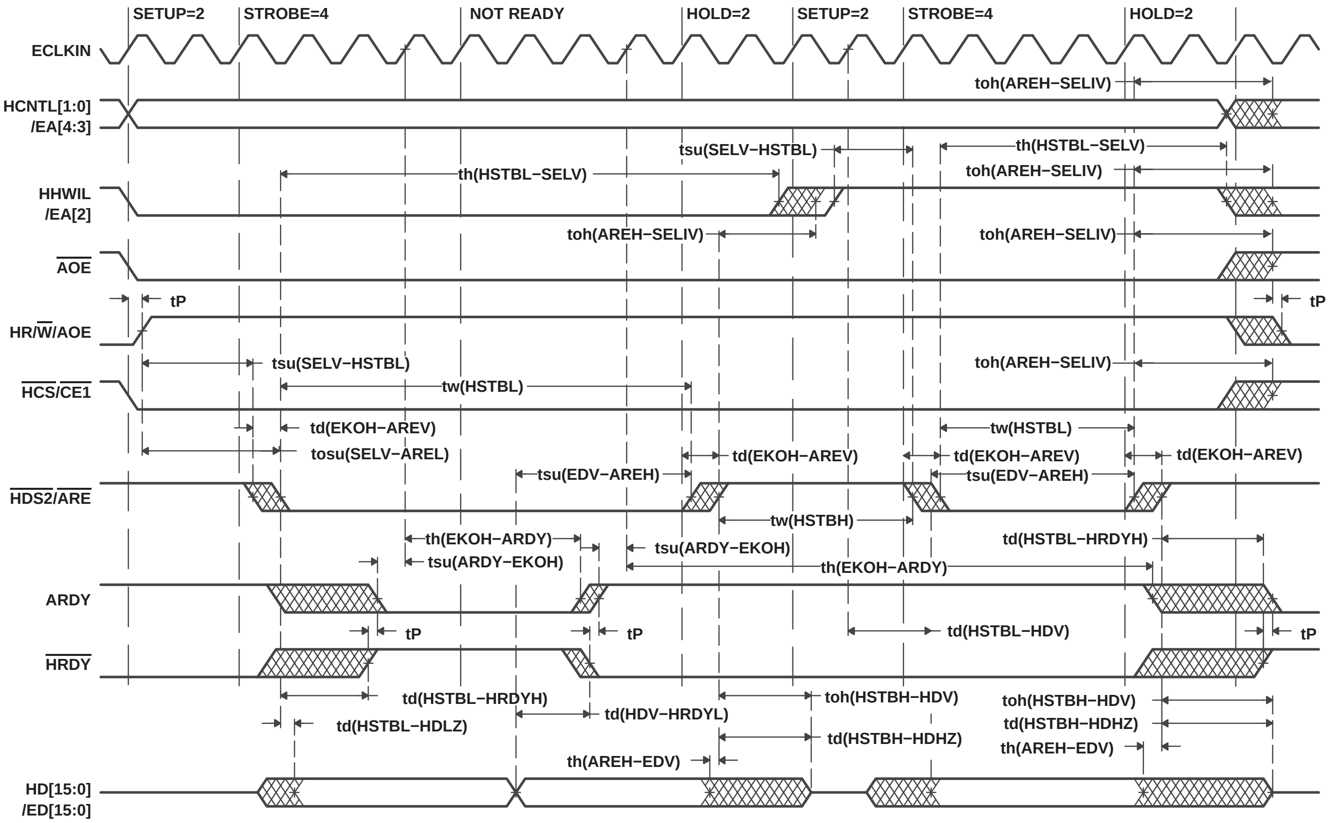


Figure 5. Master TMS320C6211/C6711 EMIF Reads Internal Memory of Slave TMS320C6211/C6711 Using HPI (Read Without Auto-Increment)

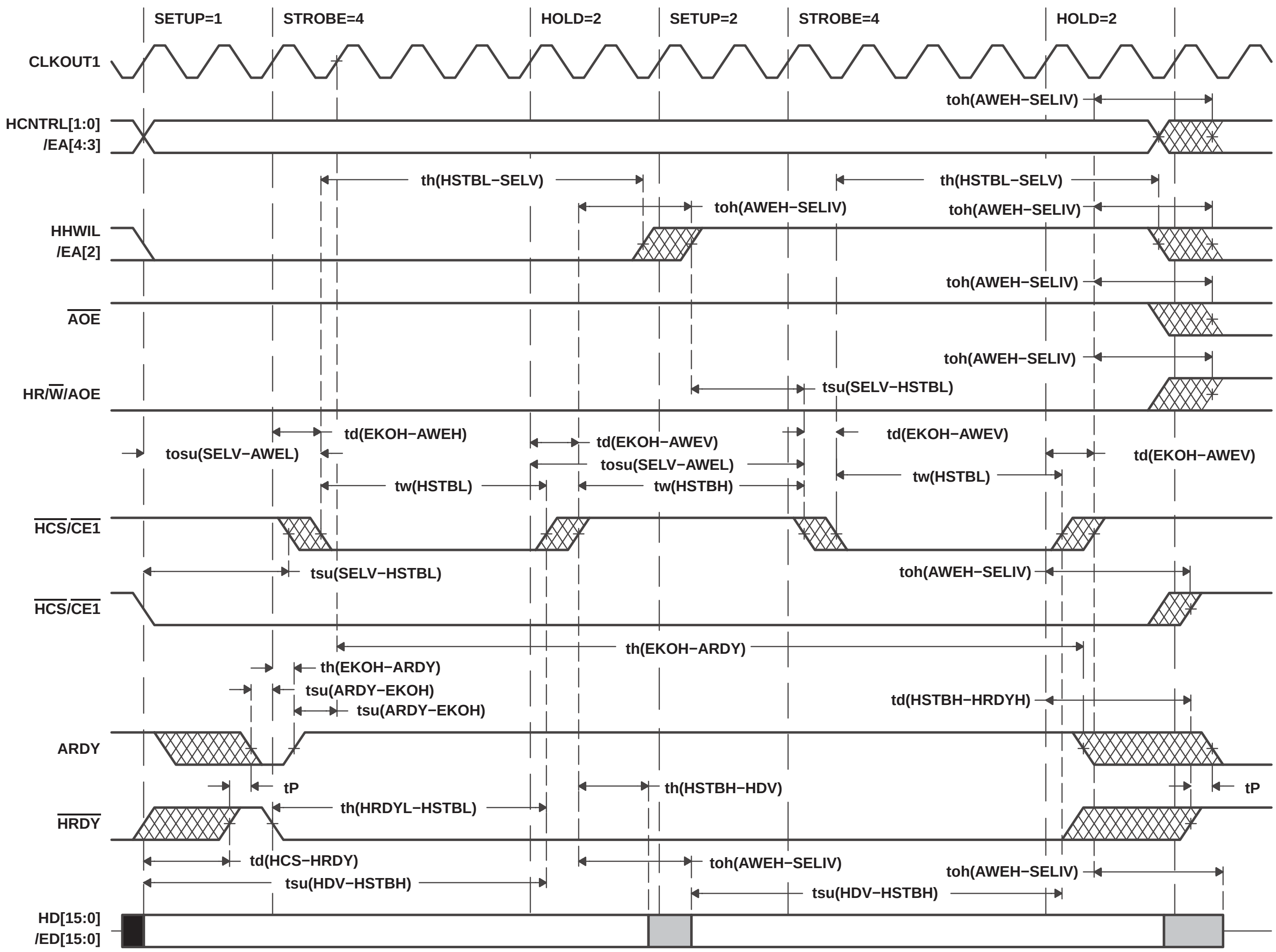


Figure 6. Master TMS320C6211/C6711 EMIF Writes to Internal Memory of Slave TMS320C6211/C6711 Using HPI

Table 10. Timing Requirements for the C6211/C6711 HPI

HPI Symbol	EMIF Symbol	Parameter	Min HPI (ns)	Min EMIF (ns)
t_{su}(SELV−HSTBL)	R°: (SETUP*E) + Min[t_d(EKOH−AREV)] – tP W°: (SETUP*E) + Min[t_d(EKOH−AREV)]	Setup time, Select signals valid before HSTROBE low	5	19.7
t_h(HSTBL−SELV)	STROBE*E – Max[td(EKOH−AREV)] +Min[td(EKOH−AREV)] +Min[toh(AREH−SELIV)]	Hold time, select signals valid after HSTROBE low	4	63.5
t_w(HSTBL)	STROBE*E – Max[$t_{d(}$EKOH−AREV)] + Min[t_d(EKOH−AREV)]	Pulse Duration, HSTROBE low	4*P=26.67	33.5
t_w(HSTBH)	(SETUP + HOLD)*E− Max[t_d(EKOH−AREV)]+ Min[$t_{d(}$EKOH−AREV)]	Pulse Duration, HSTROBE high	4*P=26.67	33.5
t_{su}(HDV−HSTBH)	(STROBE + SETUP)*E + Min[t_d(EKOH−AWEV)]	Setup time, host data valid before HSTROBE high	5	61.5
t_h(HSTBH−HDV)	Min[t_{oh}(AWEH−SELIV)]	Hold time, host data valid after HSTROBE high	3	17
t_h(HRDYL−HSTBL)	E + Min[t_d(EKOH−AWEV)]	Hold time, HSTROBE low after HRDY low	2	11.5

NOTES: 1. P = 6.67ns @ 150 MHz. E = 10ns @ 100 MHz.
NOTES: 2. E denotes the cycle time of ECLKIN. P denotes the CPU cycle time. The time required for an edge to propagate through an inverter is represented as tP.
NOTES: 3. ° R denotes a read access. W denotes a write access.
NOTES: 4. Read: SETUP = 2, STROBE = 4, HOLD = 2 Write: SETUP = 2, STROBE = 4, HOLD = 2

Table 11. Timing Requirements for the C6211/C6711 EMIF

HPI Symbol	EMIF Symbol	Parameter	Min HPI (ns)	Min EMIF (ns)
Min[t_d(HDV−HRDYL)] + tP + E	t_{su}(EDV−AREH)	Setup time, read EDx valid before ARE high	21.13 @ 150 MHz	9
Min[t_{oh}(HSTBH−HDV)]	t_h(AREH−EDV)	Hold time, read EDx valid after ARE high	3	1
Min[t_d(HDV−HRDYL)] + tP	t_h(EKOH−ARDY)	Hold time, ARDY valid after ECLKOUT high	11.13	1

NOTES: 1. E = 10ns @ 100 MHz. E denotes the cycle time of ECLKIN.
NOTES: 2. Read: SETUP = 2, STROBE = 4, HOLD = 2 Write: SETUP = 2, STROBE =4, HOLD = 2

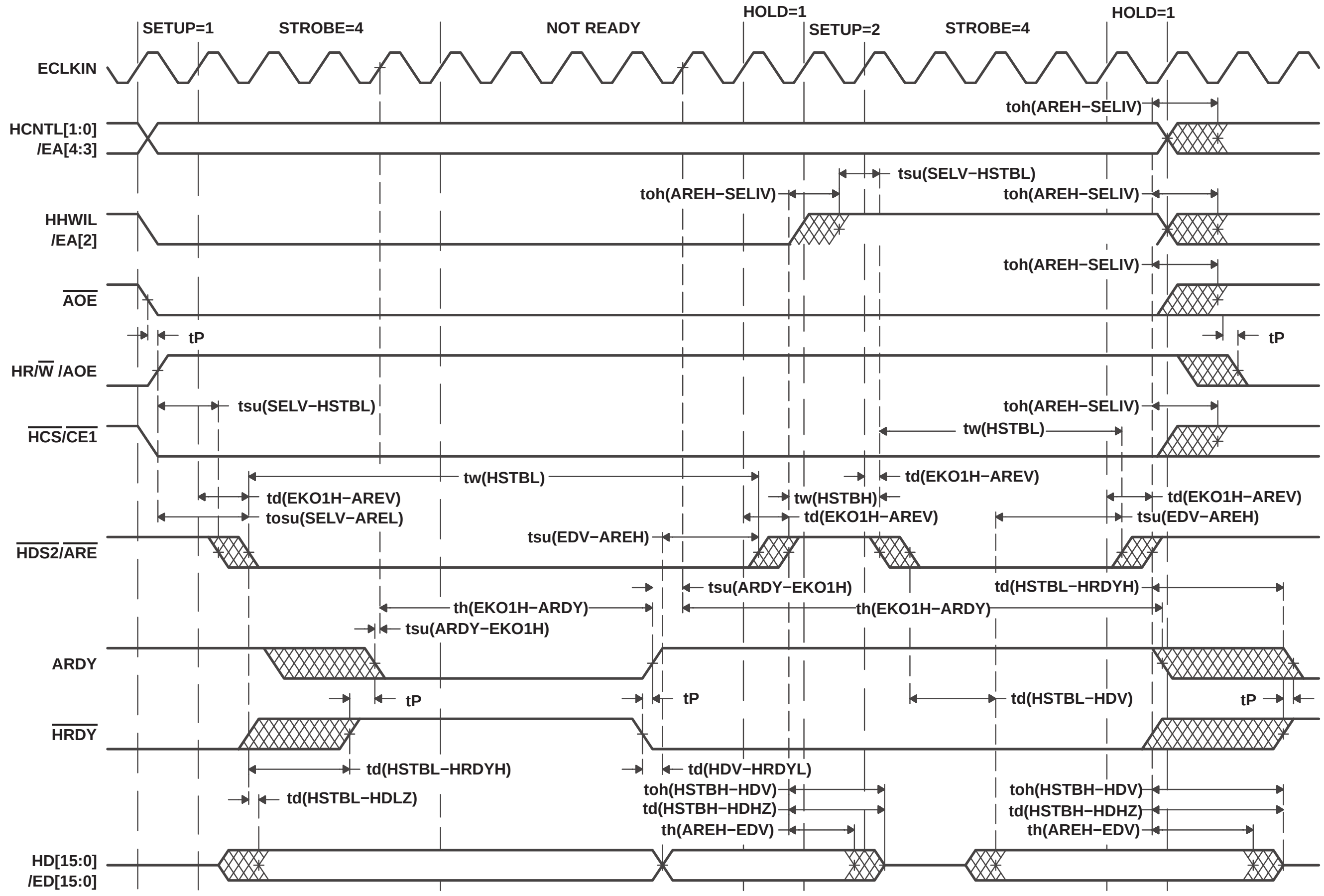


Figure 7. Master TMS320C64x EMIF Reads to Internal Memory of Slave TMS320C64x Using HPI (Read Without Auto-Increment, HPI16 Mode)

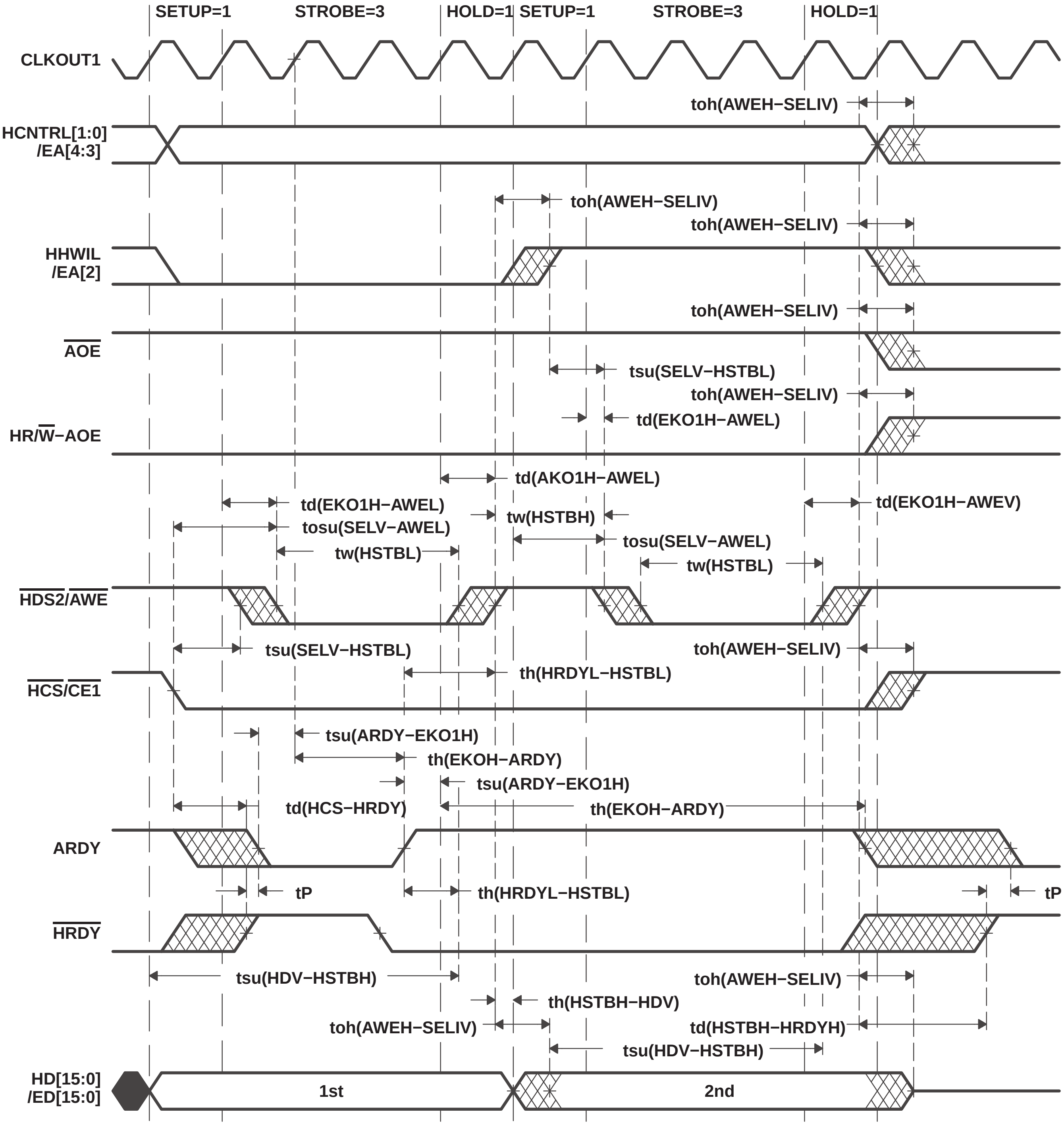


Figure 8. Master TMS320C64x EMIF Writes to Internal Memory of Slave TMS320C64x Using HPI (HPI16 Mode)

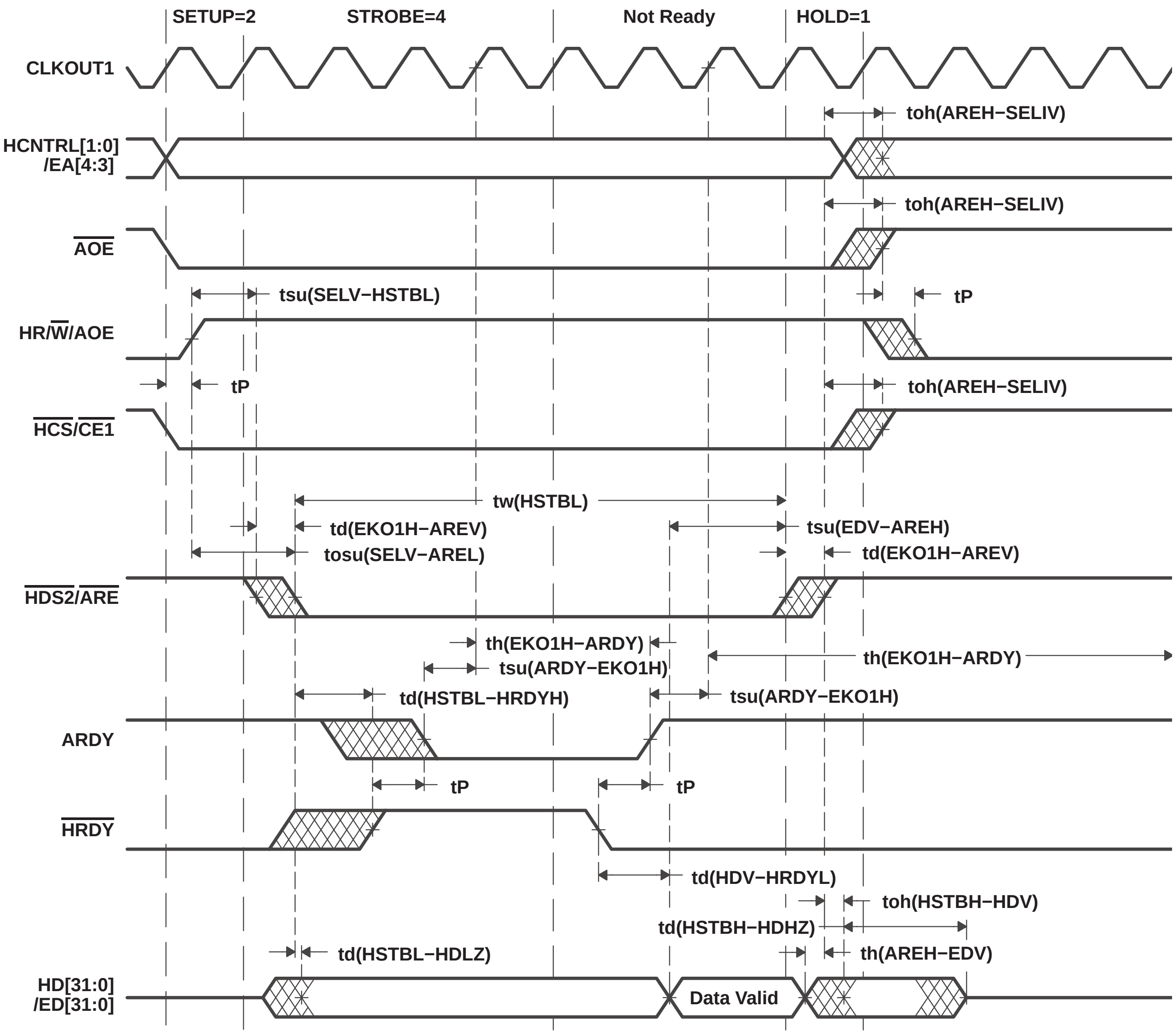


Figure 9. Master TMS320C64x EMIF Reads to Internal Memory of Slave TMS320C64x

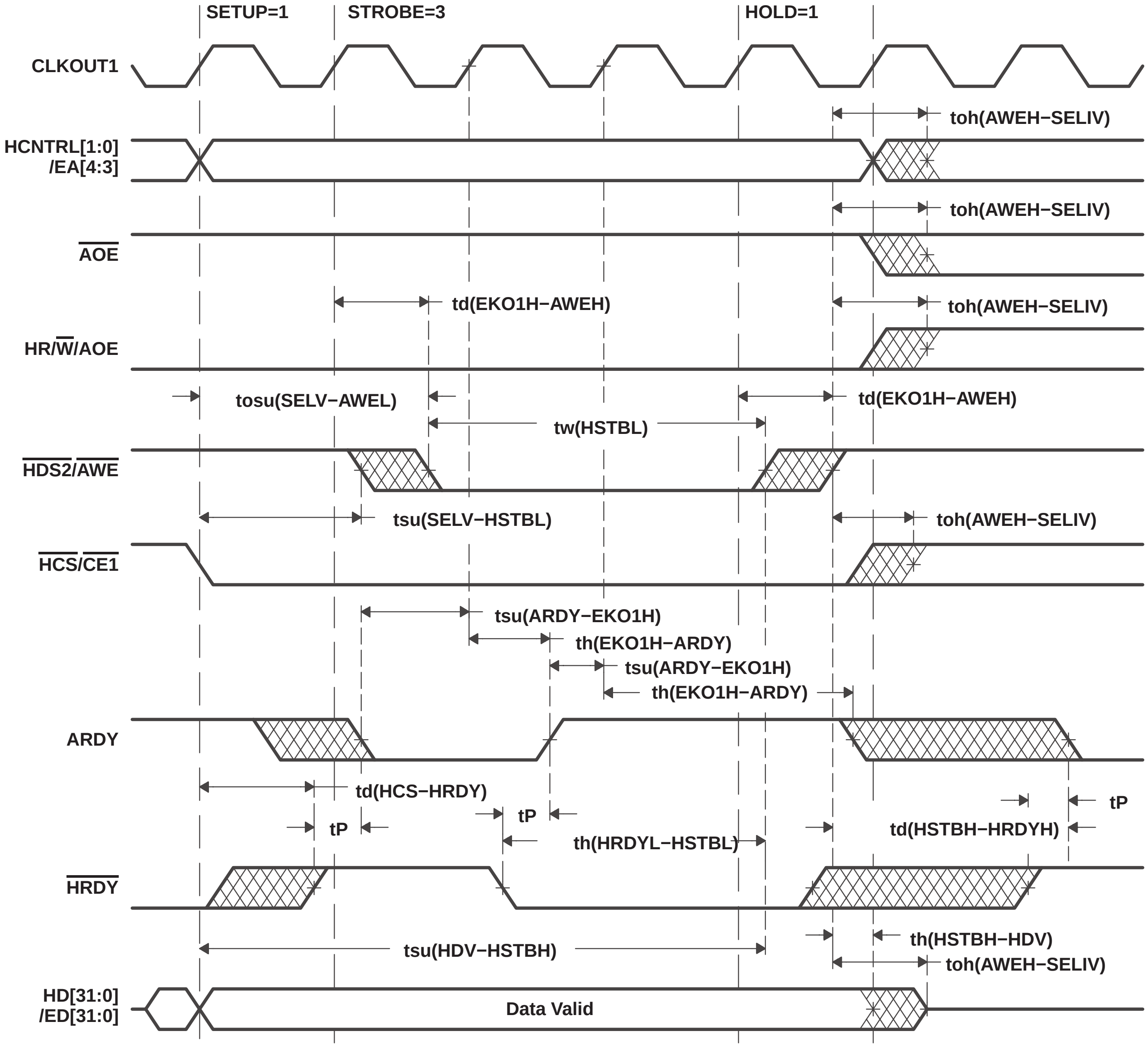


Figure 10. Master TMS320C64x EMIF Writes to Internal Memory of Slave TMS320C64x Using HPI (HPI32 Mode)

Table 12. Timing Requirements for the C64x HPI

HPI Symbol	EMIF Symbol	Parameter	Min HPI (ns)	Min EMIF (ns)
t_{su}(SELV−HSTBL)	R°: (SETUP*E) + Min[t_d(EKO1H−AREV)] – tP W°: (SETUP*E) + Min[t_d(EKO1H−AREV)]	Setup time, Select signals valid before HSTROBE low	5	9
t_h(HSTBL−SELV)	STROBE*E – Max[td(EKOH−AREV)] + Min[td(EKOH−AREV)] +Min[toh(AREH−SELIV)]	Hold time, select signals valid after HSTROBE low	2	22
t_w(HSTBL)	STROBE*E – Max[$t_{d(}$EKO1H−AREV)] + Min[t_d(EKO1H−AREV)]	Pulse Duration, HSTROBE low	4*P=10	19
t_w(HSTBH)	(SETUP + HOLD)*E − Max[t_d(EKO1H−AREV)] + Min[$t_{d(}$EKO1H−AREV)]	Pulse Duration, HSTROBE high	4*P=10	11.5
t_{su}(HDV−HSTBH)	(STROBE + SETUP)*E + Min[t_d(EKO1H−AWEV)]	Setup time, host data valid before HSTROBE high	5	31.5
t_h(HSTBH−HDV)	Min[t_{oh}(AWEH−SELIV)]	Hold time, host data valid after HSTROBE high	2	6
t_h(HRDYL−HSTBL)	E + Min[t_d(EKO1H−AWEV)]	Hold time, HSTROBE low after HRDY low	2	9

NOTES: 1. P = 2.5ns @ 400 MHz. E = 7.5ns @ 133 MHz.
NOTES: 2. E denotes the cycle time of ECLKIN. P denotes the CPU cycle time. The time required for an edge to propagate through an inverter is represented as tP.
NOTES: 3. ° R denotes a read access, W denotes a write access.
NOTES: 4. Read: SETUP = 2, STROBE = 4, HOLD = 1 Write: SETUP = 1, STROBE = 3, HOLD = 1
NOTE: The timing specifications above are preliminary, and the actual numbers may vary with a TMS part. Please refer to latest data sheet for numbers.

Table 13. Timing Requirements for the C64x EMIF

HPI Symbol	EMIF Symbol	Parameter	Min HPI (ns)	Min EMIF (ns)
Min[t_d(HDV−HRDYL)] + tP + E	t_{su}(EDV−AREH)	Setup time, read EDx valid before ARE high	6.63 @ 600 MHz	6
Min[t_{oh}(HSTBH−HDV)]	t_h(AREH−EDV)	Hold time, read EDx valid after ARE high	3	1
Min[t_d(HDV−HRDYL)] + tP	t_h(EKO1H−ARDY)	Hold time, ARDY valid after ECLKOUT1 high	10.8	1

NOTES: 1. E = 7.5ns @ 133 MHz. E denotes the cycle time of ECLKIN.
NOTES: 2. Read: SETUP = 2, STROBE = 4, HOLD = 1 Write: SETUP = 1, STROBE = 3, HOLD = 1
NOTE: The timing specifications above are preliminary, and the actual numbers may vary with a TMS part. Please refer to latest data sheet for numbers.

6 References

1. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
2. *TMS320C6201 Digital Signal Processor* (SPRS051).
3. *TMS320C6701 Floating-Point DSP* (SPRS067).
4. *TMS320C6211, TMS320C6211B Fixed-Point DSPs* (SPRS073).
5. *TMS320C6416 Fixed-Point Digital Signal Processor* (SPRS164).

Appendix A Timing Requirements

Table A−1. TMS320C6201/C6701 Host Port Timing Specifications

Characteristic	Symbol	Min (ns)	Max (ns)
Setup time, select signals§ valid before HSTROBE† low	t_{su}(SEL-HSTBL)	4	
Hold time, select signals§ valid after HSTROBE† low	t_h(HSTBL-SEL)	2	
Pulse duration, HSTROBE† low	t_w(HSTBL)	2P‡	
Pulse duration, HSTROBE† high between consecutive accesses	t_w(HSTBH)	2P‡	
Setup time, host data valid before HSTROBE† high	t_{su}(HDV-HSTBH)	3	
Hold time, host data valid after HSTROBE† high	t_h(HSTBH-HDV)	2	
Hold time, HSTROBE† low after HRDY low. HSTROBE† should not be inactivated until HRDY is active (low); otherwise, HPI writes will not complete properly.	t_h(HRDYL-HSTBL)	1	
Delay time, HCS to HRDY¶	t_d(HCS-HRDY)	1	9
Delay time, HSTROBE† low to HRDY high#	t_d(HSTBL-HRDYH)	3	12
Output hold time, HD low impedance after HSTROBE† low for an HPI read	t_{oh}(HSTBL-HDLZ)	4	
Delay time, HD valid to HRDY low	t_d(HDV-HRDYL)	P‡ – 3	P‡ + 3
Output hold time, HD valid after HSTROBE† high	t_{oh}(HSTBH-HDV)	2	12
Delay time, HSTROBE† high to HD high impedance	t_d(HSTBH-HDHZ)	3	12
Delay time, HSTROBE† low to HD valid	t_d(HSTBL-HDV)	3	12
Delay time, HSTROBE† high to HRDY high‖	t_d(HSTBH-HRDYH)	3	12

† HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.
‡ P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.
§ Select signals include: HCNTRL[1:0], HR/W, and HHWIL.
¶ HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.
# This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.
‖ This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.

Table A−2. TMS320C6201/C6701 EMIF Timing Specifications

Characteristic	Symbol	Min (ns)	Max (ns)
Setup time, read EDx valid before CLKOUT1 high	t_{su}(EDV-CKO1H)	4	
Hold time, read EDx valid after CLKOUT1 high	t_{h}(CKO1H-EDV)	0.8	
Setup time, ARDY valid before CLKOUT1 high	t_{su}(ARDY-CKO1H)	3.0	
Hold time, ARDY valid after CLKOUT1 high	t_{h}(CKO1H-ARDY)	1.8	
Delay time, CLKOUT1 high to CEx valid	t_{d}(CKO1H-CEV)	−0.2	4.0
Delay time, CLKOUT1 high to BEx valid	t_{d}(CKO1H-BEV)		4.0
Delay time, CLKOUT1 high to BEx invalid	t_{d}(CKO1H-BEIV)	−0.2	
Delay time, CLKOUT1 high to EAx valid	t_{d}(CKO1H-EAV)		4.0
Delay time, CLKOUT1 high to EAx invalid	t_{d}(CKO1H-EAIV)	−0.2	
Delay time, CLKOUT1 high to AOE valid	t_{d}(CKO1H-AOEV)	−0.2	4.0
Delay time, CLKOUT1 high to ARE valid	t_{d}(CKO1H-AREV)	−0.2	4.0
Delay time, CLKOUT1 high to EDx valid	t_{d}(CKO1H-EDV)		4.0
Delay time, CLKOUT1 high to EDx invalid	t_{d}(CKO1H-EDIV)	−0.2	
Delay time, CLKOUT1 high to AWE valid	t_{d}(CKO1H-AWEV)	−0.2	4.0

Table A−3. TMS320C6211/C6711 Host Port Timing Specifications

Characteristic	Symbol	Min (ns)	Max (ns)
Setup time, select signals[§] valid before HSTROBE[†] low	t_{su}(SEL-HSTBL)	5	
Hold time, select signals[§] valid after HSTROBE[†] low	t_h(HSTBL-SELC)	4	
Pulse duration, HSTROBE[†] low	t_w(HSTBL)	4P[‡]	
Pulse duration, HSTROBE[†] high between consecutive accesses	t_w(HSTBH)	4P[‡]	
Setup time, host data valid before HSTROBE[†] high	t_{su}(HDV-HSTBH)	5	
Hold time, host data valid after HSTROBE[†] high	t_h(HSTBH-HDV)	3	
Hold time, HSTROBE[†] low after HRDY low. HSTROBE[†] should not be inactivated until HRDY is active (low); otherwise, HPI writes will not complete properly.	t_h(HRDYL-HSTBL)	2	
Delay time, HCS to HRDY[¶]	t_d(HCS-HRDY)	1	15
Delay time, HSTROBE[†] low to HRDY high[#]	t_d(HSTBL-HRDYH)	3	15
Output hold time, HD low impedance after HSTROBE[†] low for an HPI read	t_{oh}(HSTBL-HDLZ)	2	
Delay time, HD valid to HRDY low	t_d(HDV-HRDYL)	2P[‡] – 4	2P[‡]
Output hold time, HD valid after HSTROBE[†] high	t_{oh}(HSTBH-HDV)	3	15
Delay time, HSTROBE[†] high to HD high impedance	t_d(HSTBH-HDHZ)	3	15
Delay time, HSTROBE[†] low to HD valid	t_d(HSTBL-HDV)	3	15
Delay time, HSTROBE[†] high to HRDY high[‖]	t_d(HSTBH-HRDYH)	3	15

[†] HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.

[‡] P = 1/CPU clock frequency in ns. For example, when running parts at 167 MHz, use P = 6 ns.

[§] Select signals include: HCNTRL[1:0], HR/W, and HHWIL.

[¶] HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.

[#] This parameter is used during an HPID read. At the beginning of the first half-word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.

[‖] This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.

Table A−4. TMS320C6211/C6711 EMIF Timing Specifications

Characteristic	Symbol	Min (ns)	Max (ns)
Setup time, EDx valid before ARE high	t_{su}(EDV-AREH)	9	
Hold time, EDx valid after ARE high	t_h(AREH-EDV)	1	
Setup time, ARDY[†] valid before ECLKOUT high	t_{su}(ARDY-EKOH)	3	
Hold time, ARDY[†] valid after ECKLKOUT high	t_h(EKOH-ARDY)	1	
Hold time, ARDY[†] valid after ARE low	t_{osu}(SELV-AREL)	RS[‡] * E[§] − 3	
Output hold time, ARE high to select signals[¶] invalid	t_{oh}(AREH-SELIV)	RH[‡] * E[§] − 3	
Delay time, ECLKOUT high to ARE valid	t_d(EKOH-AREV)	1.5	8
Output setup time, select signals[¶] valid to AWE low	t_{osu}(SELV-AWEL)	WS[‡] * E[§] − 3	
Output hold time, AWE high to select signals[¶] invalid	t_{oh}(AWEH-SELV)	WH[‡] * E[§] − 3	
Delay time, ECLKOUT high to AWE valid	t_d(EKOH-AWEV)	1.5	8

[†] To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is recognized in the cycle for which the setup and hold time is met. To use ARDY as an asynchronous input, the pulse width of the ARDY signal should be wide enough (e,g., pulse width = 2E) to ensure setup and hold time is met.

[‡] RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

[§] E = ECLKOUT period in ns.

[¶] Select signals include: CEx, BE[3:0], EA[21:2], AOE; and for writes, include ED[31:0].

Table A−5. TMS320C64x Host Port Timing Specifications

Characteristic	Symbol	Min (ns)	Max (ns)
Setup time, select signals[§] valid before HSTROBE[†] low	t_{su}(SELV-HSTBL)	5	
Hold time, select signals[§] valid after HSTROBE[†] low	t_{h}(HSTBL-SEL)V	2	
Pulse duration, HSTROBE[†] low	t_{w}(HSTBL)	4P[‡]	
Pulse duration, HSTROBE[†] high between consecutive accesses	t_{w}(HSTBH)	4P[‡]	
Setup time, host data valid before HSTROBE[†] high	t_{su}(HDV-HSTBH)	5	
Hold time, host data valid after HSTROBE[†] high	t_{h}(HSTBH-HDV)	2	
Hold time, HSTROBE[†] low after HRDY low. HSTROBE[†] should not be inactivated until HRDY is active (low); otherwise, HPI writes will not complete properly.	t_{h}(HRDYL-HSTBL)	2	
Delay time, HCS to HRDY[¶]	t_{d}(HCS-HRDY)	1	7
Delay time, HSTROBE[†] low to HRDY high[#]	t_{d}(HSTBL-HRDYH)	3	12
Output hold time, HD low impedance after HSTROBE[†] low for an HPI read	t_{oh}(HSTBL-HDLZ)	2	
Delay time, HD valid to HRDY low	t_{d}(HDV-HRDYL)	2P[‡] – 6	
Output hold time, HD valid after HSTROBE[†] high	t_{oh}(HSTBH-HDV)	3	
Delay time, HSTROBE[†] high to HD high impedance	t_{d}(HSTBH-HDHZ)		12
Delay time, HSTROBE[†] low to HD valid	t_{d}(HSTBL-HDV)		12
Delay time, HSTROBE[†] high to HRDY high[‖]	t_{d}(HSTBH-HRDYH)	3	12

[†] HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.

[‡] P = 1/CPU clock frequency in ns. For example, when running parts at 600 MHz, use P = 1.67 ns.

[§] Select signals include: HCNTRL[1:0], HR/W, and HHWIL.

[¶] HCS enables HRDY, and HRDY is always low when HCS is high. The case where HRDY goes high when HCS falls indicates that HPI is busy completing a previous HPID write or READ with autoincrement.

[#] This parameter is used during an HPID read. At the beginning of the first half−word transfer on the falling edge of HSTROBE, the HPI sends the request to the DMA auxiliary channel, and HRDY remains high until the DMA auxiliary channel loads the requested data into HPID.

[‖] This parameter is used after the second half-word of an HPID write or autoincrement read. HRDY remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the HRDY signal.

Table A−6. TMS320C64x EMIF Timing Specifications

Characteristic	Symbol	Min (ns)	Max (ns)
Setup time, EDx valid before ARE high	t_{su}(EDV11-AREH)	6	
Hold time, EDx valid after ARE high	t_h(AREH1-EDV)	1	
Setup time, ARDY[†] valid before ECLKOUT1 high	t_{su}(ARDY-EKO1H)	3	
Hold time, ARDY[†] valid after ECKLKOUT1 high	t_h(EKO1H-ARDY)	1	
Hold time, ARDY[†] valid after ARE low	t_{osu}(SELV-AREL)	RS[‡] * E[§] − 1.5	
Output hold time, ARE high to select signals[¶] invalid	t_{oh}(AREH-SELIV)	RH[‡] * E[§] − 1.5	
Delay time, ECLKOUT1 high to ARE valid	t_d(EKO1H-AREV)	1.5	5
Output setup time, select signals[¶] valid to AWE low	t_{osu}(SELV-AWEL)	WS[‡] * E[§] − 1.5	
Output hold time, AWE high to select signals[¶] invalid	t_{oh}(AWEH-SELIV)	WH[‡] * E[§] − 1.5	
Delay time, ECLKOUT1 high to AWE valid	t_d(EKO1H-AWEV)	1.5	5

[†] To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. The ARDY signal is recognized in the cycle for which the setup and hold time is met. To use ARDY as an asynchronous input, the pulse width of the ARDY signal should be wide enough (e,g,m pulse width = 2E) to ensure setup and hold time is met.

[‡] RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup[, WST = Write strobe, WH = Write hold. These parameters are programmed via the EMIF CE space control registers.

[§] E = ECLKOUT period in ns.

[¶] Select signals include: ACEx, ABE[3:0], AEA[21:2], AAOE; and for writes, include AED[31:0]. Select signals EMIFB include: BCEx, BBE[1:0], BEA[20:1], BAIE; and for EMIFB writes, include BED[15:0].

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