

# EVM User's Guide: LM25137F-Q1-EVM5D3

## LM25137-Q1 Evaluation Module



### Description

The LM25137F-Q1-EVM5D3 evaluation module (EVM) is designed to showcase the LM(2)5137-Q1 and LM(2)5137 dual, synchronous buck controller, which is intended for [functional safety](#) applications up to ASIL D or SIL 3. The EVM operates over a wide input voltage range of 6.5V to 36V to deliver 5V and 3.3V regulated outputs with better than 1% setpoint accuracy at load currents up to 20A per output.

### Get Started

1. Order the [LM25137F-Q1-EVM5D3](#).
2. Refer to the [LM5137-Q1](#) and [LM25137-Q1](#) product folders.
3. Review the Altium [PCB layout](#) source files.
4. Use the LM(2)5137-Q1 [quickstart calculator](#) to assist with component selection in your design.

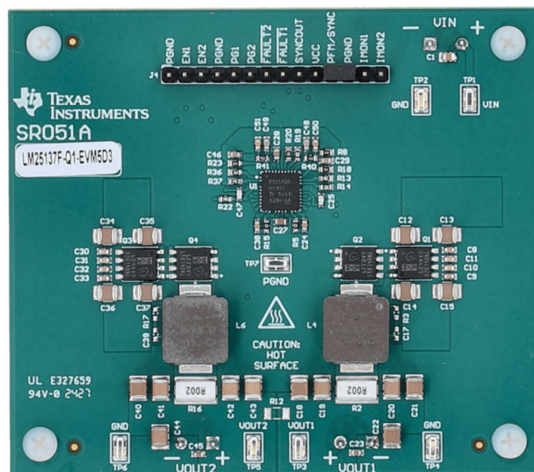
### Features

- Maximum inout voltage of 36V
  - $V_{IN}$  UVLO thresholds set at 6.5V and 4.5V
- Tightly regulated output voltages of 5V and 3.3V, each rated at 20A with 1mV load, line regulation
- High efficiency – 96% at 10A, 94% at 20A
  - VCC bias power derived from the 5V output
- Switching frequency of 440kHz synchronizable  $\pm 20\%$  with an external clock signal

- Input  $\pi$ -stage EMI filter meets CISPR 25
  - Spread spectrum (DRSS) option for lower EMI
  - Electrolytic capacitor for parallel damping
- Peak current-mode control architecture provides fast line and load transient response
  - Integrated slope compensation
  - Forced PWM (FPWM) or pulsed frequency modulation (PFM) operation
- Integrated power MOSFET gate drivers
  - 3A/2A sink/source gate drive current capability
  - Adaptive dead-time control reduces power dissipation and MOSFET temperature rise
- Integrated protection features for robust design
  - Overcurrent protection (OCP) with shunt or inductor DCR current sensing
  - Monotonic prebias output voltage startup
  - User-adjustable soft-start time set to 4.5ms
  - PG and  $\overline{\text{FAULT}}$  outputs for each channel
  - Dual current monitor outputs (IMON1, IMON2)
- Fully assembled, tested and proven PCB layout with 3.3"  $\times$  2.9" (84mm  $\times$  74mm) total footprint

### Applications

- High-current [automotive electronic systems](#) using 2-, 3- and 4-phase implementations
- Dual outputs for [ADAS](#) and [body](#) electronics
- [Infotainment systems](#) and [instrument clusters](#)
- [Automotive HEV/EV powertrain systems](#)



LM25137-Q1 EVM, 84mm  $\times$  74mm

# 1 Evaluation Module Overview

## 1.1 Introduction

The [LM25137F-Q1-EVM5D3](#) evaluation module (EVM) is a dual-channel synchronous buck DC/DC regulator that employs synchronous rectification to achieve high conversion efficiency in a small footprint. The EVM operates over a wide input voltage range of 6.5V to 36V, providing regulated outputs of 5V and 3.3V. The output voltages have better than 1% setpoint accuracy and are adjustable by modifying the feedback resistor values, permitting the user to customize the output voltage within a range of 2.5V to 8V as needed. Alternatively, as shown in [Figure 1-2](#), the EVM is configurable as a two-phase, 40A single-output design by changing the COMP network configuration, the CNFG resistor, and connecting the outputs together.

Inherent protection features for robust design include input supply voltage, VCC and gate-drive UVLO; independent IMON, PG and FAULT indicator outputs for each channel; resistor-adjustable soft start; hiccup-mode overcurrent protection; and thermal shutdown with hysteresis. The selected power-train passive components, including 40V power MOSFETs, 1μH buck inductors, 2mΩ shunts, 10μF/50V ceramic input capacitors and 47μF/10V ceramic output capacitors – are AEC-Q200 rated and available from multiple component vendors.

The module design uses the [LM25137-Q1](#) buck controller IC, which is specifically developed for [functional safety](#) applications and incorporates the following key features:

- Wide  $V_{IN}$  range of 4V to 42V
- 100% duty cycle capability
- Ultra-low shutdown and no-load standby quiescent currents
- Multi-phase capability
- Peak current-mode control loop architecture with slope compensation
- Integrated, high-current MOSFET gate drivers with adaptive dead-time
- Optional dual-random spread spectrum (DRSS) modulation for lower EMI
- Independent current monitor (IMON), power good (PG) and FAULT indicator outputs on each channel

## 1.2 Kit Contents

- A complete filter board (EVM) rated at 20A on each output, including the LM25137-Q1 buck controller IC
- EVM Disclaimer Read Me

## 1.3 Specifications

Table 1-1 lists the EVM specifications. Unless otherwise indicated,  $V_{IN} = 13.5V$ , which is a typical automotive battery voltage.

**Table 1-1. Electrical Performance Characteristics**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>					
Input voltage, $V_{IN}$	Operating range	6.5	13.5	36	V
Input UVLO turn-on threshold, $V_{IN-ON}$	$R_{UV1} = 200k\Omega$ , $R_{UV2} = 36.5k\Omega$		6.5		V
Input UVLO turn-off threshold, $V_{IN-OFF}$			4.5		V
Input supply current, no load, FPWM, $I_{IN-NL(FPWM)}$	$I_{OUT1} = I_{OUT2} = 0A$ , PFM tied to GND	$V_{IN} = 8V$		57	mA
		$V_{IN} = 13.5V$		70	
		$V_{IN} = 24V$		66	
		$V_{IN} = 36V$		56	
Input supply current, no load, PFM, $I_{IN-NL(PFM)}$	$I_{OUT1} = 0A$ , $V_{EN2} = 0V$ , PFM tied to VCC	$V_{IN} = 8V$		10	$\mu A$
		$V_{IN} = 13.5V$		10	
		$V_{IN} = 24V$		10	
		$V_{IN} = 36V$		10	
Input supply current in shutdown, $I_{IN-SHDN}$	$V_{EN1} = V_{EN2} = 0V$		4		$\mu A$
<b>OUTPUT CHARACTERISTICS</b>					
Output voltage, $V_{OUT1}$ <sup>(1)</sup>	FB1 tied to VDDA with 24.9k $\Omega$	4.95	5.0	5.05	V
Output voltage, $V_{OUT2}$ <sup>(1)</sup>	FB2 tied to VDDA with 7.5k $\Omega$	3.27	3.3	3.33	
Output currents, $I_{OUT1}$ , $I_{OUT2}$	$V_{IN} = 6.5V$ to 36V, airflow = 100LFM	0		20	A
Output voltage regulation in FPWM, $\Delta V_{OUT1}$ , $\Delta V_{OUT2}$	Load regulation	$I_{OUT1}$ , $I_{OUT2} = 0A$ to 20A		1	mV
	Line regulation	$V_{IN} = 6.5V$ to 36V		1	
Output voltage ripple, $V_{OUT1-AC}$ , $V_{OUT2-AC}$	$I_{OUT1} = I_{OUT2} = 20A$		10		mV <sub>RMS</sub>
Output overcurrent protection, $I_{OUT1-OC}$ , $I_{OUT2-OC}$	$R_{S1} = R_{S2} = 2m\Omega$		26		A
Soft-start time, $t_{SS}$	$R_{SS} = 20k\Omega$		4.5		ms
Hiccup time, $t_{RES}$	16384 clock cycles		37		ms
<b>SYSTEM CHARACTERISTICS</b>					
Switching frequency, $F_{SW}$	$R_T = 52.4k\Omega$		440		kHz
Half-load efficiency, $\eta_{HALF}$ <sup>(1)</sup>	$I_{OUT1} = I_{OUT2} = 10A$	$V_{IN} = 8V$		96.5%	
		$V_{IN} = 13.5V$		96%	
		$V_{IN} = 18V$		95.5%	
		$V_{IN} = 24V$		94.5%	
Full-load efficiency, $\eta_{FULL}$	$I_{OUT1} = I_{OUT2} = 20A$	$V_{IN} = 8V$		94%	
		$V_{IN} = 13.5V$		94%	
		$V_{IN} = 18V$		93.5%	
		$V_{IN} = 24V$		93%	
LM25137-Q1 junction temperature, $T_J$		-40		150	$^{\circ}C$

(1) The default output voltages of this EVM are 5V and 3.3V. Efficiency and other performance metrics can change based on the operating input voltage, load currents, externally-connected output capacitors and other parameters.

### 1.3.1 Application Circuit Diagrams

Figure 1-1 shows an LM25137-Q1 synchronous buck regulator (not including the EMI filter stage). Furthermore, as detailed in Figure 1-2, we implement a two-phase, single-output regulator by tying the outputs together, connecting COMP1 to COMP2, shorting FB2 to AGND, and setting the CNFG resistor to 41.2kΩ.

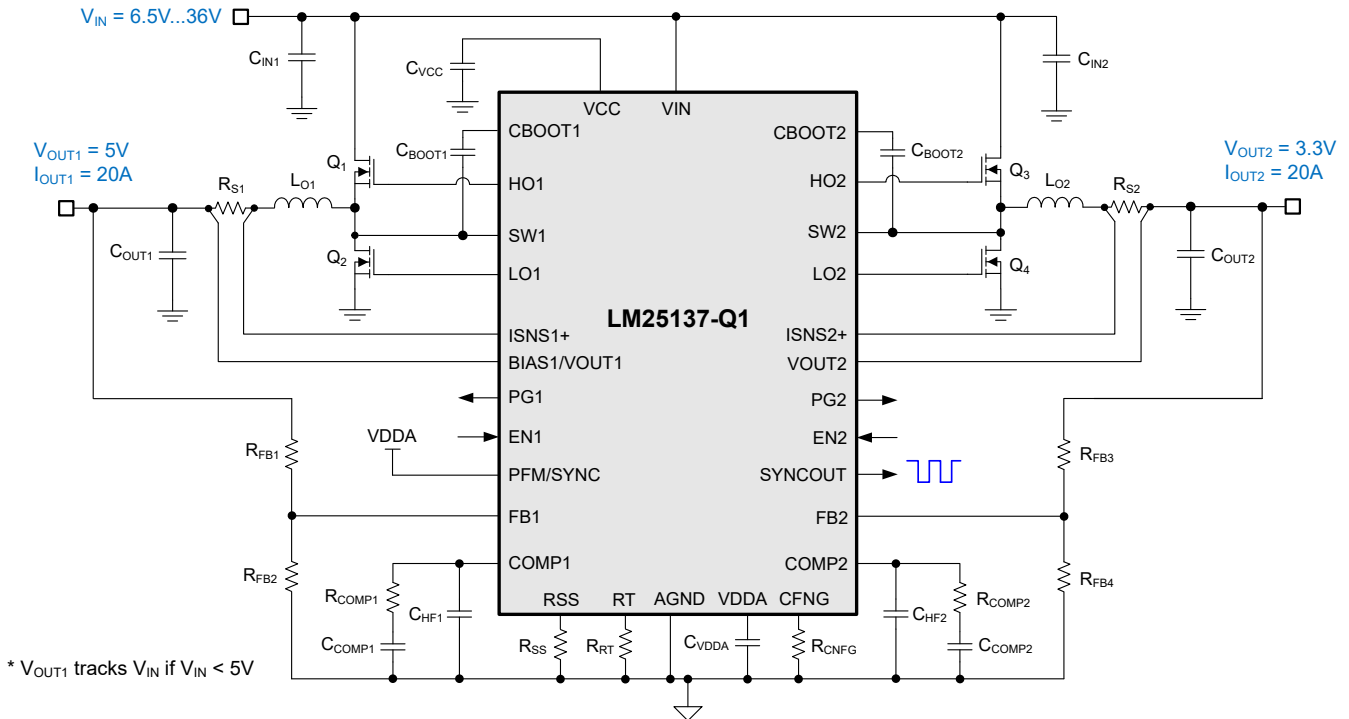


Figure 1-1. LM25137-Q1 Dual-Output Synchronous Buck Regulator Simplified Schematic

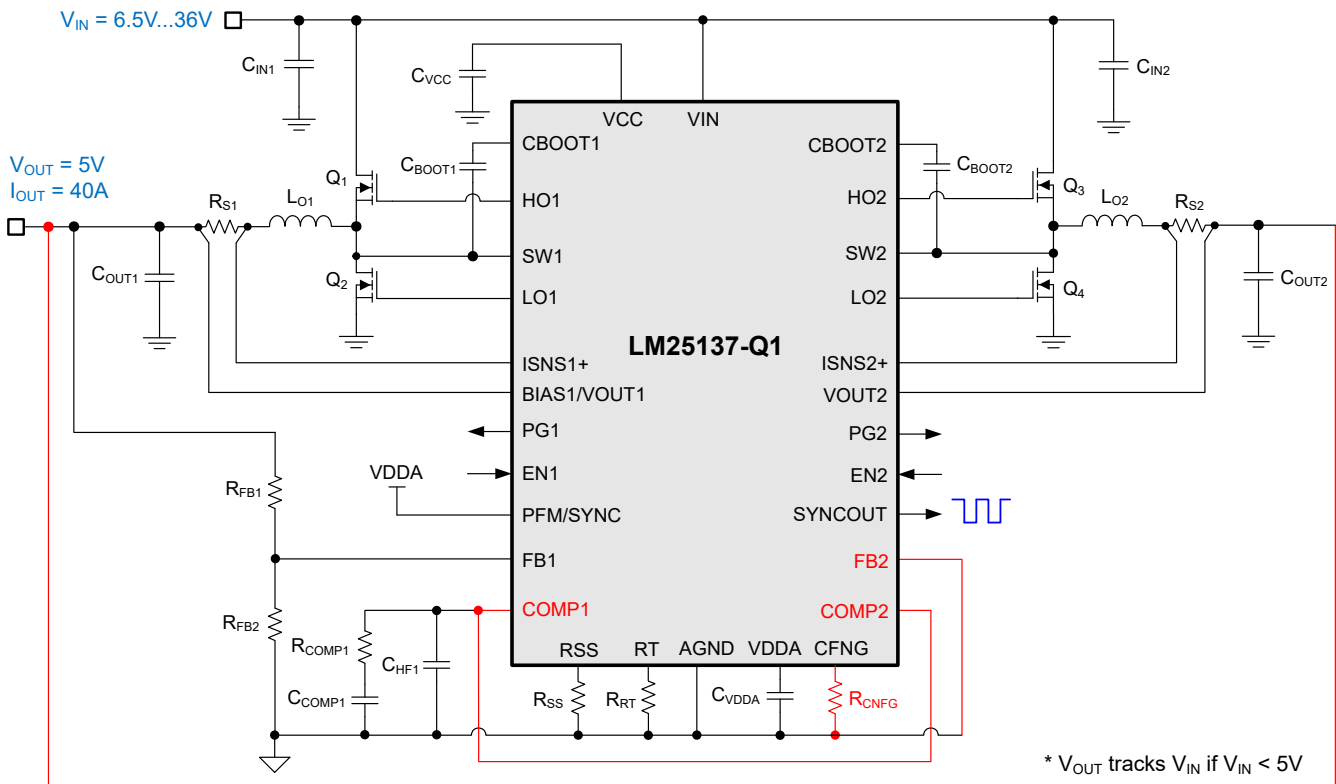


Figure 1-2. LM25137-Q1 Two-Phase Single-Output Synchronous Buck Regulator Simplified Schematic

## 1.4 Device Information

With an input operating voltage as low as 3.5V and up to 100V as specified in [Table 1-2](#), the LM(2)514x-Q1 family of automotive synchronous buck controllers from TI provides flexibility, scalability, and optimized design size for a variety of applications.

With the LM5137-Q1 and LM25137-Q1 now available to aid in functional safety system design up to ASIL D, the controller family enables DC/DC designs with high density, low EMI and increased system reliability. All controllers are rated for a maximum operating junction temperature of 150°C and have AEC-Q100 grade 1 qualification.

**Table 1-2. Automotive Synchronous Buck DC/DC Controller Family**

DC/DC Controller	Single or Dual	V <sub>IN</sub> Range	Control Method	Gate Drive Voltage	Sync Output	Programmable Spread Spectrum
<a href="#">LM5137-Q1</a>	Dual	4V to 80V	Peak current mode	5V	90° phase shift	DRSS (5% or 10%)
<a href="#">LM25137-Q1</a>	Dual	4V to 42V	Peak current mode	5V	90° phase shift	DRSS (5% or 10%)
<a href="#">LM5140-Q1</a>	Dual	3.8V to 65V	Peak current mode	5V	180° phase shift	N/A
<a href="#">LM5141-Q1</a>	Single	3.8V to 65V	Peak current mode	5V	N/A	Triangular
<a href="#">LM25141-Q1</a>	Single	3.8V to 42V	Peak current mode	5V	N/A	Triangular
<a href="#">LM5143A-Q1</a>	Dual	3.5V to 65V	Peak current mode	5V	90° phase shift	Triangular
<a href="#">LM25143-Q1</a>	Dual	3.5V to 42V	Peak current mode	5V	90° phase shift	Triangular
<a href="#">LM5145-Q1</a>	Single	5.5V to 75V	Voltage mode	7.5V	180° phase shift	N/A
<a href="#">LM5146-Q1</a>	Single	5.5V to 100V	Voltage mode	7.5V	180° phase shift	N/A
<a href="#">LM5148-Q1</a>	Single	3.5V to 80V	Peak current mode	5V	180° phase shift	DRSS
<a href="#">LM25148-Q1</a>	Single	3.5V to 42V	Peak current mode	5V	180° phase shift	DRSS
<a href="#">LM5149-Q1</a>	Single	3.5V to 80V	Peak current mode	5V	180° phase shift	DRSS
<a href="#">LM25149-Q1</a>	Single	3.5V to 42V	Peak current mode	5V	180° phase shift	DRSS

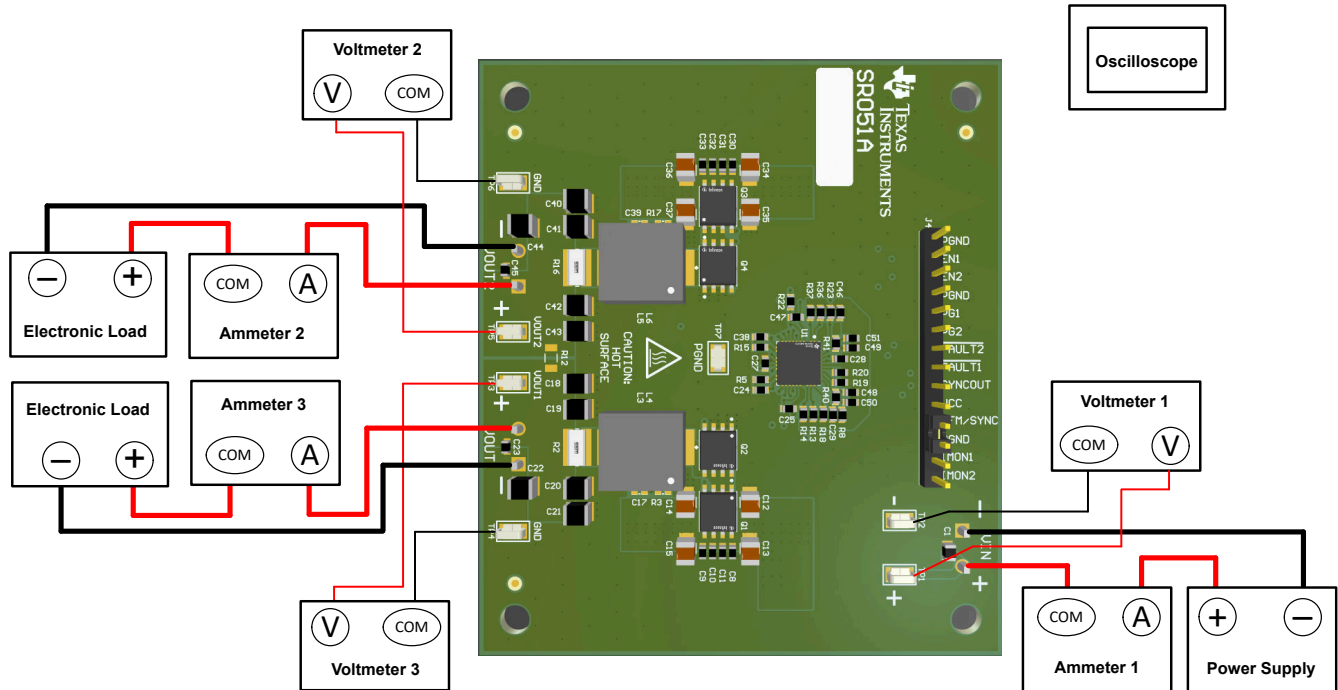
The [LM25137-Q1](#) is available in a 36-pin VQFN package with 6mm × 6mm footprint to enable DC/DC designs with high density and low component count. Use the LM25137-Q1 with [WEBENCH® Power Designer](#) to create a custom regulator design. To optimize component selection and examine predicted efficiency performance across line and load ranges, download the LM(2)5137-Q1 [quickstart calculator](#).

## 2 Hardware

### 2.1 Test Setup and Procedure

#### 2.1.1 EVM Connections

Referencing the EVM connections described in [Table 2-1](#), [Figure 2-1](#) shows the recommended test setup to evaluate the LM25137F-Q1-EVM5D3. Working at an ESD-protected workstation, verify that any wrist straps, boot straps or mats are connected and referencing the user to earth ground before handling the EVM.



**Figure 2-1. EVM Test Setup**

**Table 2-1. EVM Power Connections**

LABEL	DESCRIPTION
VIN	Positive input voltage power and sense connection
GND	Negative input voltage power and sense connection
VOUT1	Channel 1 positive output voltage power and sense connection
VOUT2	Channel 2 positive output voltage power and sense connection
GND	Negative output voltage power and sense connection

**Table 2-2. EVM Signal Connections**

LABEL	DESCRIPTION
PGND	GND connection
EN1, EN2	ENABLE inputs – tie to GND to disable the respective channel
PG1, PG2	Power Good outputs
FAULT1, FAULT2	FAULT outputs
SYNCOUT	Synchronization output
VCC	Bias rail connection
PFM/SYNCIN	Synchronization input
IMON1, IMON2	Current monitor outputs

### CAUTION

Refer to the [LM5137-Q1](#) data sheet, [quickstart calculator](#) and [WEBENCH® Power Designer](#) for additional guidance pertaining to component selection and controller operation.

## 2.1.2 Test Equipment

**Voltage Source:** Use an input voltage source capable of supplying 0V to 36V and 25A.

### Multimeters:

- **Voltmeter 1:** Input voltage at VIN to GND. Set voltmeter to an input impedance of 100M $\Omega$ .
- **Voltmeter 2:** Output voltage at VOUT1 to GND. Set voltmeter to an input impedance of 100M $\Omega$ .
- **Voltmeter 3:** Output voltage at VOUT2 to GND. Set voltmeter to an input impedance of 100M $\Omega$ .
- **Ammeter 1:** Input current. Set ammeter to 1-second aperture time.
- **Ammeter 2:** Output current for channel 1. Set ammeter to 1-second aperture time.
- **Ammeter 2:** Output current for channel 2. Set ammeter to 1-second aperture time.

**Electronic Load:** The load must be an electronic constant-resistance (CR) or constant-current (CC) mode load capable of 0A to 20A at 5V. For a no-load input current measurement, disconnect the electronic load because the load can draw a small residual current.

**Oscilloscope:** With the scope set to 20MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the ground barrel of the probe through the ground lead to the negative terminal of the capacitor. TI does not recommend using a long-leaded ground connection because this can induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

**Safety:** Always use caution when touching any circuits that can be live or energized.

## 2.1.3 Recommended Test Setup

### 2.1.3.1 Input Connections

- Prior to connecting the DC input source, set the current limit of the input supply to 0.1A maximum. Make sure the input source is initially set to 0V and connected to the VIN+ and VIN– connection points as shown in [Figure 2-1](#). TI recommends an additional input bulk capacitor to provide damping when using long input lines.
- Connect voltmeter 1 at the VIN+ and VIN– sense points to measure the input voltage.
- Connect ammeter 1 to measure the input current and set to at least 1-second aperture time.

### 2.1.3.2 Output Connections

- Connect electronic loads to VOUT1 and VOUT2 power connections. Set the loads to constant-resistance mode or constant-current mode at 0A before applying input voltage.
- Connect voltmeter 2 at VOUT1 and GND connections to measure the output voltage of channel 1.
- Connect voltmeter 3 at VOUT2 and GND connections to measure the output voltage of channel 2.
- Connect ammeter 2 and ammeter 3 to measure the output currents.

## 2.1.4 Test Procedure

### 2.1.4.1 Line and Load Regulation, Efficiency

- Set up the EVM as described above.
- Set load to constant resistance or constant current mode and to sink 0A.
- Increase input source from 0V to 12V; use voltmeter 1 to measure the input voltage.
- Increase the current limit of the input supply to 25A.
- Using voltmeter 2 to measure the output voltage,  $V_{OUT1}$ , vary the load current from 0A to 20A;  $V_{OUT1}$  must remain within the load regulation specification.
- Using voltmeter 3 to measure the output voltage,  $V_{OUT2}$ , vary the load current from 0A to 20A;  $V_{OUT2}$  needs to remain within the load regulation specification.
- Set the load currents to 10A (50% rated load) and vary the input source voltage from 6.5V to 36V;  $V_{OUT1}$  and  $V_{OUT2}$  must remain within the line regulation specification.
- Decrease the load to 0A. Decrease the input source voltage to 0V.

### 3 Implementation Results

#### 3.1 Test Data and Performance Curves

Figure 3-1 through Figure 3-14 present typical performance curves for the LM25137F-Q1-EVM5D3. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements.

##### 3.1.1 Efficiency

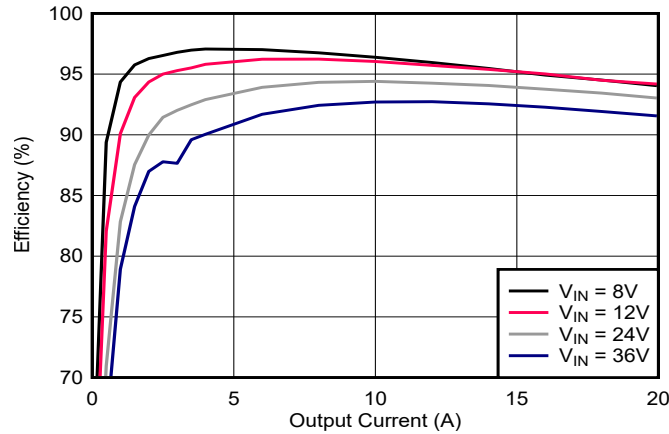


Figure 3-1. Combined Efficiency, V<sub>OUT1</sub> = 5V, V<sub>OUT2</sub> = 3.3V

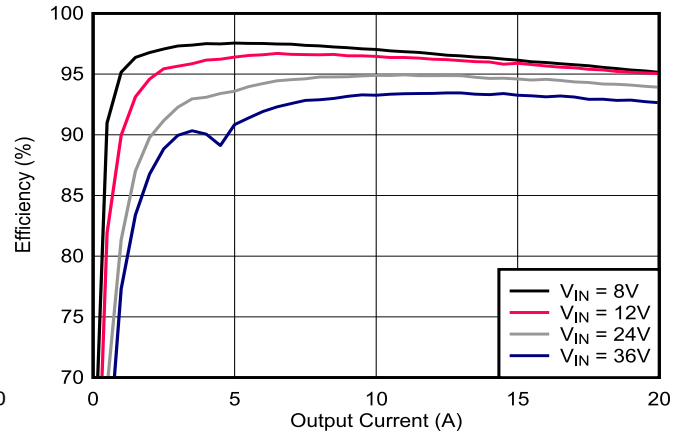


Figure 3-2. Ch1 Efficiency, V<sub>OUT1</sub> = 5V, FPWM, Channel 2 OFF

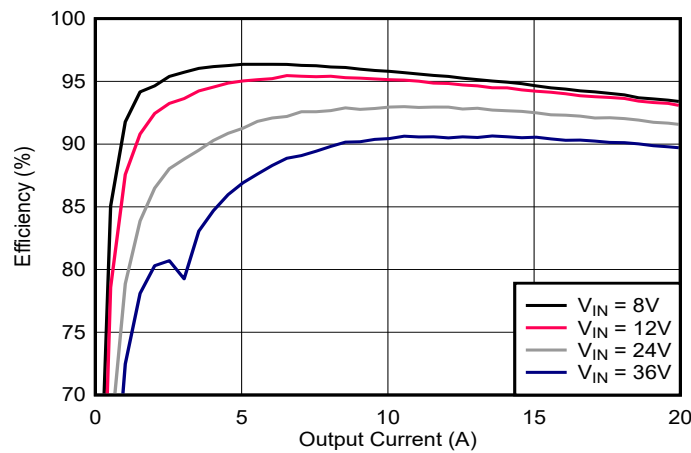


Figure 3-3. Ch2 Efficiency, V<sub>OUT2</sub> = 3.3V, FPWM, Channel 1 OFF



### 3.1.2 Operating Waveforms

#### 3.1.2.1 Load Transient Response

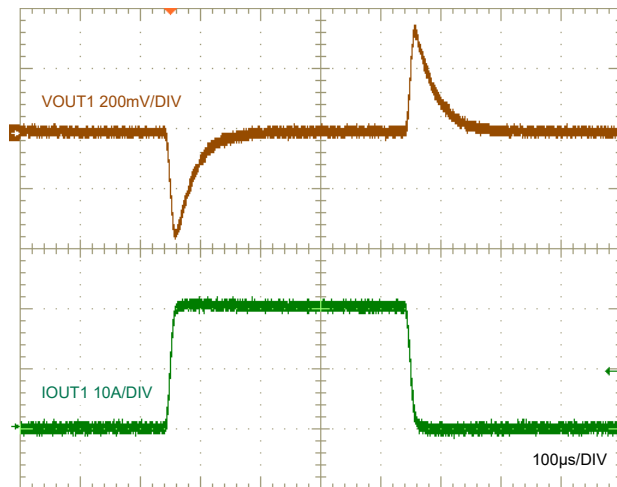


Figure 3-4. Ch1 (5V) Load Transient Response,  $V_{IN} = 12V$ , FPWM, 0A to 20A at  $2A/\mu s$

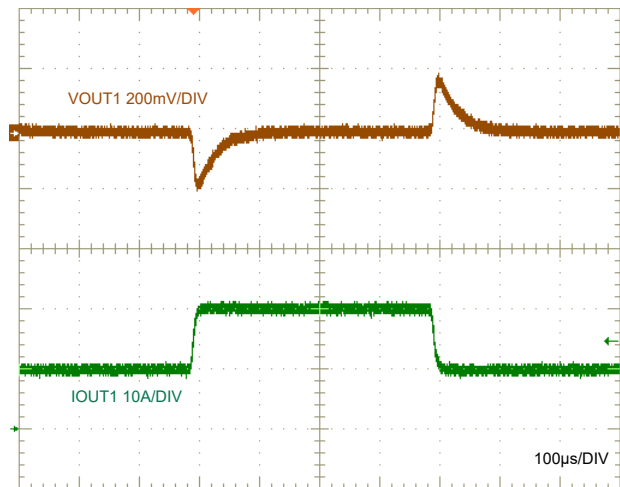


Figure 3-5. Ch1 (5V) Load Transient Response,  $V_{IN} = 12V$ , FPWM, 10A to 20A at  $2A/\mu s$

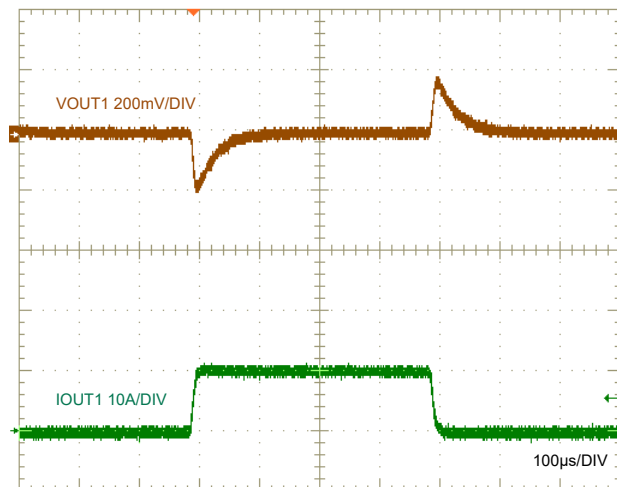


Figure 3-6. Ch1 (5V) Load Transient Response,  $V_{IN} = 12V$ , FPWM, 0A to 10A at  $2A/\mu s$

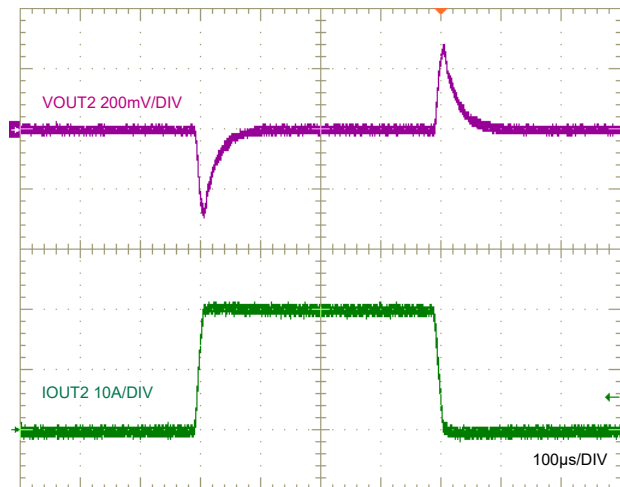


Figure 3-7. Ch2 (3.3V) Load Transient Response,  $V_{IN} = 12V$ , FPWM, 0A to 20A at  $2A/\mu s$

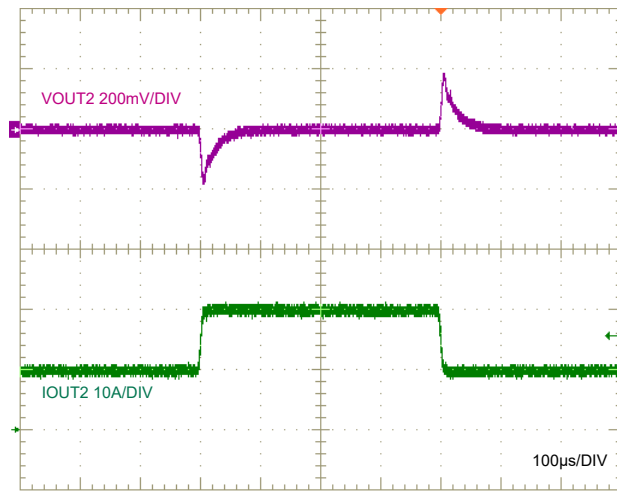


Figure 3-8. Ch2 (3.3V) Load Transient Response,  $V_{IN} = 12V$ , FPWM, 10A to 20A at 2A/µs

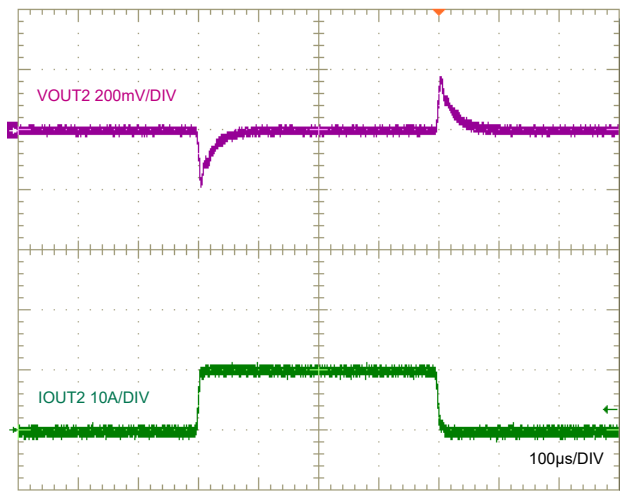


Figure 3-9. Ch2 (3.3V) Load Transient Response,  $V_{IN} = 12V$ , FPWM, 0A to 10A at 2A/µs

### 3.1.2.2 Startup/Shutdown With $V_{IN}$

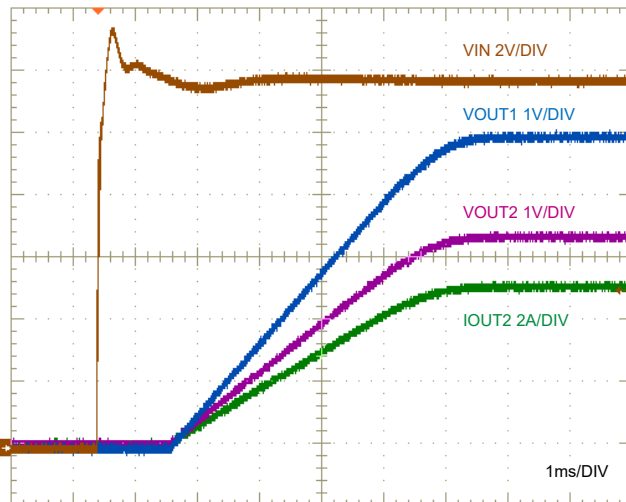


Figure 3-10. Startup Characteristic,  $V_{IN}$  Stepped to 12V,  $I_{OUT1} = I_{OUT2} = 5A$  Resistive,  $R_{SS} = 20k\Omega$

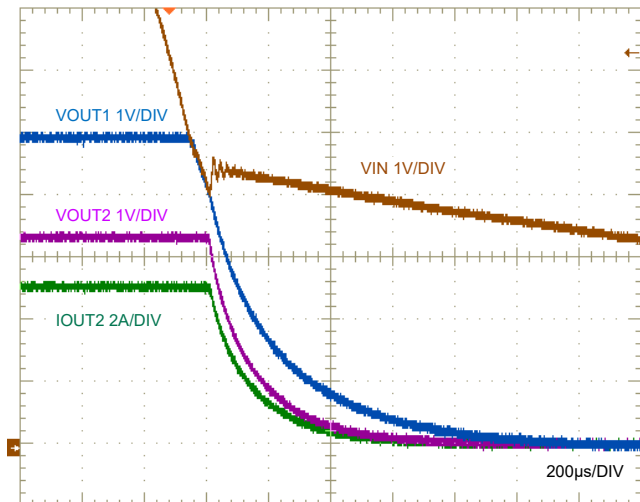


Figure 3-11. Shutdown Characteristic,  $V_{IN} = 12V$ ,  $I_{OUT1} = I_{OUT2} = 5A$  Resistive

### 3.1.2.3 Startup/Shutdown With ENABLE ON and OFF

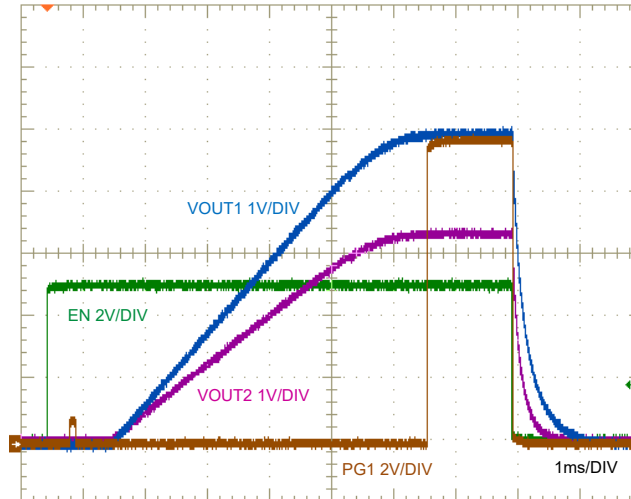


Figure 3-12. ENABLE ON and OFF,  $V_{IN} = 12V$ ,  $I_{OUT1} = I_{OUT2} = 5A$  Resistive,  $R_{SS} = 20k\Omega$

### 3.1.2.4 Switching

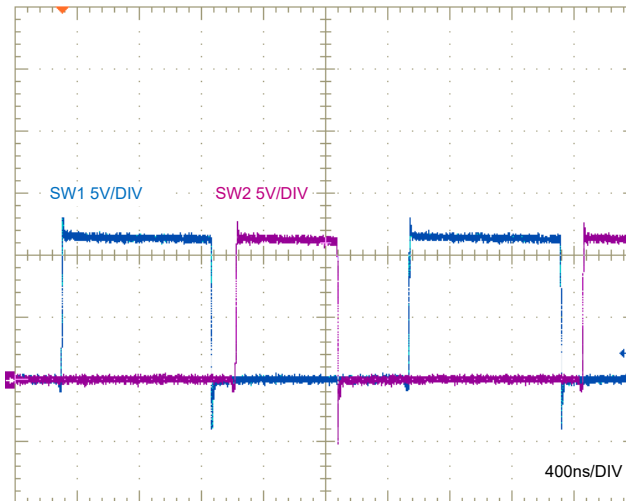


Figure 3-13. Switch-node Voltages,  $V_{IN} = 12V$ ,  $I_{OUT1} = I_{OUT2} = 10A$

### 3.1.3 Thermal Performance

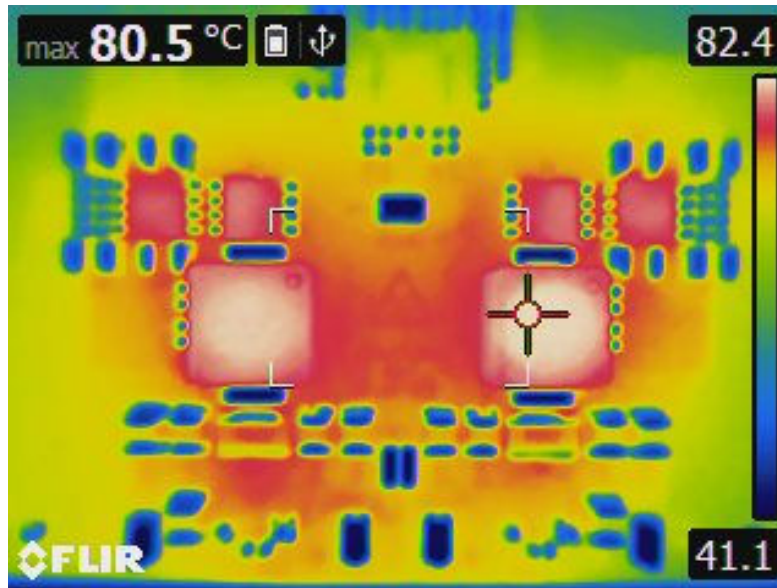


Figure 3-14. Thermal Performance,  $V_{IN} = 12V$ ,  $I_{OUT1} = I_{OUT2} = 15A$ , Free Convection Airflow

## 4 Hardware Design Files

For development support see the following:

- LM(2)5137-Q1 [quickstart calculator](#)
- LM25137F-Q1-EVM5D3 [Altium layout source files](#)
- LM5137-Q1 PSPICE for TI and SIMPLIS [simulation models](#)
- For TI's reference design library, visit [TI Reference Design library](#)
- To design a low-EMI power supply, review TI's comprehensive [EMI Training Series](#)
- Application Note:
  - [Improve High-current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout](#)

## 4.1 Schematic

Figure 4-1 provides the EVM schematic (using the ASIL D version of the LM5137-Q1).

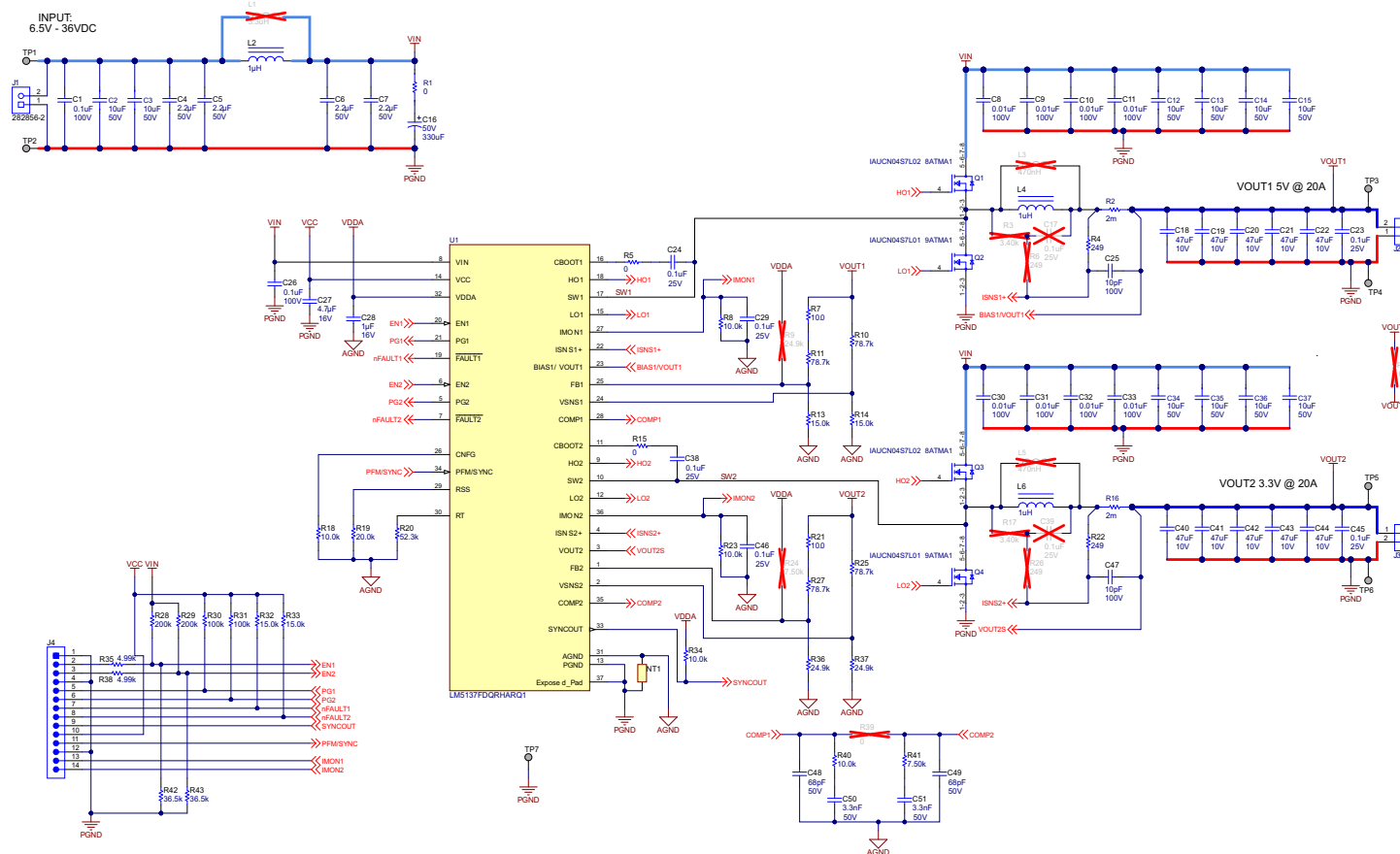


Figure 4-1. EVM Schematic

## 4.2 PCB Layout

Figure 4-2 through Figure 4-9 show the design of the EVM using a 6-layer PCB with 2-oz copper thickness. The EVM is essentially a single-sided design except for certain input filtering and small-signal components located on the bottom side.

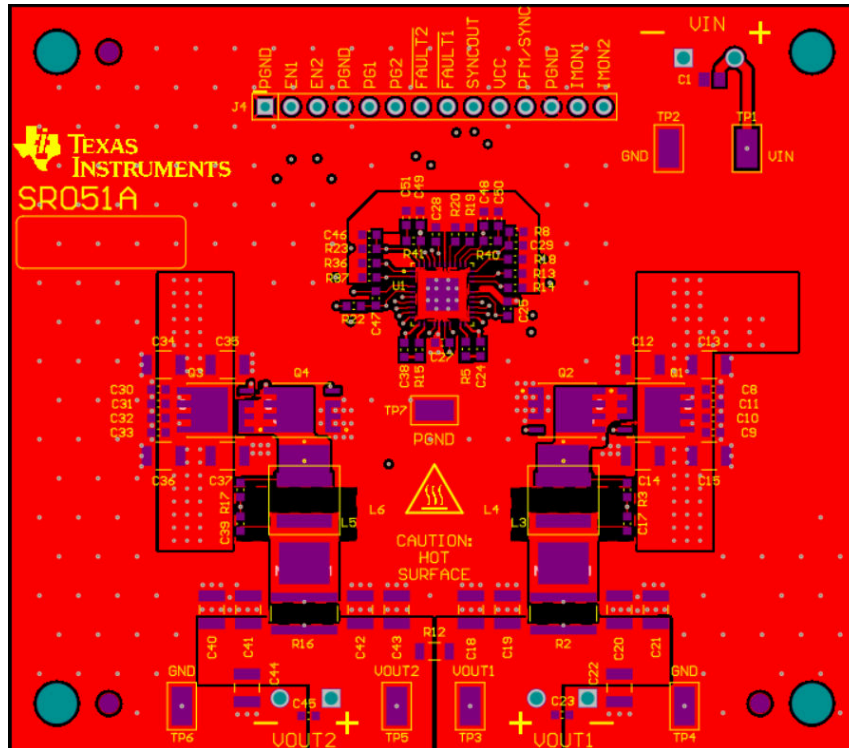


Figure 4-2. Top Copper (Top View)

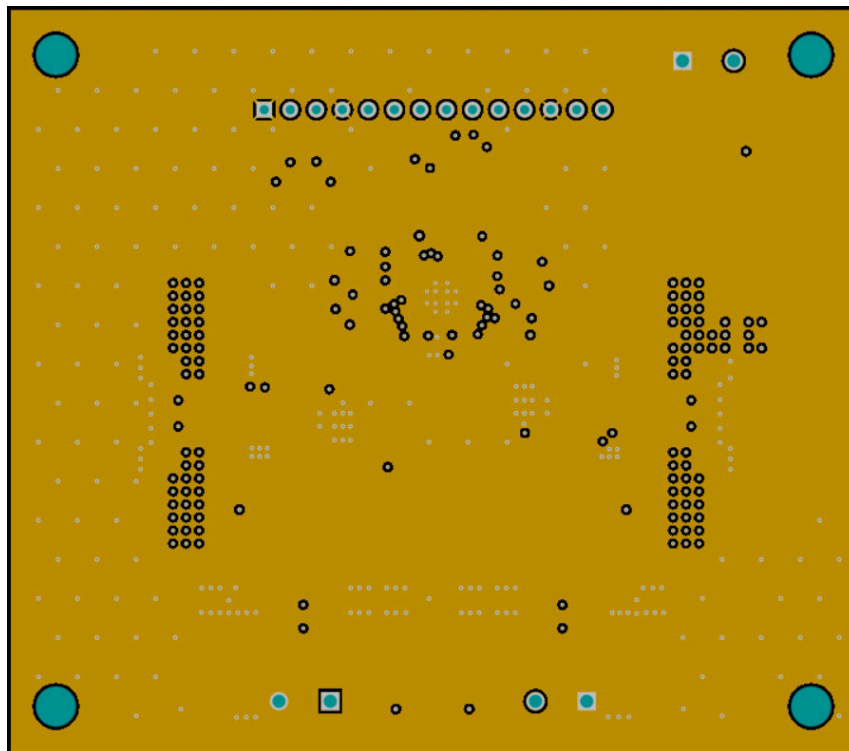


Figure 4-3. Layer 2 Copper (Top View)

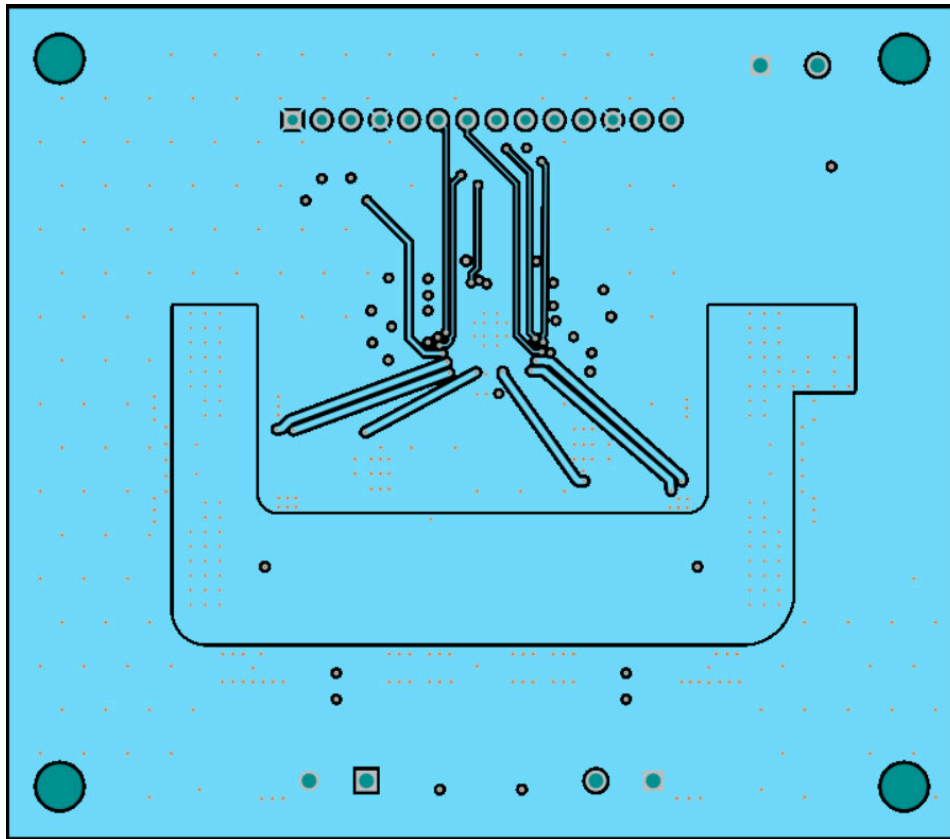


Figure 4-4. Layer 3 Copper (Top View)

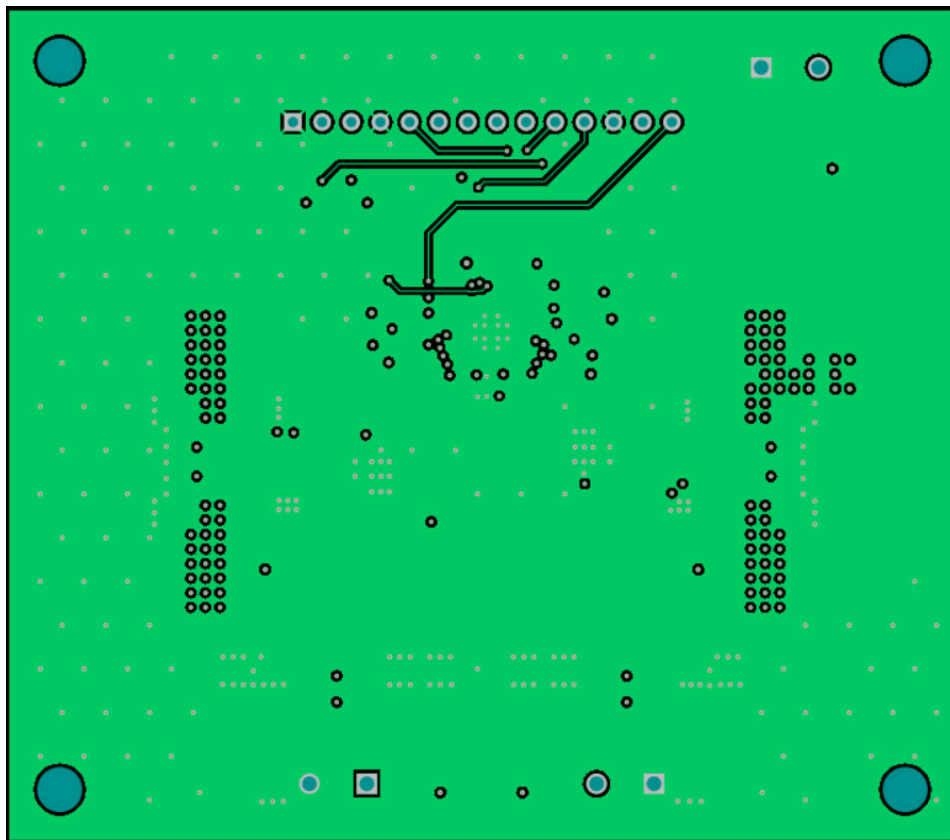


Figure 4-5. Layer 4 Copper (Top View)

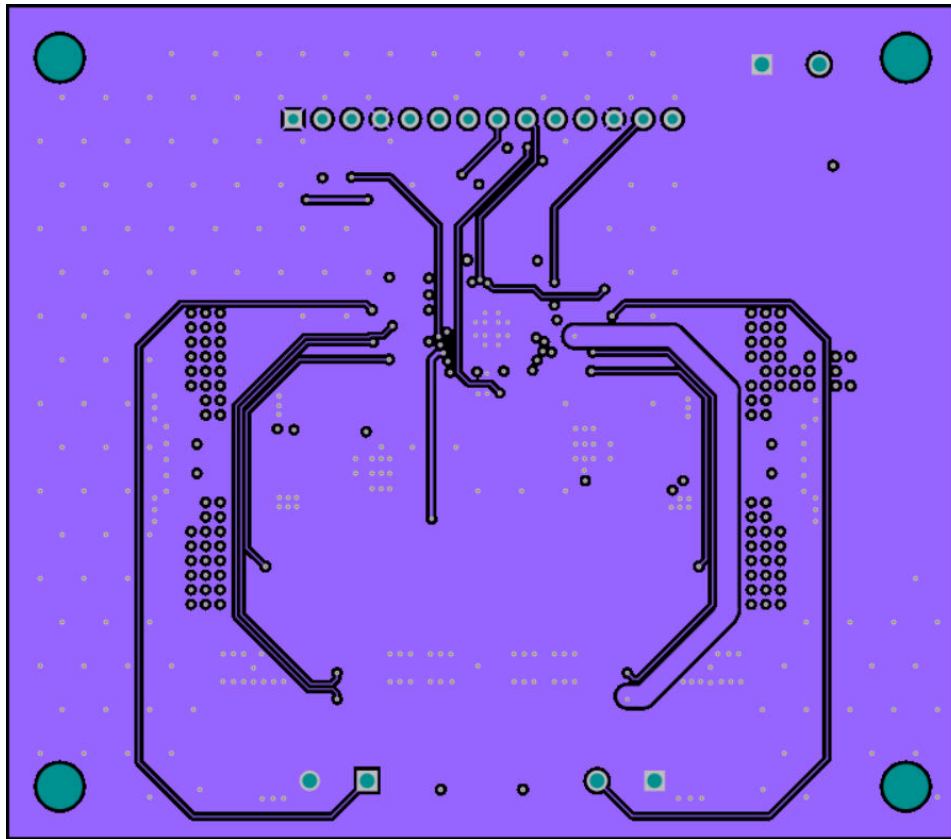


Figure 4-6. Layer 5 Copper (Top View)

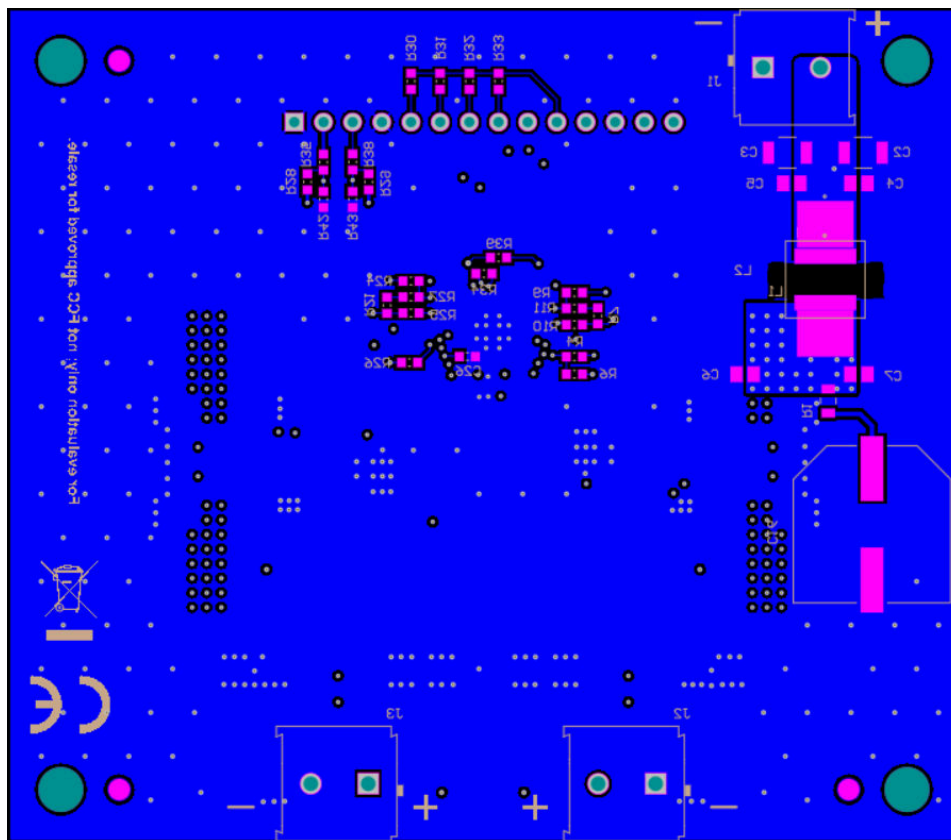
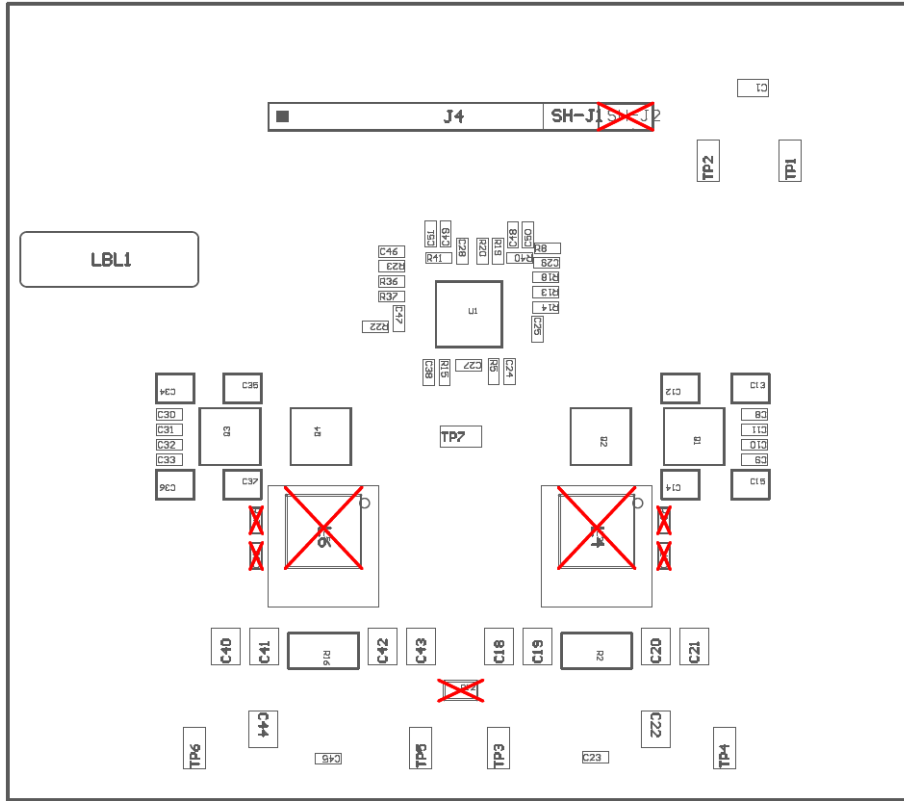


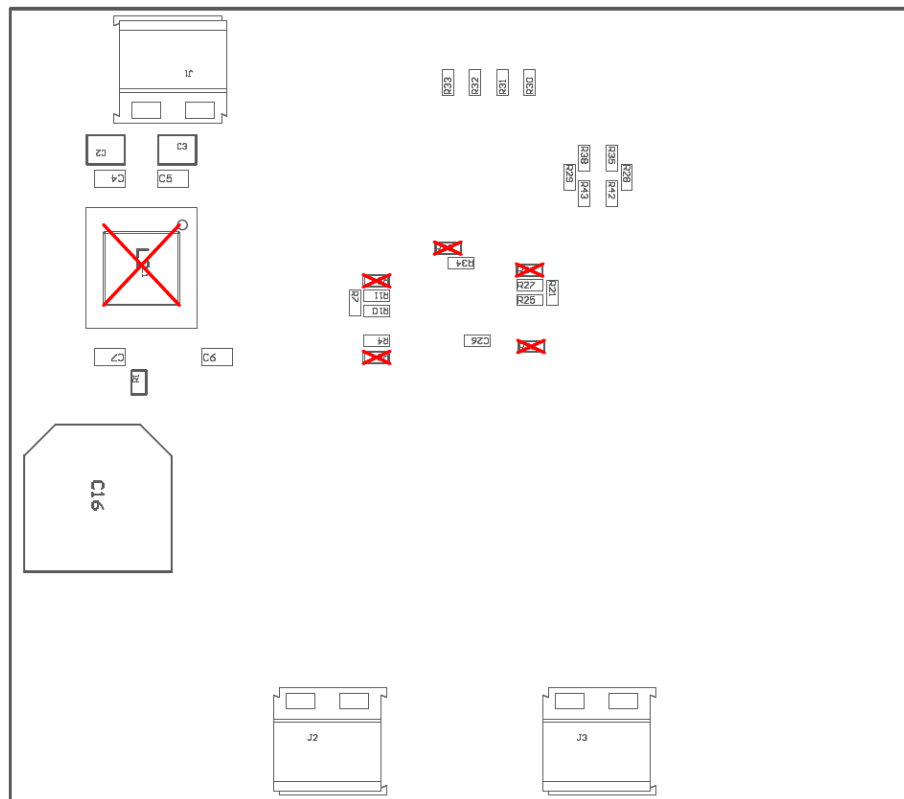
Figure 4-7. Bottom Copper (Top View)



### 4.2.1 Component Drawings



**Figure 4-8. Top Component Drawing**



**Figure 4-9. Bottom Component Drawing**

## 4.2.2 Layout Guidelines

Figure 4-10 shows the top layer of the PCB with layer 2 as a power-loop ground return path directly underneath the top layer to create a low-area switching power loop of approximately 2mm<sup>2</sup>. This loop area, and hence parasitic inductance, must be as small as possible to minimize switch-node voltage overshoot and ringing (and hence the overall EMI signature).

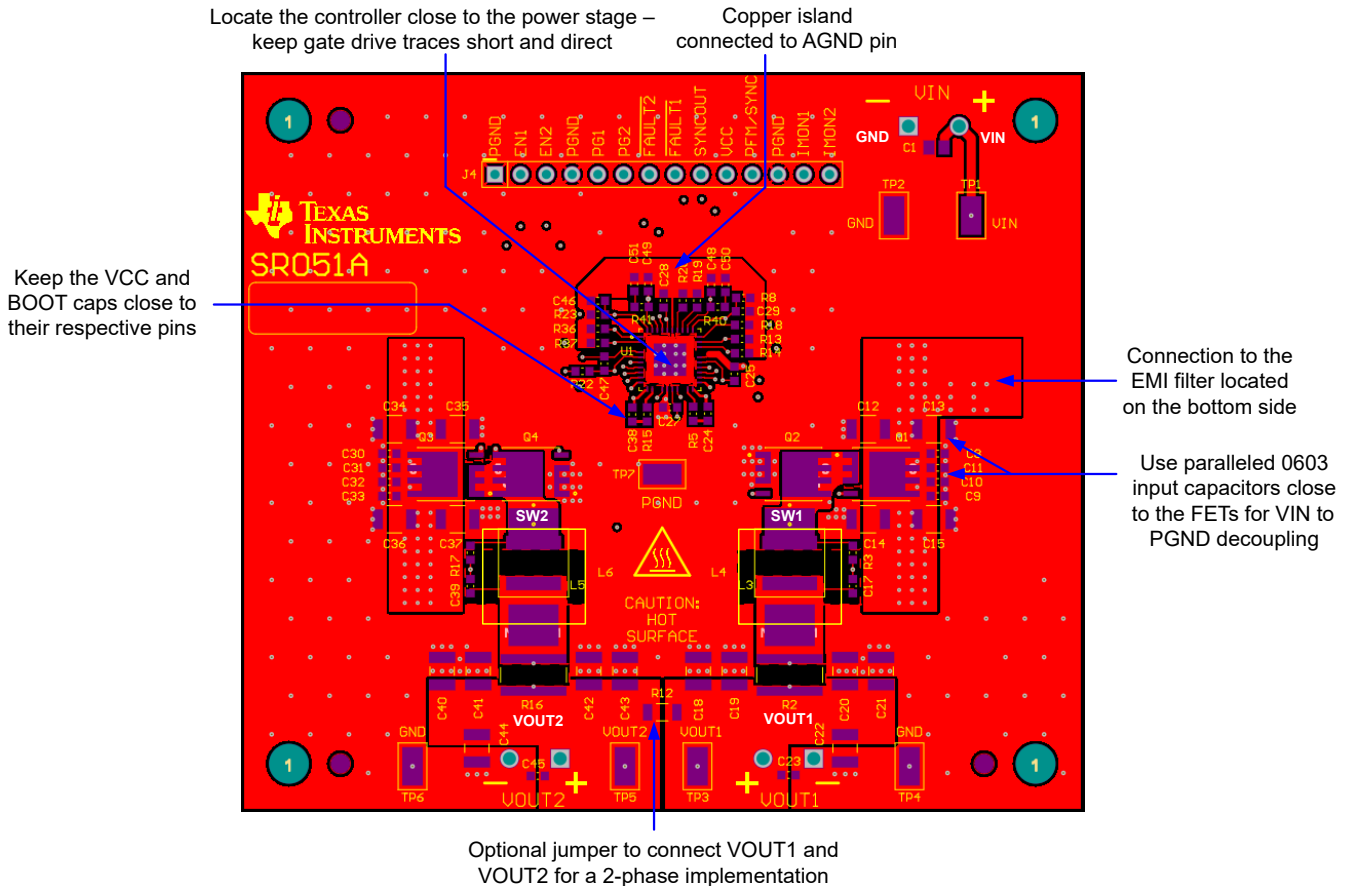


Figure 4-10. PCB Top Layer With Layout Guidelines

As shown in Figure 4-11, the high-frequency power loop current flows through MOSFETs Q3 and Q4, through the power ground plane on layer 2, and back to VIN through the 0603 ceramic capacitors C30 through C33. The currents flowing in opposing directions in the vertical loop configuration provide field self-cancellation, reducing parasitic loop inductance. Figure 4-12 shows a side view to illustrate the concept of creating a low-profile, self-canceling loop in a multilayer PCB structure. The layer-2 GND plane layer, shown in Figure 4-11, provides a tightly-coupled current return path directly under the MOSFETs to the source terminals of Q4.

Four 10nF input capacitors with small 0603 case size place in parallel close to the drain of each high-side MOSFET. The low ESL and high self-resonant frequency (SRF) of the small footprint capacitors yield excellent high-frequency performance. The negative terminals of these capacitors connect to the layer-2 GND plane with multiple 12mil (0.3mm) diameter vias, further reducing parasitic inductance.

The following list describes additional important steps in a layout design. Refer to the [LM5137-Q1 Automotive, 4V to 80V, 100% Duty Cycle Capable, Dual-Channel Synchronous Buck Controller Family for Functional Safety Applications data sheet](#) layout guidelines for more detail.

- Keep the SW connection from the power MOSFETs to the inductor (for each channel) at minimum copper area to reduce capacitive coupling and radiated EMI.
- Position the IC between the two phase and relatively close to the power MOSFET gate terminals. Route the gate drive traces short and direct, and keep HO and SW traces together to minimize gate loop parasitic inductance.

- Create an analog ground plane near the IC for sensitive analog components. Connect the AGND plane and the PGND power ground planes at a single point at the die attach pad (DAP) of the IC.
- Route the current sense traces from the shunt to the IC as a differential pair and keep away from noise sources, such as the switch node and gate drive traces. Increase the width of the trace to the BIAS1/VOU1 pin, as the trace carries the bias current for the IC.

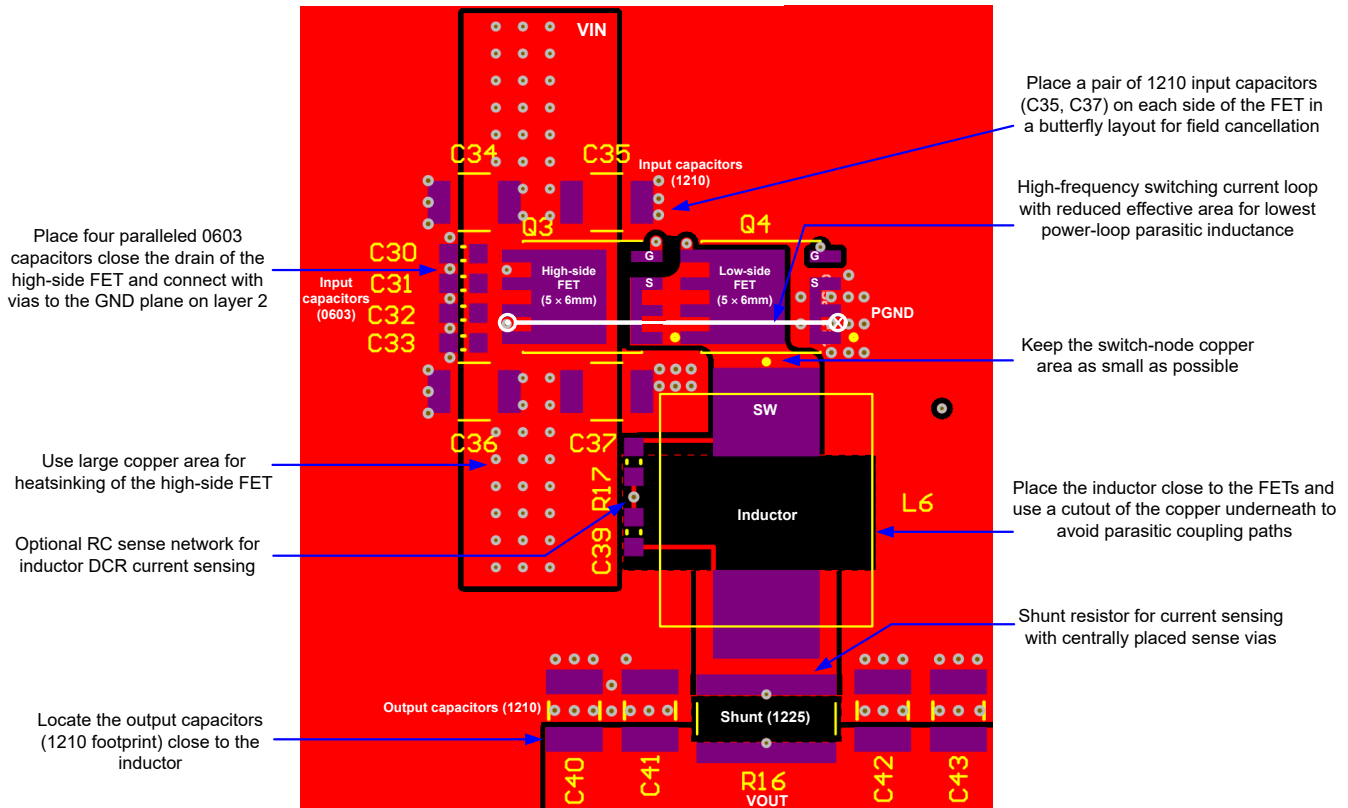
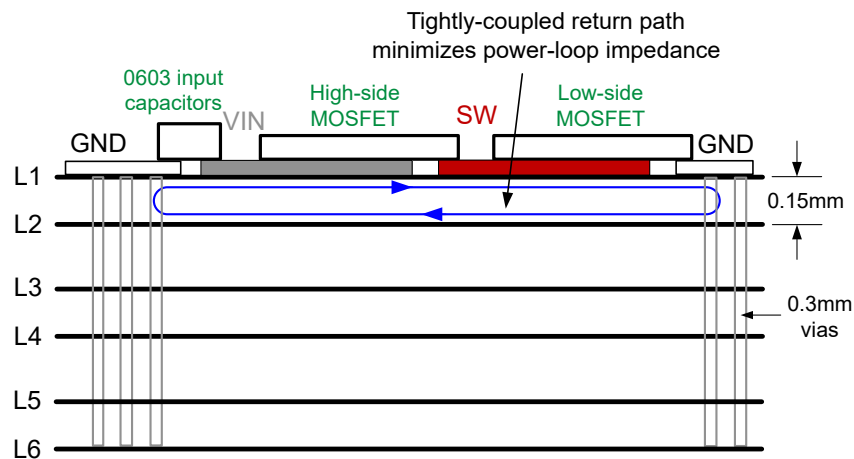


Figure 4-11. Power Stage Component Layout



Note

Refer to the [Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout application brief](#) for more detail.

Figure 4-12. PCB Stack-Up Diagram With Low L1-L2 Intra-layer Spacing

### 4.3 Bill of Materials

**Table 4-1. Bill of Materials**

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	C1	Capacitor, ceramic, 0.1μF, 100V, X7R, 0805	Std	Std
10	C2, C3, C12, C13, C14, C15, C34, C35, C36, C37	Capacitor, ceramic, 10μF, 50V, X7S, 1210, AEC-Q200	GCM32EC71H106KA03L	Murata
		Capacitor, ceramic, 10μF, 50V, X7R, 1210, AEC-Q200	CNA6P1X7R1H106K250AE	TDK
4	C4, C5, C6, C7	Capacitor, ceramic, 2.2μF, 50V, X7R, 0805, AEC-Q200	CGA4J3X7R1H225K125AE	TDK
8	C8, C9, C10, C11, C30, C31, C32, C33	Capacitor, ceramic, 10nF, 100V, X7R, 0603	GRM188R72A103KA01D	Murata
1	C16	Capacitor, electrolytic, 330μF, 50V, AEC-Q200	EEV-FK1H331Q	Panasonic
10	C18, C19, C20, C21, C22, C40, C41, C42, C43, C44	Capacitor, ceramic, 47μF, 10V, X7R, 1210, AEC-Q200	GRM32ER71A476KE15L	Murata
6	C23, C24, C29, C38, C45, C46	Capacitor, ceramic, 0.1μF, 25V, X7R, 0603	Std	Std
1	C26	Capacitor, ceramic, 0.1μF, 100V, X7R, 0603	Std	Std
1	C27	Capacitor, ceramic, 4.7μF, 16V, X7R, 0603	Std	Std
1	C28	Capacitor, ceramic, 1μF, 16V, X7R, 0603	Std	Std
2	C48, C49	Capacitor, ceramic, 68pF, 50V, C0G, 5%, 0603	Std	Std
2	C50, C51	Capacitor, ceramic, 3.3nF, 50V, X7R, 10%, 0603	Std	Std
4	H1, H2, H3, H4	Hex standoff threaded #4-40 nylon 0.750", 3/4" natural	1902D	Keystone
4	H5, H6, H7, H8	#4-40 pan head machine screw Phillips drive nylon	NY PMS 440 0038 PH	Building Fasteners
3	J1, J2, J3	Terminal block, 5mm, 2-pole, tin, TH	282856-2	TE Connectivity
1	J4	Header, 100mil, 14 × 1, Gold, TH	TSW-114-07-G-S	Samtec
3	L2, L4, L6	Inductor, 1μH, 37A, 2.3mΩ, AEC-Q200	VCHA105D-1R0MS6	Cyntec
		Inductor, 1μH, 33.8A, 2.7mΩ, AEC-Q200	784373680010	Würth Elektronik
2	Q1, Q3	MOSFET, N-channel, 40V, 2.8mΩ, AEC-Q101	IAUCN04S7L028ATMA1	Infineon
2	Q2, Q4	MOSFET, N-channel, 40V, 1.9mΩ, AEC-Q101	IAUCN04S7L019ATMA1	Infineon
1	R1	Resistor, 0Ω, 0805	Std	Std
1	R2, R16	Resistor, 2mΩ, 3W, 2%, 1225, AEC-Q200	KRL6432E-M-R002-G-T1	Susumu
2	R4, R22	Resistor, 249Ω, 1/10W, 1%, 0603	Std	Std
2	R5, R15	Resistor, 0Ω, 1/10W, 1%, 0603	Std	Std
2	R7, R21	Resistor, 10Ω, 1/10W, 1%, 0603	Std	Std
5	R8, R18, R23, R30, R40	Resistor, 10kΩ, 1/10W, 1%, 0603	Std	Std
4	R10, R11, R25, R27	Resistor, 78.7kΩ, 1/10W, 1%, 0603	Std	Std
4	R13, R14, R32, R33	Resistor, 15kΩ, 1/10W, 1%, 0603	Std	Std
1	R19	Resistor, 20kΩ, 1/10W, 1%, 0603	Std	Std
1	R20	Resistor, 52.3kΩ, 1/10W, 1%, 0603	Std	Std
2	R28, R29	Resistor, 200kΩ, 1/10W, 1%, 0603	Std	Std
2	R30, R31	Resistor, 100kΩ, 1/10W, 1%, 0603	Std	Std
2	R12, R15	Resistor, 49.9Ω, 1/10W, 1%, 0603	Std	Std
2	R35, R38	Resistor, 4.99kΩ, 1/10W, 1%, 0603	Std	Std
2	R36, R37	Resistor, 24.9kΩ, 1/10W, 1%, 0603	Std	Std
1	R41	Resistor, 7.5kΩ, 1/10W, 1%, 0603	Std	Std
2	R42, R43	Resistor, 36.5kΩ, 1/10W, 1%, 0603	Std	Std
7	TP1, TP2, TP3, TP4, TP5, TP6, TP7	Test point, miniature, SMT	5019	Keystone
1	U1	IC, LM5137-Q1, 80V dual synchronous buck controller, VQFN-36	LM5137FDQRHARQ1	TI
1	PCB1	PCB, FR4, 6 layer, 2oz, 84mm × 74mm	PCB	–

## 5 Additional Information

### 5.1 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.  
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## 6 Device and Documentation Support

### 6.1 Device Support

#### 6.1.1 Development Support

For development support see the following:

- For TI's reference design library, visit [TI Designs](#)
- For TI's WEBENCH design environments, visit the [WEBENCH® Design Center](#)
- LM(2)5137-Q1 DC/DC controller [quickstart calculator](#) and [PSPICE](#) simulation models

### 6.2 Documentation Support

#### 6.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [LM5137-Q1 Automotive, 4V to 80V, 100% Duty Cycle Capable, Dual-Channel Synchronous Buck Controller Family for Functional Safety Applications](#) data sheet
- Texas Instruments, [LM5143-Q1 4-Phase Buck Regulator Design](#) application report
- Texas Instruments, [Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout](#) application report
- Texas Instruments, [Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics](#) analog design journal
- Texas Instruments, [AN-2162 Simple Success with Conducted EMI from DC-DC Converters](#) application report
- White papers:
  - Texas Instruments, [Valuing Wide  \$V\_{IN}\$ , Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications](#)
  - Texas Instruments, [An Overview of Conducted EMI Specifications for Power Supplies](#)
  - Texas Instruments, [An Overview of Radiated EMI Specifications for Power Supplies](#)

#### 6.2.1.1 PCB Layout Resources

- Texas Instruments, [Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout](#) application report
- Texas Instruments, [AN-1149 Layout Guidelines for Switching Power Supplies](#) application report
- Texas Instruments, [AN-1229 Simple Switcher PCB Layout Guidelines](#)
- Texas Instruments, [Constructing Your Power Supply – Layout Considerations](#) seminar
- Texas Instruments, [Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x](#) application report

#### 6.2.1.2 Thermal Design Resources

- Texas Instruments, [AN-2020 Thermal Design by Insight, Not Hindsight](#) application report
- Texas Instruments, [AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages](#) application report
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#) application report
- Texas Instruments, [Thermal Design Made Simple with LM43603 and LM43602](#) application report
- Texas Instruments, [PowerPAD™ Thermally Enhanced Package](#) application report
- Texas Instruments, [PowerPAD™ Made Easy](#) application report
- Texas Instruments, [Using New Thermal Metrics](#) application report

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (July 2024) to Revision A (August 2024)</b>	<b>Page</b>
• First public release of the EVM user's guide.....	1
• Updated the hardware image.....	1
• Updated the application circuit diagrams.....	4
• Added <a href="#">Section 4.2.2</a> .....	18

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## STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
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**NOTE:**

**EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.**

### 3 Regulatory Notices:

#### 3.1 United States

##### 3.1.1 Notice applicable to EVMs not FCC-Approved:

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

##### 3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

#### **CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

#### **FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

#### 3.2 Canada

##### 3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

#### **Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### **Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.



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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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3.3.1 *Notice for EVMs delivered in Japan:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page) 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 <https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html>

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3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

- 
4. *EVM Use Restrictions and Warnings:*
    - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
    - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
    - 4.3 *Safety-Related Warnings and Restrictions:*
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      - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
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