User's Guide

LM61495RPHEVM EVM User's Guide

ABSTRACT

The LM61495RPHEVM evaluation module (EVM) is designed to help customers evaluate the performance of the LM61495-Q1 synchronous step-down voltage converter. The EVM contains one LM61495-Q1 device in a 16-pin wettable flanks QFN (VQFN-HR) HotRod™ package. It is capable of delivering 5-V output voltage and up to 10-A load current with exceptional efficiency and output accuracy in a very small solution size. The EVM provides multiple power connectors, jumpers, resistors and capacitors to enable connection and configuration of output voltage, spread spectrum, mode setting options, and more for customer convenience. It also provides a good layout example which is optimized for EMI performance and passes CISPR 25 Class 5 standards. The layout is also optimized for thermal performance, operating with ΘJA = 21.6°C/W on a 102 mm x 76 mm, 4-layer board with 2 oz / 1 oz / 1 oz / 2 oz copper thickness stack.

Table 1-1. Device and Package Configurations

CONVERTER	IC	PACKAGE
U1	LM61495-Q1	16-pin wettable flanks HotRod QFN (VQFN-HR) 3.5 mm × 4.5 mm × 0.9 mm

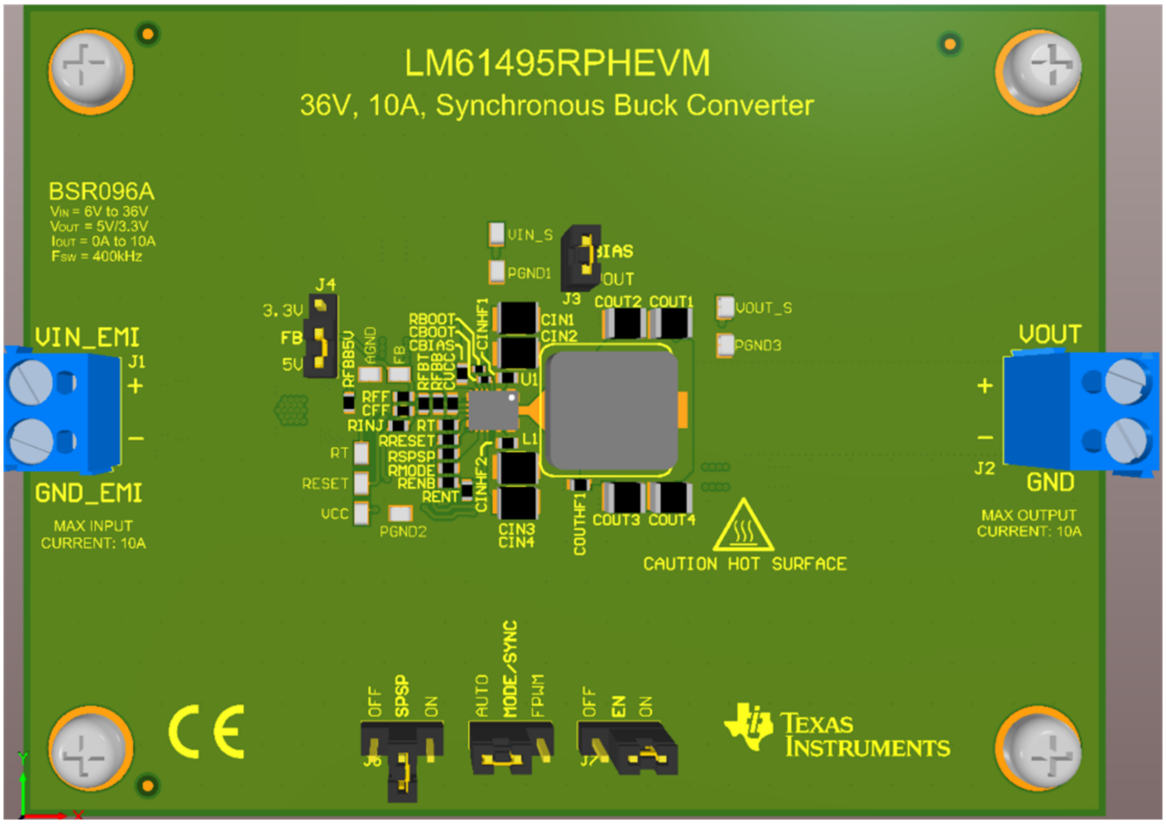


Figure 1-1. LM61495RPHEVM 3D Board Image

Table of Contents

List of Figures

List of Tables

Trademarks

HotRod™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

1.1 LM61495RPHEVM Synchronous Step-Down Voltage Converter

The LM61495-Q1 is an easy-to-use synchronous step-down DC-DC converter capable of driving up to 10 A of load current from a supply voltage ranging from 3 V to 36 V. The LM61495-Q1 provides exceptional efficiency and output accuracy in a very small solution size. The LM61495-Q1 implements peak-current-mode control. Additional features such as adjustable/synchronizable switching frequency, pin selectable dual-random spread spectrum (DRSS), true slew rate control, FPWM/AUTO selection, power-good/RESET flag, and precision enable provide both flexible and easy-to-use solutions for a wide range of applications. Automatic frequency foldback (AUTO mode) at light load and optional external bias improve efficiency over the entire load range. The device family requires few external components and has a pinout designed for simple PCB layout with excellent EMI and thermal performance. Protection features include thermal shutdown, input undervoltage lockout, cycle-by-cycle current limiting, and hiccup short-circuit protection. The LM61495-Q1 is pin-to-pin compatible with LM62460-Q1 and LM61480-Q1 for easy current scaling.

The pin configuration of the LM61495-Q1 is shown in Figure 1-1.

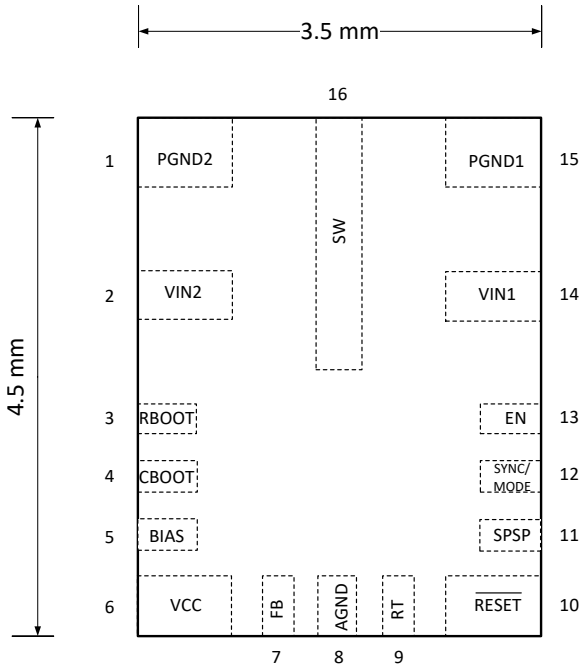


Figure 1-1. LM61495-Q1 Pin Configuration (16-Pin VQFN-HR Package Top View)

2 Quick Start

1. Connect the voltage supply between VIN_EMI and GND_EMI terminals using short, thick wires.
2. Connect the load of the converter between VOUT and GND (J2) terminals, using short, thick wires.
3. Set the supply voltage (V_{IN}) at an appropriate level between 6 V to 36 V. Set the current limit of the supply to an appropriate level depending on the connected load.
4. Turn on the power supply. With the default configuration, the EVM should power up and provide V_{OUT} = 5 V.
5. Monitor the output voltage. The maximum rated load current is 10 A.

3 Detailed Descriptions

This section describes the connectors and the test points on the EVM.

VIN_EMI (J1) Input voltage to the converter connecting to V_{IN} of the converter through an EMI filter.

VIN_EMI terminal connects to the input capacitors and the VIN pins of the LM61495-Q1 through an input EMI filter. Connect the supply voltage (battery, bench-top supply, or other supply) between VIN_EMI and GND_EMI connectors. The voltage range should be higher than 3.5 V for the device to start up, and above 3V to continue operation. V_{IN} higher than 6 V provides regulated 5 V output voltage. V_{IN} should be no higher than 36 V to avoid damaging the device. The current limit on the supply must be high enough to provide the needed supply current, otherwise the supply voltage may not maintain the desired voltage. The supply voltage should be connected to the board with short, thick wires to handle the pulsing input current.

GND_EMI (J1) Ground connection near the input filter.

This is the current return path for the supply connected to VIN_EMI.

VOUT (J2) Output voltage of the converter.

VOUT terminal connects to the power inductor and the output capacitors. Connect the loading device between VOUT and GND connectors on J2 to load the converter output. Connect the loading device to the board with short, thick wires to handle the large DC output current.

GND (J2) Ground connection near the output.

This is the current return path for the output voltage connected to VOUT.

Input Filter Prevents noise from contaminating supply voltage

The input filter consists of a ferrite bead, filter inductor, and filter capacitors, located on the bottom side of the PCB. The output of the filter is connected to the V_{IN} net, which is connected to the VIN pins of the LM61495-Q1 and the input capacitors.

Conducted EMI arises from the normal operation of switching circuits. The ON and OFF actions of the power switches generate large discontinuous currents. The discontinuous currents are present at the input side of buck converters. Voltage ripple generated by discontinuous currents can be conducted to the voltage supply of the buck converter via physical contact of the conductors. Without control, excessive input voltage ripple can compromise operation of other devices connected to the source. The input filter helps to smooth out the voltage perturbations leading to the source.

VIN_S Test point to monitor the input voltage of the device.

PGND1 Test point for GND reference when measuring VIN_S.

VOUT_S Test point to monitor the output voltage of the device.

PGND3 Test point for GND reference when measuring VOUT_S.

FB Test point for measuring the voltage on the FB pin of the device.

AGND Test point for AGND reference when measuring FB.

RT Test point for measuring the voltage on the RT pin of the device.

RESET Test point for measuring the voltage on the RESET (power good) pin of the device.

VCC Test point for measuring the voltage on the VCC pin of the device.

PGND2 Additional GND reference point for test point measurements.

BIAS jumper (J3) Plate the shunt to connect V_{OUT} to BIAS to improve efficiency.

FB jumper (J4) Place the shunt connecting FB and 5V to set V_{OUT} = 5V. Place the shunt connecting FB and 3.3V to set V_{OUT} = 3.3V.

SPSP jumper (J5)	Place the shunt connecting SPSP and OFF to disable spread spectrum. Place the shunt connecting SPSP and ON to enable spread spectrum. Remove the shunt to enable spread spectrum with ripple cancellation.
MODE/SYNC jumper (J6)	Place the shunt connecting MODE/SYNC and AUTO to enable automatic frequency foldback in light loads to improve light load efficiency. Place the shunt connecting MODE/SYNC and FPWM to enable forced FPWM mode to maintain a constant switching frequency regardless of load. Apply a clock signal to the MODE/SYNC pin to synchronize the device to an external clock.
EN jumper (J7)	Place the shunt connecting EN and OFF to disable the device. Place the shunt connecting EN and ON to enable the device. Remove the shunt to enable undervoltage lockout to enable the device when the supply voltage exceeds 6V.

4 Schematic

The LM61495RPHEVM schematic is shown in Figure 4-1.

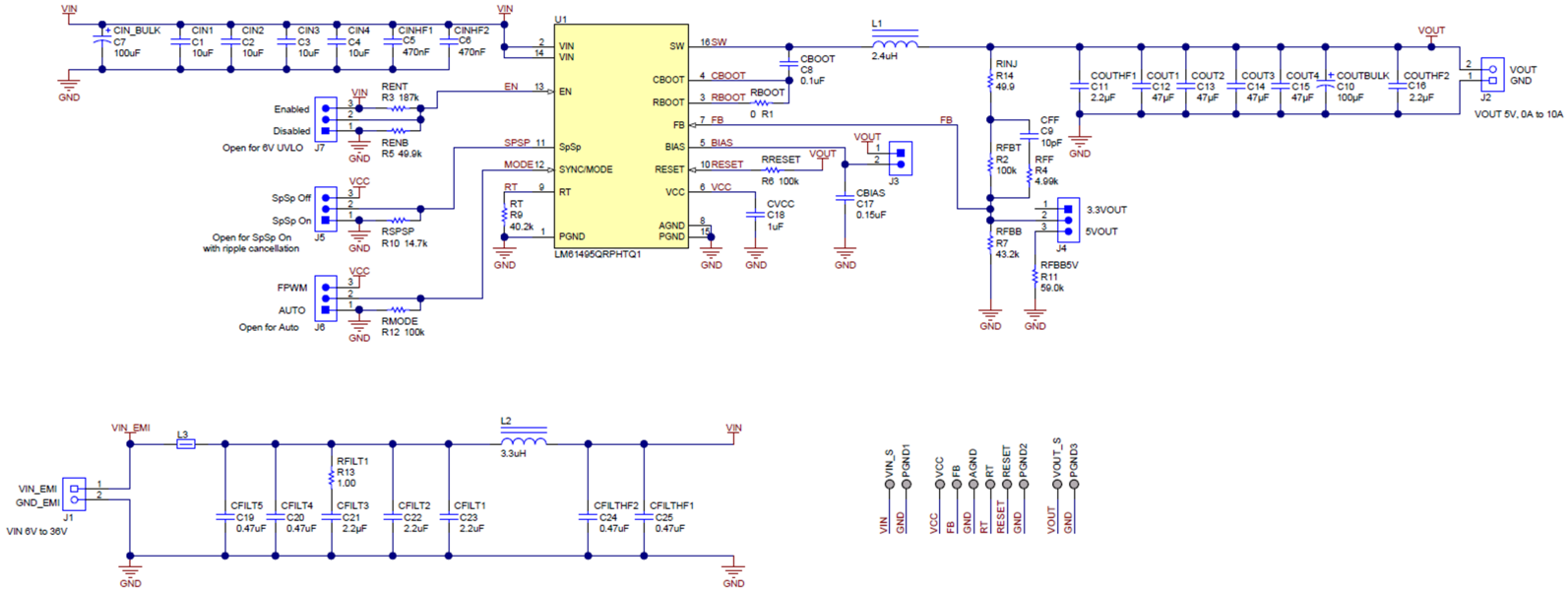


Figure 4-1. LM61495RPHEVM Schematic

5 Board Layout

Figure 5-1 through Figure 5-6 show the board layout for the LM61495RPHEVM. The EVM offers resistors, capacitors, and jumpers to configure the output voltage and precision enable pin, and set frequency and external clock synchronization among the other features of the LM61495-Q1.

The PCB is optimized for thermal performance. The board contains 4 layers. There are 2-oz copper layers on the top and bottom and 1-oz copper mid-layers. The LM61495-Q1 does not have a thermal pad so the best path to move the heat out of the IC is through the pins and into the board. The PGND pins connect to the large GND plane which spreads the heat to the rest of the board. The GND plane also has thermal vias to spread the heat more efficiently to other layers for additional improved thermal performance.

The PCB is also optimized for EMI performance. The layout minimizes the area of high dv/dt nodes like SW and BOOT. The small high-frequency ceramic input capacitors are placed very close to the IC to minimize the loop formed from VIN pins, through the capacitor, to the PGND pins. The board also features an EMI filter on the back-side of the board with options for an inductor, ferrite bead, and filter capacitors to tune the desired EMI performance. The full filter may not be necessary to pass particular EMI requirements but the components and pads are available for flexibility in adjustments.

The screw terminals J1 and J2 allow for high-current connections to the board. Jumper J3 connects V_{OUT} to BIAS for improved light-load efficiency. Jumper J4 allows the user to select the output voltage, 5V or 3.3V. J5 allows the user to turn on or off Spread Spectrum. J6 allows the user to operate the device in AUTO mode (pulse frequency modulation at light loads) or FPWM (forced pulse width modulation). The MODE/SYNC pin on J6 also acts as a SYNC pin to synchronize to an external clock if desired. J7 allows the user to enable or disable the IC.

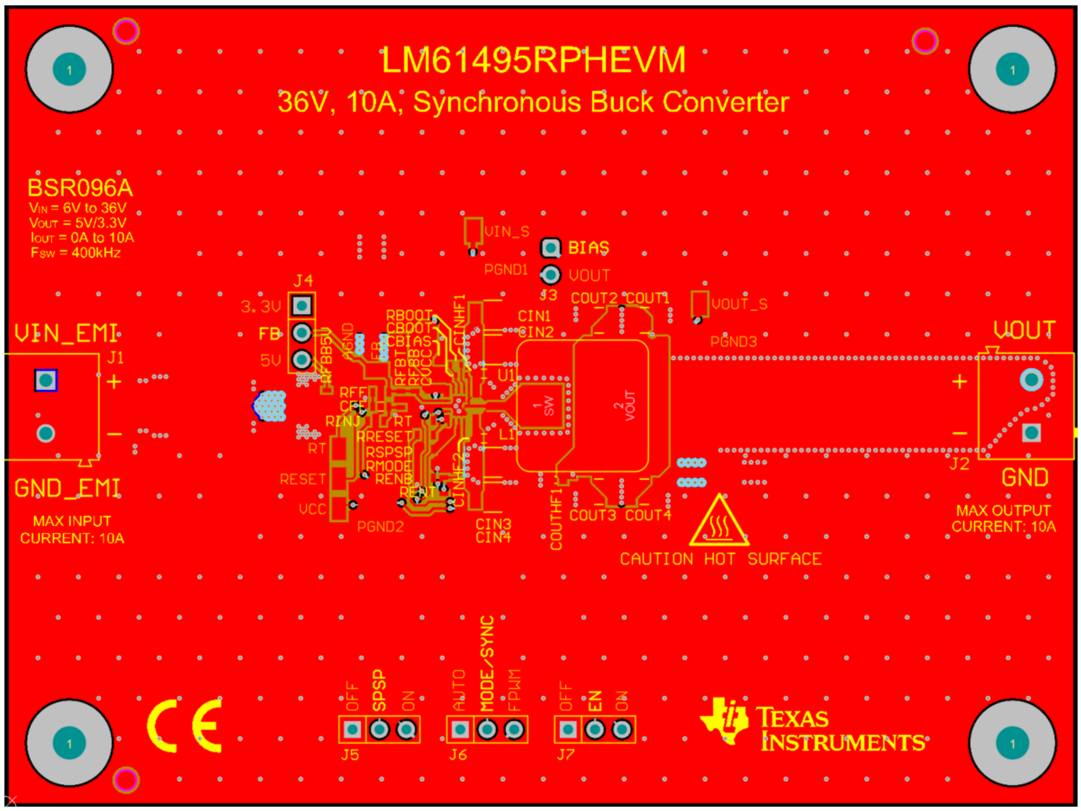


Figure 5-1. Top layer and top silkscreen

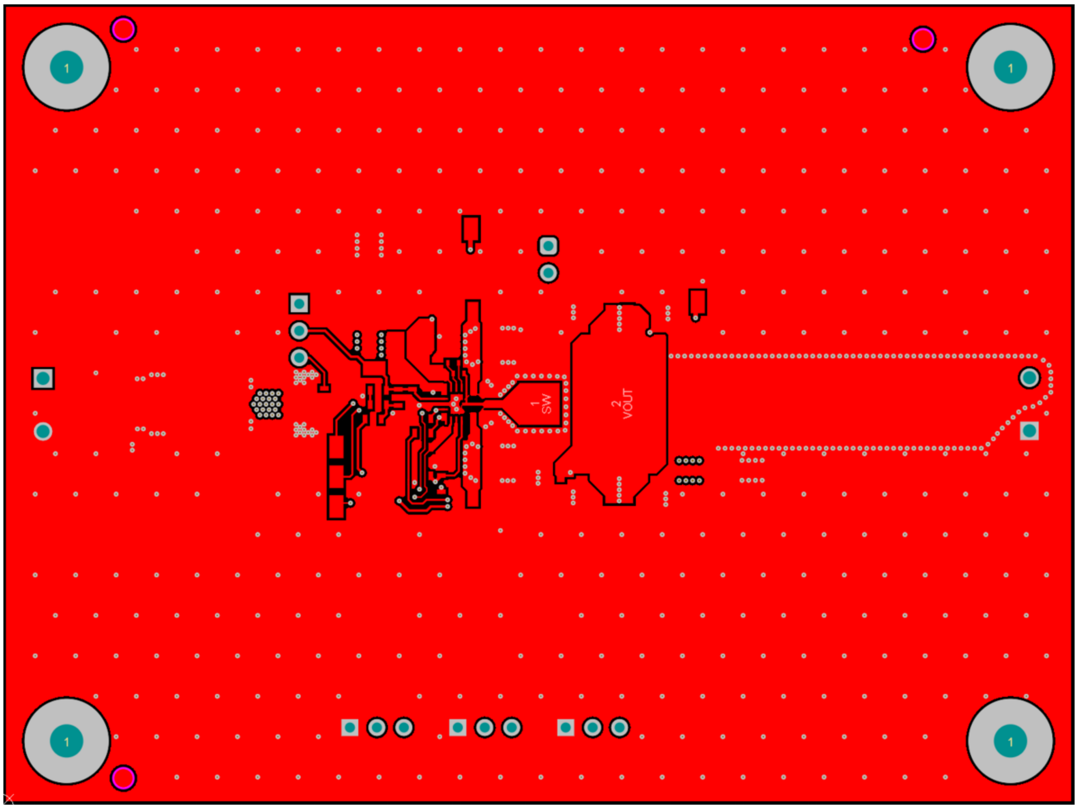


Figure 5-2. Top layer routing

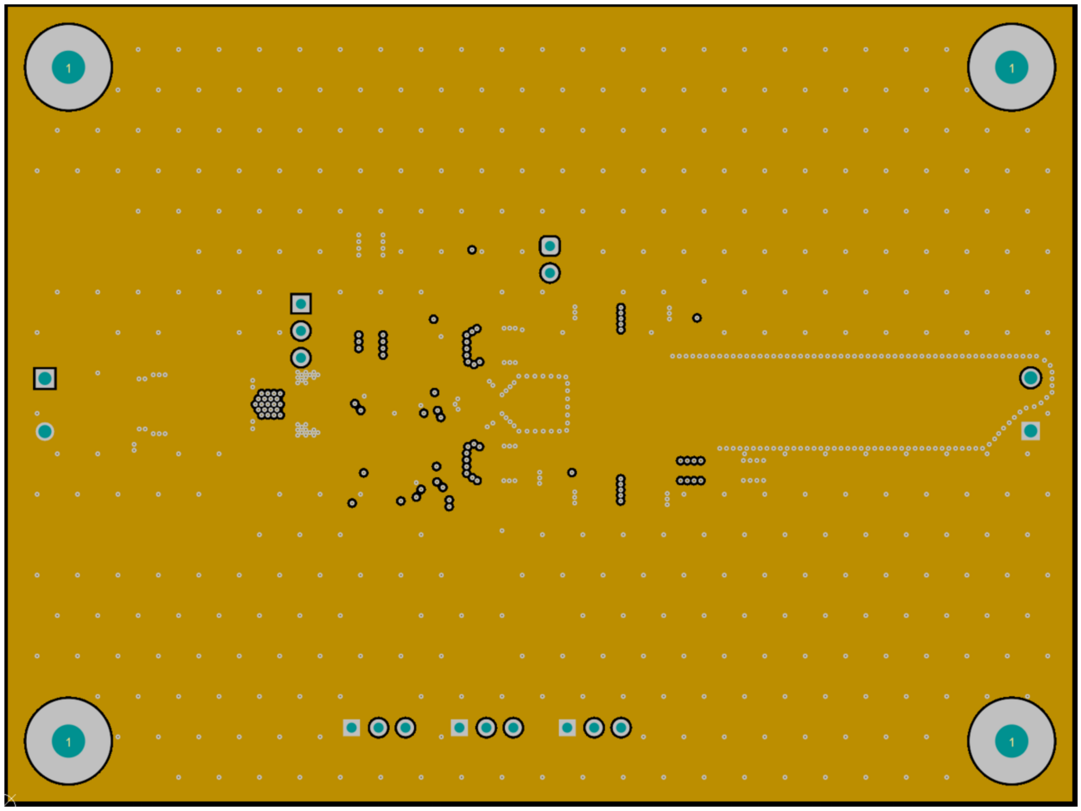


Figure 5-3. Mid-layer 1 ground plane

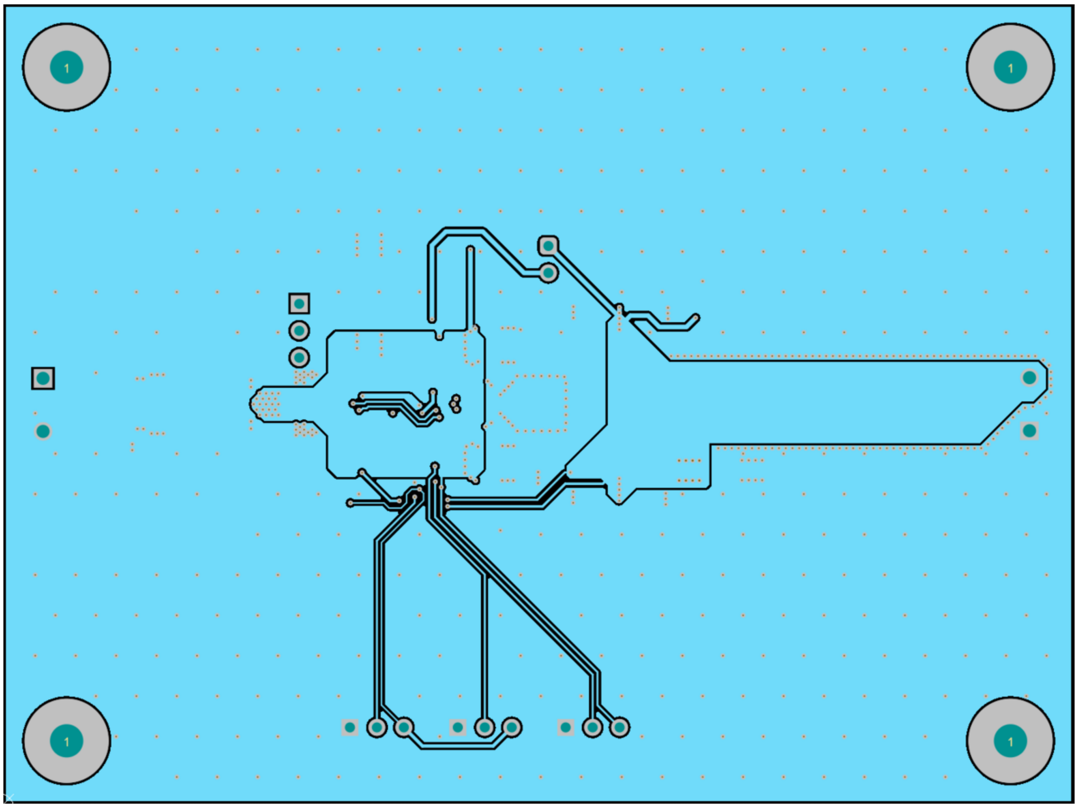


Figure 5-4. Mid-layer 2 routing

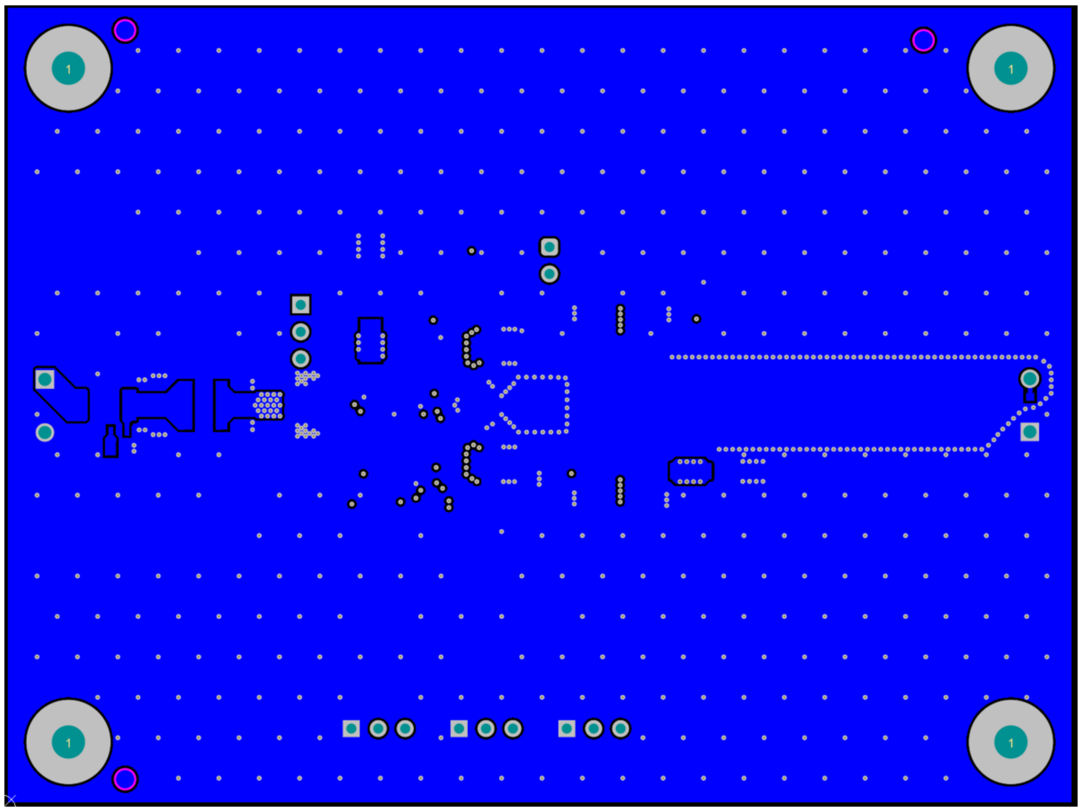


Figure 5-5. Bottom layer routing

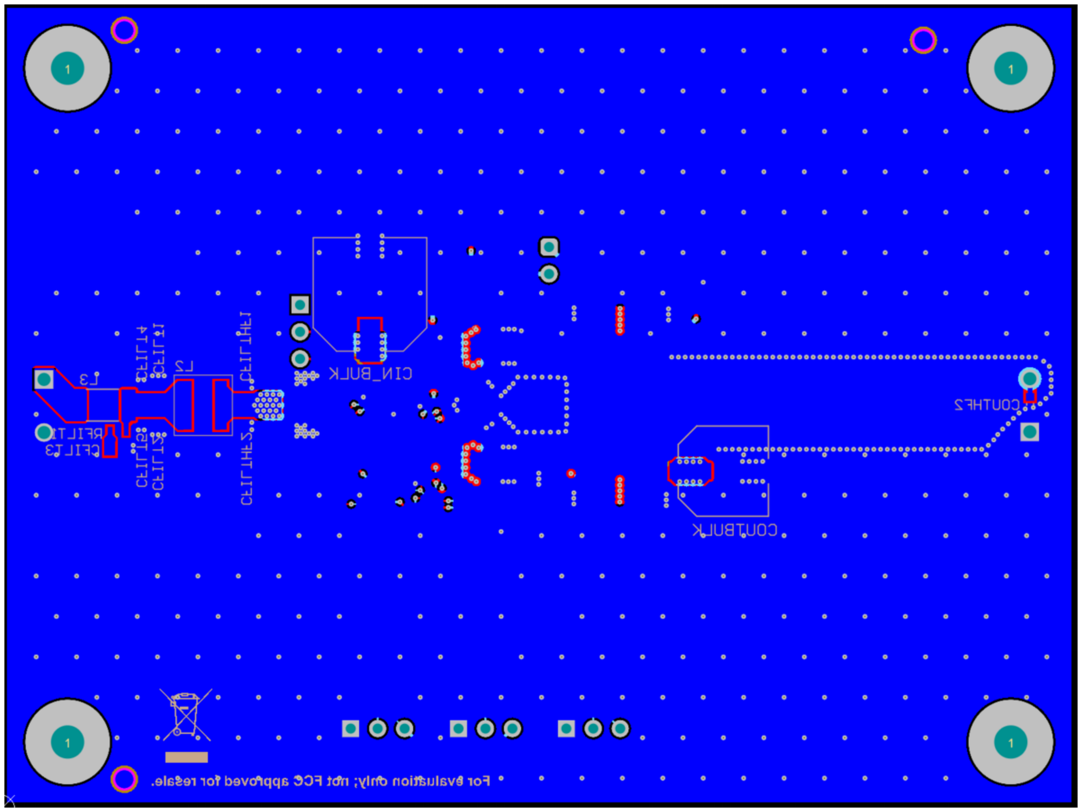


Figure 5-6. Bottom layer and bottom silkscreen

6 Board Curves

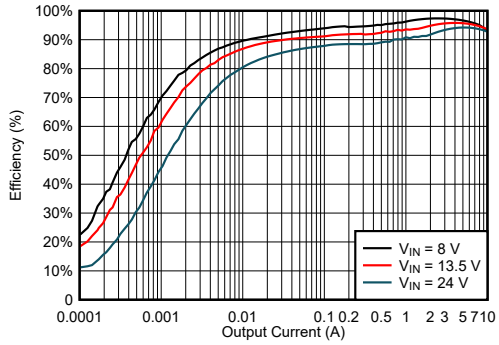


Figure 6-1. LM61495-Q1 5-V 400-kHz Efficiency in Auto Mode

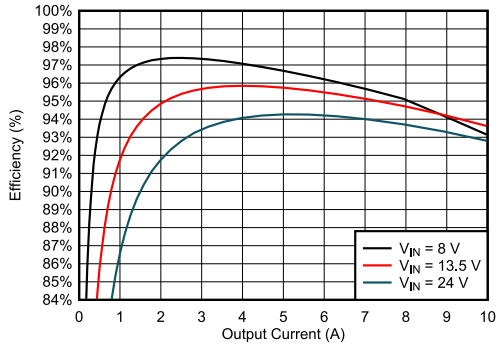


Figure 6-2. LM61495-Q1 5-V 400-kHz Efficiency in FPWM Mode

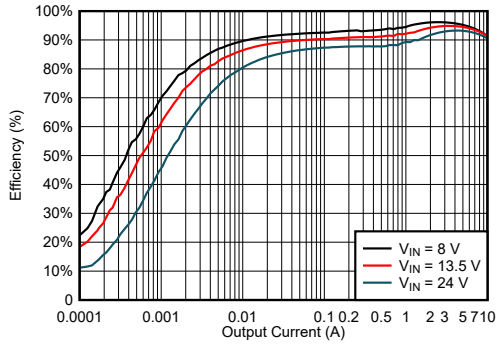


Figure 6-3. LM61495-Q1 3.3-V 400-kHz Efficiency in Auto Mode

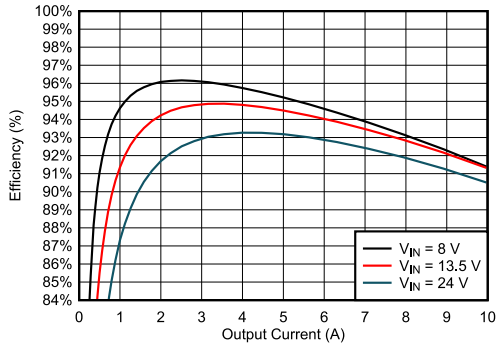


Figure 6-4. LM61495-Q1 3.3-V 400-kHz Efficiency in FPWM Mode

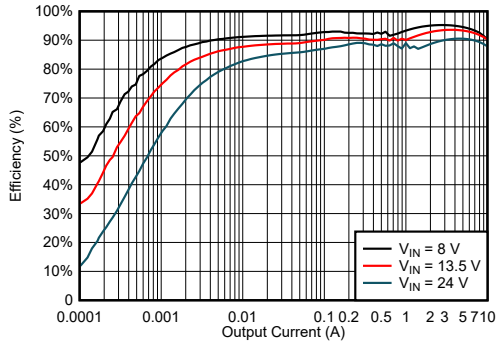


Figure 6-5. LM61495-Q1 5-V 2.2-MHz Efficiency in Auto Mode

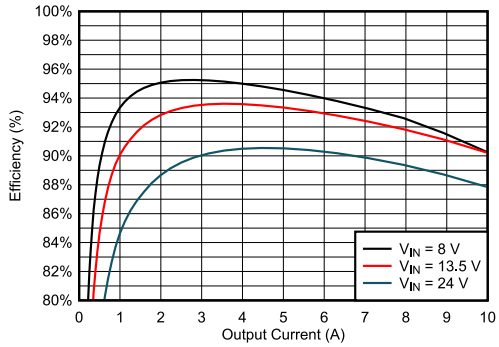


Figure 6-6. LM61495-Q1 5-V 2.2-MHz Efficiency in FPWM Mode

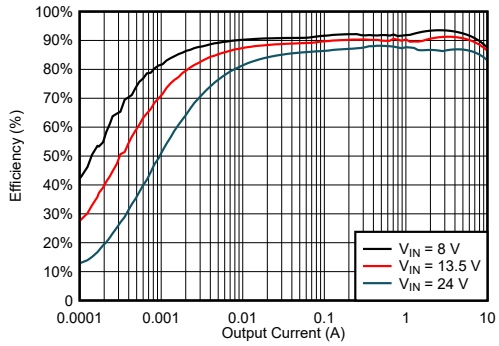


Figure 6-7. LM61495-Q1 3.3-V 2.2-MHz Efficiency in Auto Mode

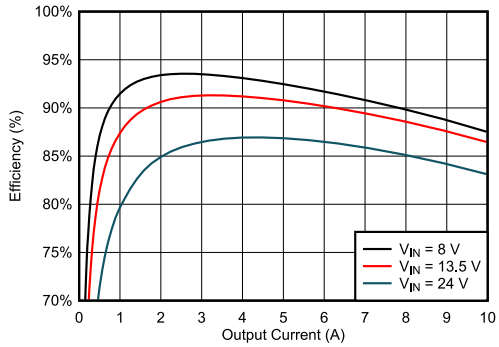


Figure 6-8. LM61495-Q1 3.3-V 2.2-MHz Efficiency in FPWM Mode

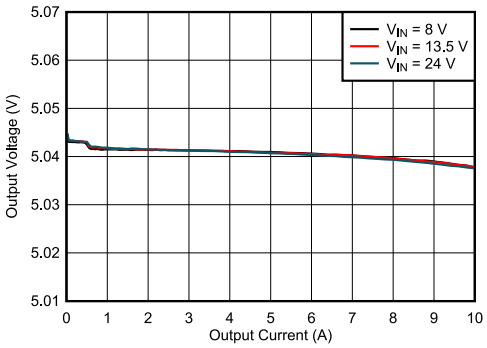


Figure 6-9. LM61495-Q1 5-V 400-kHz V_{OUT} Regulation in Auto Mode

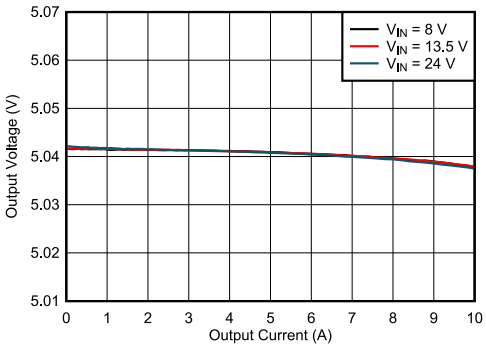
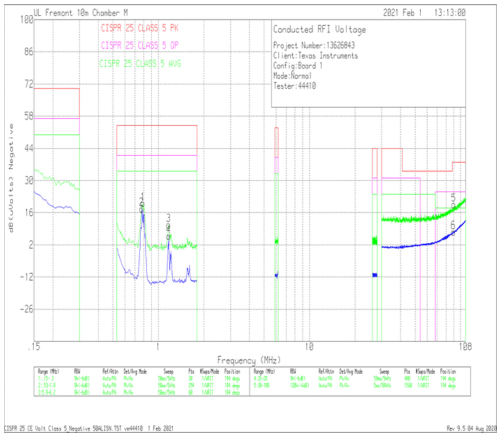


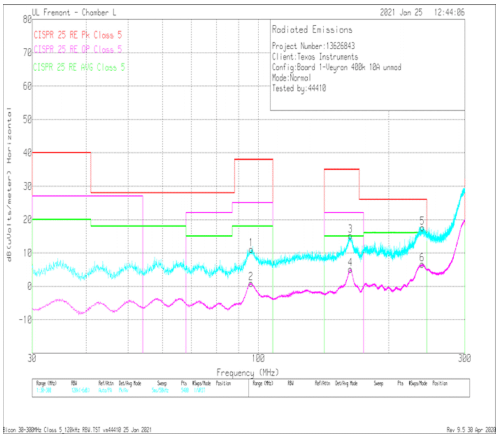
Figure 6-10. LM61495-Q1 5-V 400-kHz V_{OUT} Regulation in FPWM Mode



V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A

Frequency Tested: 0.15 MHz to 108 MHz

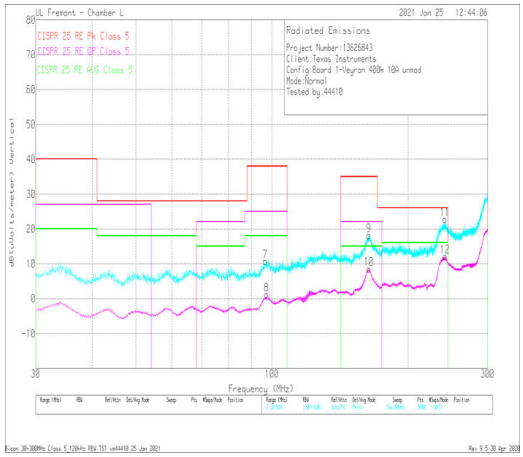
Figure 6-11. Conducted EMI versus CISPR25 Class 5 Limits (Green: Peak Signal, Blue: Average Signal)



V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A

Frequency Tested: 30 MHz to 300 MHz

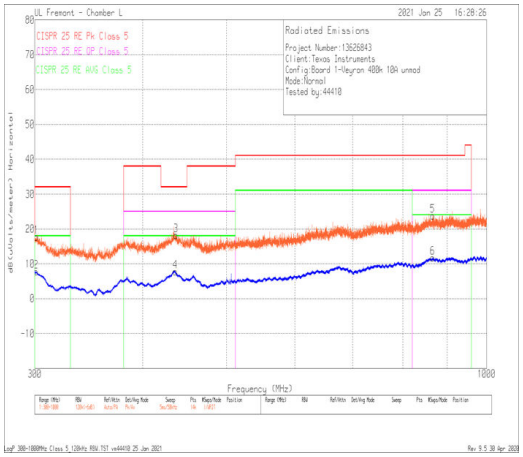
Figure 6-12. Radiated EMI Bicon Horizontal versus CISPR25 Class 5 Limits



V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A

Frequency Tested: 30 MHz to 300 MHz

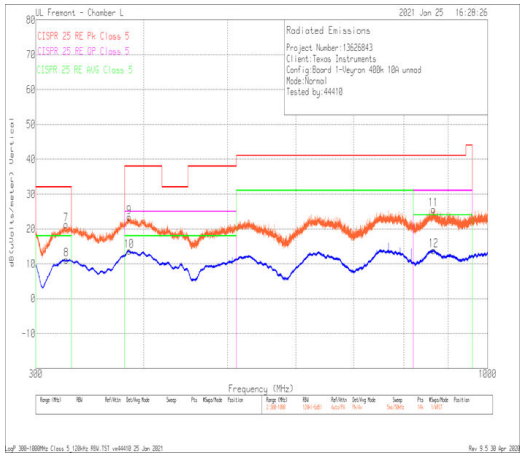
Figure 6-13. Radiated EMI Bicon Vertical versus CISPR25 Class 5 Limits



V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A

Frequency Tested: 300 MHz to 1 GHz

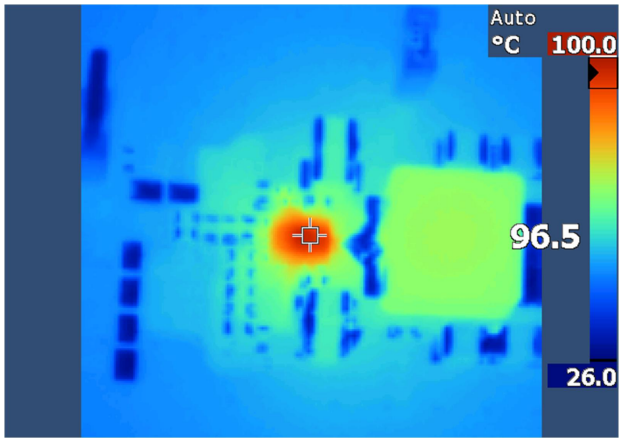
Figure 6-14. Radiated EMI Log Horizontal versus CISPR25 Class 5 Limits



V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A

Frequency Tested: 300 MHz to 1 GHz

Figure 6-15. Radiated EMI Log Vertical versus CISPR25 Class 5 Limits



V_{OUT} = 5 V F_{SW} = 400 kHz I_{OUT} = 10 A

Figure 6-16. LM61495-Q1 EVM Thermal Performance with V_{IN} = 12 V Providing ΘJA = 21.6°C/W

Table 6-1. BOM for Board Curves

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	C_{IN} + C_{HF}	L
3.3 V	400 kHz	43.2 kΩ	4 x 47 µF + 100 µF electrolytic + 2 x 2.2 µF	4 × 10 µF + 2 × 470 nF + 100 µF electrolytic	2.4 µH (744325240)
3.3 V	2200 kHz	43.2 kΩ	2 x 47 µF + 100 µF electrolytic + 2 x 2.2 µF	2 × 10 µF + 2 × 470 nF + 100 µF electrolytic	0.68 µH (744373460068)
5 V	400 kHz	24.9 kΩ	4 x 47 µF + 100 µF electrolytic + 2 x 2.2 µF	4 × 10 µF + 2 × 470 nF + 100 µF electrolytic	2.4 µH (744325240)
5 V	2200 kHz	24.9 kΩ	2 x 47 µF + 100 µF electrolytic + 2 x 2.2 µF	2 × 10 µF + 2 × 470 nF + 100 µF electrolytic	0.68 µH (744373460068)

7 Bill of Materials

The bills of materials of the LM61495RPHEVM is shown in Table 7-1.

Table 7-1. LM61495RPHEVM 10-A 400-kHz EVM Bill of Materials

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
AGND, FB, PGND1, PGND2, PGND3, RESET, RT, VCC, VIN_S, VOUT_S	Test Point, SMT	Harwin	S2751-46R	10
C1, C2, C3, C4	CAP, CERM, 10 uF, 50 V, +/- 10%, X5R, 1210	TDK	C3225X5R1H106K250AB	4
C5, C6	CAP, CERM, 0.47 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E3X7R1H474K080AB	2
C7	CAP, AL, 100 uF, 63 V, +/- 20%, 0.35 ohm, AEC-Q200 Grade 2, SMD	Panasonic	EEE-FK1J101P	1
C8	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	TDK	CGA2B3X7R1H104K050BB	1
C9	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	TDK	CGA3E2C0G1H100D080AA	1
C10	CAP, AL, 100 µF, 16 V, +/- 20%, AEC-Q200 Grade 3, SMD	Panasonic	EEE-1CA101AP	1
C11, C16	CAP, CERM, 2.2 µF, 10 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GRM188R71A225KE15J	2
C12, C13, C14, C15	CAP, CERM, 47 µF, 10 V,+/- 10%, X7S, AEC-Q200 Grade 1, 1210	MuRata	GCM32EC71A476KE02K	4
C17	CAP, CERM, 0.15 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E3X7R1H154K080AB	1
C18	CAP, CERM, 1 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCM188R71C105MA64D	1
C19, C20, C24, C25	CAP, CERM, 0.47 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E3X7R1H474K080AE	4
C21, C22, C23	CAP, CERM, 2.2 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	TDK	CGA4J3X7R1H225K125AB	3
H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	4
H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4
J1, J2	Terminal Block, 5 mm, 2x1, Tin, TH	Wurth Elektronik	691 101 710 002	2
J3	Header, 100mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S	1
J4, J5, J6, J7	Header, 100mil, 3x1, Gold, TH	Sullins Connector Solutions	PBC03SAAN	4
L1	Inductor, Shielded Drum Core, Superflux, 2.4 uH, 14 A, 0.0046 ohm, SMD	Wurth Elektronik	744325240	1
L2	Inductor, Shielded, Composite, 3.3 µH, 8.1 A, 0.02 ohm, AEC-Q200 Grade 1, SMD	Coilcraft	XAL5030-332MEB	1
L3	Ferrite Bead, 100 ohm @ 100 MHz, 8 A, 1812	Wurth Elektronik	74279226101	1
R1	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04020000Z0ED	1
R2, R6, R12	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA	3
R3	RES, 187 k, 1%, 0.1 W, 0603	Yageo	RC0603FR-07187KL	1
R4	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06034K99FKEA	1
R5	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060349K9FKEA	1
R7	RES, 43.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060343K2FKEA	1
R9	RES, 40.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060340K2FKEA	1
R10	RES, 14.7 k, 1%, 0.1 W, 0603	Yageo	RC0603FR-0714K7L	1
R11	RES, 59.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060359K0FKEA	1
R13	RES, 1.00, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031R00FKEA	1
R14	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060349R9FKEA	1
SH-J3, SH-J4, SH-J5, SH-J6, SH-J7	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G	5
U1	LM61495QRPHTQ1, RPH0016A (VQFN-HR-16)	Texas Instruments	LM61495QRPHTQ1	1

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2019) to Revision A (March 2021)	Page
• Added Detailed Descriptions	5
• Added board curves and updated board images (schematic, layout, and 3D image)	12

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265