LM5175 4-Switch Buck-Boost Converter High Density EVM

User's Guide

Literature Number: SNVU439
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Contents

List of Figures

List of Tables

LM5175 High Density Evaluation Module

The LM5175EVM-HD high density evaluation module (EVM) is a 4-switch synchronous buck-boost DC/DC regulator that employs synchronous rectification to achieve high conversion efficiency in a small footprint at 72-W output power. It operates over a wide input voltage range of 5.5 V to 42 V providing a fixed 12-V output. The output voltage is adjustable using only a single resistor or voltage source, permitting the user to customize the output voltage from 0.8 V to 24 V as needed.

Such user configurability is especially useful when traditional buck or boost DC/DC converters cannot meet system requirements for operating input and output voltage ranges, efficiency, power density, or volume. More specifically, this LM5175 EVM is ideal for applications where the input voltage is expected to vary continuously above, equal to, or below the regulated output voltage setpoint in buck, buck-boost, and boost operating modes, respectively.

The module design uses the LM5175 high performance, synchronous buck-boost controller with current-mode PWM control loop and adaptive slope compensation, integrated high- and low-side MOSFET gate drivers, cycle-by cycle overcurrent protection, precision enable, and AEC-Q100 automotive grade qualification. The EVM's output voltage has better than 1.5% setpoint accuracy. The switching frequency is 400 kHz and is synchronizable to a higher frequency if required. Moreover, a dither function provides a smoother EMI signature for noise-sensitive applications. Input UVLO protects the module at low input voltage conditions, and it is possible to tailor the minimum operating input voltage to the application requirements by suitable adjustment of the programmable input UVLO components.

The LM5175 buck-boost PWM controller is available in HTSSOP-28 PowerPAD™ package to enable high power density and superior thermal performance. Please consult the LM5175 datasheet for more details. Even though the LM5175 is WEBENCH® Designer enabled, the reader is also encouraged to avail of the LM5175 quick-start calculator, particularly for guidance with powertrain and compensation circuit component selection.

1 High Density EVM Description

The LM5175 high density EVM is designed to use a regulated or non-regulated input bus (5.5 V–42 V) to produce a tightly regulated output of 12 V at power levels up to 72 W. The output current range is 0 A to 6 A across the full input voltage operating range. In particular, the converter is rated to accommodate the high inductor current when operating in deep boost mode (low input voltage) at full load.

The EVM is intended to demonstrate the LM5175 PWM controller in a typical battery voltage to fixed 12-V bus application while providing a number of test points to evaluate the performance of the LM5175. The output voltage is user-adjustable by connecting a resistor from the TRIM terminal to VOUT or GND as appropriate. Many of the power train passive components selected in this design are available with AEC-Q200 qualification, including ceramic and electrolytic input and output capacitors as well as the current sense resistor.

1.1 Typical Applications

- Point-of-load synchronous buck-boost regulators
- High current density modules
- Communications, cloud, storage
- Automotive body electronics, infotainment, audio amplification, and start-stop
- Embedded computing, industrial PC

1.2 Features and Electrical Performance

- Adjustable output voltage, nominally set to 12 V with 1.5% feedback accuracy
- Wide input voltage operating range of 5.5 V to 42 V through buck and boost operating modes
- Ultra-high power conversion efficiency:
  - >98% at 12 V x 6 A output over 8 V to 18 V input range
  - >96% at 12 V x 3 A output over 5.5 V to 24 V input range
- 50 mm x 43 mm PCB footprint, including high-current input and output connectors and bulk capacitors
- 400-kHz free-running switching frequency set by resistor
- Cycle-by-cycle overcurrent protection via shunt resistor current sensing
- Default forced PWM (CCM) fixed switching operation with option to set diode emulation mode (DCM)
- User-adjustable soft-start time set to 8 ms
- Monotonic pre-bias output voltage startup
- Programmable input UVLO set to turn on and off at 5.5 V and 4.8 V, respectively
- Current-mode PWM control architecture supporting all-ceramic output capacitor design or ceramic/electrolytic implementation
- Output voltage adjustable from 0.8 V to 24 V using trim resistance or external voltage source
- Spread spectrum dither option for reduced EMI
- Power Good indicator
- Input circuit damping and energy storage provided by bulk electrolytic capacitor
- Synchronizable to an external clock signal up to 600 kHz
- Simple access to IC features including PGOOD, ENABLE, TRIM and SYNC
- Convenient test points for simple, non-invasive measurements of converter performance

1.3 Thermal Performance

For an efficient high density buck-boost design, component selection (particularly power MOSFETs and inductor) seeks to attain lowest power dissipation, thus maximizing efficiency. In buck or boost modes, one low-side power MOSFET is completely off, offsetting the adjacent high-side device that necessarily conducts full current. For deep buck or boost operating points, MOSFET selection can tilt towards minimizing low-side power loss, thereby reducing that MOSFET's operating T_J.

In this design, the high-side MOSFETs' drains are attached on three PCB layers with short connections to VIN and VOUT power terminals through heat spreading copper planes. The low-side MOSFETs are attached to SW nodes copper polygons that are necessarily small to minimize capacitive & radiated EMI coupling. Maximizing performance in convective airflow, MOSFETs placed on the top side of the PCB are not airflow shadowed by taller profile components, e.g. inductor and electrolytic capacitors. The inductor placed on bottom side of the PCB impedes conductive heat transfer to the top, and the inductor inherently acts essentially as its own heat sink. If deemed necessary for a higher current design, a PCB layout to accommodate larger 5 mm x 6 mm footprint MOSFETs is attained with relatively minor edit to that presented here.

2 Electrical Performance Specifications

Table 1. Electrical Performance Specifications

Parameter	Test Conditions		MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input voltage range, V_{IN}	Non-operating				60	V
	Operating		5.5	12	42	
Input voltage turn on, $V_{IN(ON)}$	Set by EN/UVLO resistors		5.3	5.55	5.8	V
Input voltage turn off, $V_{IN(OFF)}$			4.6	4.85	5.1	V
Input voltage hysteresis, $V_{IN(HYS)}$				0.7		V
Input current, full load, $I_{IN(MAX)}$ (1)	I_{OUT} = 6 A	V_{IN} = 5.5 V		13.93		A
		V_{IN} = 42 V		1.84		A
Input current, no load, $I_{IN(NL)}$	I_{OUT} = 0 A	V_{IN} = 12 V		20		mA
		V_{IN} = 24 V		38		mA
Input current, disabled, $I_{IN(OFF)}$	V_{EN} = 0 V	V_{IN} = 12 V		1		mA
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT} (1)			11.88	12.00	12.12	V
Output current, I_{OUT}	V_{IN} = 5.5 V to 42 V		0		6	A
Output voltage regulation, ΔV_{OUT}	Load Regulation	I_{OUT} = 0 A to 6 A		0.2%		
	Line Regulation	V_{IN} = 5.5 V to 42 V		0.2%		
Output voltage ripple, $V_{OUT(AC)}$	I_{OUT} = 3 A	V_{IN} = 18 V		10		mVpp
Output overcurrent protection, I_{OCP}	V_{IN} = 18 V		9	11	13	A
Soft-start time, t_{SS}				8		ms
SYSTEM CHARACTERISTICS						
Switching frequency (free running), $F_{SW(nom)}$ (1)				400		kHz
Switching frequency range (using SYNC)			$F_{SW(nom)}$		600	kHz
Dither modulating frequency, F_{DITHER}	With Cd = 47 nF installed			10		kHz
Peak efficiency, η_{PK}	I_{OUT} = 4.5 A	V_{IN} = 12 V		98.5%		
Full load efficiency, η_{FULL}	I_{OUT} = 6 A	V_{IN} = 6 V		94.3%		
		V_{IN} = 8 V		96.6%		
		V_{IN} = 12 V		98.4%		
		V_{IN} = 24 V		96.8%		
		V_{IN} = 42 V		94.5%		
Loop bandwidth, f_c	V_{IN} = 18 V	I_{OUT} = 3 A		10		kHz
Phase margin, φ_M				55		°
External bias supply, $V_{BIAS-EXT}$	Connected to BIAS pin			12	36	V
Ambient temperature, T_A			-40	25	125	ºC
LM5175 junction temperature, T_J					125	ºC
PCB temperature hotspot, T_{PCB}					125	ºC

(1) The default output voltage and switching frequency are 12 V and 400 kHz, respectively. Efficiency and other parameters will change based on chosen output voltage, load current, and frequency.

3 Application Circuit Diagram

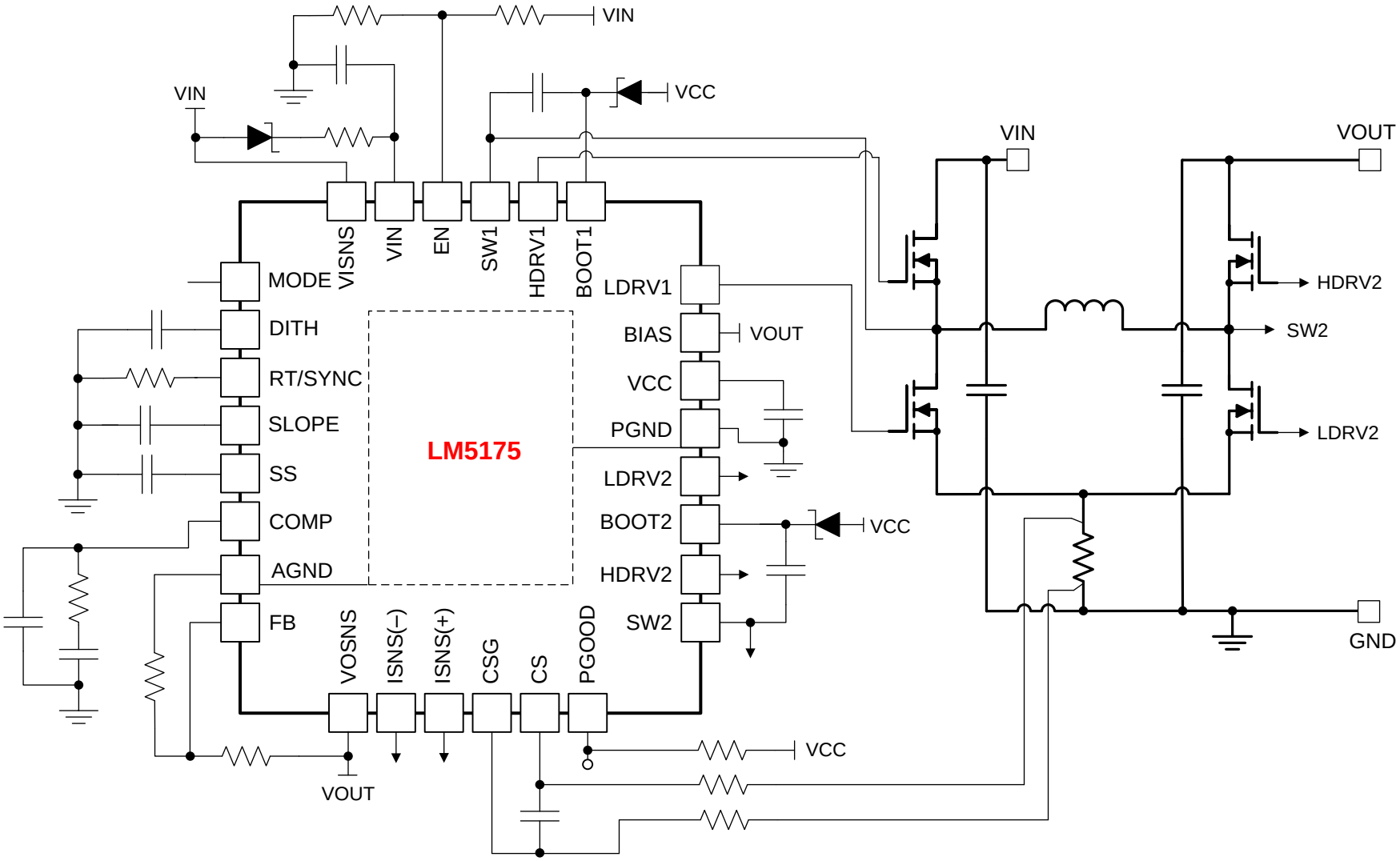


Figure 1. LM5175 Buck-boost Converter Circuit Diagram

4 EVM Photos

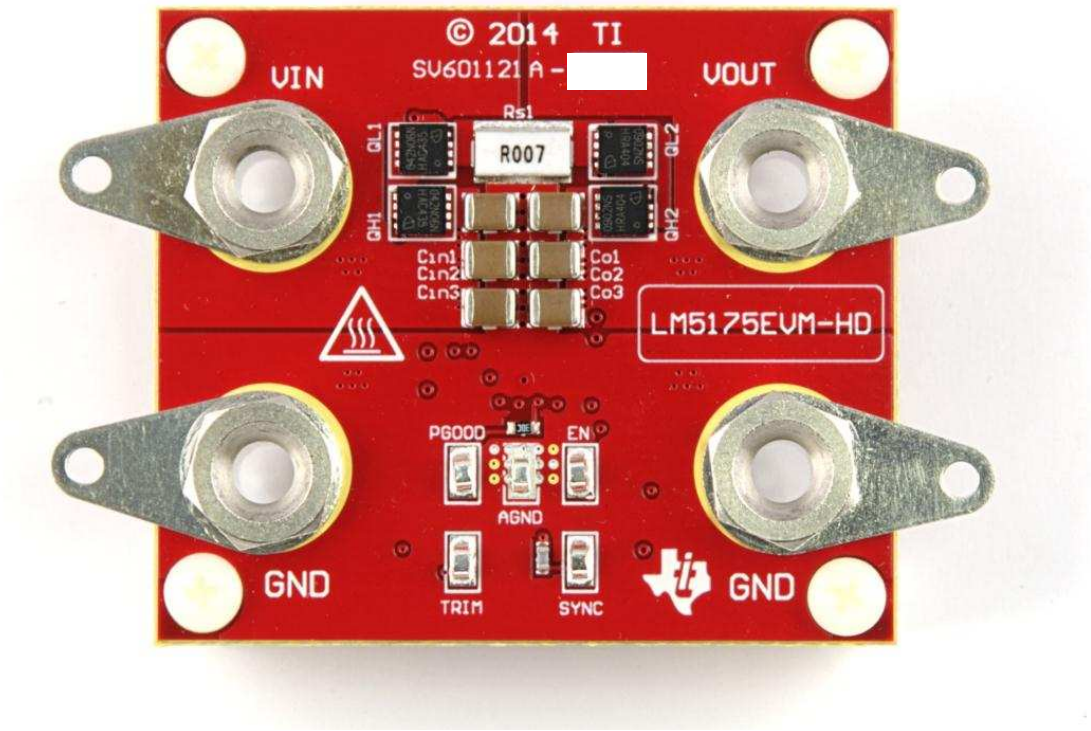


Figure 2. EVM top side

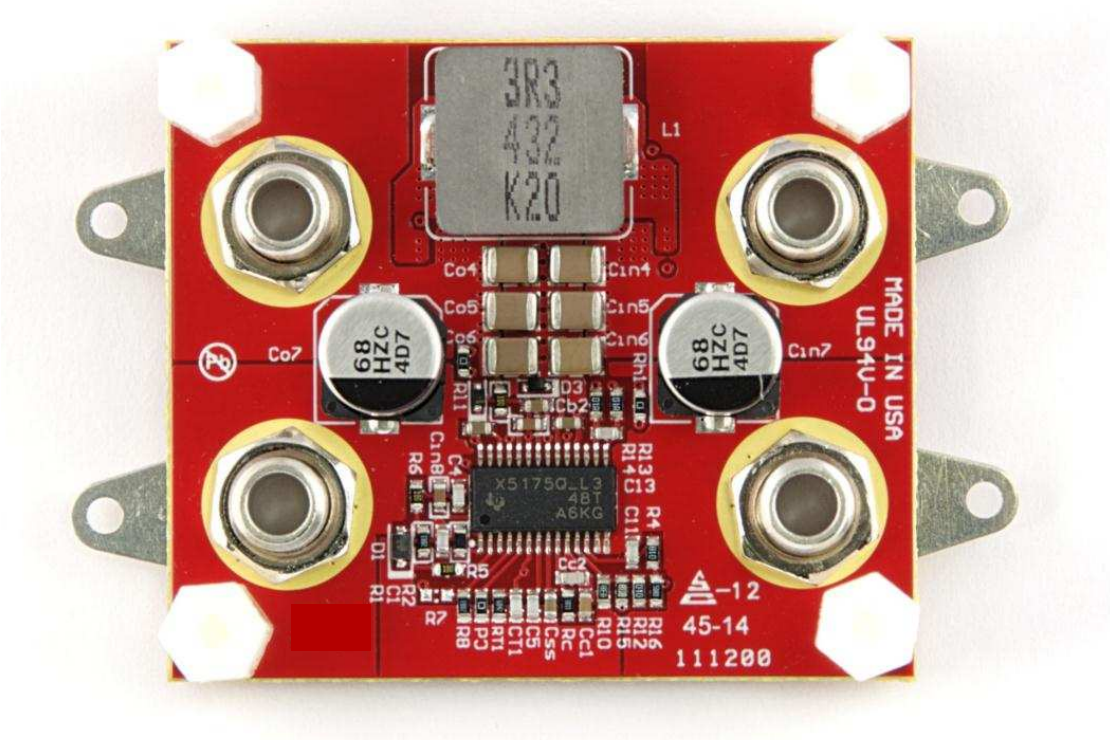


Figure 3. EVM bottom side

5 Signal Connections and Test Point Descriptions

5.1 Test Point Descriptions

Table 2. Test Point Descriptions

LABEL	DESCRIPTION
VIN	Input voltage positive power and sense connection
GND	Input voltage negative power and sense connection
VOUT	Output voltage positive power and sense connection
GND	Output voltage negative power and sense connection
AGND	Analog GND
SYNC	SYNC input
EN	ENABLE input; tie to GND to disable converter
PGOOD	Power Good output

5.2 Signal Connections

5.2.1 Input Voltage Monitoring

The LM5175EVM-HD provides two solder lug test points for measuring input voltage at the input banana connections. This allows the user to measure the actual input voltage without losses from input cables and connectors. All input voltage measurements should be made between VIN and GND test points.

5.2.2 Output Voltage Monitoring

The LM5175EVM-HD provides two solder lug test points for measuring output voltage at the output banana connections. This facilitates measurement of the output voltage without losses related to output cables and connectors.

5.2.3 Power Good Voltage Output

The LM5175EVM-HD provides a test point for measuring the PGOOD flag voltage. A 20-kΩ pullup resistor, Rpg, to VCC is included. For true open-drain operation with no pullup, remove Rpg. One possible scenario where a PGOOD pullup is not required involves PGOOD of an upstream converter connected to the EN input of a downstream converter to provide sequential startup of multiple regulators.

5.2.4 Enable Voltage Input

The LM5175EVM-HD provides a test point for measuring the EN voltage. Shorting this test point to GND disables the converter. The EN/UVLO voltage should not exceed the input voltage.

5.2.5 SYNC Input

The LM5175EVM-HD provides a test point for applying a synchronization (SYNC) input signal. The free-running switching frequency is set at 400 kHz by resistor RT1. However, the converter aligns in frequency and phase with that of the applied SYNC signal up to 600 kHz. If required, apply an external SYNC signal with maximum ac voltage amplitude of 2 V and pulse width between 75 ns and 500 ns.

CAUTION

Some parameters can be configured, such as control loop compensation, to values that can result in unexpected behavior of this EVM. Please refer to the LM5175 datasheet, LM5175 quick-start tool, or WEBENCH® Power Designer for guidance related to component selection.

6 Test Setup and Procedure

Figure 4 shows the recommended test setup to evaluate the LM5175EVM-HD. Working at an ESD workstation, make sure that any wrist straps, boot straps or mats are connected referencing the user to earth ground before power is applied to the EVM.

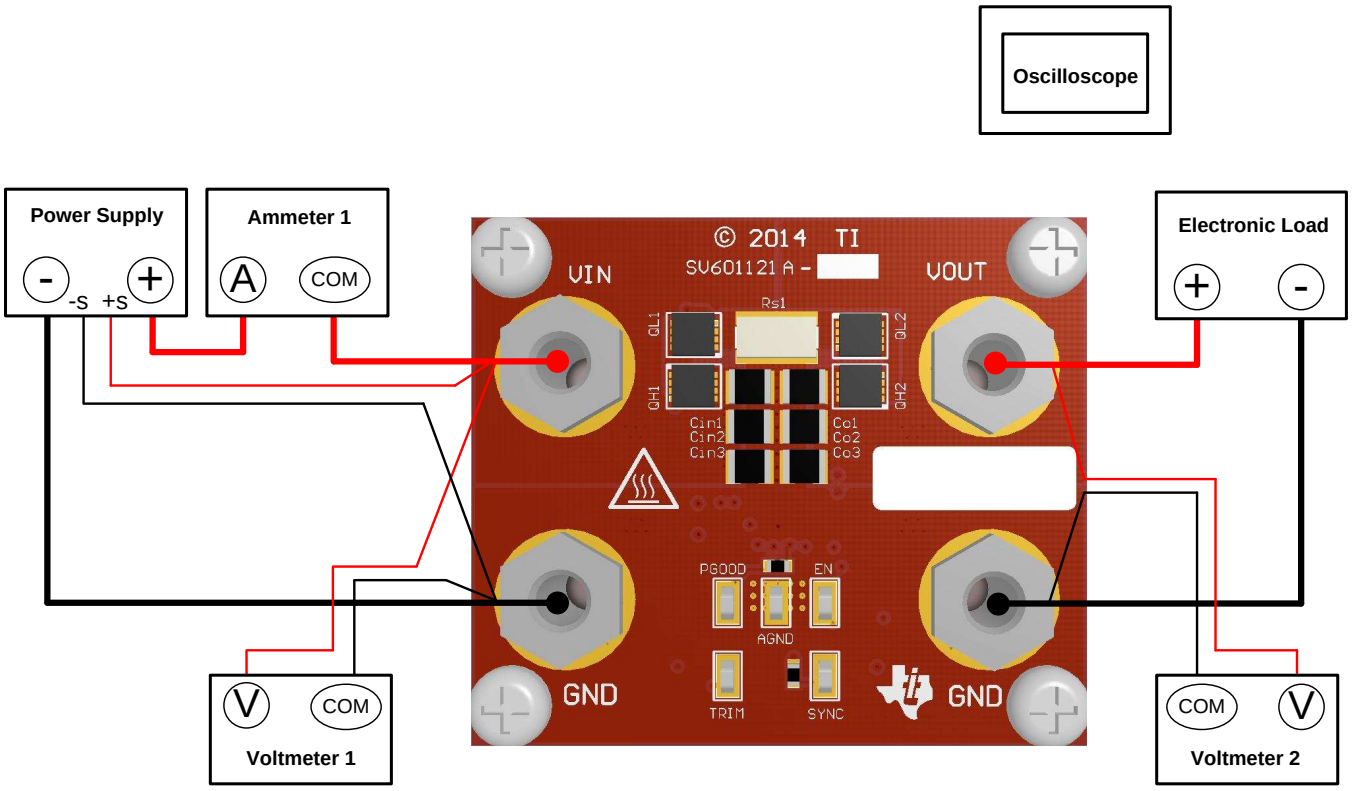


Figure 4. Test Setup Connection Diagram

6.1 Test Equipment

Voltage Source: The input voltage source VIN should be a 0–50-V variable dc source capable of supplying 10 A.

Multimeters:

- **Voltmeter 1:** Input voltage at VIN to GND
- **Voltmeter 2:** Output voltage at VOUT to GND
- **Ammeter 1:** Input current (or use the power supply readout if its accuracy is deemed acceptable)

Electronic Load: The output load should be an electronic constant-resistance or constant-current mode load capable of 0 Adc to 10 Adc at 12 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure pertinent converter waveforms. With the scope set to 20-MHz bandwidth and AC coupling, the output voltage ripple can be measured directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the probe's ground barrel through the ground lead to the capacitor's negative terminal. It is not recommended to use a long leaded ground connection because this may induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

Fan: Depending on the EVM's operating conditions, the temperature rise of certain powertrain components can approach 50°C. Although not mandatory, use a small fan capable of 200–400 LFM to reduce component temperatures while the EVM is operating. Exercise care when touching the EVM while the fan is not running. Always use caution when touching any circuits that may be live or energized.

Recommended Wire Gauge:

- **Input Source to VIN and GND:** The recommended wire size is 1 × AWG #14 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).
- **VOUT to LOAD:** The minimum recommended wire size is 2 × AWG #14, with the total length of wire less than 4 feet (2 feet input, 2 feet return).

6.2 Recommended Test Setup

6.2.1 Input Connections

- Prior to connecting the DC input source, it is advisable to limit the source current to 10 A maximum. Make sure the input source is initially set to 0 V and connected to VIN and GND banana connections as shown in Figure 4. While the on-board hybrid electrolytic capacitor provides input circuit damping, an additional high-ESR input capacitor may be required if long input lines are used.
- Connect voltmeter 1 at VIN and GND test points to measure the input voltage.
- Connect ammeter 1 to measure the input current.

6.2.2 Output Connections

- Connect an electronic load to VOUT and GND connections. Set the load to constant-resistance mode or constant-current mode at 0 Adc before applying input voltage. Use short load lines to minimize voltage drop to the load.
- Connect voltmeter 2 at VOUT and GND solder lugs to measure the output voltage.
- The output current level is taken from the electronic load readout (if its accuracy is deemed acceptable).

6.3 Test Procedure

6.3.1 Line, Load Regulation and Efficiency

- Set up the EVM as described above.
- Set load to constant resistance or constant current mode and to sink 0 Adc.
- Increase input source from 0 V to 42 V, using voltmeter 1 to measure input voltage.
- Use voltmeter 2 to measure output voltage, V_{OUT}.
- Vary load from 0 to 6 Adc, V_{OUT} should remain within load regulation specification.
- Vary input source voltage from 5.5 V to 42 V, V_{OUT} should remain within line regulation specification.
- Decrease load to 0 A. Decrease input source voltage to 0 V.

6.3.2 Control Loop Gain and Phase

The 10-Ω positive sense resistor of the LM5175EVM-HD is a convenient injection point for loop response analysis.

- Set up EVM as described previously.
- Connect isolation transformer secondary across R16.
- Connect output signal amplitude measurement probe (TEST) to VOUT and input signal amplitude measurement (REF) probe to opposite side of R16.
- Connect ground leads to the AGND test point as required.
- Apply 10 mV or less AC signal to the isolation transformer primary. Adjust amplitude as necessary.
- Sweep the frequency over the frequency range of interest (e.g. 100 Hz to 100 kHz) with 10 Hz or lower post filter.
- Measure the control loop gain and phase characteristic. Record the crossover frequency and phase margin.
- Disconnect isolation transformer before making other measurements (signal injection into the loop may interfere with the integrity of other measurements).

7 Test Data and Performance Curves

Figure 5 through Figure 50 present typical performance curves for the LM5175EVM-HD. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

7.1 Efficiency

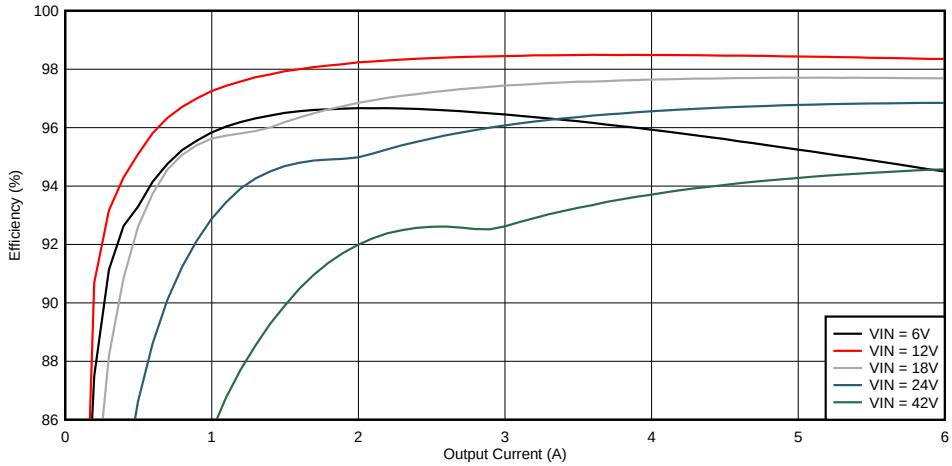


Figure 5. Efficiency vs. Output Current

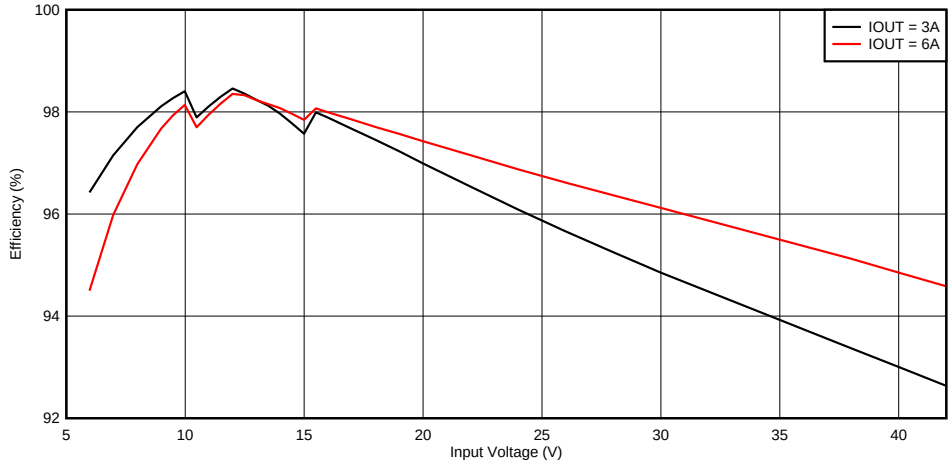


Figure 6. Efficiency vs. Input Voltage

7.2 Load Regulation

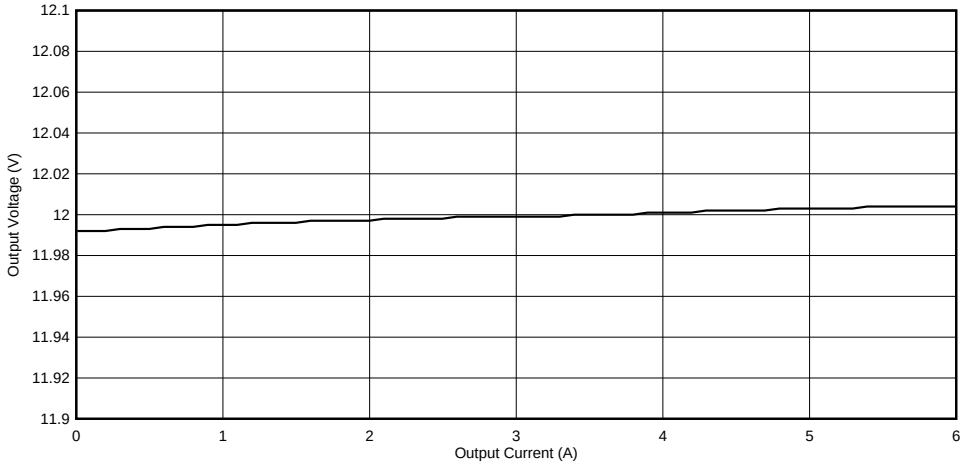


Figure 7. Load Regulation

7.3 Line Regulation

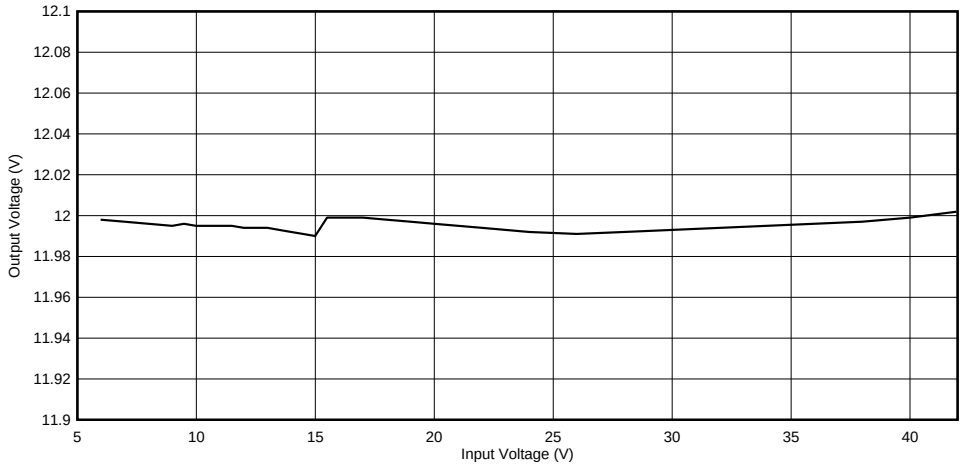
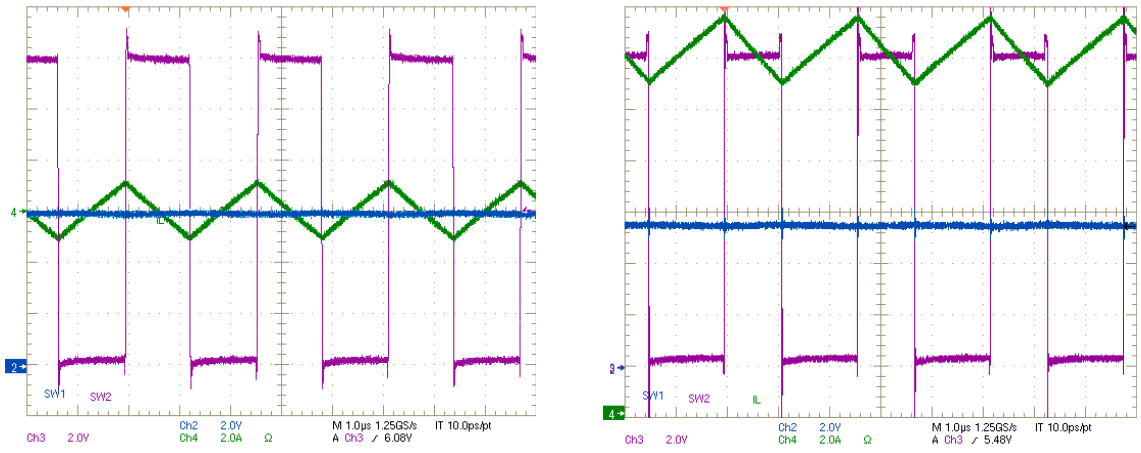


Figure 8. Line Regulation

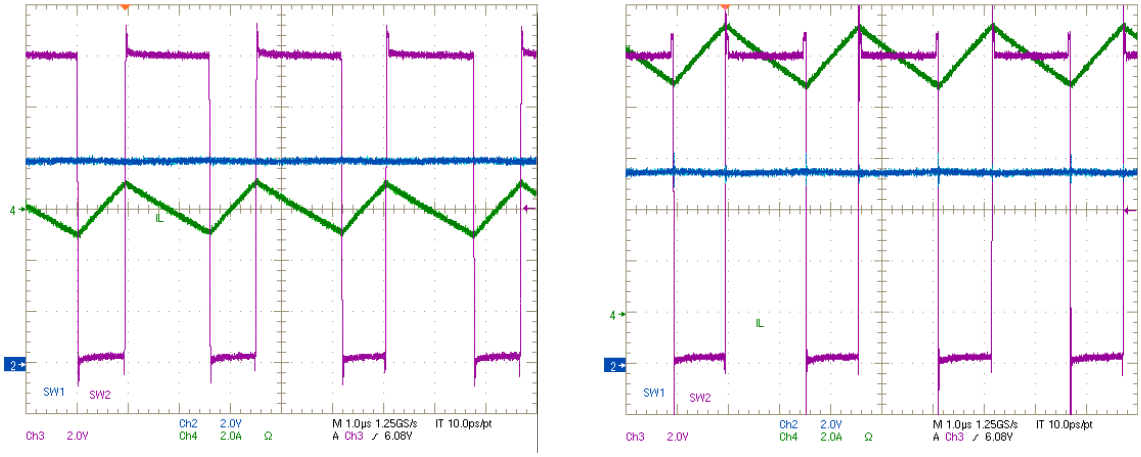
7.4 Operating Waveforms

7.4.1 Switch Node Voltages and Inductor Current



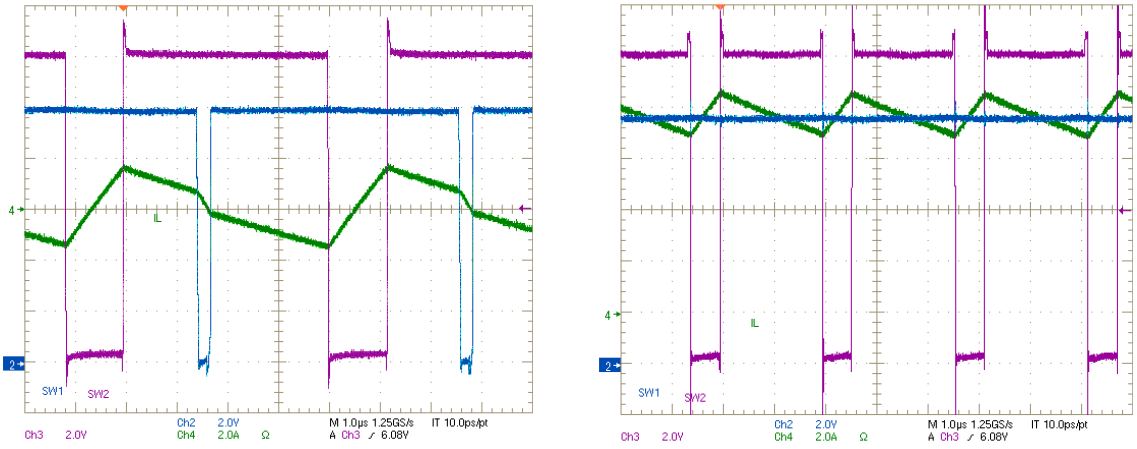
(a) (b)

Figure 9. SW1, SW2, I_L Waveforms: V_{IN} = 6 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



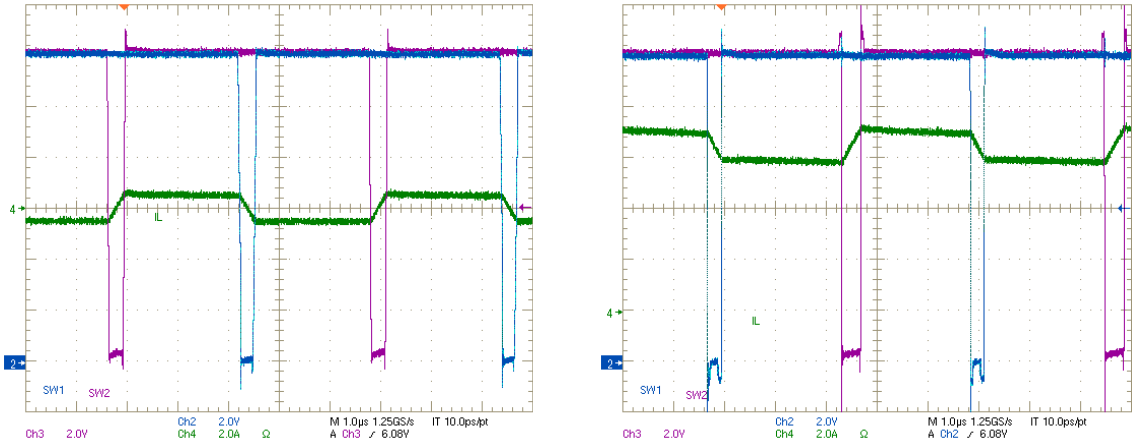
(a) (b)

Figure 10. SW1, SW2, I_L Waveforms: V_{IN} = 8 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



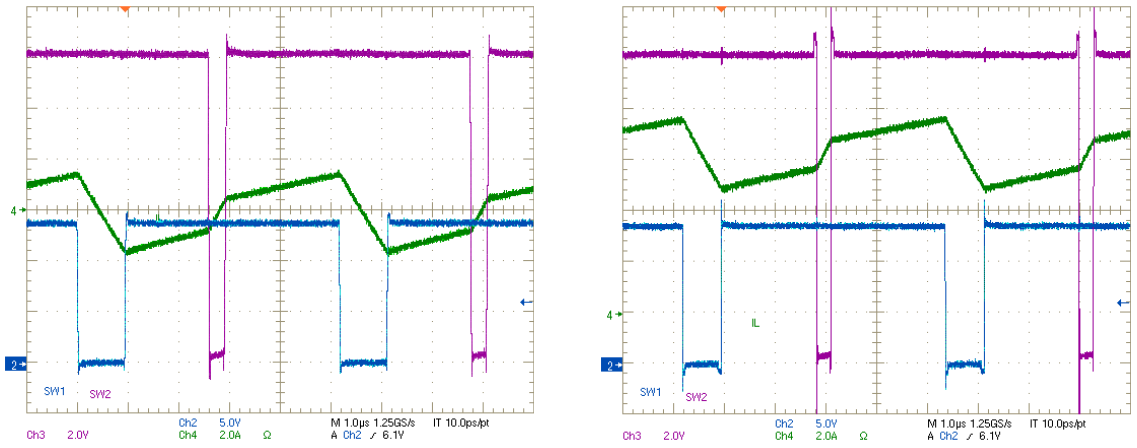
(a) (b)

Figure 11. SW1, SW2, I_L Waveforms: V_{IN} = 10 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



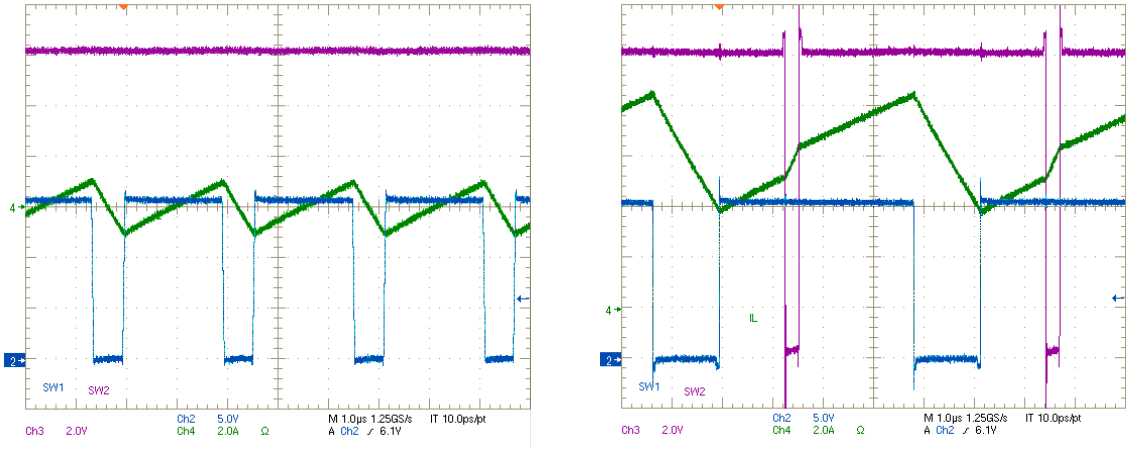
(a) (b)

Figure 12. SW1, SW2, I_L Waveforms: V_{IN} = 12 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



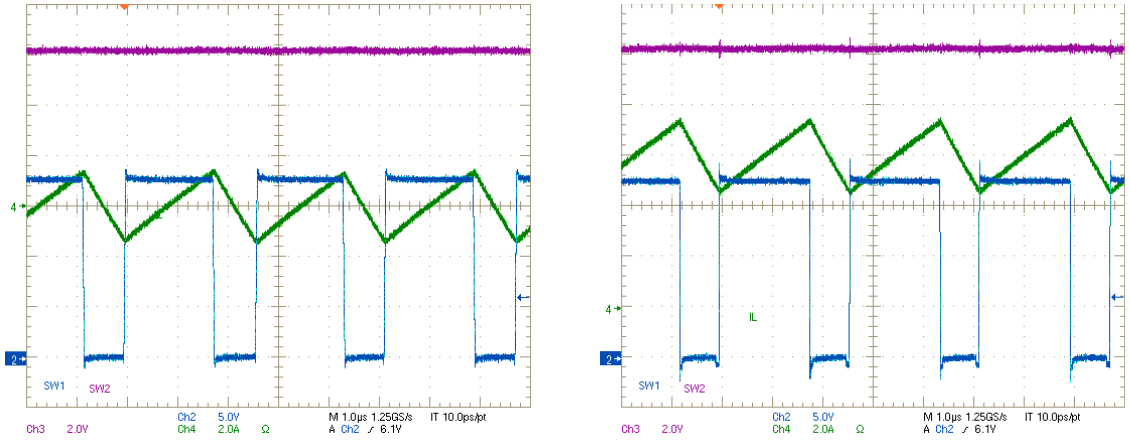
(a) (b)

Figure 13. SW1, SW2, I_L Waveforms: V_{IN} = 14 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



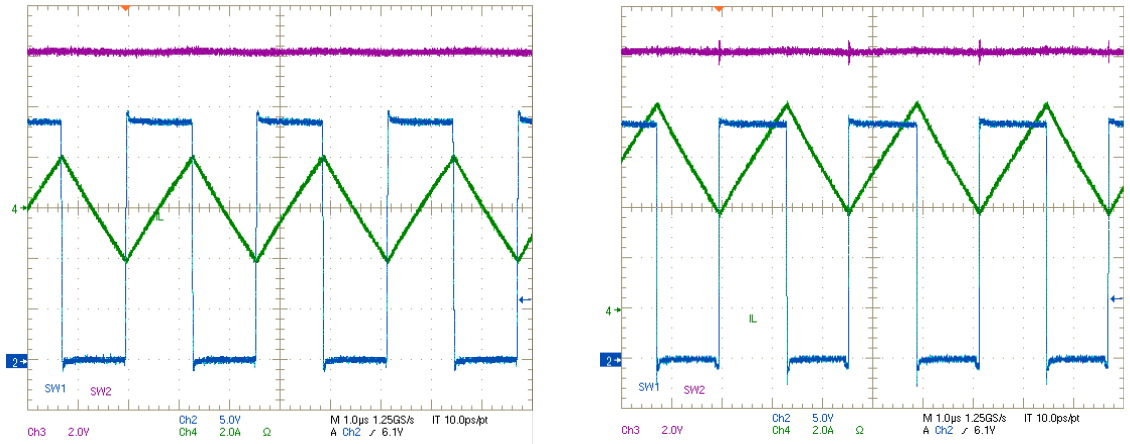
(a) (b)

Figure 14. SW1, SW2, I_L Waveforms: V_{IN} = 16 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



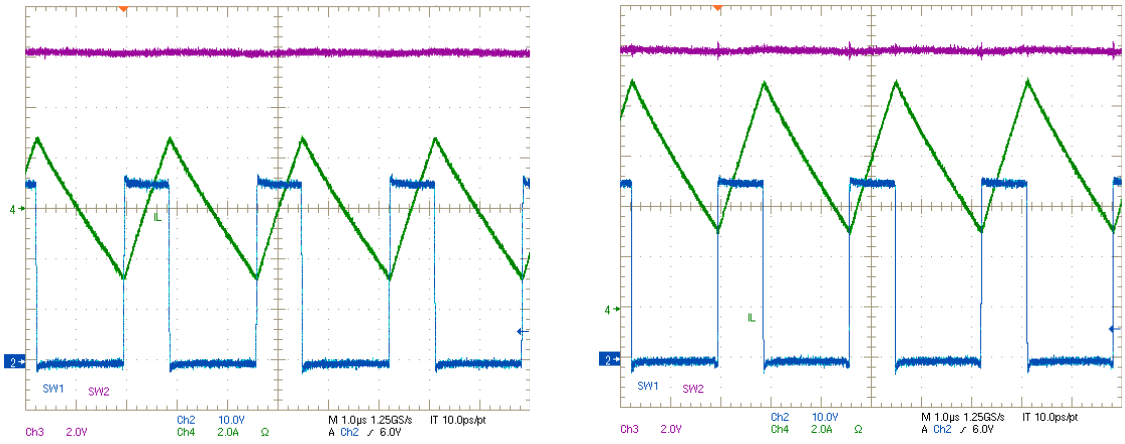
(a) (b)

Figure 15. SW1, SW2, I_L Waveforms: V_{IN} = 18 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



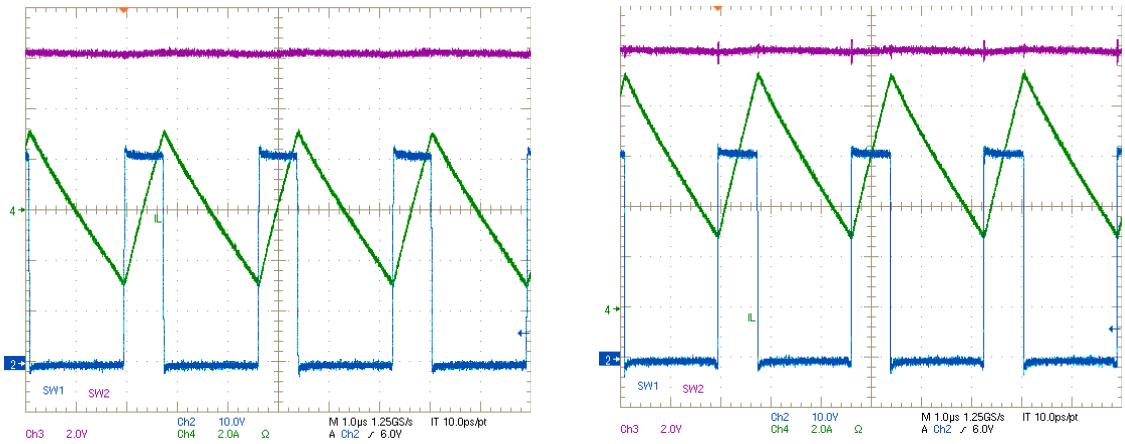
(a) (b)

Figure 16. SW1, SW2, I_L Waveforms: V_{IN} = 24 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



(a) (b)

Figure 17. SW1, SW2, I_L Waveforms: V_{IN} = 36 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



(a) (b)

Figure 18. SW1, SW2, I_L Waveforms: V_{IN} = 42 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A

7.4.2 Buck-Leg Switching Waveforms

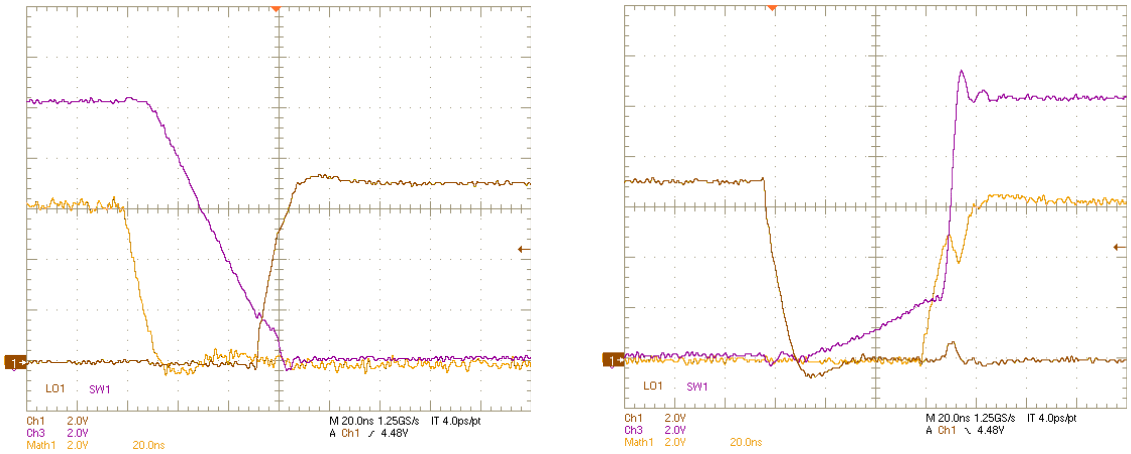


Figure 19. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 10.5 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON

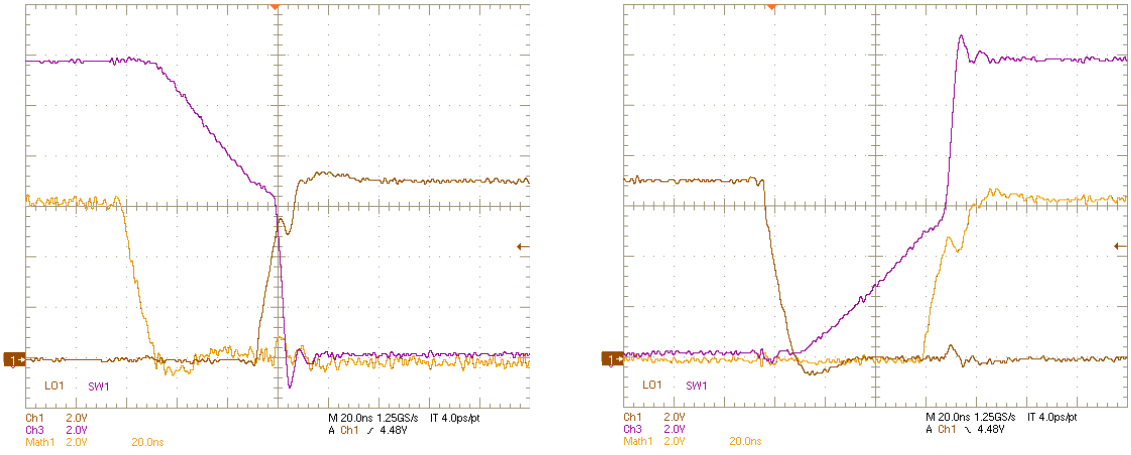


Figure 20. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 12 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON

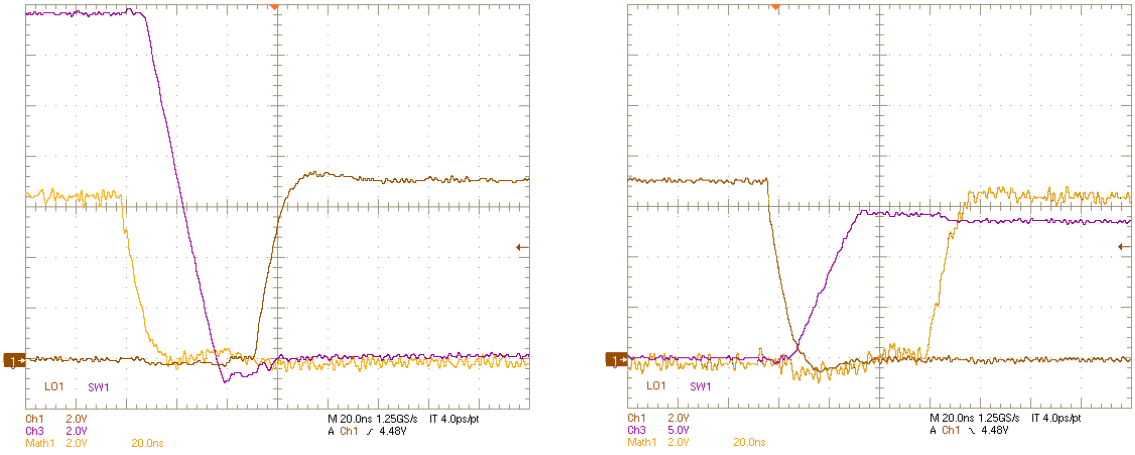
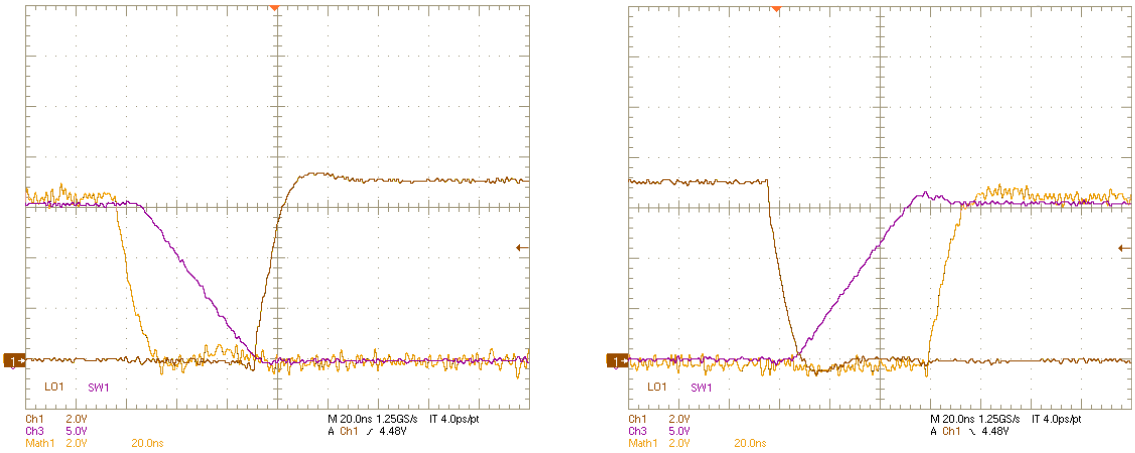
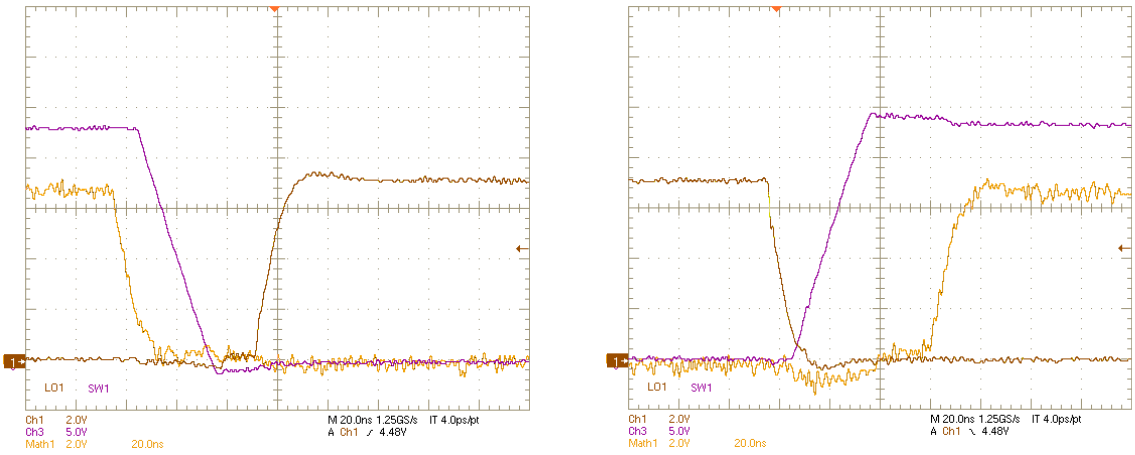


Figure 21. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 14 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



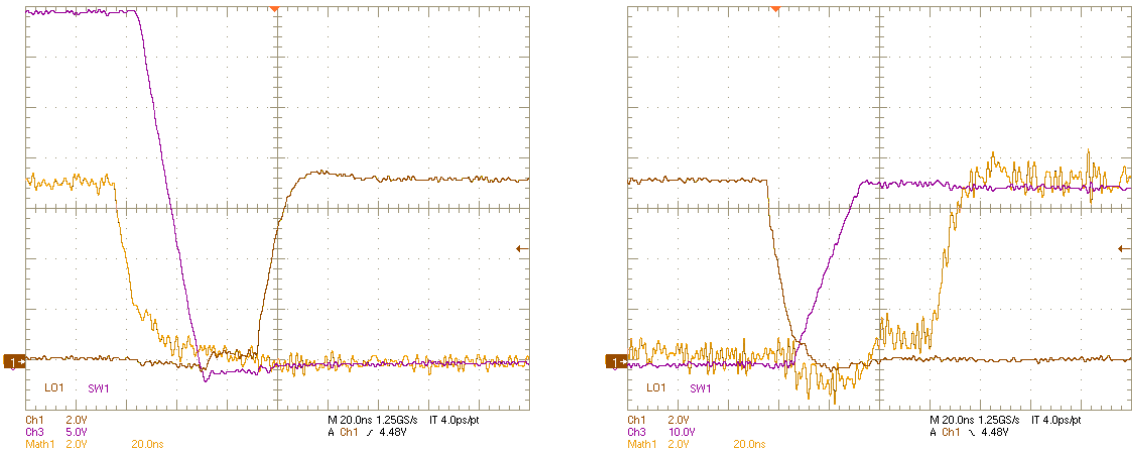
(a) (b)

Figure 22. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 16 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



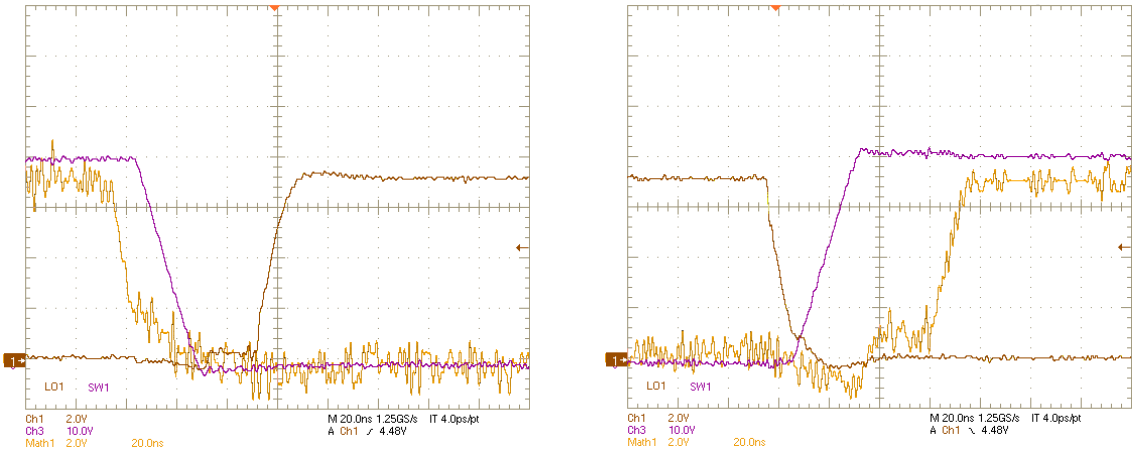
(a) (b)

Figure 23. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



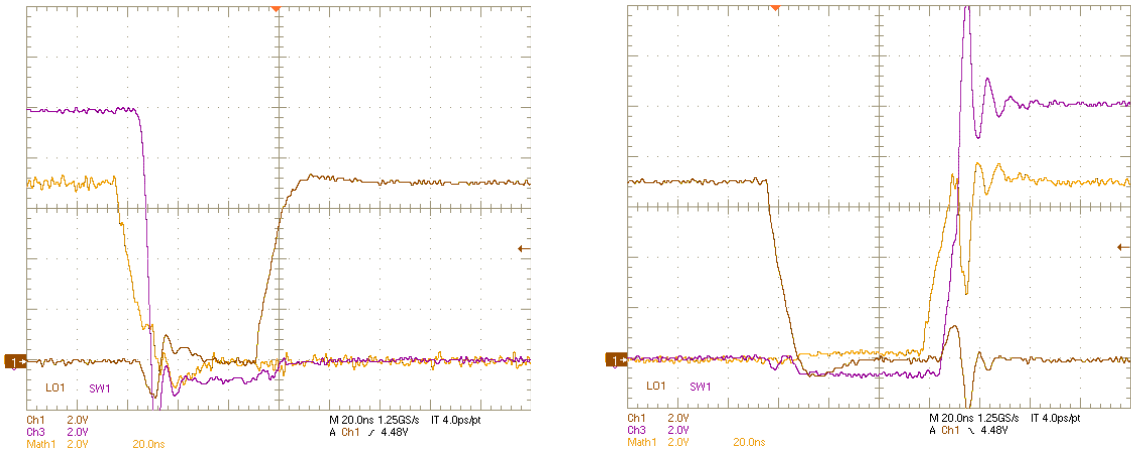
(a) (b)

Figure 24. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 36 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



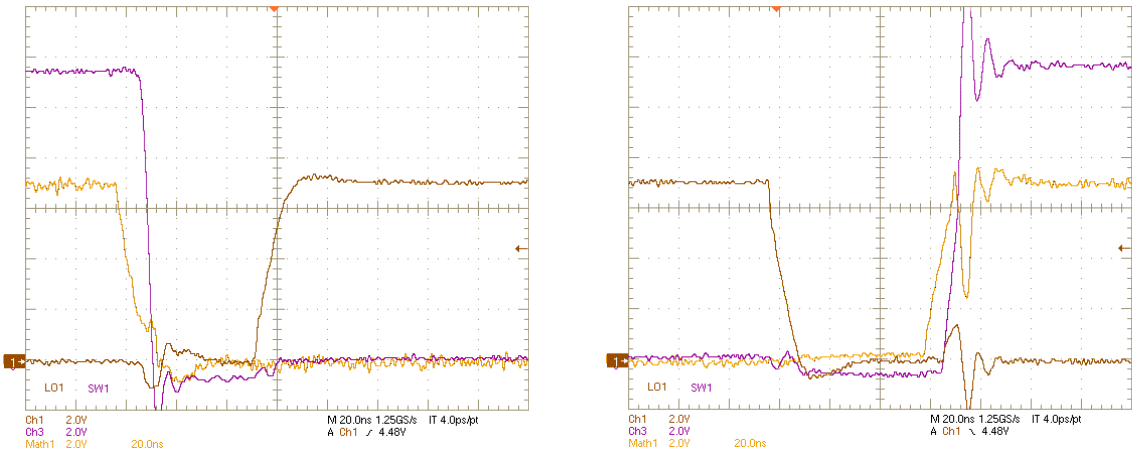
(a) (b)

Figure 25. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 42 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



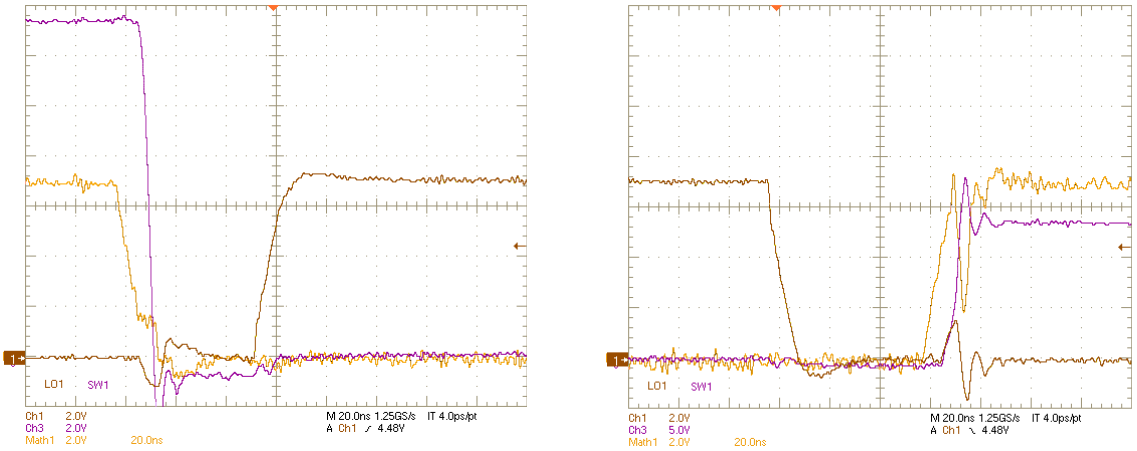
(a) (b)

Figure 26. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 10.5 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



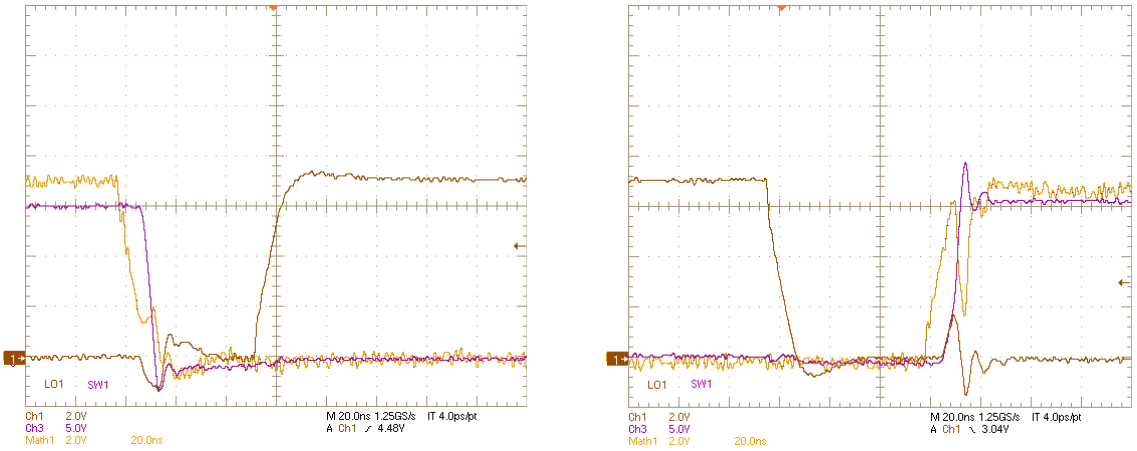
(a) (b)

Figure 27. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 12 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



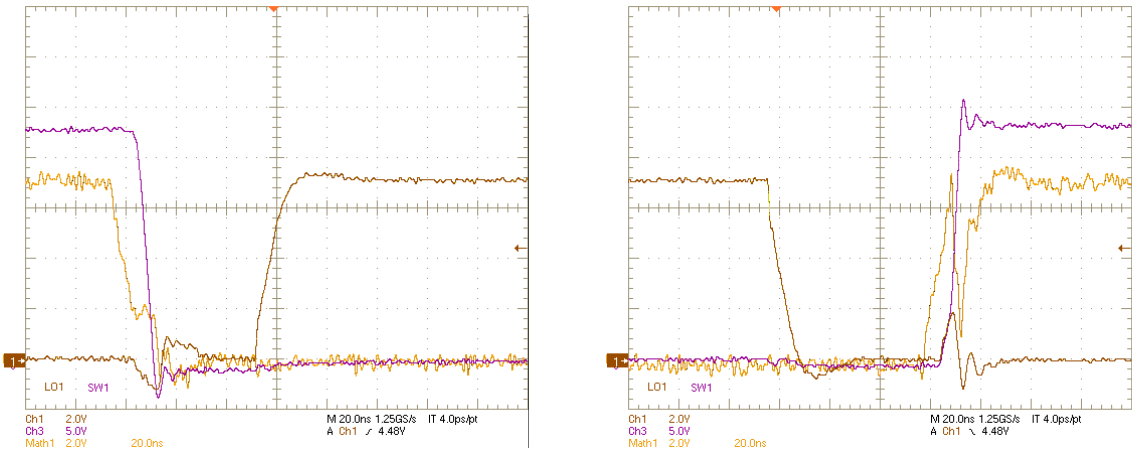
(a) (b)

Figure 28. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 14 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



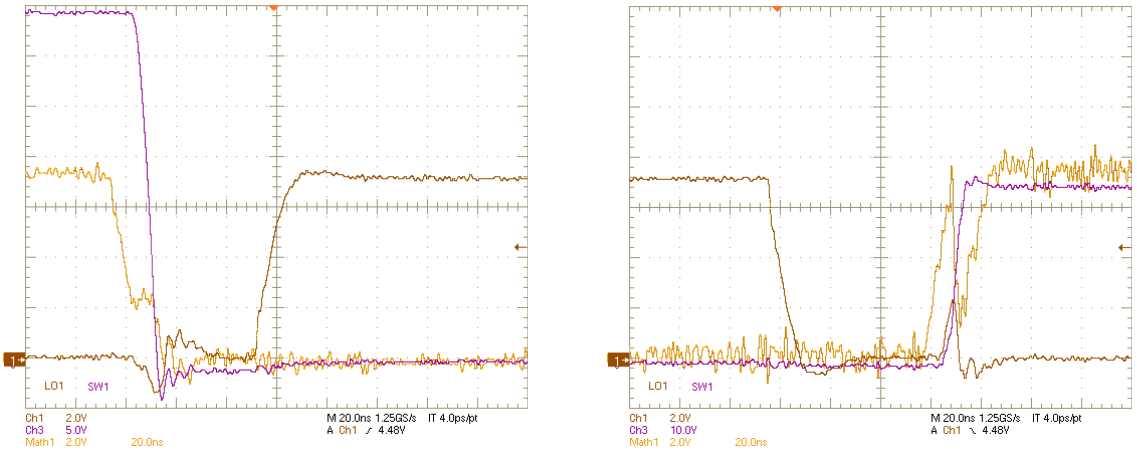
(a) (b)

Figure 29. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 16 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



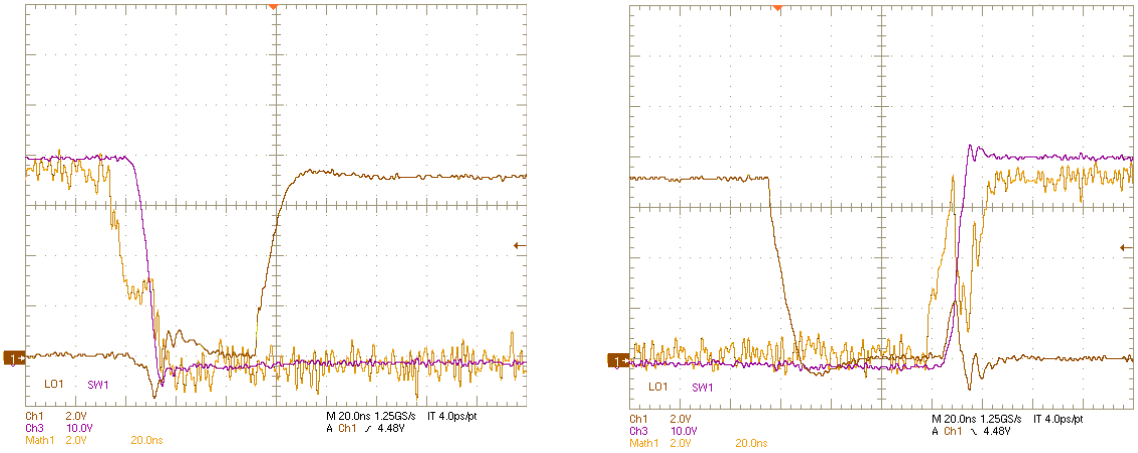
(a) (b)

Figure 30. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



(a) (b)

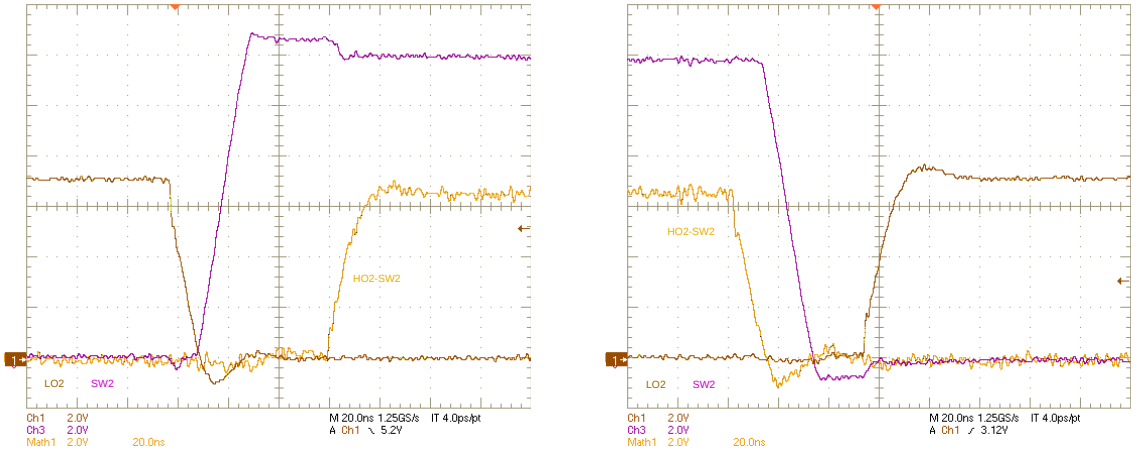
Figure 31. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 36 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



(a) (b)

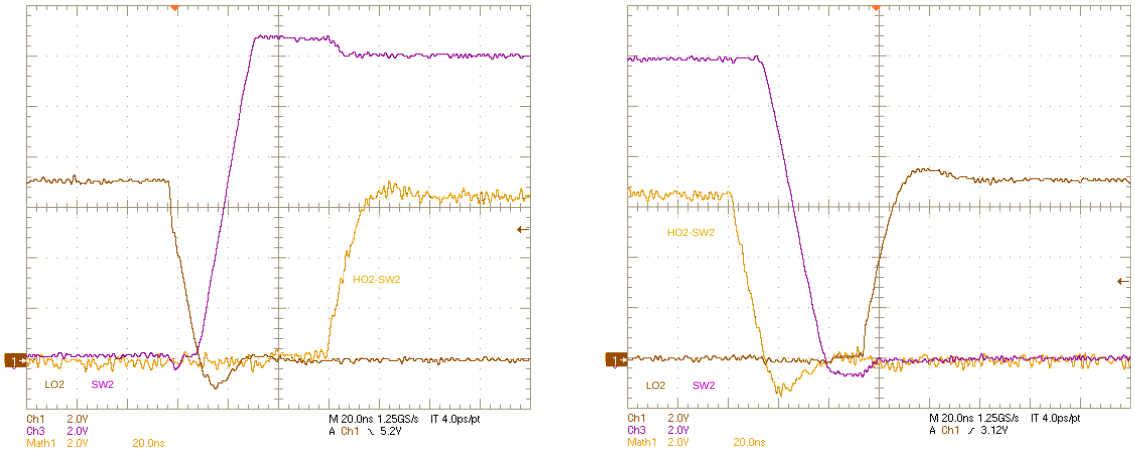
Figure 32. SW1, LO1, (HO1–SW1) Voltages: V_{IN} = 42 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON

7.4.3 Boost-Leg Switching Waveforms



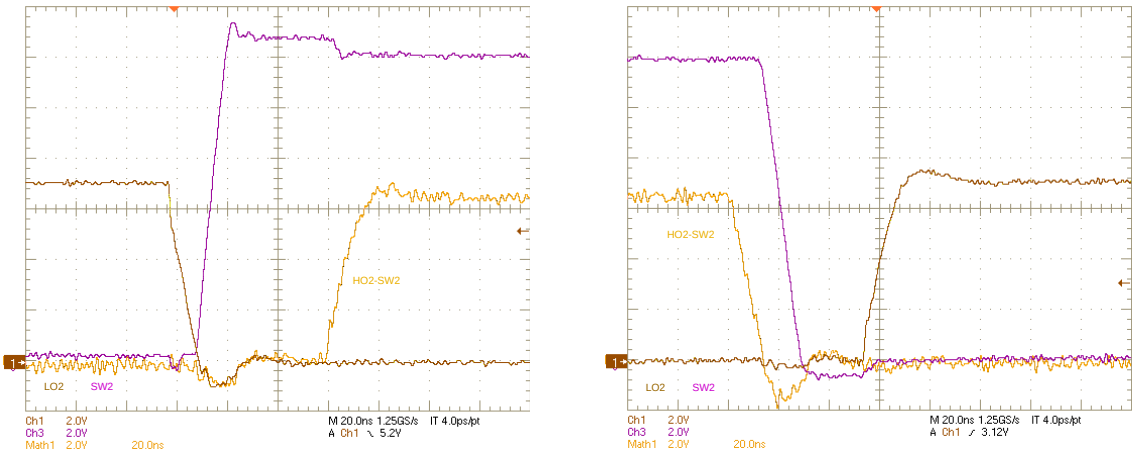
(a) (b)

Figure 33. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 6 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



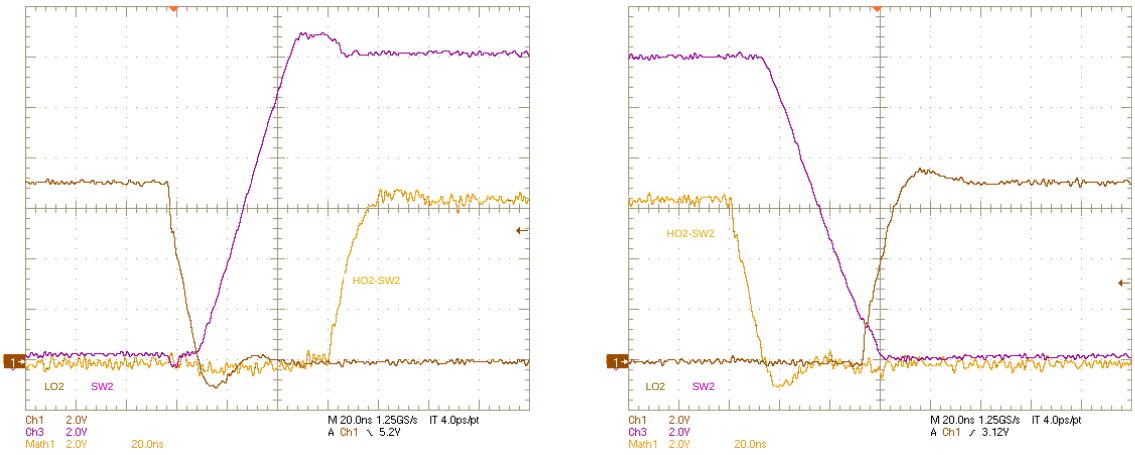
(a) (b)

Figure 34. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 8 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



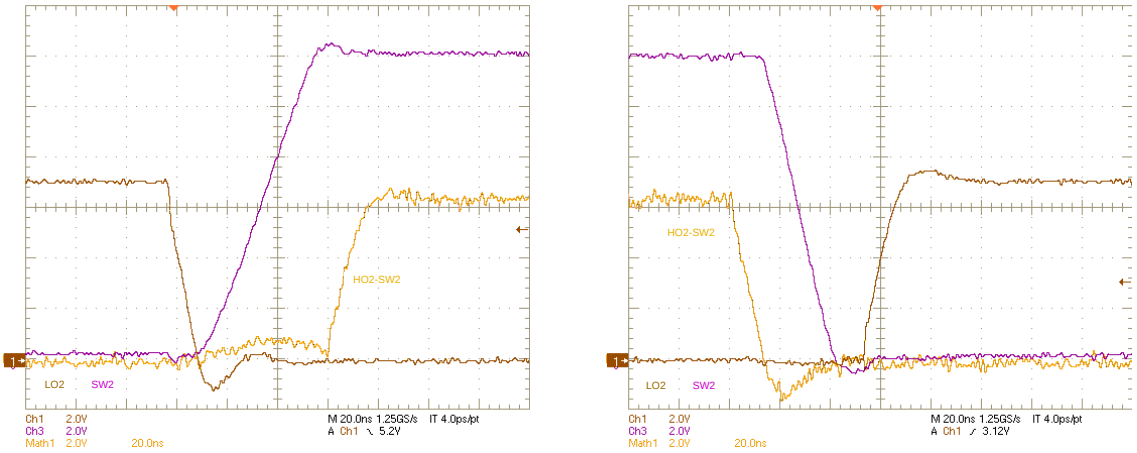
(a) (b)

Figure 35. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 10 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



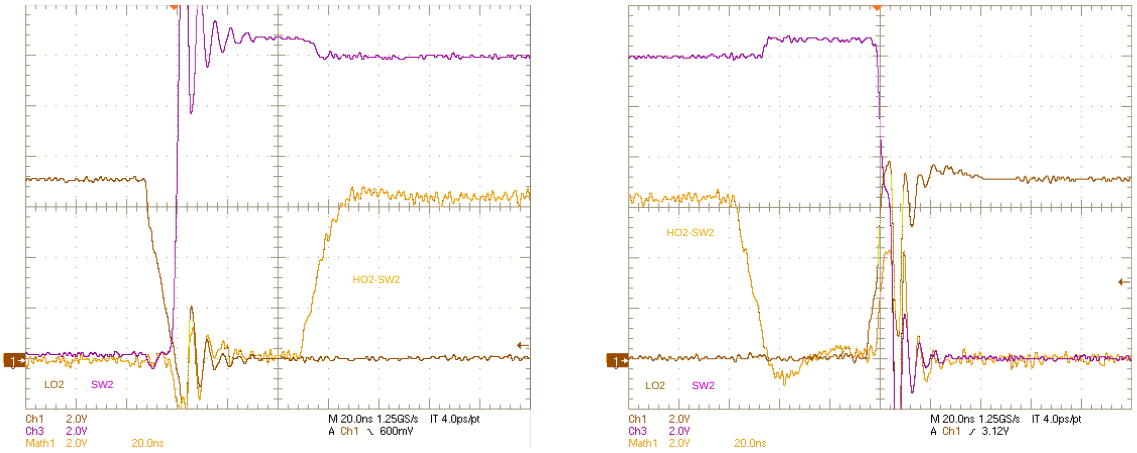
(a) (b)

Figure 36. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 12 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



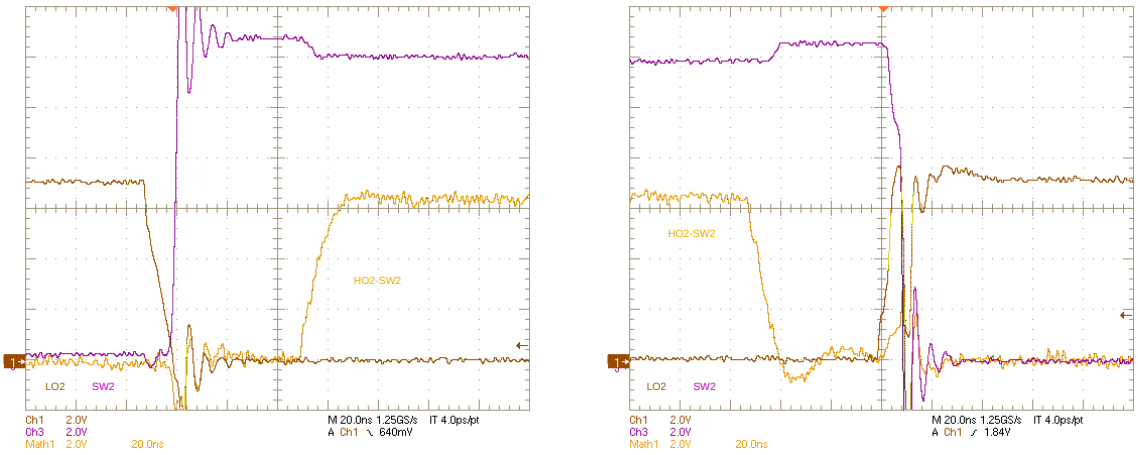
(a) (b)

Figure 37. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 14 V, V_{OUT} = 12 V, I_{OUT} = 0 A, (a) OFF, (b) ON



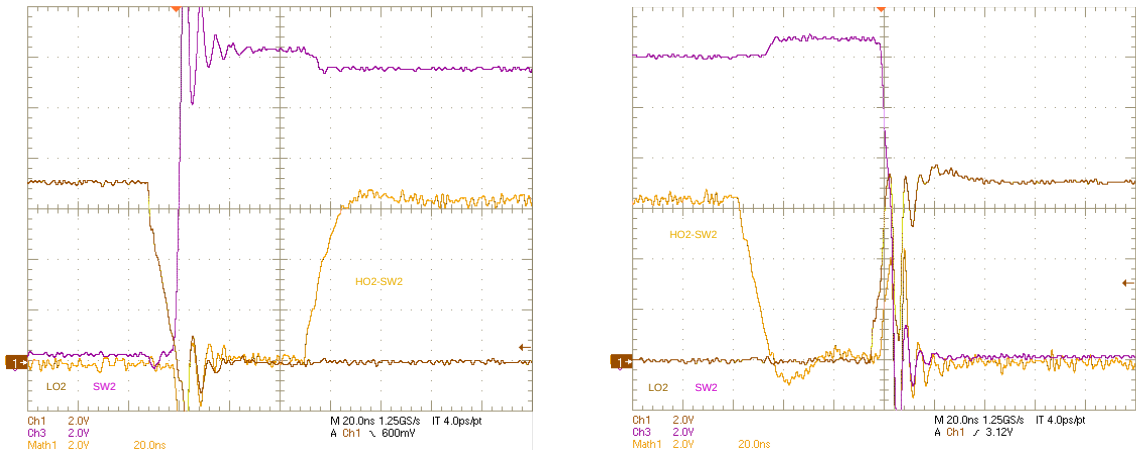
(a) (b)

Figure 38. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 6 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



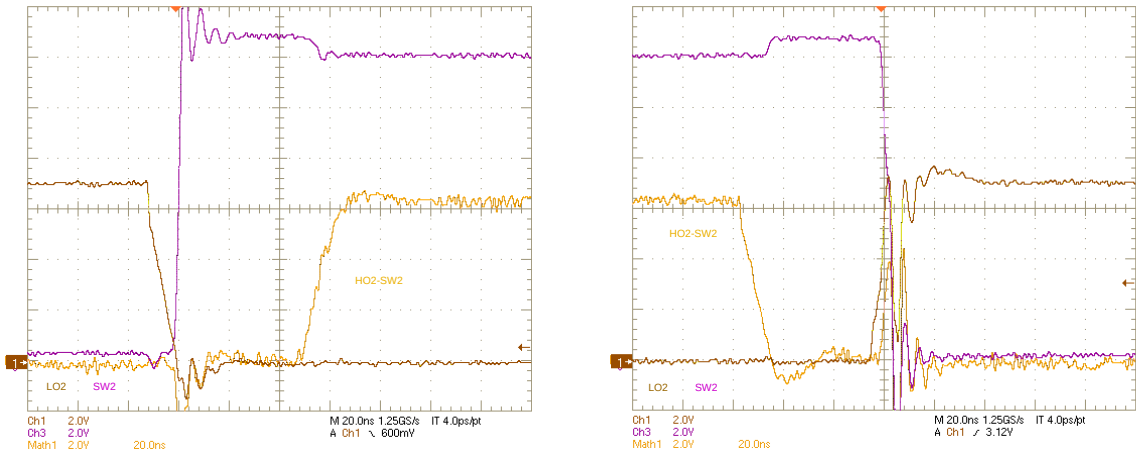
(a) (b)

Figure 39. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 8 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



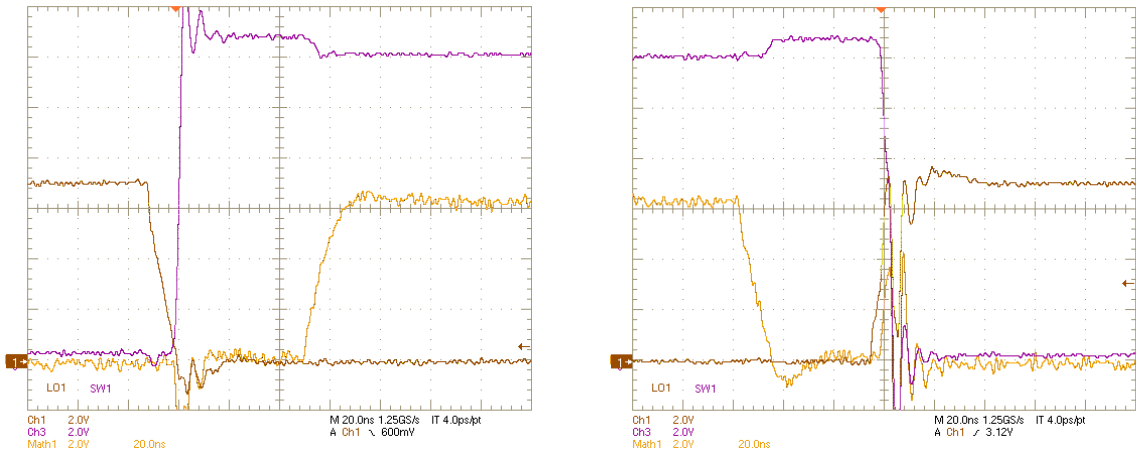
(a) (b)

Figure 40. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 10 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



(a) (b)

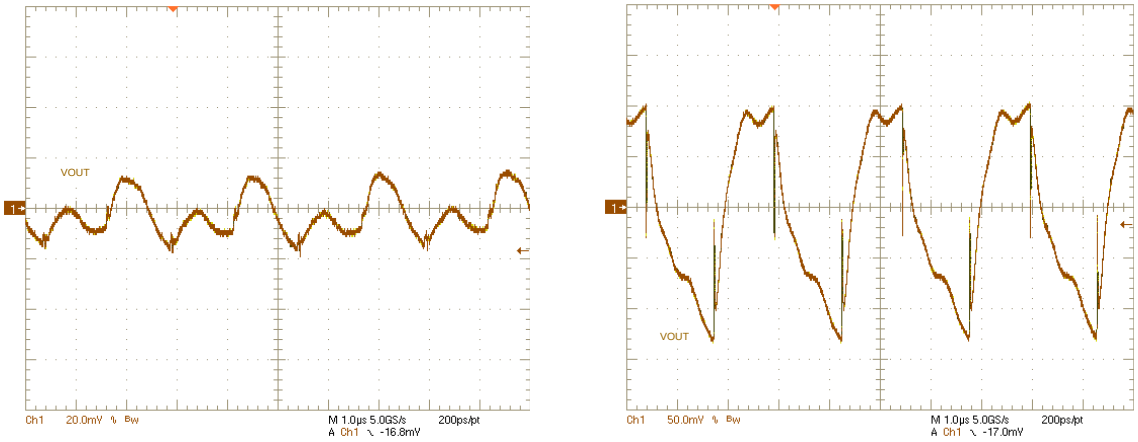
Figure 41. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 12 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON



(a) (b)

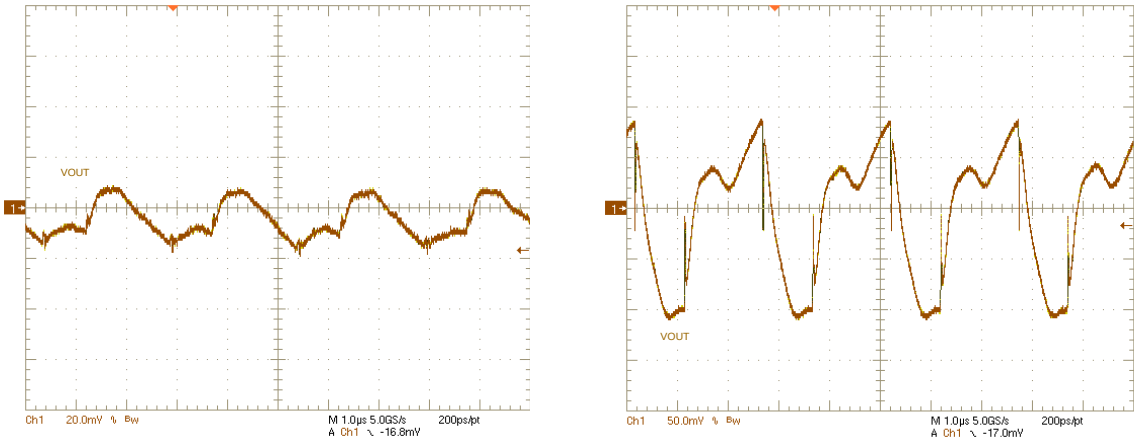
Figure 42. SW2, LO2, (HO2–SW2) Voltages: V_{IN} = 14 V, V_{OUT} = 12 V, I_{OUT} = 6 A, (a) OFF, (b) ON

7.4.4 Output Voltage Ripple, 20-MHz Bandwidth



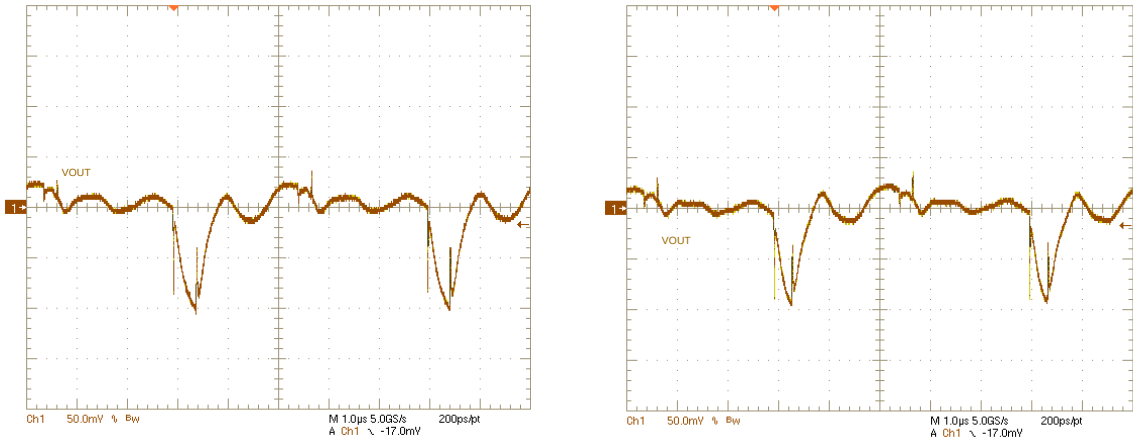
(a) (b)

Figure 43. V_{OUT} ripple: V_{IN} = 6 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



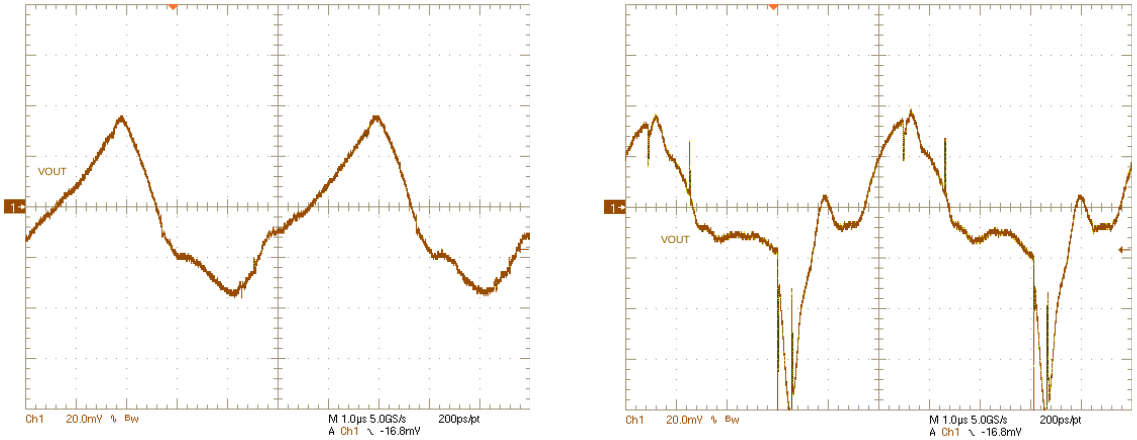
(a) (b)

Figure 44. V_{OUT} ripple: V_{IN} = 8 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



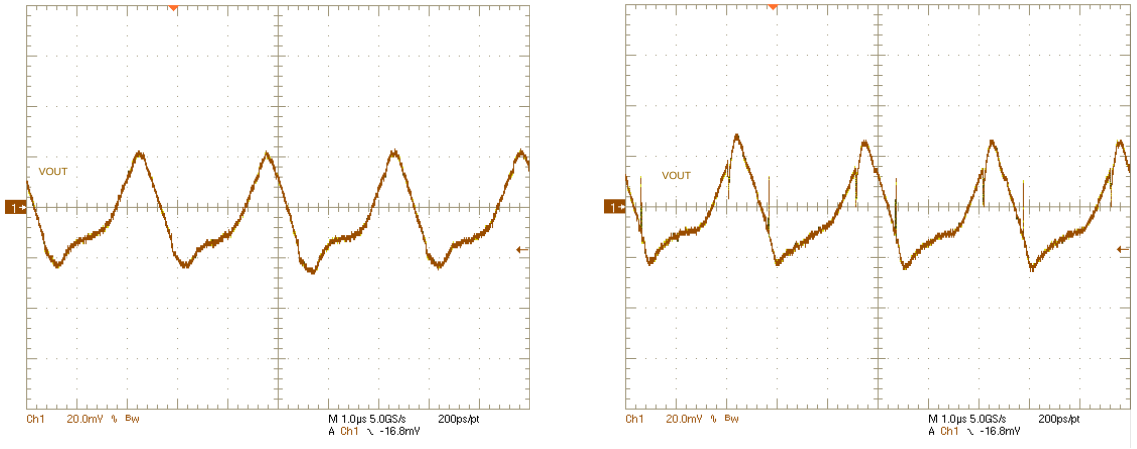
(a) (b)

Figure 45. V_{OUT} ripple: V_{IN} = 12 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



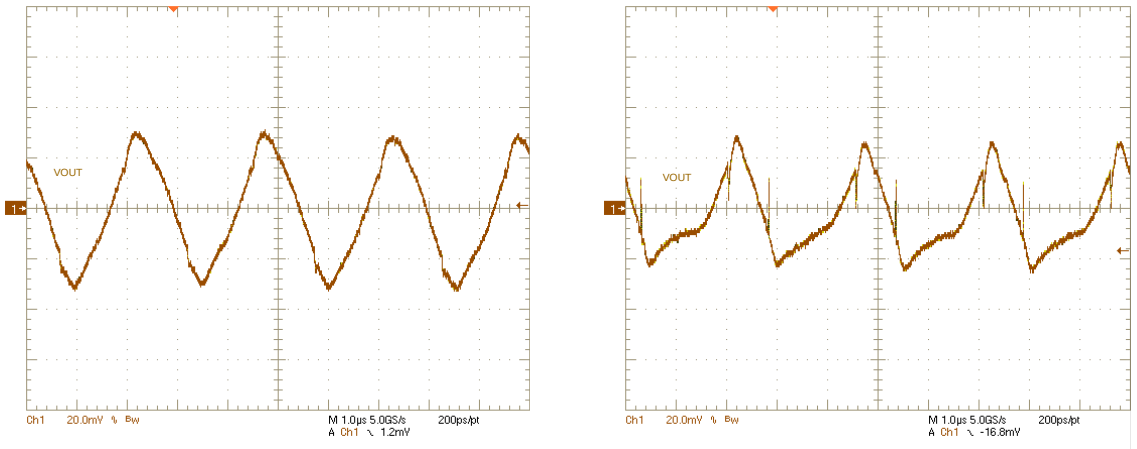
(a) (b)

Figure 46. V_{OUT} ripple: V_{IN} = 14 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



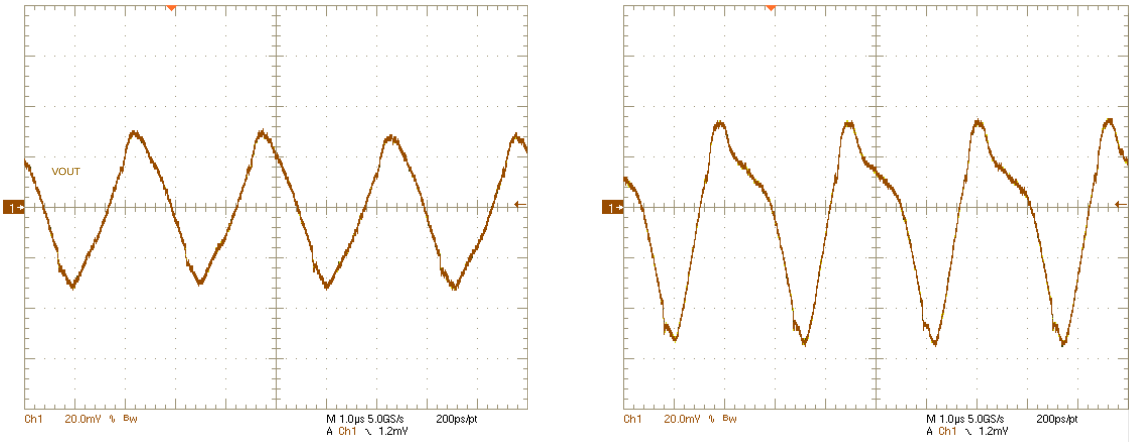
(a) (b)

Figure 47. V_{OUT} ripple: V_{IN} = 18 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



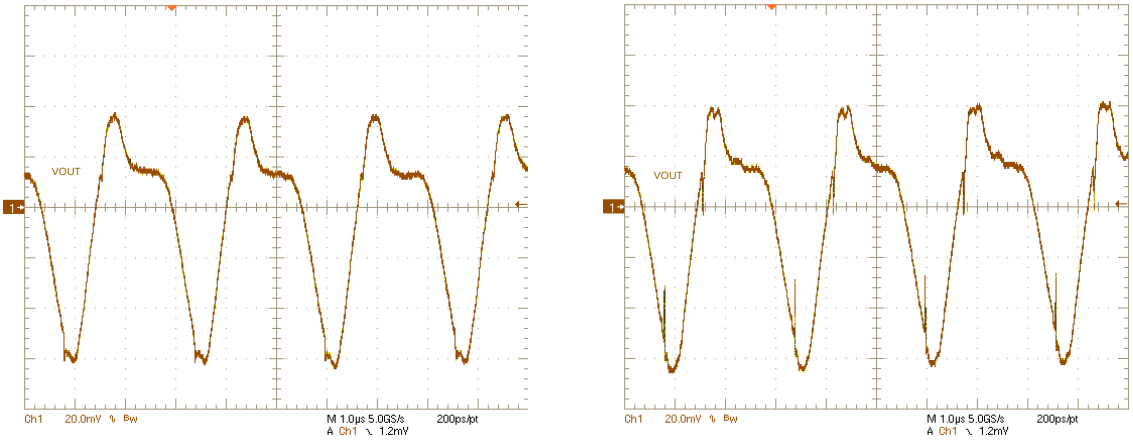
(a) (b)

Figure 48. V_{OUT} ripple: V_{IN} = 24 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



(a) (b)

Figure 49. V_{OUT} ripple: V_{IN} = 36 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A



(a) (b)

Figure 50. V_{OUT} ripple: V_{IN} = 42 V, V_{OUT} = 12 V, (a) I_{OUT} = 0 A, (b) I_{OUT} = 6 A

8 EVM Documentation

8.1 Schematic

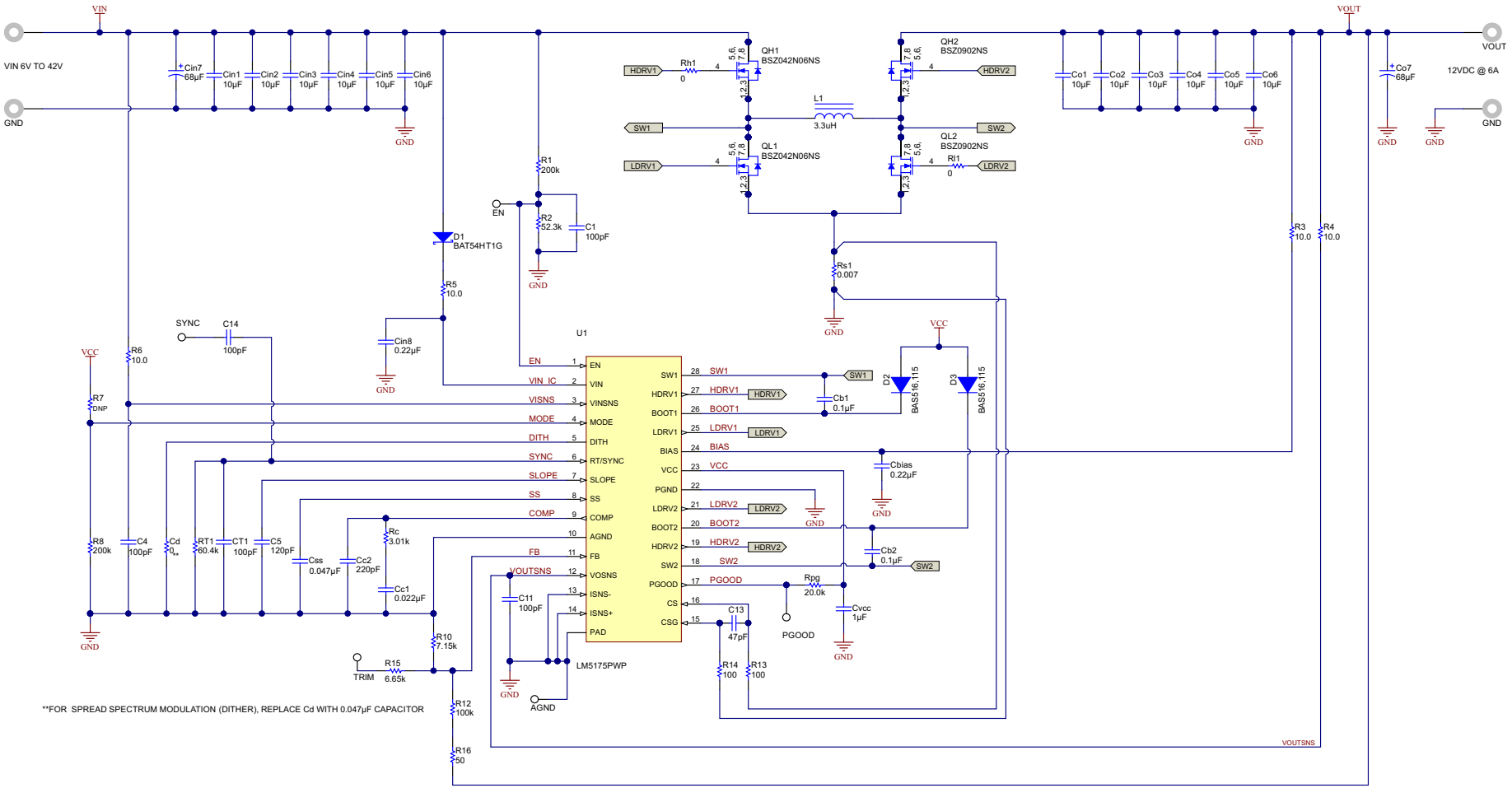


Figure 51. EVM Schematic

8.2 PCB Layout

Figure 52 through Figure 61 show the design of the LM5175 6-layer PCB with 2-oz copper thickness. The EVM is a two-sided design, and it includes positions for input and output bulk capacitors.

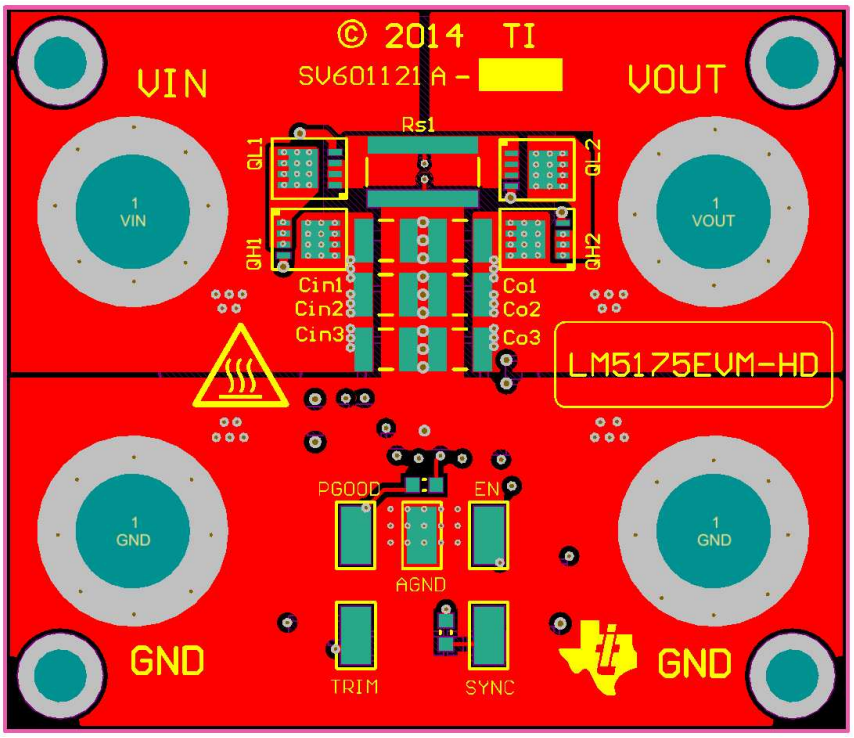


Figure 52. Top Copper (Top view)

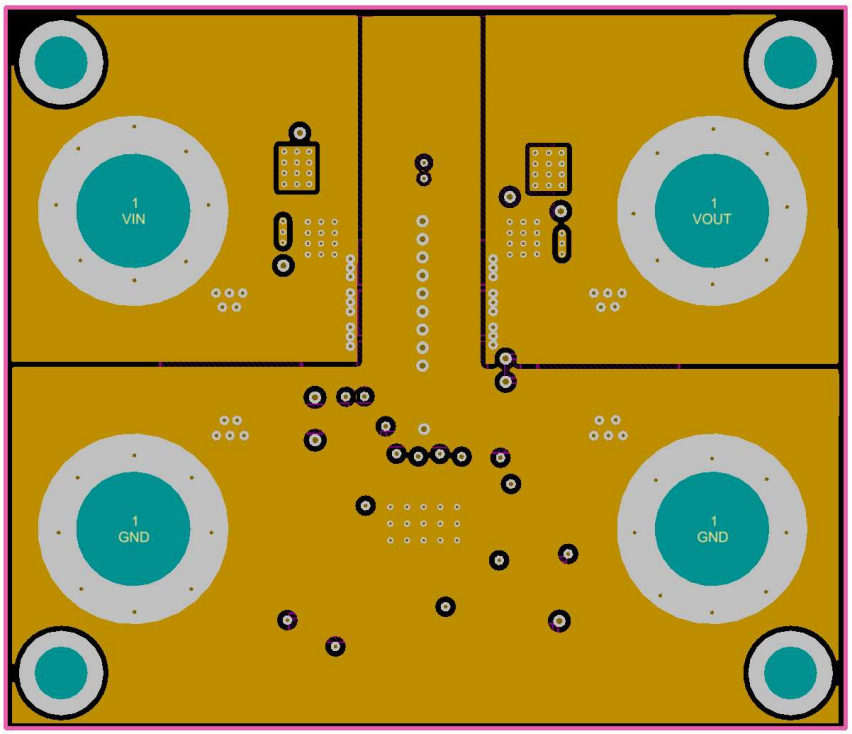


Figure 53. Layer 2 (Top view)

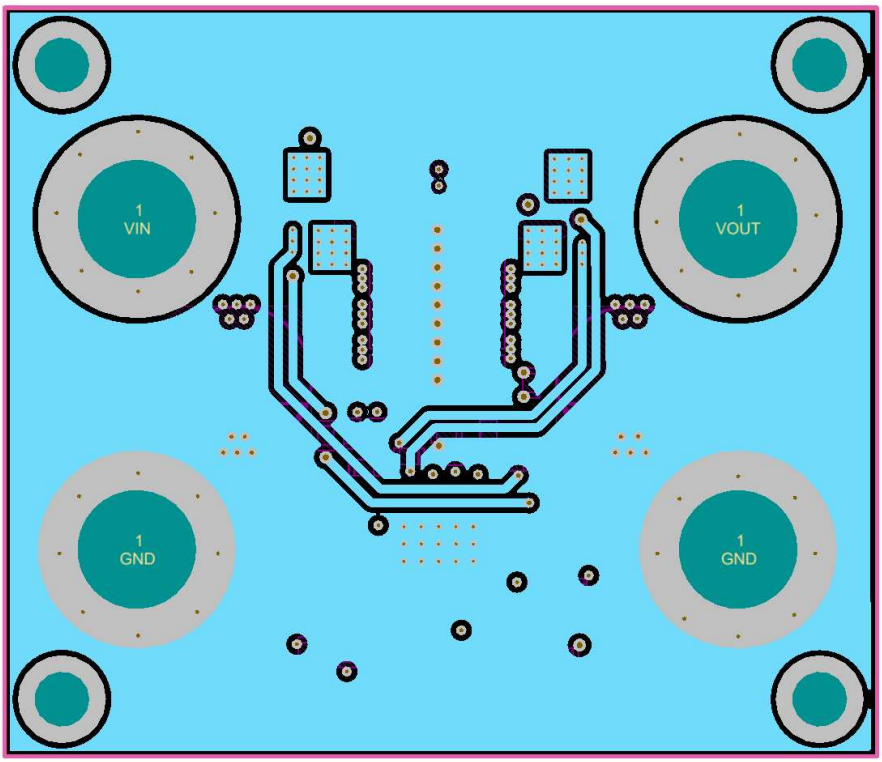


Figure 54. Layer 3 (Top view)

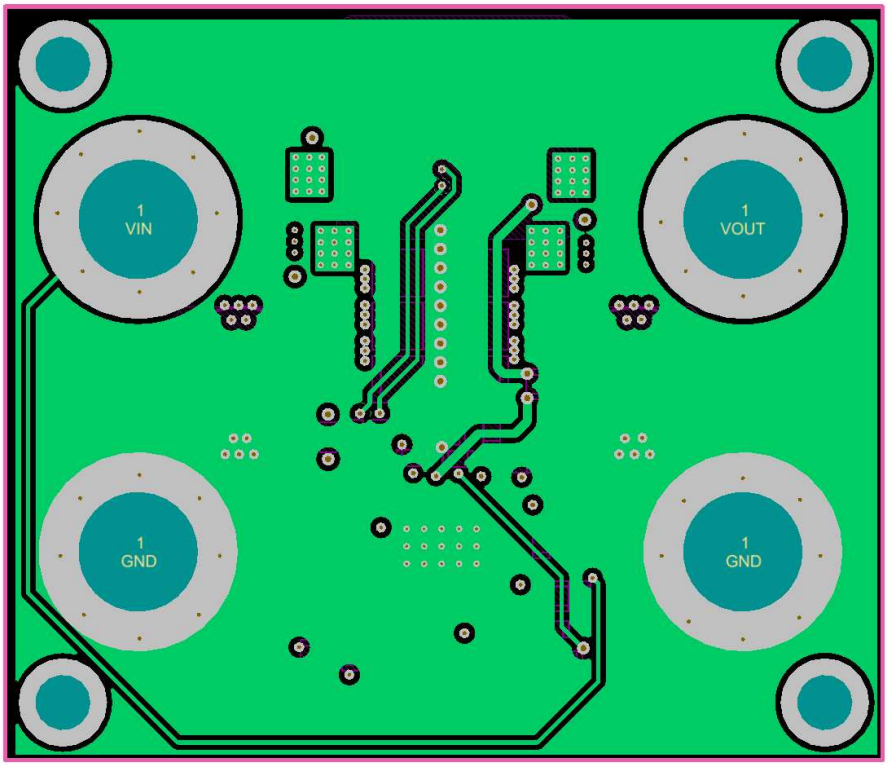


Figure 55. Layer 4 (Top view)

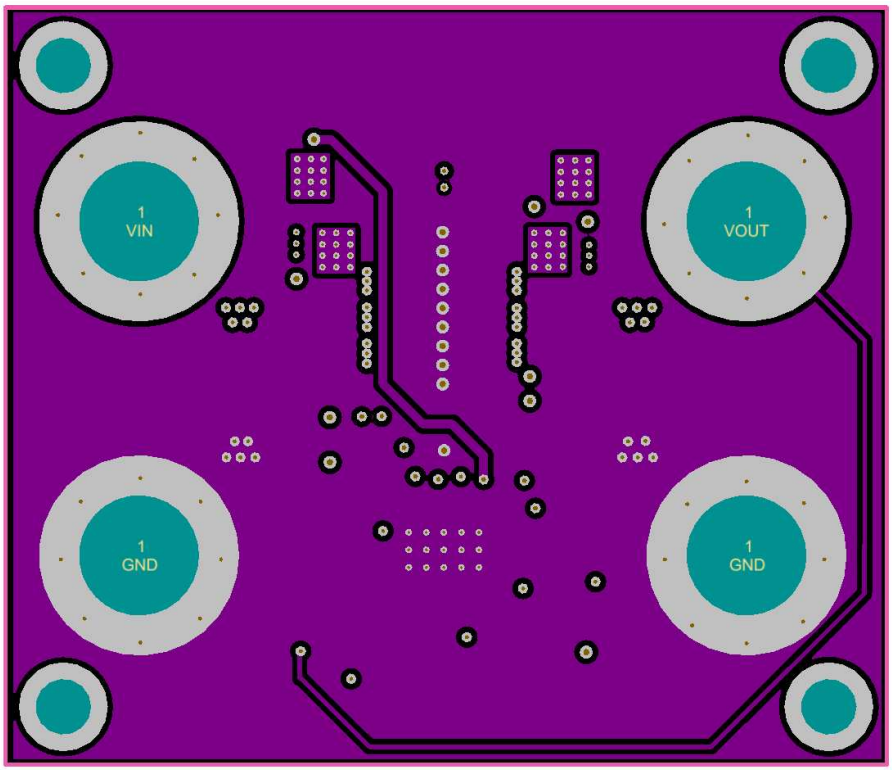


Figure 56. Layer 5 (Top view)

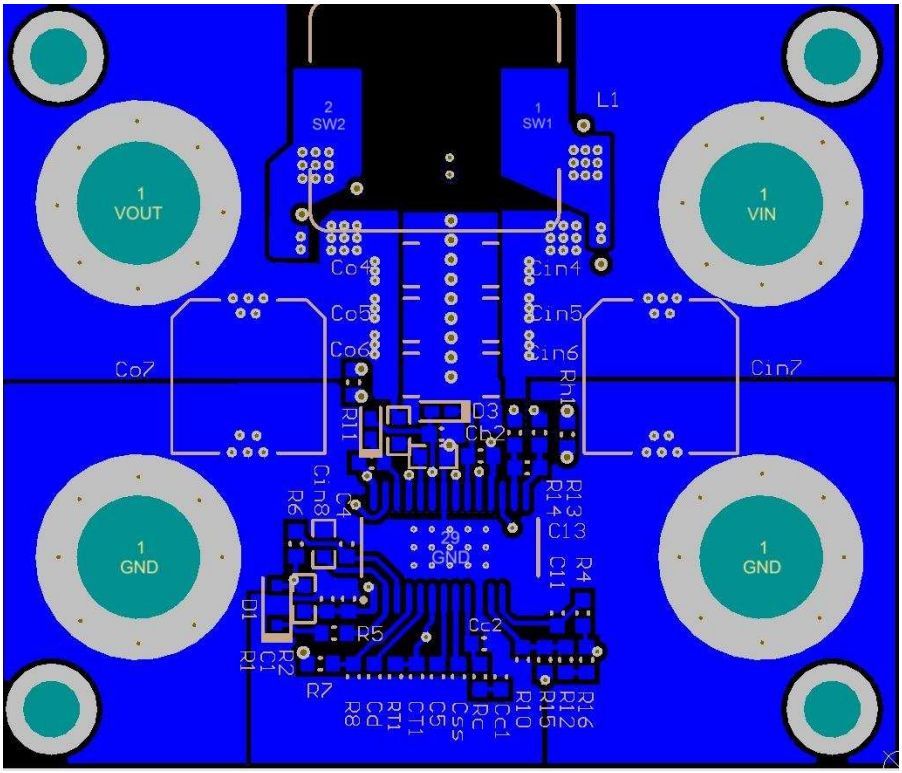


Figure 57. Bottom Copper (Bottom view)

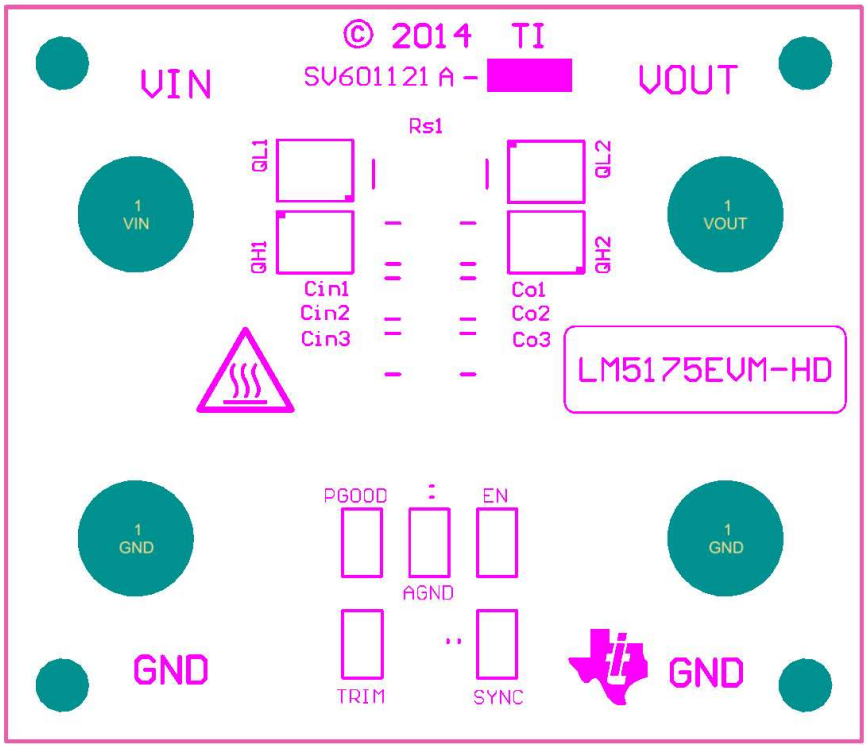


Figure 58. Top Layer Silkscreen (Top view)

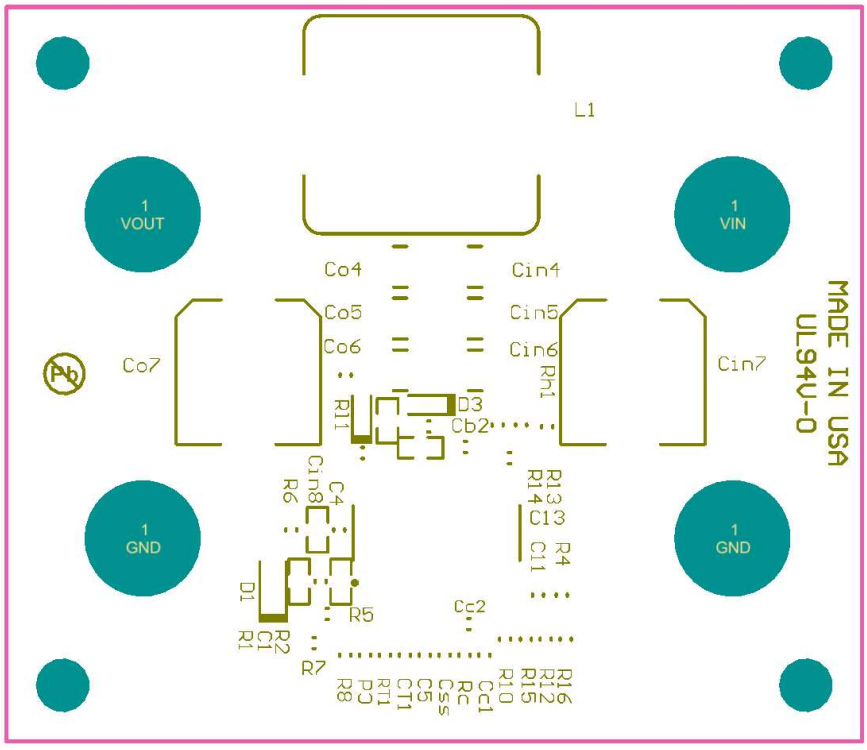


Figure 59. Bottom Layer Silkscreen (Bottom view)

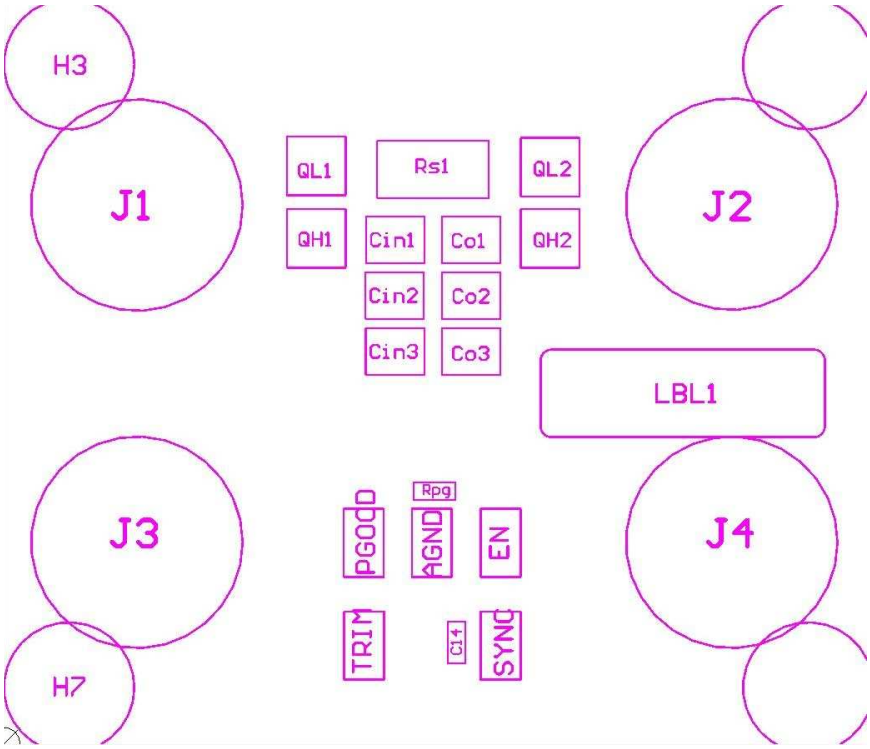


Figure 60. Top Assembly

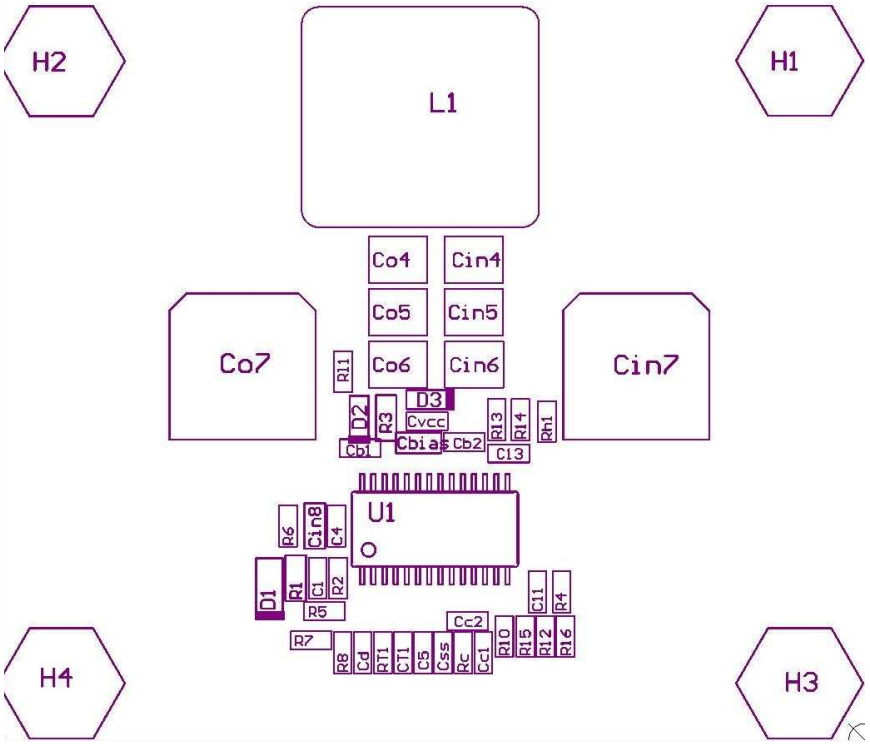


Figure 61. Bottom Assembly

8.3 Bill of Materials

Table 3. Bill of Materials

Count	Ref Des	Description	Part Number	MFR
4	C1, C4, C11, CT1	Capacitor, Ceramic, 100pF, 50V, C0G, 5%, 0603	Std	Std
1	Cc1	Capacitor, Ceramic, 22nF, 25V, X7R, 10%, 0603	Std	Std
1	Cc2	Capacitor, Ceramic, 220pF, 50V, C0G, 5%, 0603	Std	Std
1	Css	Capacitor, Ceramic, 33nF, 25V, X7R, 10%, 0603	Std	Std
1	C5	Capacitor, Ceramic, 120pF, 50V, C0G, 5%, 0603	Std	Std
1	C13	Capacitor, Ceramic, 47pF, 50V, C0G, 5%, 0603	Std	Std
1	C14	Capacitor, Ceramic, 2.2nF, 50V, X7R, 10%, 0603	Std	Std
2	Cb1, Cb2	Capacitor, Ceramic, 0.1µF, 25V, X7R, 10%, 0603	Std	Std
2	Cbias, Cin8	Capacitor, Ceramic, 0.22µF, 50V, X7R, 10%, 0603	Std	Std
12	Cin1, Cin2, Cin3, Cin4, Cin5, Cin6, Co1, Co2, Co3, Co4, Co5, Co6	Capacitor, Ceramic, 10µF, 50V, X7S, 10%, 1210	GRM32EC71H106KA03L	Murata
			CGA6P3X7S1H106K250AE	TDK
		Capacitor, Ceramic, 10µF, 50V, X7R, 10%, 1210	C1210C106K5RACTU	Kemet
			GRM32ER71H106KA12L	Murata
			UMK325AB7106KM-T	Taiyo Yuden
2	Cin7, Co7	Capacitor, AL, 68µF, 50V, 20%, 30mΩ, 4000hr	EEHZC1H680P	Pansonic
			NSPE-Z680M50V8X10	NIC Components
1	Cvcc	Capacitor, Ceramic, 1µF, 25V, X7R, 10%, 0603	GRM188R71C105KA12D	Murata
1	D1	Diode Schottky, 30V, 200mA, SOD-323	BAT54HT1G	On Semi
2	D2, D3	Diode, 100V, 0.2A, SOD-523	BAS516	NXP
1	L1	Inductor, 3.3µH, 5.9mΩ DCR, 22A Isat	PIMB135T-3R3MS	Cyntec
		Inductor, 3.7µH, 4.9mΩ DCR, 16A Isat	7443551370	Wurth
2	QH1, QL1	MOSFET, N-Channel, 60V, 40A, PG-TSDSON-8	BSZ042N06NS	Infineon
2	QH2, QL2	MOSFET, N-Channel, 30V, 40A, PG-TSDSON-8	BSZ0902NS	Infineon
2	R1, R8	Resistor, Chip, 200kΩ, 1/10W, 1%, 0603	Std	Std
1	R2	Resistor, Chip, 52.3kΩ, 1/10W, 1%, 0603	Std	Std
5	R3, R4, R5, R6, R16	Resistor, Chip, 10Ω, 1/10W, 1%, 0603	Std	Std
1	R10	Resistor, Chip, 7.15kΩ, 1/10W, 1%, 0603	Std	Std
1	R12	Resistor, Chip, 100kΩ, 1/10W, 1%, 0603	Std	Std
2	R13, R14	Resistor, Chip, 100Ω, 1/10W, 1%, 0603	Std	Std
1	R15	Resistor, Chip, 6.65kΩ, 1/10W, 1%, 0603	Std	Std
1	Rpg	Resistor, Chip, 20kΩ, 1/10W, 1%, 0603	Std	Std
1	Rc	Resistor, Chip, 3.01kΩ, 1/10W, 1%, 0603	Std	Std
3	Rh1, Rl1, R7	Resistor, Chip, 0Ω, 1/10W, 5%, 0603	Std	Std
1	Rs1	Resistor, 7mΩ, 3W, 1%, 2512 WIDE	KRL6432E-M-R007	Susumu
			CSR1225FK07L0	Stackpole
			LRF3WLF-01-R007	TT Electronics
1	RT1	Resistor, Chip, 60.4kΩ, 1/10W, 1%, 0603	Std	Std
1	U1	IC, Synchronous Buck-Boost Controller, TSSOP-28	LM5175PWP	TI
1	PCB1	PCB, FR4, 6 layer, 2 oz, 50 mm x 43 mm	PCB	Any
4	VIN, VOUT, GND, GND	Banana Jack Power Terminal with Solder Lug	108-0740-001	Emerson
4	H3, H4, H7, H8	Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F
4	H1, H2, H5, H6	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone
5	AGND, EN, TRIM, PGOOD, SYNC	Test Point, SMT	5016	Keystone

Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS AND CONDITIONS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT MADE, CONCEIVED OR ACQUIRED PRIOR TO OR AFTER DELIVERY OF THE EVM.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS ANDCONDITIONS OR THE USE OF THE EVMS PROVIDED HEREUNDER, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS OCCURRED.

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