

+/- 5V Isolated, Low Noise Split Rail Generator (0.25A, 2.5W total)

National Semiconductor
RD-171
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1.0 Design Specifications

Inputs	Output #1	Output #2
VinMin=9V	Vout1=5V	Vout2=-5V
VinMax=30V	Iout1=0.25A	Iout2=0.25A

2.0 Design Description

A very low noise differential power supply for split rail systems requiring low noise +5V and -5V (higher or lower voltage is possible). This design is fully isolated and capable of floating to over 500V differential from Vin to Vout (higher is possible). The LM5001 IC is a fully integrated flyback regulator which performs all of the current mode control for tight regulation and transient response. The design is small and uses only one side of a double sided FR4 PCB for components. Smaller IC packages are available so the layout can be further optimized.

This design provides very low noise bias rails for ground referenced analog circuitry (under 20 mV p-p total noise up to 1GHz). The design utilizes a very small size PCB footprint. This approach is ideal for many applications including low noise cable drivers, medical electronics, high fidelity low power audio, and other sensitive circuitry that can benefit from very low noise split rail biasing. Input to output isolation is

employed for those applications where the input and output voltages might be at different potentials or when the input voltage travels across cabling which might pickup noise. The floating outputs avoid unwanted ground currents and the potential for additional noise pickup. For those that do not require isolation they can remove the feedback isolation section of the design and use a simple resistor divider for setting the feedback voltage.

3.0 Features

- Very Low Noise, <20 mV P-P
- Fully Isolated Outputs, > 500V
- Small Size
- Wide Input Range > 10V - 30V
- Double sided PCB
- 600 KHz Operation

4.0 Block Diagram

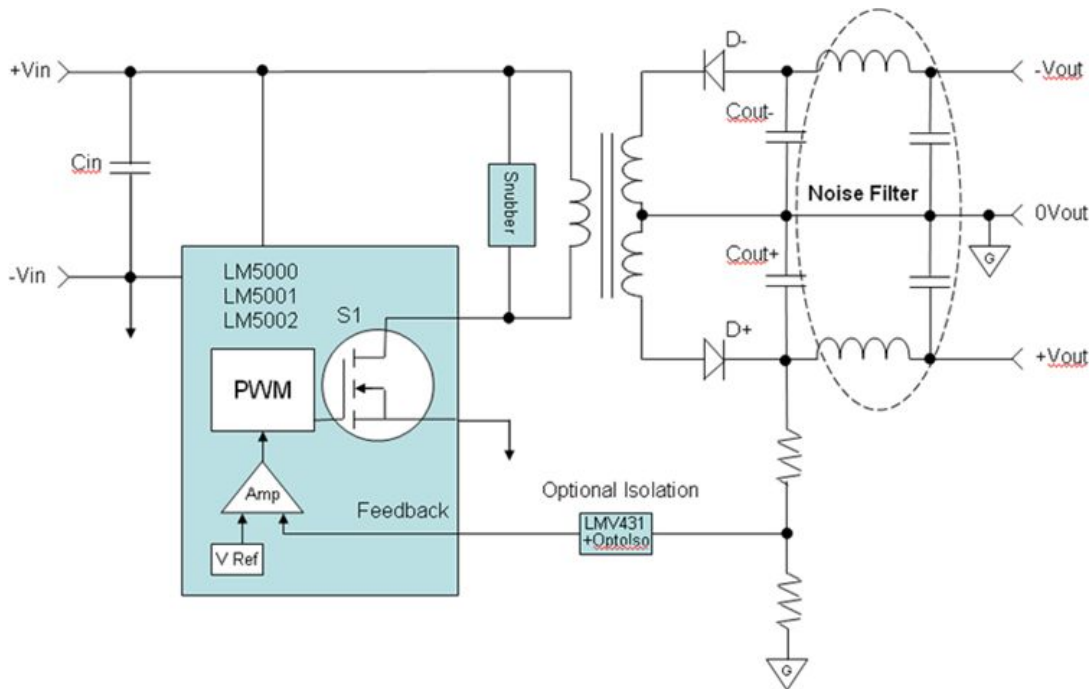
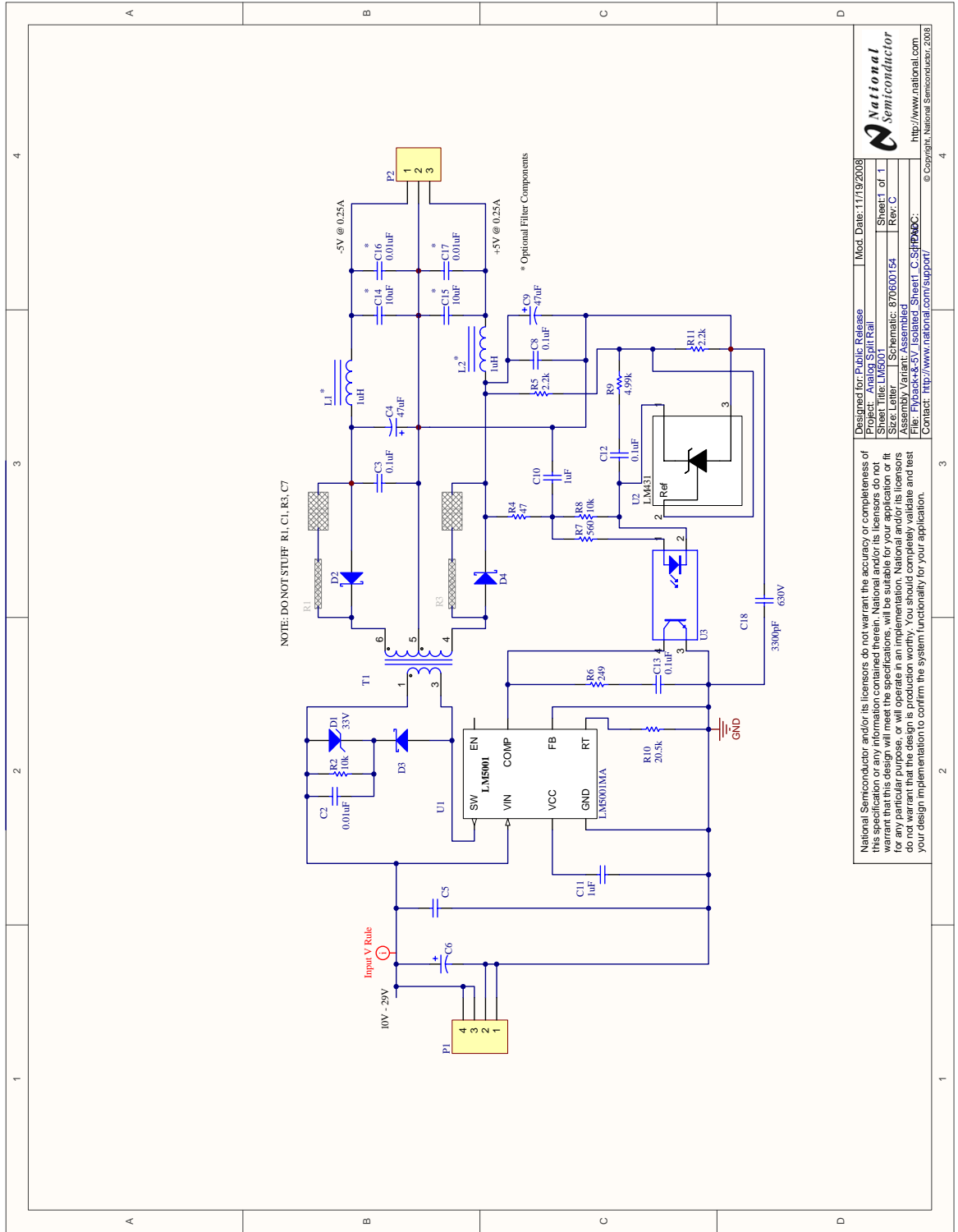


FIGURE 1. Block Diagram

diagram3

5.0 Schematic



Designed for Public Release	Mod. Date: 11/19/2008
Sheet Title: L14501	Sheet 1 of 1
Size: Letter	Schematic: 870600154
Assembly Variant: Assembled	Rev: C
File: Flyback-5V Isolated_Sheet1_C_SchPAC	
Contact: http://www.national.com/support/	

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FIGURE 2. Schematic

6.0 Bill of Materials

Designator	Value	PackageReference	Characteristics	Manufacturer	PartNumber	RoHS
C2	0.01uF	0603	Ceramic, X7R, 50V, 10%	MuRata	GRM188R71H103KA01D	Y
C3, C5, C8, C12, C13	0.1uF	0805	Ceramic, X7R, 50V, 5%	Kemet	C0805C104J5RACTU	Y
C4, C9	47uF	SMT Radial D	AL, 16V, 20%, 0.36Ohm ESR	Panasonic	EEE-FK1C470P	Y
C6	10uF	E61	AL, 50V, 20%	Nippon Chemi-Con	EMZA500ADA100ME61G	Y
C10	1uF	0805	Ceramic, X5R, 20V, 10%	Taiyo Yuden	TMK212BJ105KG-T	Y
C11	1uF	1210	Ceramic, X7R, 50V, 10%	MuRata	GRM32RR71H105KA01L	Y
C14, C15	10uF	0805	Ceramic, X5R, 16V, 10%	Taiyo Yuden	EMK212BJ106KG-T	Y
C16, C17	0.01uF	0603	Ceramic, X7R, 50V, 10%	TDK	C1608X7R1H103K	Y
C18	3300pF	1206	Ceramic, C0G/NP0, 630V, 5%	TDK	C3216C0G2J332J	Y
D1	33V	SMB		ON Semiconductor	1SMB5937BT3G	Y
D2, D4	0.45V	SOD-123	Vr = 40V, Io = 1A, Vf = 0.45V	Diodes Inc.	1N5819HW-7-F	Y
D3	1V	SOD-123	Vr = 100V, Io = 0.2A, Vf = 1V	ST Microelectronics	BAT41ZFILM	Y
L1, L2	1uH	ME3220	Unshielded Drum Core, 2.7A, 0.058 Ohm	Coilcraft Inc.	ME3220-102MLB	Y
P1	1x4			Molex	90120-0124	Y
P2	1x3			Molex	90120-0123	Y
R2, R8	10k	0603	5%, 0.1W	Vishay-Dale	CRCW060310k0JNEA	Y
R4	47	0603	5%, 0.1W	Vishay-Dale	CRCW060347R0JNEA	Y
R5, R11	2.2k	0603	5%, 0.1W	Vishay-Dale	CRCW06032k20JNEA	Y
R6	249	0603	1%, 0.1W	Vishay-Dale	CRCW0603249RFKEA	Y
R7	560	0603	5%, 0.1W	Vishay-Dale	CRCW0603560RJNEA	Y
R9	4.99k	0603	1%, 0.1W	Vishay-Dale	CRCW06034k99FKEA	Y
R10	20.5k	0603	1%, 0.1W	Vishay-Dale	CRCW060320k5FKEA	Y
T1				Renco Electronics, INC.	RL-8800	Y
U1				National Semiconductor	LM5001MA	Y
U2				National Semiconductor	LM431CCM3	Y
U3		FOD121		Fairchild Semiconductor	FODM121	Y

FIGURE 3. BOM

7.0 Other Operating Values

Operating Values

Description	Parameter	Value	Unit
Switching Frequency	Frequency	600	KHz
Output power (minimum)	Pout	2.5	W
Steady State Efficiency	Efficiency	82.5	%
Peak-to-Peak differential noise	Vout p-p	13	mV

8.0 Board Photos

bom4

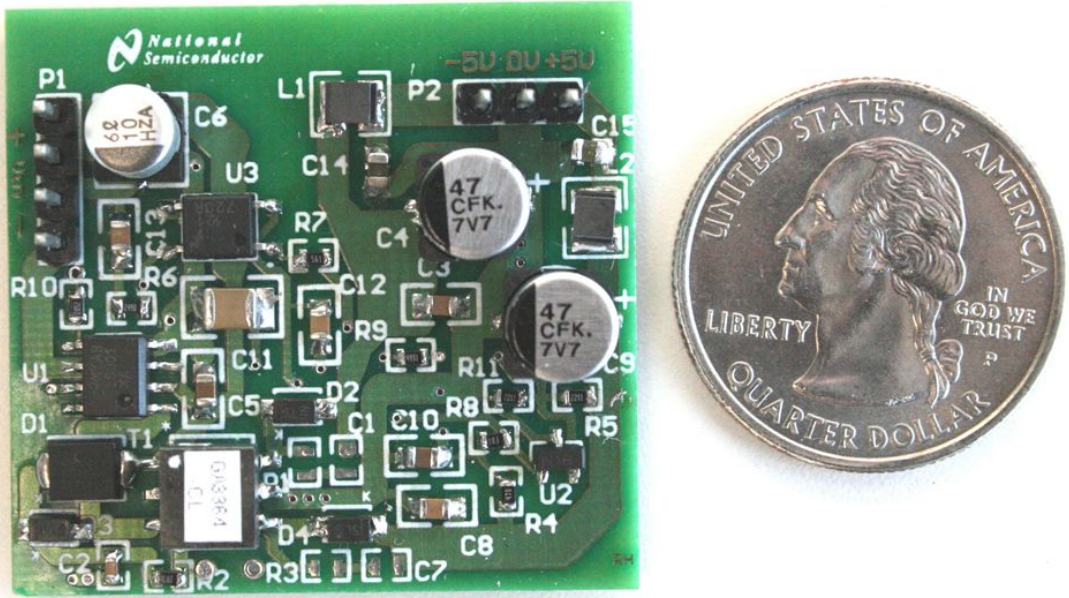
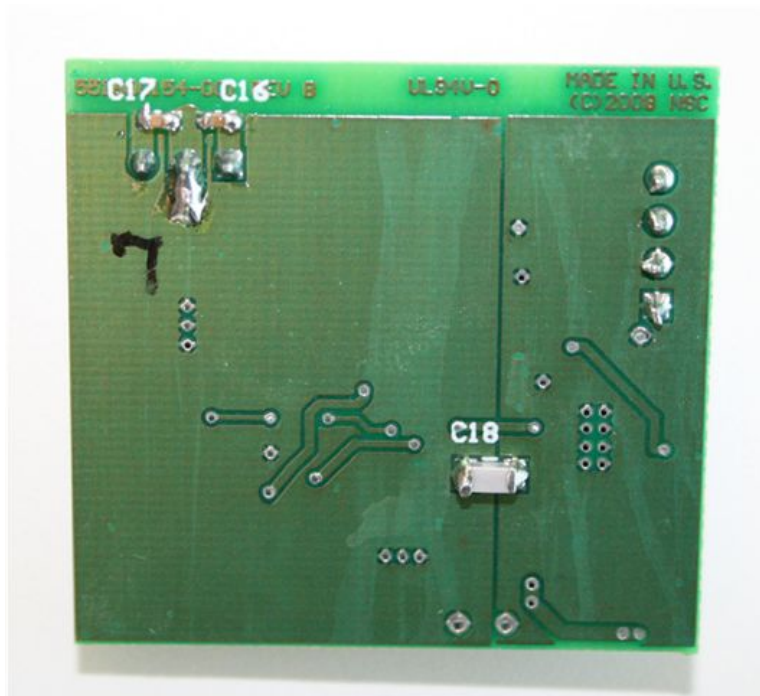


FIGURE 4. PCB

other



boardphoto4

FIGURE 5. Backside

9.0 Quick Start

Connect a lab power supply to connector P1 with the polarity as shown on the PCB (+ and - is in copper). Connect separate + and - loads or a differential load across the output connector P2 (polarity is again shown in copper). Set the input voltage between 8 and 35V and measure the appropriate output voltage and current.

10.0 Hardware Description

This is a very low noise +5V and -5V power supply optimized for driving analog signal path circuits. This circuit employs a flyback switching topology to provide a small PCB footprint. The design can operate from below 10V to above 30V and provides over 80% efficiency. By using a flyback topology both output rails are being switched at the same time which provides common mode benefits when biasing analog circuitry. The differential noise from the +5V to the -5V is well below 20mV including ripple and switching transient noise. An LC post filter is employed on each output to significantly reduce switching noise and ripple without significantly effecting load regulation. These filters can be removed for applications that do not require low noise. Without the post filters (L1/C14, L2/C15) one can expect approximately 100mV p-p ripple+noise on each output.

The PWM frequency is set to operate at 600 KHz via R10. This frequency was chosen to provide a balance of good efficiency while maintaining low noise. One could further trade-off efficiency for noise by adjusting the PWM frequency.

The flyback topology within the LM5001 employs a switch between the primary winding of the transformer and ground. When the switch is closed energy is transferred from the input to the primary winding. When the switch is opened the energy is moved from the secondary of the transformer to the outputs. The switch is controlled by a PWM modulator. The modulator is stimulated by an error amplifier which creates an error term related to the output voltage in relation to a reference voltage. When the flyback control loop is in steady state continuous conduction mode, the PWM duty cycle (D) relates to the Vin, Vout, and the turns ratio of the transformer and the forward voltage drop of secondary catch diodes.

$$D = (V_o + V_f) / (V_o + V_f + ((N_s/N_p) * V_{in}))$$

Where:

Ns = Turns on the secondary windings

Np = Turns on the primary windings

Vf = Forward voltage drop of the catch diodes

During phase 1 the transformer core is charged, the secondary catch diodes (D2 and D4) remain off, and energy is delivered to the output from the output capacitors (C4 and C9). During phase 2 the secondary delivers energy to the output capacitors via the forward biased catch diodes. The output capacitors are charged during phase 2 to ensure continuous delivery of energy during phase 1.

A primary RCD snubber is employed by R2, C2, D3. These values were chosen to minimize the transient noise and ringing generated when the switch inside the LM5001 is open. The values of this snubber are chosen to dissipate minimal power while providing sufficient transient suppression. D1 is a zener diode which acts like an additional snubber yet only turns on when extreme transients are produced across the primary winding of T1. Extreme transients can occur when the output is changed from a very low to a very high load as when the output is inadvertently shorted and then opened. During these situations the Zener will turn on as the voltage increases above approximately (Vin + (Vz of D1) + (Vf of D3)). The

zener diode protects the LM5001 from exceeding its maximum switch voltage of 76V on pin 1 while dissipating minimal power during normal operation (snubbers employing a zener diode during normal operation negatively impact efficiency). One could reduce the BOM cost a bit by employing only a zener snubber, yet this will forfeit some efficiency and possibly increase system noise.

This design includes snubbers for both secondary outputs (C1/R1, C7/R3). After bench testing it was determined that the additional noise reduction with these snubbers added was minimal, so the components were not stuffed for the testing shown.

Isolation is provided between the input and outputs, allowing the output ground reference and voltages to float above or below the input voltage and ground. The transformer T1 provides the isolation for the forward path and the opto-isolator U3 provides isolation of the feedback voltage. An LM431 voltage reference/amp IC is used to monitor the output voltage and feedback an error current through the opto-isolator to the LM5001. Separate primary and secondary ground planes are provided, yet the grounds are connected with a high voltage capacitor to reduce unwanted output noise during switching. Isolation limits are set by the breakdown limits of the transformer, the opto-isolator, and the capacitor across the ground planes. This design should be capable of supporting up to 500V differential across the input to output,

Though the LM5001 IC provides over-current protection on its switch output (pin 1), the secondary of the transformer does not have direct current limiting. A shorted output (to ground or V+ to V-) will result in current limiting of the primary, avoiding any damage to the IC. Because of higher power dissipation in the transformer T1, increased temperature may result in degradation of the transformer. Thermal protection is also provided in the LM5001 IC.

11.0 Test Results

The following efficiency measurements were made using a standard Agilent bench power supply (Model E3532A), where the Vin was established by measuring the voltage at the input connector P1. The input voltage was measured using a Fluke 189 and the voltage was set by adjusting the power supply to obtain within 1 mV accuracy. The same meter and probes were used for measuring the output voltage, The absolute accuracy of the Vin or Vout measurements are not as important and a consistent input to output measurement so the same equipment and probes were used.

The output load used for the efficiency measurements was a Kikusui PLZ164WA Dynamic Load across the V+ to V-. The dynamic load was used for the measurement of the load current and the Agilent E3532A was used for the input current measurements.

The efficiency at higher voltages are sacrificed by the internal 6.9V bias generator. As described in the datasheet for the IC, one can externally drive this bias from a voltage between 7 - 12V to reduce power dissipation and slightly improve efficiency. This can be accomplished by adding an additional winding to the transformer to feed a lower bias voltage directly into the device.

The noise measurements were made using a LeCroy 454 Oscilloscope with a LeCroy AP033 Active Probe placed directly across the output connector P2. Each of the outputs were loaded using 20 ohm power resistors.

Because of the symmetry of the flyback secondary design, the differential noise is not simply the addition of the noise on each rail. As shown, the flyback approach for developing a

split rail system results in inherent cancellation of the synchronous noise. This advantage is not evident in other split rail power supply architectures. Symmetrical layout of the secondary circuit can further improve the differential noise cancellation.

The Bode plot was measured with $V_{in} = 15V$ using a AP instrument Model 200 Network Analyzer with both outputs delivering 250 mA. Control loop compensation is accomplished

by the RC circuit connected to the Comp pin of the LM5001 (R6/C13 and R9/C12). In this circuit the feedback signal is safely fed into the same COMP pin of the regulator and the Feedback pin is shorted to ground. This provides a method to bypass the voltage reference and error amplifier internal to the LM5001, allowing the use of a separate reference and amplifier on the secondary side of the transformer (U3 – LM431).

12.0 Waveforms

Vin	Iout(A)	Iin (A)	V+	V-	Vout (+ to -)	Pin	Pout	Efficiency
10.000	0.050	0.059	4.99	4.984	9.974	0.590	0.499	84.53%
10.000	0.100	0.118	4.984	4.982	9.966	1.180	0.997	84.46%
10.000	0.150	0.178	4.981	4.977	9.958	1.780	1.494	83.92%
10.000	0.200	0.243	4.977	4.973	9.95	2.430	1.990	81.89%
10.000	0.250	0.312	4.972	4.969	9.941	3.120	2.485	79.66%
10.000	0.300	0.387	4.966	4.966	9.932	3.870	2.980	76.99%
12.000	0.050	0.051	4.987	4.983	9.97	0.612	0.499	81.45%
12.000	0.100	0.099	4.981	4.983	9.964	1.188	0.996	83.87%
12.000	0.150	0.148	4.98	4.977	9.957	1.776	1.494	84.10%
12.000	0.200	0.2	4.976	4.973	9.949	2.400	1.990	82.91%
12.000	0.250	0.255	4.973	4.968	9.941	3.060	2.485	81.22%
12.000	0.300	0.313	4.968	4.966	9.934	3.756	2.980	79.35%
24.000	0.050	0.029	4.988	4.984	9.972	0.696	0.499	71.64%
24.000	0.100	0.051	4.984	4.98	9.964	1.224	0.996	81.41%
24.000	0.150	0.077	4.981	4.977	9.958	1.848	1.494	80.83%
24.000	0.200	0.101	4.978	4.974	9.952	2.424	1.990	82.11%
24.000	0.250	0.126	4.975	4.974	9.949	3.024	2.487	82.25%
24.000	0.300	0.152	4.971	4.968	9.939	3.648	2.982	81.74%
30.000	0.050	0.025	4.989	4.983	9.972	0.750	0.499	66.48%
30.000	0.100	0.043	4.984	4.98	9.964	1.290	0.996	77.24%
30.000	0.150	0.063	4.982	4.977	9.959	1.890	1.494	79.04%
30.000	0.200	0.083	4.978	4.975	9.953	2.490	1.991	79.94%
30.000	0.250	0.102	4.976	4.97	9.946	3.060	2.487	81.26%
30.000	0.300	0.122	4.972	4.967	9.939	3.660	2.982	81.47%

image

FIGURE 6. Efficiency Chart

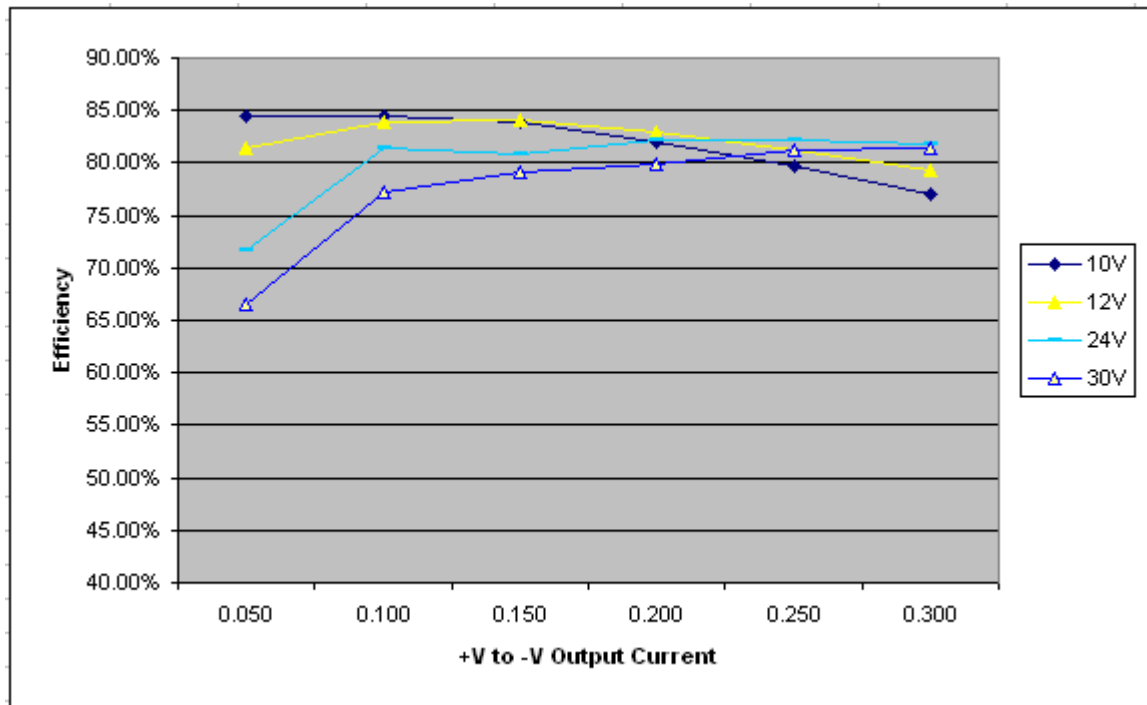


image1

FIGURE 7. Efficiency Graph

Vin = 15V	-.5V=1800hm (27mA)		-.5V=200hm (250mA)	
Iout +5V	Vout +5V	Vout -5V	Vout +5V	Vout -5V
0.025	4.99	-4.97	4.99	-4.71
0.050	4.98	-5.03	4.98	-4.79
0.100	4.98	-5.10	4.98	-4.86
0.150	4.98	-5.14	4.98	-4.90
0.200	4.97	-5.19	4.98	-4.94
0.250	4.97	-5.23	4.97	-4.97

waveform2

FIGURE 8. Cross Regulation

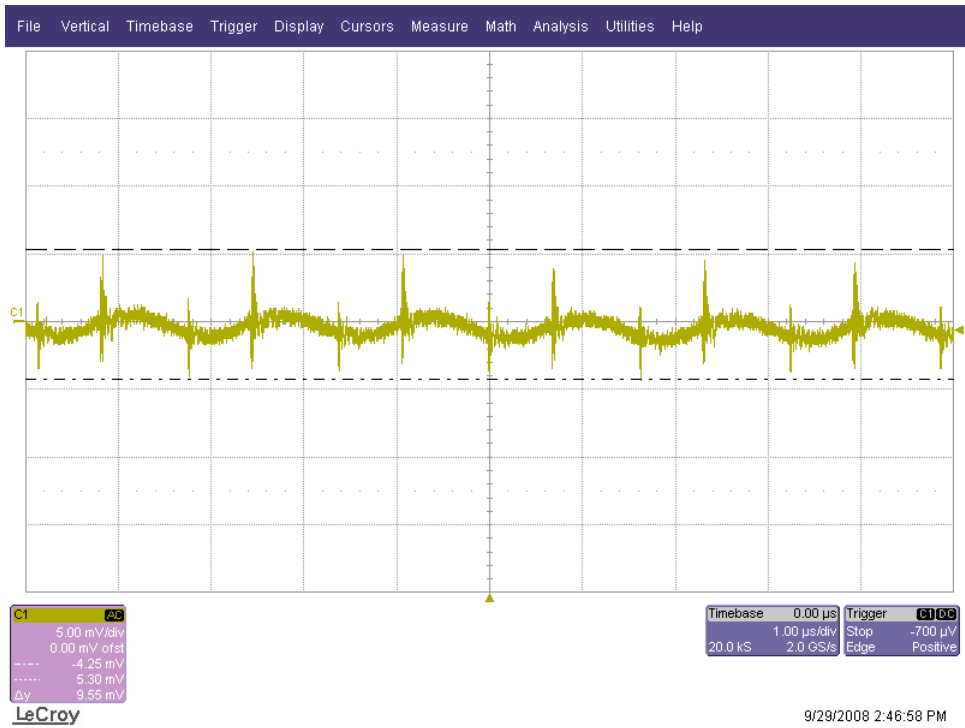


FIGURE 9. +5V Noise = 9.55mV P-P

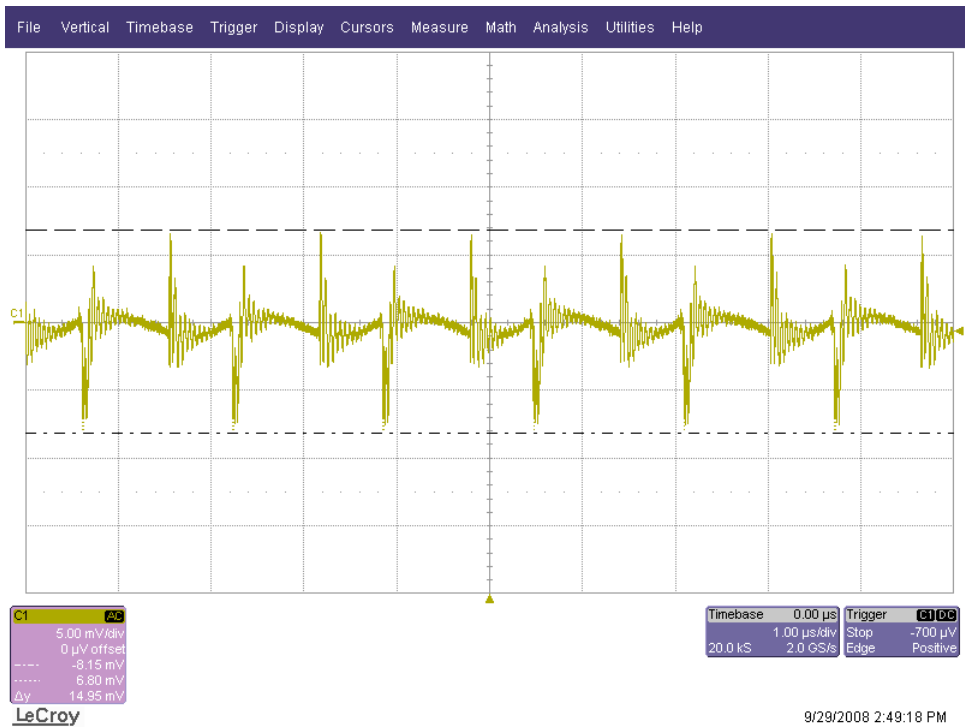


FIGURE 10. -5V Noise = 14.95mV P-P

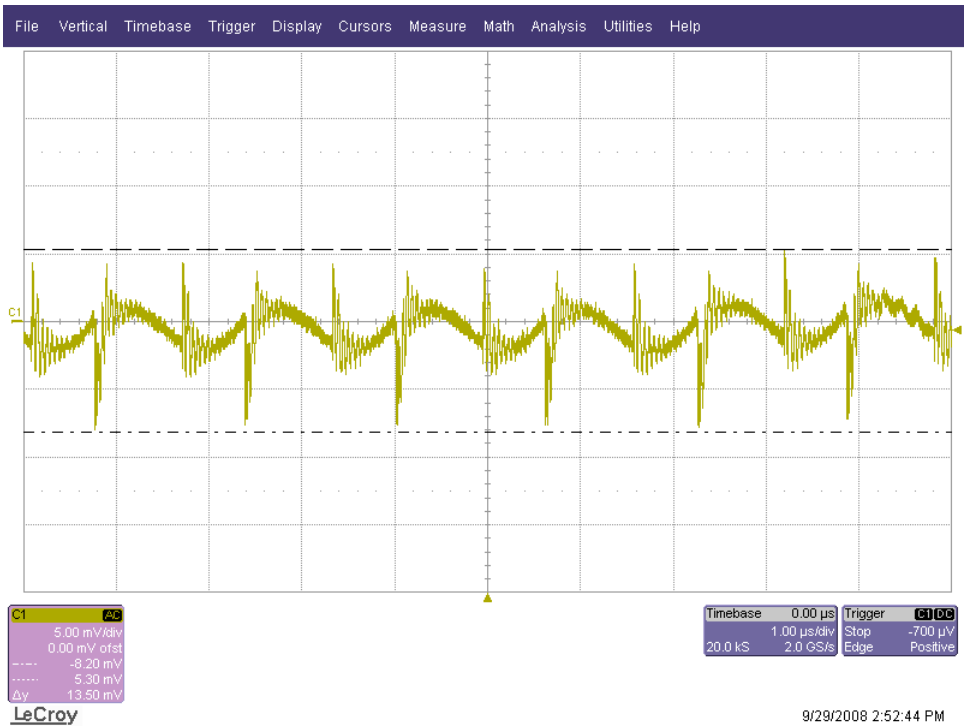
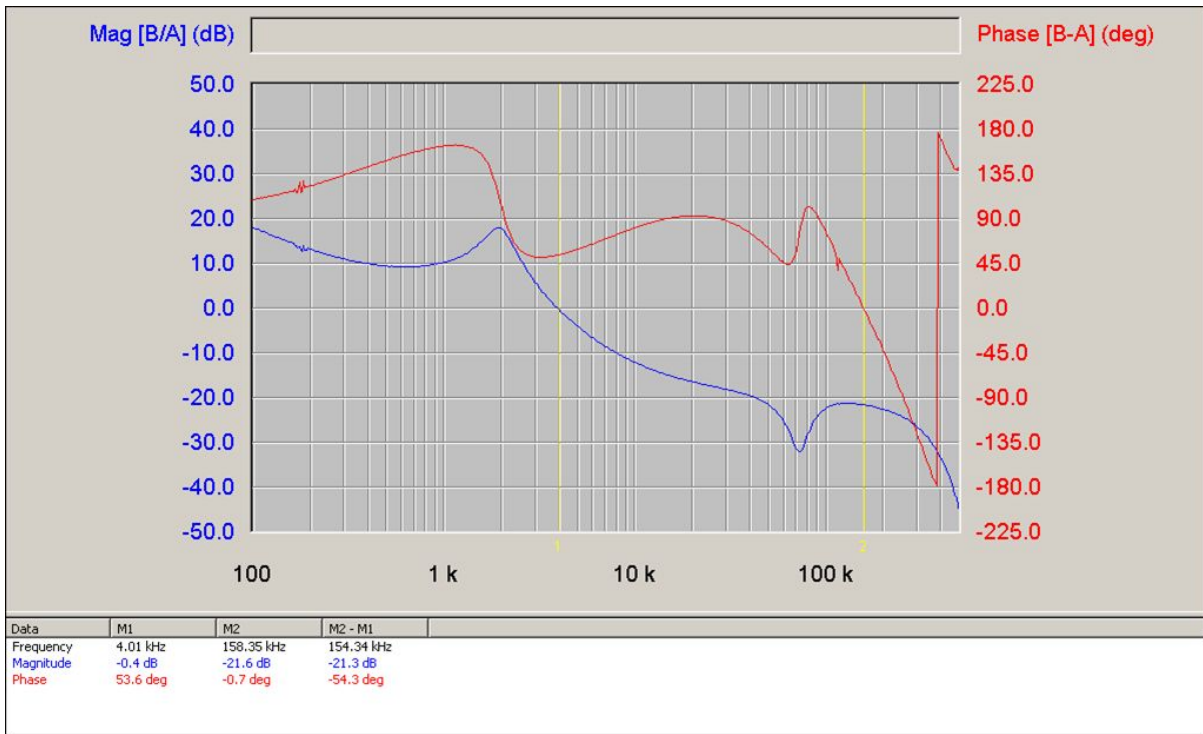


FIGURE 11. Differential Noise =12.60mV P-P



waveform3

FIGURE 12. Bode Plot: Vin = 15V, Iout = 0.25A

Notes

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