Small +/- 5V Isolated Split Rail Generator

National Semiconductor
RD-186
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1.0 Design Specifications

Inputs	Output #1	Output #2
VinMin=10V	Vout1=5V	Vout2=-5V
VinMax=29V	Iout1=0.25A	Iout2=0.25A

2.0 Design Description

A very low noise differential power supply for split rail systems requiring +5V and -5V (higher or lower voltage is possible). This design is fully isolated and capable of floating to over 500V differential from Vin to Vout (higher is possible). The LM5001 IC is a fully integrated flyback regulator which performs all of the current mode control for tight regulation and transient response. This design is a smaller version of RD-171. Design uses smaller components on only one side of a double sided FR4 PCB.

This design provides low noise bias rails for ground referenced analog circuitry (under 2 mV p-p ripple noise up to 1GHz). The design utilizes a very small size PCB footprint. This approach is ideal for many applications including low noise cable drivers, medical electronics, high fidelity low power audio, and other sensitive circuitry that can benefit from very low noise split rail biasing. Input to output isolation is employed for those applications where the input and output voltages might be at different potentials or when the input voltage travels across cabling which might pickup noise. The floating outputs avoid unwanted ground currents and the potential for additional noise pickup. For those that do not require isolation they can remove the feedback isolation section of the design and use a simple resistor divider for setting the feedback voltage.

3.0 Features

- Very Low Noise, <20 mV P-P
- Fully Isolated Outputs, > 500V
- Small Size
- Wide Input Range 10V - 29V
- Double sided PCB
- Top Side Components
- 600 KHz Operation

4.0 Block Diagram

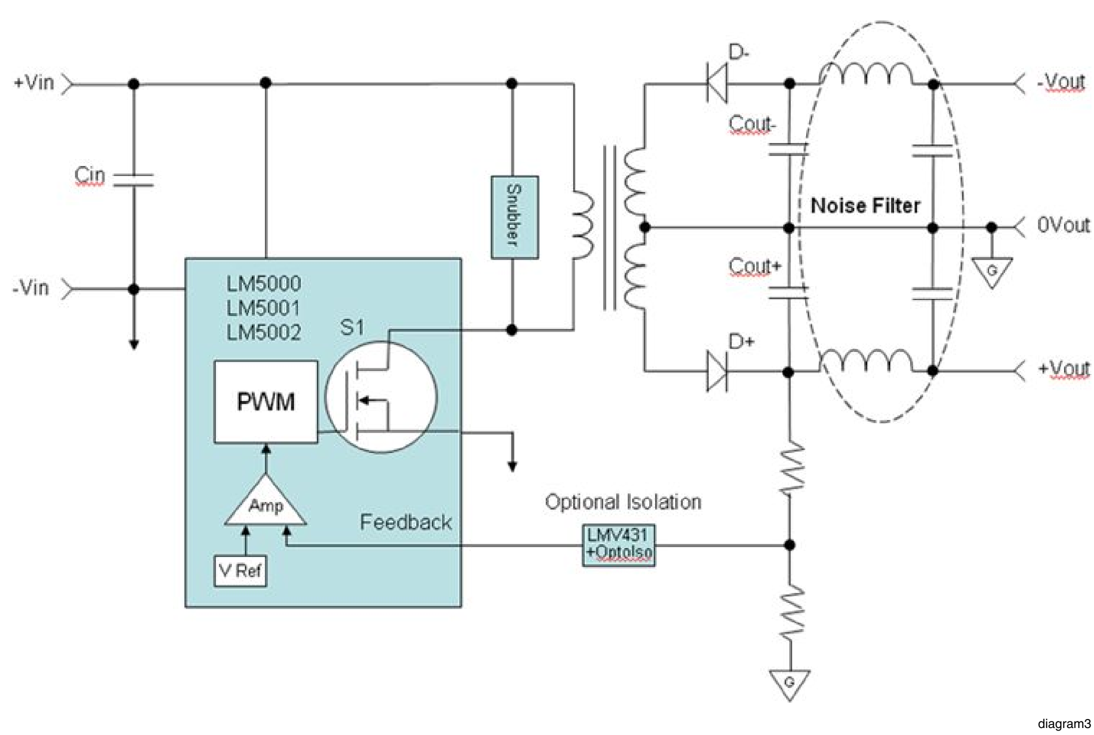

FIGURE 1. Block Diagram

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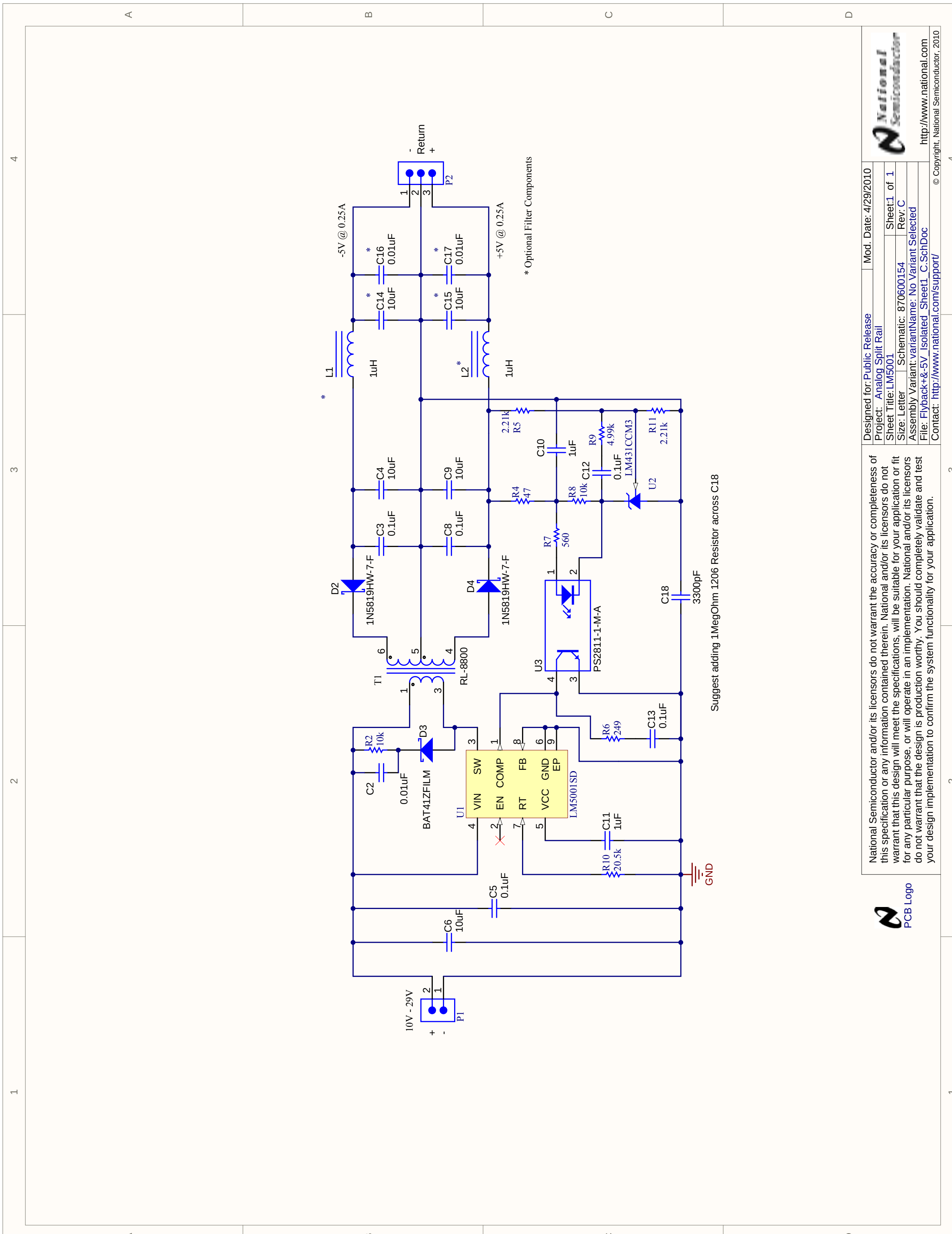
5.0 Schematic



schematic9

FIGURE 2. SplitRail_Flyback_RevC

6.0 Bill of Materials

Designator	Description	Manufacturer	Part Number	RoHS
C2	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H103KA01D	Y
C3, C8, C12, C13	CAP, CERM, 0.1uF, 10V, +/-10%, X5R, 0402	TDK	C1005X5R1A104K	Y
C4, C9, C14, C15	CAP, CERM, 10uF, 16V, +/-10%, X5R, 0805	Taiyo Yuden	EMK212BJ106KG-T	Y
C5	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H104KA93D	Y
C6	Cap, Ceramic Y5V, -20/+80%, 1210	Panasonic	ECJ-4YF1H106Z	Y
C10, C11	CAP, CERM, 1uF, 10V, +80/-20%, Y5V, 0603	TDK	C1608Y5V1A105Z	Y
C16, C17	CAP, CERM, 0.01uF, 16V, +/-10%, X7R, 0402	TDK	C1005X7R1C103K	Y
C18	CAP, CERM, 3300pF, 630V, +/-5%, C0G/NP0, 1206	TDK	C3216C0G2J332J	Y
D2, D4	Diode, Schottky, 40V, 1A, SOD-123	Diodes Inc.	1N5819HW-7-F	Y
D3	Diode, Schottky, 100V, 0.2A, SOD-123	ST Microelectronics	BAT41ZFILM	Y
L1, L2	Inductor, Drum Core, Ferrite, 1uH, 2.6A, 0.058 ohm, SMD	Coilcraft	ME3220-102MLB	Y
P1	Header, TH, 100mil, 1x2, Gold plated, 230 mil above insulator	Samtec Inc.	TSW-102-07-G-S	Y
P2	Header, TH, 100mil, 1x3, Gold plated, 230 mil above insulator	Samtec Inc.	TSW-103-07-G-S	Y
R2, R8	RES, 10k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040210K0JNED	Y
R4	RES, 47 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW040247R0JNED	Y
R5, R11	RES, 2.21k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04022K21FKED	Y
R6	RES, 249 ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW0402249RFKED	Y
R7	RES, 560 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW0402560RJNED	Y
R9	RES, 4.99k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW04024K99FKED	Y
R10	RES, 20.5k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040220K5FKED	Y
T1	Flyback Transfomer +5V/-5V @ 2.5W	Renco Electronics, INC.	RL-8800	Y
U1	High Voltage Switch Mode Regulator	National Semiconductor	LM5001SD	Y
U2	Adjustable Precision Zener Shunt Regulator	National Semiconductor	LM431CCM3	O
U3	Low Input Current, Hight CTR Photocoupler	NEC	PS2811-1-M-A	Y

bom6

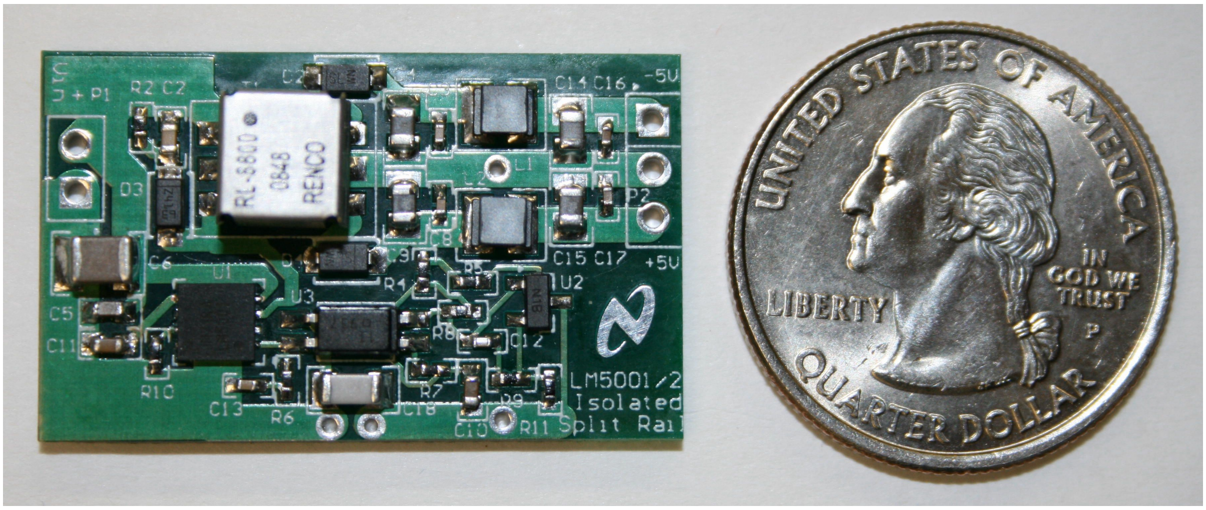
FIGURE 3. Reference Design Bill of Materials-FlybackRevC

7.0 Other Operating Values

Operating Values

Description	Parameter	Value	Unit
Switching Frequency	Frequency	600	KHz
Output power (minimum)	Pout	2.5	W
Steady State Efficiency	Efficiency	81.5	%
Peak-to-Peak Ripple Noise	Vout p-p	2	mV
Peak-to-Peak Differential Noise	Vout p-p	19	mV

8.0 Board Photos



other

FIGURE 4. Pos_Neg5V

9.0 Quick Start

Connect a lab power supply to connector P1 with the polarity as shown on the PCB (+ and - is in copper). Connect separate + and - loads or a differential load across the output connector P2 (polarity is again shown in copper). Set the input voltage between 10 and 29V and measure the output voltage and current.

10.0 Hardware Description

This is a very low noise +5V and -5V power supply optimized for driving analog signal path circuits. This circuit employs a flyback switching topology to provide a small PCB footprint. The design can operate from below 10V to above 30V and provides over 80% efficiency. By using a flyback topology both output rails are being switched at the same time which provides common mode benefits when biasing analog circuitry. The differential noise from the +5V to the -5V is well below 20mV including ripple and switching transient noise. An LC post filter is employed on each output to significantly reduce switching noise and ripple without significantly effecting load regulation. These filters can be removed for applications that do not require low noise. Without the post filters (L1/C14, L2/C15) one can expect approximately 100mV p-p ripple+noise on each output.

The PWM frequency is set to operate at 600 KHz via R10. This frequency was chosen to provide a balance of good efficiency while maintaining low noise. One could further trade-off efficiency for noise by adjusting the PWM frequency.

The flyback topology within the LM5001 employs a switch between the primary winding of the transformer and ground. When the switch is closed energy is transferred from the input to the primary winding. When the switch is opened the energy is moved from the secondary of the transformer to the outputs. The switch is controlled by a PWM modulator. The modulator is stimulated by an error amplifier which creates an error term related to the output voltage in relation to a reference voltage. When the flyback control loop is in steady state continuous conduction mode, the PWM duty cycle (D) relates to the Vin, Vout, and the turns ratio of the transformer and the forward voltage drop of secondary catch diodes.

D= (Vo+Vf)/(Vo+Vf+((Ns/Np)*Vin))

Where:

Ns = Turns on the secondary windings
Np = Turns on the primary windings
Vf = Forward voltage drop of the catch diodes

During phase1 the transformer core is charged, the secondary catch diodes (D2 and D4) remain off, and energy is delivered to the output from the output capacitors (C4 and C9). During phase 2 the secondary delivers energy to the output capacitors via the forward biased catch diodes. The output capacitors are charged during phase 2 to ensure continuous delivery of energy during phase 1.

A primary RCD snubber is employed by R2, C2, D3. This circuit minimizes the transient noise and ringing generated when the switch inside the LM5001, limiting the potential of overstressing the IC. The values of this snubber are chosen to dissipate minimal power while providing sufficient transient suppression.

Isolation is provided between the input and outputs, allowing the output ground reference and voltages to float above or below the input voltage and ground. The transformer T1 provides the isolation for the forward path and the opto-isolator U3 provides isolation of the feedback voltage. An LM431 voltage reference/amp IC is used to monitor the output voltage and feedback an error current through the opto-isolator to the LM5001. Separate primary and secondary ground planes are provided, yet the grounds are connected with a high voltage capacitor to reduce unwanted output noise during switching. Isolation limits are set by the breakdown limits of the transformer, the opto-isolator, and the capacitor across the ground planes. This design should be capable of supporting up to 500V differential across the input to output,

Though the LM5001 IC provides over-current protection on its switch output (pin 1), the secondary of the transformer does not have direct current limiting. A shorted output (to ground or V+ to V-) will result in current limiting of the primary, avoiding any damage to the IC. Because of higher power dissipation in the transformer T1, increased temperature may result in degradation of the transformer. Thermal protection is also provided in the LM5001 IC.

11.0 Test Results

The following efficiency measurements were made using a standard Agilent bench power supply (Model E3532A), where the Vin was established by measuring the voltage at the input connector P1. The input voltage was measured using a Fluke 189 and the voltage was set by adjusting the power supply to obtain within 1 mV accuracy. The same meter and probes were used for measuring the output voltage, The absolute accuracy of the Vin or Vout measurements are not as important and a consistent input to output measurement so the same equipment and probes were used.

The output load used for the efficiency measurements was a Kikusui PLZ164WA Dynamic Load across the V+ to V-. The dynamic load was used for the measurement of the load current and the Agilent E3532A was used for the input current measurements.

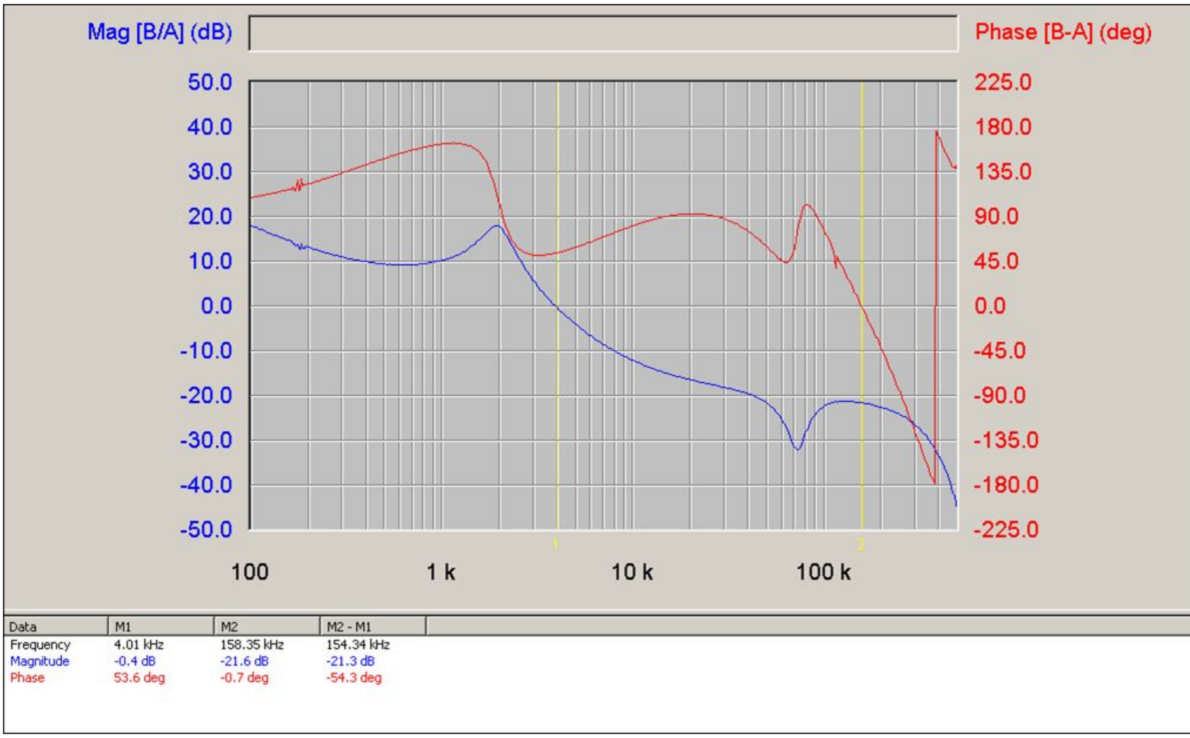
The efficiency at higher voltages are sacrificed by the internal 6.9V bias generator. As described in the datasheet for the IC, one can externally drive this bias from a voltage between 7 - 12V to reduce power dissipation and slightly improve efficiency. This can be accomplished by adding an additional winding to the transformer to feed a lower bias voltage directly into the device.

The noise measurements were made using a LeCroy 454 Oscilloscope with a LeCroy AP033 Active Probe placed directly across the output connector P2. Each of the outputs were loaded using 20 ohm power resistors.

Because of the symmetry of the flyback secondary design, the differential noise is not simply the addition of the noise on each rail. As shown, the flyback approach for developing a split rail system results in inherent cancellation of the synchronous noise. This advantage is not evident in other split rail power supply architectures. Symmetrical layout of the secondary circuit can improve the differential noise cancellation.

The Bode plot was measured with Vin = 15V using a AP instrument Model 200 Network Analyzer with both outputs delivering 250 mA. Control loop compensation is accomplished by the RC circuit connected to the Comp pin of the LM5001 (R6/C13 and R9/C12). In this circuit the feedback signal is safely fed into the same COMP pin of the regulator and the Feedback pin is shorted to ground. This provides a method to bypass the voltage reference and error amplifier internal to the LM5001, allowing the use of a separate reference and amplifier on the secondary side of the transformer (U3 – LM431).

12.0 Waveforms

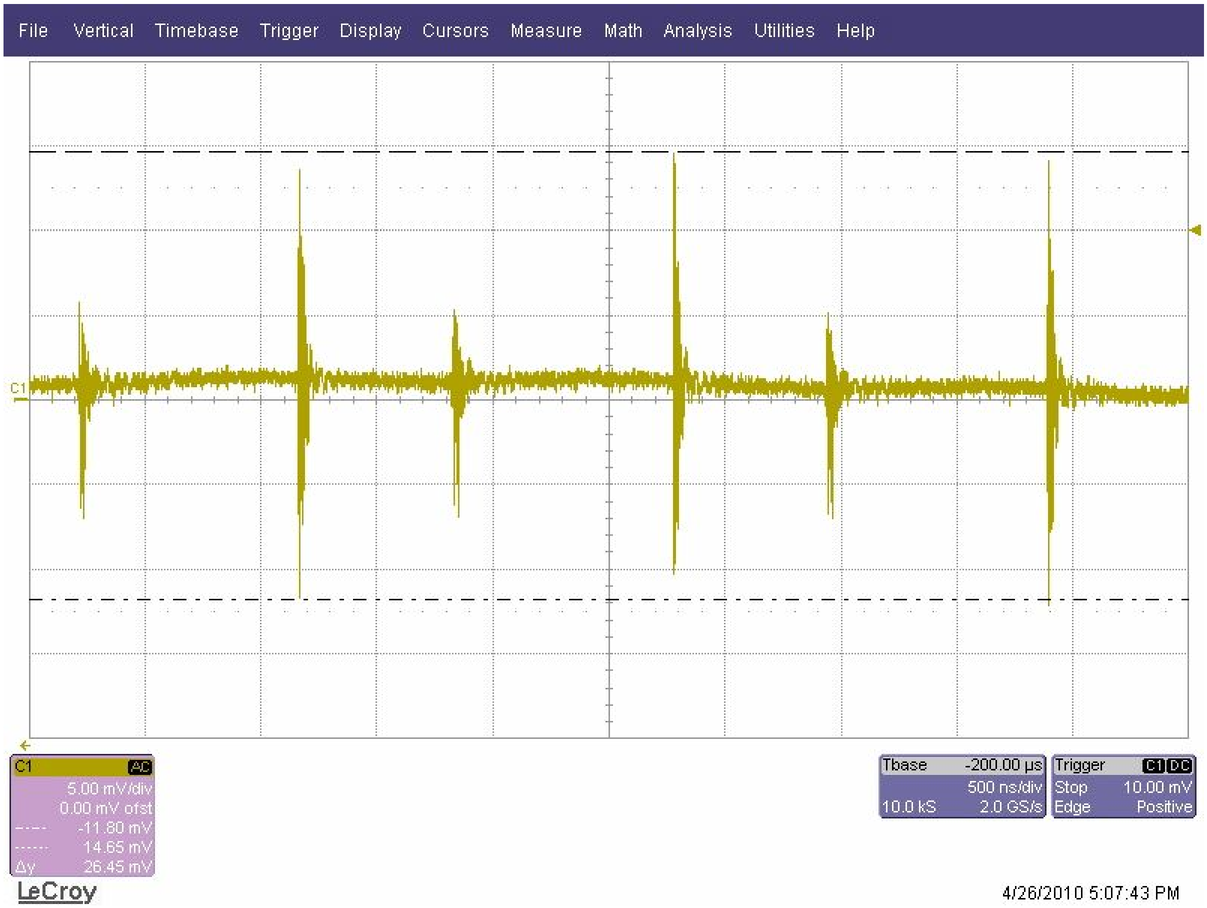


waveform3

FIGURE 5. Bode Plot: Vin = 15V, Iout = 0.25A

waveform3

FIGURE 6. Differential Noise



waveform4

FIGURE 7. + Noise

FIGURE 8. - Noise

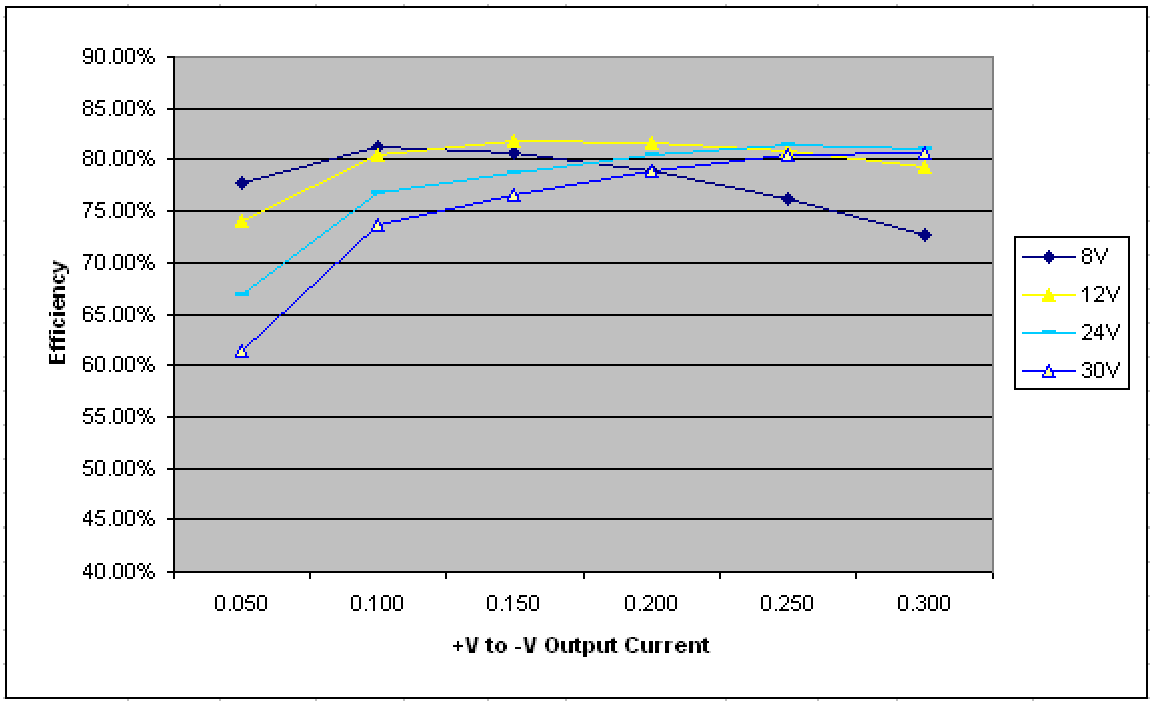


FIGURE 9. Efficiency Graph

Vin	Iout(A)	Iin (A)	V+	V-	Vout (+ to -)	Pin	Pout	Efficiency
8.000	0.025	0.045	4.985	4.976	9.961	0.360	0.249	69.17%
8.000	0.050	0.08	4.984	4.969	9.953	0.640	0.498	77.76%
8.000	0.100	0.153	4.982	4.963	9.945	1.224	0.995	81.25%
8.000	0.150	0.231	4.979	4.963	9.942	1.848	1.491	80.70%
8.000	0.200	0.315	4.975	4.960	9.935	2.520	1.987	78.85%
8.000	0.250	0.407	4.972	4.954	9.926	3.256	2.482	76.21%
8.000	0.300	0.512	4.968	4.955	9.923	4.096	2.977	72.68%
12.000	0.025	0.032	4.985	4.980	9.965	0.384	0.249	64.88%
12.000	0.050	0.056	4.984	4.975	9.959	0.672	0.498	74.10%
12.000	0.100	0.103	4.982	4.970	9.952	1.236	0.995	80.52%
12.000	0.150	0.152	4.979	4.967	9.946	1.824	1.492	81.79%
12.000	0.200	0.203	4.976	4.964	9.940	2.436	1.988	81.61%
12.000	0.250	0.256	4.972	4.960	9.932	3.072	2.483	80.83%
12.000	0.300	0.313	4.968	4.956	9.924	3.756	2.977	79.27%
24.000	0.025	0.019	4.984	4.980	9.964	0.456	0.249	54.63%
24.000	0.050	0.031	4.984	4.974	9.958	0.744	0.498	66.92%
24.000	0.100	0.054	4.982	4.968	9.950	1.296	0.995	76.77%
24.000	0.150	0.079	4.979	4.964	9.943	1.896	1.491	78.66%
24.000	0.200	0.103	4.976	4.961	9.937	2.472	1.987	80.40%
24.000	0.250	0.127	4.972	4.960	9.932	3.048	2.483	81.46%
24.000	0.300	0.153	4.969	4.957	9.926	3.672	2.978	81.09%
30.000	0.025	0.017	4.984	4.981	9.965	0.510	0.249	48.85%
30.000	0.050	0.027	4.982	4.978	9.960	0.810	0.498	61.48%
30.000	0.100	0.045	4.979	4.974	9.953	1.350	0.995	73.73%
30.000	0.150	0.065	4.977	4.970	9.947	1.950	1.492	76.52%
30.000	0.200	0.084	4.973	4.968	9.941	2.520	1.988	78.90%
30.000	0.250	0.103	4.971	4.963	9.934	3.090	2.484	80.37%
30.000	0.300	0.123	4.968	4.959	9.927	3.690	2.978	80.71%

waveform10

FIGURE 10. Efficiency Chart

	Vin=15V			
	.-5V=180Ohm (27mA)		.-5V=20Ohm (250mA)	
Iout_+5V	Vout_+5V	Vout_-5V	Vout_+5V	Vout_-5V
0.025	4.99	-4.97	4.99	-4.75
0.050	4.99	-5.01	4.98	-4.81
0.100	4.98	-5.07	4.98	-4.86
0.150	4.98	-5.10	4.98	-4.90
0.200	4.97	-5.14	4.97	-4.93
0.250	4.97	-5.17	4.97	-4.96
delVo	-0.012	-0.199	-0.012	-0.208
%	-0.2%	-4.0%	-0.2%	-4.2%

waveform11

FIGURE 11. Cross Regulation

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