Functional Safety Information

LM76005-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM76005-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

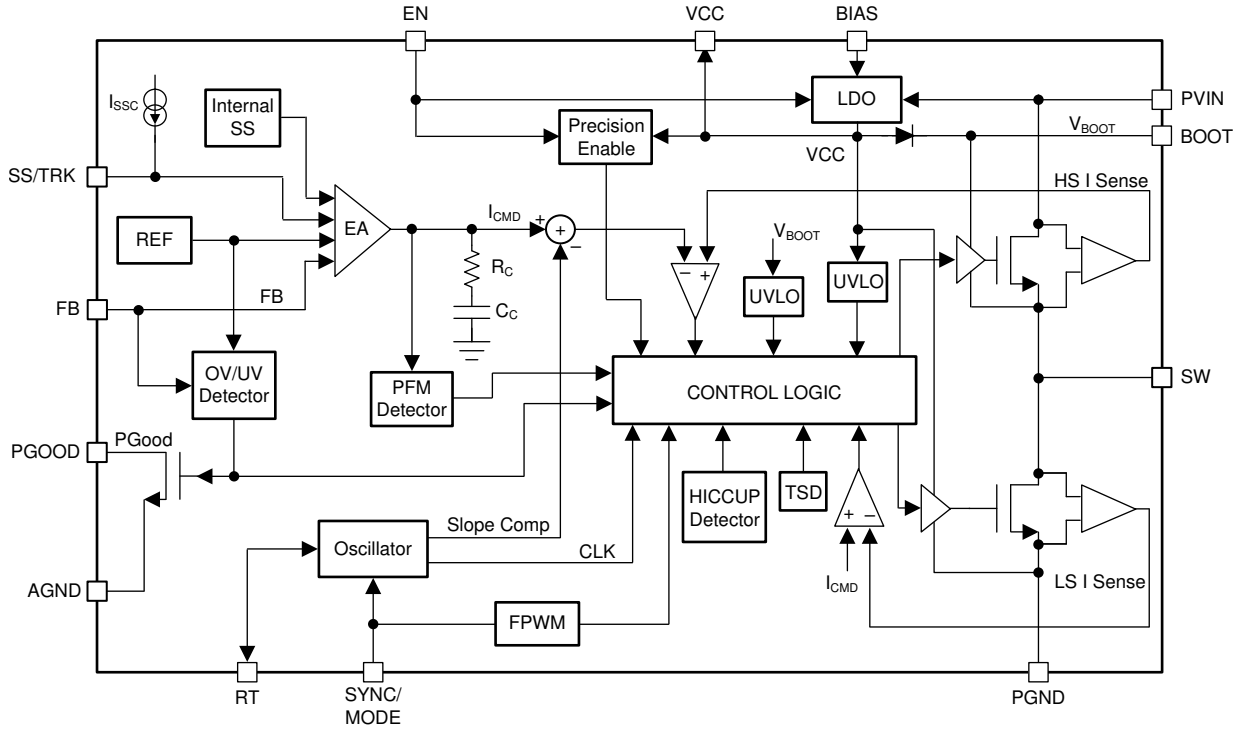

Figure 1-1. Functional Block Diagram

LM76005-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM76005-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	21
Die FIT Rate	11
Package FIT Rate	10

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1400 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM76005-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No OUTPUT (Output low)	30%
OUTPUT High (Following Input)	20%
OUTPUT not in specification	35%
Short circuit any two pins	5%
PGOOD – False Trip or Failure to Trip	5%
EN - False Enable or Failure to Enable	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM76005-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM76005-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM76005-Q1 data sheet.

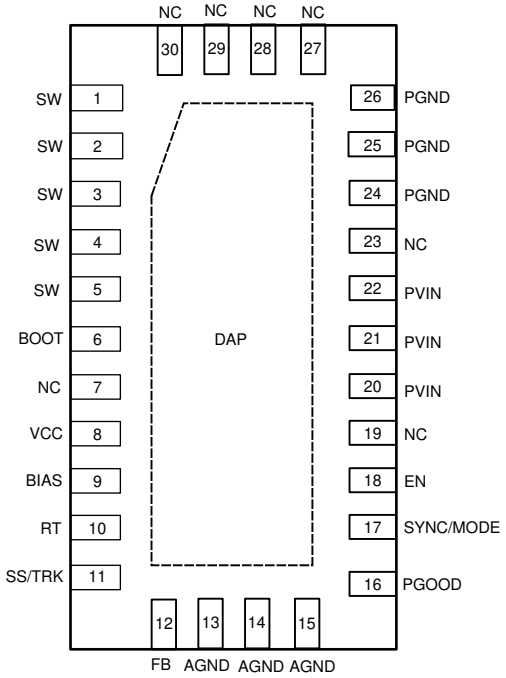

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the 'Recommended Operating Conditions' and the 'Absolute Maximum Ratings' found in the LM76005-Q1 data sheet.
- Configuration as shown in the 'Example Application Circuit' found in the LM76005-Q1 data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1, 2, 3, 4, 5	Damage to internal power FETs	A
BOOT	6	Damage to internal circuits	A
N/C	7	None functional pin, no connection	D
VCC	8	Fault mode will shut the device down.	B
BIAS	9	Normal operation	D
RT	10	Set to frequency much higher than 500 KHz and can cause damge to internal circuit.	B
SS/TRK	11	Set output to zero voltage.	B
FB	12	Shorting FB will cause no voltage regulation control.	B
AGND	13, 14, 15	Normal operation	D
PGOOD	16	PGOOD not valid signal, VOUT in regulation	D
SYNC/MODE	17	Shorted to GND is DCM/PFM operation	C
EN	18	Vout = 0 V	B
NC	19	None functional pin, no connection	D
PVIN	20, 21, 22	Device will not operate.	B
N/C	23	None functional pin, no connection	D
PGND	24, 25, 26	Normal operation	D
N/C	27, 28, 29, 30	None functional pin, no connection	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1, 2, 3, 4, 5	Loss of output voltage regulation	B
BOOT	6	Loss of output voltage regulation	B
N/C	7	None functional pin, no connection	D
VCC	8	VCC will be unstable and cause damage to internal circuits.	A
BIAS	9	Normal operation	D
RT	10	Set to default frequency 400 KHz.	C
SS/TRK	11	Use the 6.3-ms internal soft-start ramp.	D
FB	12	Floating FB will cause no voltage regulation control.	B
AGND	13, 14, 15	Can cause damage to internal circuits	A
PGOOD	16	PGOOD not valid signal, VOUT in regulation	D
SYNC/MODE	17	Floating this pin can cause unexpected operation mode.	B
EN	18	Device may not power up.	B
NC	19	None functional pin, no connection	D
PVIN	20, 21, 22	Device can become damaged if only one PVIN pin is connected to PCB board.	A
N/C	23	None functional pin, no connection	D
PGND	24, 25, 26	Device can become damaged if only one PGND pin is connected to PCB board.	A
N/C	27, 28, 29, 30	None functional pin, no connection	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1, 2, 3, 4	SW pin 1 to pin 5 are expected to be shorted.	D
SW	5	Loss of output voltage regulation, possible damage internal circuits	A
BOOT	6	Normal operation	D
N/C	7	None functional pin, no connection	D
VCC	8	VCC will be unstable if BIAS voltage is noisy or cause damage if BIAS >5.5 V.	A
BIAS	9	Switching frequency set to near 0 Hz or damage to internal circuits > 5 V	A
RT	10	Switching frequency set to near 0 Hz.	B
SS/TRK	11	Switching frequency set to near 0 Hz.	B
FB	12	Shorting FB will cause no voltage regulation control.	B
AGND	13	Shorting FB will cause no voltage regulation control.	B
AGND	14, 15	Normal operation	D
PGOOD	16	Can cause damage to internal circuits	A
SYNC/MODE	17	If voltage exceeds 5.5 V, damage to internal circuits will happen.	A
EN	18	Normal operation	D
NC	19	None functional pin, no connection	D
PVIN	20, 21, 22	No impact	D
N/C	23	None functional pin, no connection	D
PGND	24, 25, 26	Device is operational.	D
N/C	27, 28, 29, 30	None functional pin, no connection	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SW	1, 2, 3, 4, 5	Damage to LS FET	A
BOOT	6	Damage to internal circuits	A
N/C	7	None functional pin, no connection	D
VCC	8	Damage if voltage exceeds 5.5 V	A
BIAS	9	Damage to internal circuits if voltage exceeds 30 V	A
RT	10	If voltage exceeds 5.5 V, damage to internal circuits will happen.	A
SS/TRK	11	If voltage exceeds 5 V, damage to internal circuits will happen.	A
FB	12	If voltage exceeds 5 V, damage to internal circuits will happen.	A
AGND	13, 14, 15	Can cause damage to internal circuits	A
PGOOD	16	Can cause damage to internal circuits if voltage exceeds 20 V	A
SYNC/MODE	17	If voltage exceeds 5.5 V, damage to internal circuits will happen.	A
EN	18	EN pin can handle ≤ 60 V. Greater than 60 V can cause damage to internal circuits.	D
NC	19	None functional pin, no connection	D
PVIN	20, 21, 22	Normal operation	D
N/C	23	None functional pin, no connection	D
PGND	24, 25, 26	Can cause damage to internal circuits or package	A
N/C	27, 28, 29, 30	None functional pin, no connection	D

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