# LM26420-Q1 Functional Safety FIT Rate, FMD and Pin FMA
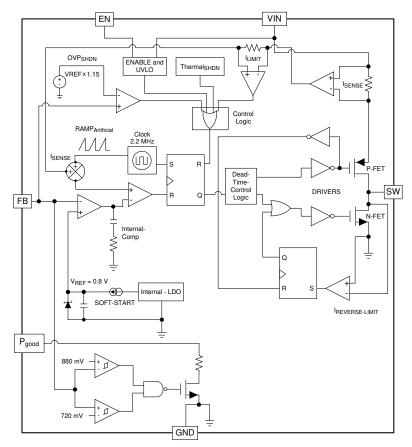
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## 1 Overview

This document contains information for LM26420-Q1 (HTSSOP and WQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

**Figure 1. Functional Block Diagram**

LM26420-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2   Functional Safety Failure In Time (FIT) Rates

### 2.1   HTSSOP Package

This section provides Functional Safety Failure In Time (FIT) rates for the HTSSOP package of LM26420-Q1 based on an industry-wide used reliability standard:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

**Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 16 |
| Die FIT Rate | 4 |
| Package FIT Rate | 12 |

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: automotive control from Table 11
- Power dissipation: 750 mW
- Climate type: world-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

## 2.2 WQFN Package

This section provides Functional Safety Failure In Time (FIT) rates for the WQFN package of LM26420-Q1 based on an industry-wide used reliability standard:

- Table 2 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

**Table 2. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 15 |
| Die FIT Rate | 4 |
| Package FIT Rate | 11 |

The failure rate and mission profile information in Table 2 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: automotive control from Table 11
- Power dissipation: 750 mW
- Climate type: world-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

## 3    Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM26420-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| SW1/2 no output | 45% |
| SW1/2 output not in specification – voltage or timing | 40% |
| SW1/2 power FET stuck on | 5% |
| PG1/2 false trip, fails to trip | 5% |
| Short circuit any two pins | 5% |

# 4    Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM26420-Q1 (HTSSOP and WQFN package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5 and Table 9)
- Pin open-circuited (see Table 6 and Table 10)
- Pin short-circuited to an adjacent pin (see Table 7 and Table 11)
- Pin short-circuited to supply (see Table 8 and Table 12)

Table 5 through Table 12 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

**Table 4. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assumption the device is running in the typical application. Please refer to the 'Typical Application Circuit' on the 1st page in the datasheet.

## 4.1    HTSSOP Package

Figure 2 shows the LM26420-Q1 pin diagram for the HTSSOP package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the LM26420-Q1 datasheet.
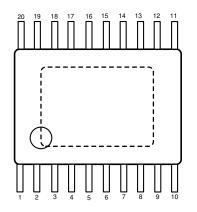


**Figure 2. Pin Diagram (HTSSOP Package)**

**Table 5. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VINC | 1 | Device does not power up | B |
| EN1 | 2 | Intended functionality if the converter 1 is shutdown | D |
| VIND1 | 3 | Device does not power up | B |
| VIND1 | 4 | Device does not power up | B |
| SW1 | 5 | Potential device damage | A |

**Table 5. Pin FMA for Device Pins Short-Circuited to Ground (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|----------|---------|--------------------------------------------|----------------------|
| PGND1 | 6 | No effect | D |
| PGND1 | 7 | No effect | D |
| FB1 | 8 | Output voltage regulated to VIN (100% mode). | B |
| PG1 | 9 | Intended functionality if PG1 is not used | D |
| DAP | 10 | No effect | D |
| DAP | 11 | No effect | D |
| PG2 | 12 | Intended functionality if PG2 is not used | D |
| FB2 | 13 | Output voltage regulated to VIN (100% mode). | B |
| PGND2 | 14 | No effect | D |
| PGND2 | 15 | No effect | D |
| SW2 | 16 | Potential device damage | A |
| VIND2 | 17 | Device does not power up | B |
| VIND2 | 18 | Device does not power up | B |
| EN2 | 19 | Intended functionality if the converter 2 is shutdown | D |
| AGND | 20 | No effect | D |
| DAP | - | No effect | D |

**Table 6. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|----------|---------|--------------------------------------------|----------------------|
| VINC | 1 | Device not functional | B |
| EN1 | 2 | Undetermined device status, device may not power up | B |
| VIND1 | 3 | Device does not power up. | B |
| VIND1 | 4 | Device does not power up. | B |
| SW1 | 5 | Converter 1 not functional, open loop operation | B |
| PGND1 | 6 | Device not functional | B |
| PGND1 | 7 | Device not functional | B |
| FB1 | 8 | Undetermined converter 1 output voltage | B |
| PG1 | 9 | Intended functionality if PG1 is not used | D |
| DAP | 10 | Functional but impact on thermal behavior / reliability | C |
| DAP | 11 | Functional but impact on thermal behavior / reliability | C |
| PG2 | 12 | Intended functionality if PG2 is not used | D |
| FB2 | 13 | Undetermined converter 2 output voltage | B |
| PGND2 | 14 | Device not functional | B |
| PGND2 | 15 | Device not functional | B |
| SW2 | 16 | Converter 2 not functional, open loop operation | B |
| VIND2 | 17 | Device does not power up. | B |
| VIND2 | 18 | Device does not power up. | B |
| EN2 | 19 | Undetermined device status, device may not power up | B |
| AGND | 20 | Device not functional | B |
| DAP | - | Functional but impact on thermal behavior / reliability | C |

## Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

| Pin Name | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VINC | EN1 | Intended functionality | D |
| EN1 | VIND1 | Intended functionality | D |
| VIND1 | VIND1 | Redundant pin | D |
| VIND1 | SW1 | Potential device damage | A |
| SW1 | PGND1 | Potential device damage | A |
| PGND1 | PGND1 | Redundant pin | D |
| PGND1 | FB1 | Output voltage regulated to VIN (100% mode). | B |
| FB1 | PG1 | Potential device damage | A |
| PG1 | DAP | Intended functionality if PG1 is not used | D |
| DAP | PG2 | Intended functionality if PG2 is not used | D |
| PG2 | FB2 | Potential device damage | A |
| FB2 | PGND2 | Output voltage regulated to VIN (100% mode). | B |
| PGND2 | PGND2 | Redundant pin | D |
| PGND2 | SW2 | Potential device damage | A |
| SW2 | VIND2 | Potential device damage | A |
| VIND2 | VIND2 | Redundant pin | D |
| VIND2 | EN2 | Intended functionality | D |
| EN2 | AGND | Intended functionality if the converter 2 is shutdown | D |

## Table 8. Pin FMA for Device Pins Short-Circuited to supply

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VINC | 1 | Intended functionality | D |
| EN1 | 2 | Intended functionality | D |
| VIND1 | 3 | Intended functionality | D |
| VIND1 | 4 | Intended functionality | D |
| SW1 | 5 | Potential device damage | A |
| PGND1 | 6 | Device does not power up | B |
| PGND1 | 7 | Device does not power up | B |
| FB1 | 8 | Potential device damage | A |
| PG1 | 9 | PG doesn't indicate the status | B |
| DAP | 10 | Device does not power up | B |
| DAP | 11 | Device does not power up | B |
| PG2 | 12 | PG doesn't indicate the status | B |
| FB2 | 13 | Potential device damage | A |
| PGND2 | 14 | Device does not power up | B |
| PGND2 | 15 | Device does not power up | B |
| SW2 | 16 | Potential device damage | A |
| VIND2 | 17 | Intended functionality | D |
| VIND2 | 18 | Intended functionality | D |
| EN2 | 19 | Intended functionality | D |
| AGND | 20 | Device does not power up | B |
| DAP | - | Device does not power up | B |

## 4.2 WQFN Package

Figure 3 shows the LM26420-Q1 pin diagram for the WQFN package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the LM26420-Q1 datasheet.
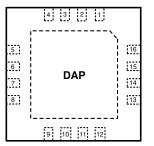


**Figure 3. Pin Diagram (WQFN Package)**

**Table 9. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VIND1 | 1 | Device does not power up | B |
| VIND1 | 2 | Device does not power up | B |
| SW1 | 3 | Potential device damage | A |
| PGND1 | 4 | No effect | D |
| FB1 | 5 | Output voltage regulated to VIN (100% mode) | B |
| PG1 | 6 | Intended functionality if PG1 is not used | D |
| PG2 | 7 | Intended functionality if PG2 is not used | D |
| FB2 | 8 | Output voltage regulated to VIN (100% mode). | B |
| PGND2 | 9 | No effect | D |
| SW2 | 10 | Potential device damage | A |
| VIND2 | 11 | Device does not power up | B |
| VIND2 | 12 | Device does not power up | B |
| EN2 | 13 | Intended functionality if the converter 2 is shutdown | D |
| AGND | 14 | No effect | D |
| VINC | 15 | Device does not power up | B |
| EN1 | 16 | Intended functionality if the converter 1 is shutdown | D |
| DAP | - | No effect | D |

**Table 10. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VIND1 | 1 | Device does not power up. | B |
| VIND1 | 2 | Device does not power up. | B |
| SW1 | 3 | Converter 1 not functional, open loop operation | B |
| PGND1 | 4 | Device not functional | B |
| FB1 | 5 | Undetermined converter 1 output voltage | B |
| PG1 | 6 | Intended functionality if PG1 is not used | D |
| PG2 | 7 | Intended functionality if PG2 is not used | D |
| FB2 | 8 | Undetermined converter 2 output voltage | B |
| PGND2 | 9 | Device not functional | B |
| SW2 | 10 | Converter 2 not functional, open loop operation | B |

**Table 10. Pin FMA for Device Pins Open-Circuited (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VIND2 | 11 | Device does not power up. | B |
| VIND2 | 12 | Device does not power up. | B |
| EN2 | 13 | Undetermined device status, device may not power up | B |
| AGND | 14 | Device not functional | B |
| VINC | 15 | Device not functional | B |
| EN1 | 16 | Undetermined device status, device may not power up | B |
| DAP | - | Functional but impact on thermal behavior / reliability | C |

**Table 11. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VIND1 | VIND1 | Redundant pin | D |
| VIND1 | SW1 | Potential device damage | A |
| SW1 | PGND1 | Potential device damage | A |
| FB1 | PG1 | Potential device damage | A |
| PG1 | PG2 | PG output may be wrong | C |
| PG2 | FB2 | Potential device damage | A |
| PGND2 | SW2 | Potential device damage | A |
| SW2 | VIND2 | Potential device damage | A |
| VIND2 | VIND2 | Redundant pin | D |
| EN2 | AGND | Intended functionality if the converter 2 is shutdown | D |
| AGND | VINC | Device will not power up | B |
| VINC | EN1 | Intended functionality | D |

**Table 12. Pin FMA for Device Pins Short-Circuited to supply**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| VIND1 | 1 | Intended functionality | D |
| VIND1 | 2 | Intended functionality | D |
| SW1 | 3 | Potential device damage | A |
| PGND1 | 4 | Device will not power up | B |
| FB1 | 5 | Potential device damage | A |
| PG1 | 6 | PG doesn't indicate the status | B |
| PG2 | 7 | PG doesn't indicate the status | B |
| FB2 | 8 | Potential device damage | A |
| PGND2 | 9 | Device will not power up | B |
| SW2 | 10 | Potential device damage | A |
| VIND2 | 11 | Intended functionality | D |
| VIND2 | 12 | Intended functionality | D |
| EN2 | 13 | Intended functionality | D |
| AGND | 14 | Device will not power up | B |
| VINC | 15 | Intended functionality | D |
| EN1 | 16 | Intended functionality | D |
| DAP | - | Device will not power up | B |

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