LM833

AN-1002 ADC16071/ADC16471 Analog Layout and Interface Design Considerations

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ADC16071/ADC16471 Analog Layout and Interface Design Considerations

National Semiconductor
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INTRODUCTION

The ADC16071 and the ADC16471 are 16-bit oversampling delta-sigma ($\Delta\Sigma$) analog to digital converters that are capable of delivering high performance signal conversions at data output rates up to 192 kSps (kilo samples per second). The ADC16071/ADC16471's ultimate performance is dependent on the analog interface, the digital interface, and the printed circuit board on which it is placed. While the board design and layout can sometimes be taken for granted in lower resolution ADC applications, it is critical in obtaining best performance from high-resolution ADCs. Extracting all of the performance that the ADC16071/ADC16471 is capable of delivering requires special attention to such areas as board layout, ground planes, power supply bypassing, power supply routing, socketing, clock generation, signal routing, and analog signal conditioning.

ANALOG INPUT RANGE

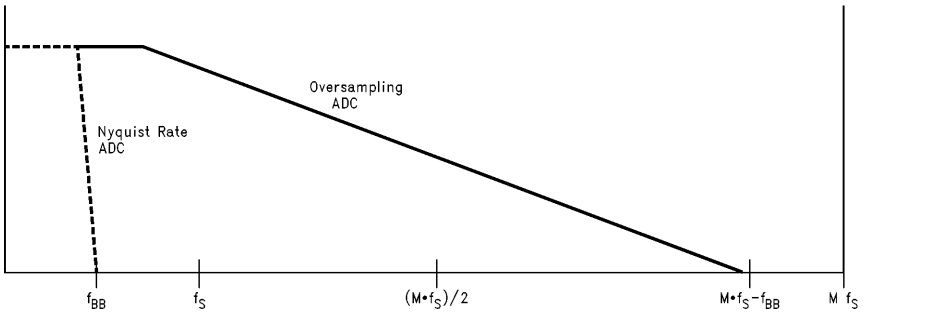
The ADC16071/ADC16471 produces a 16-bit, twos compliment output according to the following equation:

$$\text{output} = \frac{32768 \bullet (V_{IN+} - V_{IN-})}{(V_{REF+} - V_{REF-})}$$

The signals applied to V_{IN+} and V_{IN-} must have potentials between the analog supply (V_{A+}) and analog ground (AGND). For accurate conversions, the absolute difference between V_{IN+} and V_{IN-} should be less than the difference between V_{REF+} and V_{REF-}. Best harmonic performance will result when a balanced voltage is applied to V_{IN+} and V_{IN-} that has a common mode voltage at or below V_{MID}, where V_{MID} is an output pin on the ADC16071/ADC16471 with a potential equal to one half of the analog supply ($V_A{}^+/2$). The ADC16471 has an internal 2.5V bandgap reference that sets $V_{REF+} = V_{MID} + 1.25V$ and $V_{REF-} = V_{MID} - 1.25V$. The ADC16071 requires an externally applied reference whose range ($V_{REF+} - V_{REF-}$) can be varied from 1V to V_{A+}. See *Reference Voltage Generation for the ADC16071* for examples of driving the ADC16071's reference inputs.

ANTI-ALIASING FILTER CONSIDERATIONS

One of the biggest advantages of oversampling $\Delta\Sigma$ ADCs is their relaxed requirements for anti-aliasing filters. With any ADC, aliasing will not occur provided that no frequencies greater than one half the sampling rate are present at the analog input pins. To prevent aliasing and maximize bandwidth with a Nyquist rate (non-oversampling) ADC, the analog anti-aliasing filter typically must have a flat response up to about $0.45 \bullet f_S$ and attenuate all frequencies above $0.5 \bullet f_S$ to levels below the noise floor. Designing a filter with such a sharp drop-off can be difficult and expensive, requiring precision components and additional board space. Furthermore, analog "brick wall" filters usually have a non-linear phase response. If phase distortion is a concern, the implementation of such a filter can be even more difficult, if not impossible. *Figure 1* compares the anti-aliasing filter requirements for a Nyquist rate ADC to those of an oversampling ADC such as the ADC16071/ADC16471.



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M = Oversampling Ratio
f_S = Output Data Rate
f_{BB} = Desired Frequency (Base Band)

FIGURE 1. AAF Requirements for Nyquist Rate ADC vs Oversampling ADC

The ADC164071/ADC16471's modulator samples the analog input at a rate equal to $f_{CLK}/2$, where f_{CLK} is the frequency of the clock applied to the ADC16071/ADC16471's CLK pin. The output data rate (f_S) is equal to 1/64 (the oversampling ratio) of the modulator's sample rate, or $f_{CLK}/128$. The analog baseband (f_{BB}) is equal to one half of the data output rate, or $f_{CLK}/256$.

By oversampling the analog input at 64 times the Nyquist rate (f_S) for the desired analog baseband, the ADC16071/ADC16471 pushes out the point at which aliasing occurs. This dramatically relaxes the performance requirements for the anti-aliasing filter. The critical point of attenuation for an oversampling ADC's anti-aliasing filter is typically pushed out even further because of on-chip digital filtering. The ADC16071/ADC16471 contains a 246 tap internal, linear phase, finite impulse response (FIR) filter that cuts off all frequencies above the analog baseband (f_{BB}).

Aliased frequencies are mirrored about half the sampling rate of the modulator, $(M \bullet f_S)/2$. Therefore, any frequencies between $(M \bullet f_S)/2$ and $M \bullet f_S$ are aliased into the range between $(M \bullet f_S)/2$ and DC. Since all frequencies greater than the baseband (f_{BB}) are filtered out by the on-chip digital filters, the only potentially damaging frequencies are those above $M \bullet f_S - f_{BB}$, which are aliased into the baseband. Thus the external anti-aliasing filter for the ADC16071/ADC16471 need only cut off frequencies above $M \bullet f_S - f_{BB}$. The ADC16071/ADC16471 has an oversampling ratio of 64 ($M = 64$). This ratio allows the ADC16071/ADC16471's anti-aliasing filter's critical point of attenuation to be pushed out 127 times ($63.5 \bullet f_S$ vs $0.5 \bullet f_S$) higher than what it would need to be for a Nyquist rate converter with equivalent output bandwidth!

PASSIVE RC ANTI-ALIASING FILTER NETWORK

A recommended, simple anti-aliasing input network is the first-order, passive, low-pass RC filter shown in *Figure 2.* This network has a flat frequency and linear phase response in the analog baseband, and eliminates analog frequency components above $M \bullet f_S - f_{BB}$ that may cause aliasing. In addition, C_1, C_2, and C_3 provide a charge reservoir for the ADC16071/ADC16471 modulator's input capacitors (see *Analog Interface Amplifier Considerations*). The filter's −3 dB cutoff frequency is:

$$f_c = \frac{1}{6\pi RC}$$

where $R = R_1 = R_2$ and $C = C_1 = C_2 = C_3$

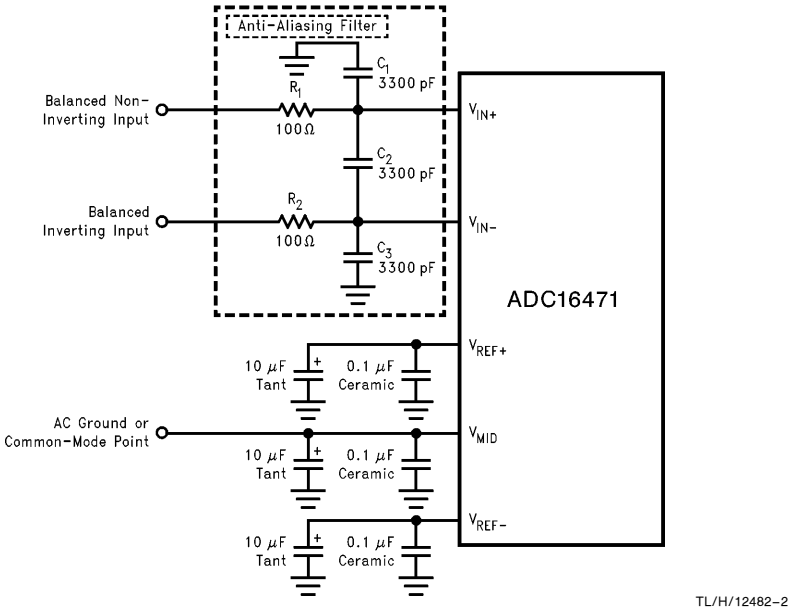

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FIGURE 2. Simple, Passive, Low-Pass Input Network

To ensure that the filter's frequency response is flat in the baseband and that it provides sufficient attenuation to frequencies above $M \bullet f_S - f_{BB}$, the values of R and C should be chosen so that the filter's 3 dB cutoff is between $f_{CLK}/250$ and $f_{CLK}/100$. With an f_{CLK} of 24.576 MHz (192 kHz data output rate), typical values for R and C are 100Ω and 3300 pF, respectively. These values result in a 3 dB cutoff equal to approximately 160 kHz, or $f_{CLK}/150$ and an attenuation of about 40 dB at $M \bullet f_S - f_{BB}$.

LEVEL SHIFTING THE INPUT SIGNAL

For best conversion performance, the signal applied to the ADC16071/ADC16471's analog input pins, V_{IN+} and V_{IN-}, should be a balanced AC signal with a common mode voltage at or below one-half of the ADC's supply voltage (V_{MID}). The simplest way to do this is to capacitively couple the applied input signal and connect the V_{MID} output to V_{IN+} and V_{IN-} through 4.7 kΩ resistors *(Figure 3)*.

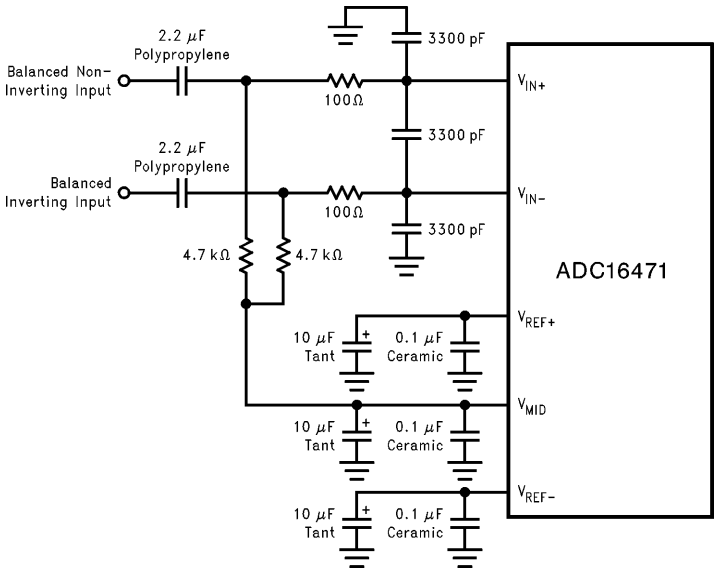

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FIGURE 3. Capacitively Coupling and Level Shifting a Balanced Input Signal

RELATION BETWEEN CAPACITOR DIELECTRIC AND SIGNAL DISTORTION.

For any capacitors connected to the ADC16071/ADC16471's analog inputs, the dielectric plays an important role in determining the amount of distortion generated in the input signal. The dielectric must have low dielectric absorption. This requirement is fulfilled by using capacitors that have film dielectrics. Of these, polypropylene and polystyrene are the best. These are followed by polycarbonate and mylar. If ceramic capacitors are chosen, use only capacitors with NPO dielectrics.

INPUT SIGNAL MAGNITUDE AND OVERLOAD

Following the switched capacitor input of the ADC16071/ADC16471, the analog input and reference voltages are fed into a pseudo fourth order, MASH (Multistage noise Shaping) delta sigma modulator. The modulator is designed to act as a high-pass filter to the quantization noise introduced by its comparators. This high-pass noise shaping characteristic minimizes the amount of quantization noise present in the baseband at the output of the modulator. The higher frequency quantization noise that is present at the output of the modulator is filtered by the internal, brick wall FIR. See Appendix: *Noise Shaping in Delta Sigma Modulators* for further discussion.

Due to overload in the modulator's comparators, as the analog input amplitude approaches full scale, the modulator's feedback coefficients begin to change. This tends to reduce the cutoff frequency of the modulator's noise shaping characteristic, allowing more quantization noise to pass in the analog baseband. Since anything passed in the analog baseband won't be filtered by the FIR, added quantization noise will be present in the output of the ADC16071/ADC16471. When examining an output spectrum from the ADC16071/ADC16471, this additional quantization noise can be seen as a slight raising of the noise floor toward the upper end of the analog baseband and increased odd harmonic distortion. *Figures 4* and *5* show output spectra from the same ADC16071 with input amplitudes of −3 dB and −0.8 dB below full scale (dBFS), respectively. The raised noise floor and additional odd harmonic distortion are visually noticeable with a −0.8 dB input.

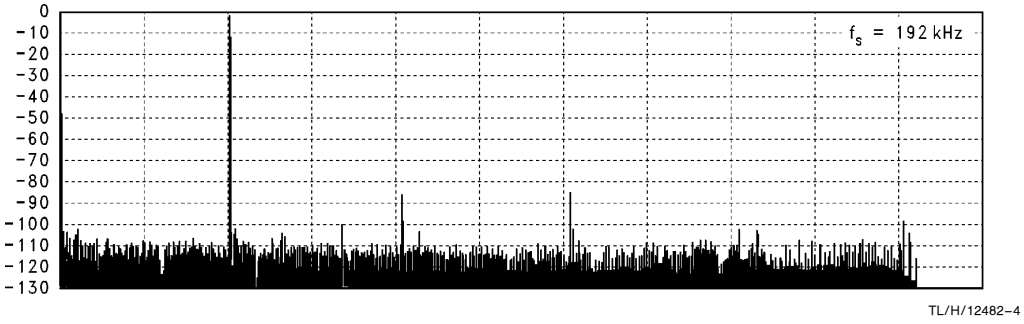

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FIGURE 4. Output Spectrum with a −3 dB Input Amplitude

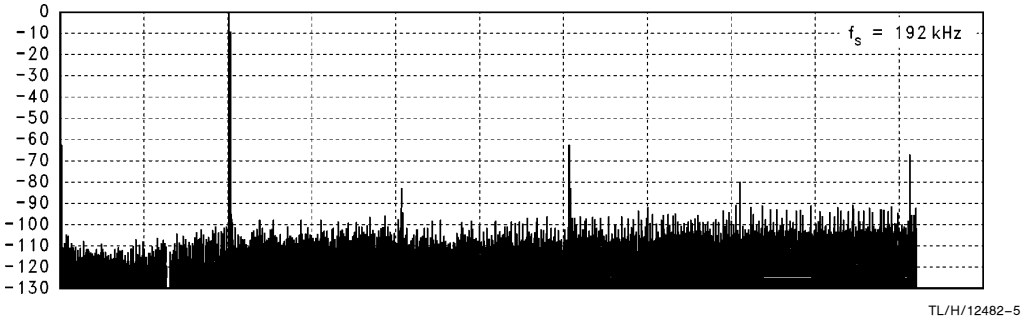

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FIGURE 5. Output Spectrum with a −0.8 dB Input Amplitude

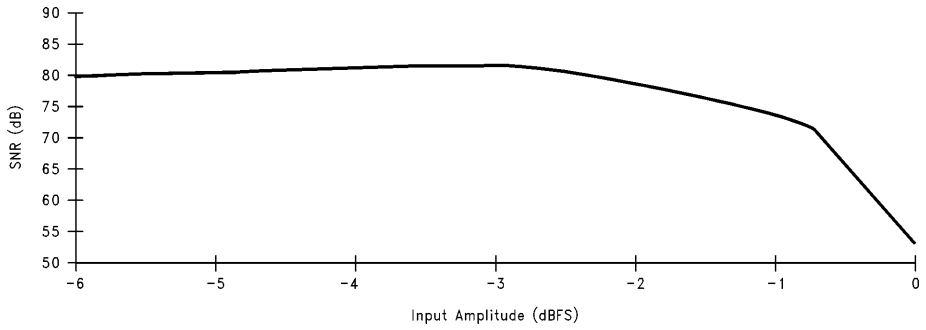

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FIGURE 6. Dynamic Performance Degradation Due to Modulator Overload

At room temperature, the ADC16071/ADC16471 performs well (meets its published specifications) with input amplitudes up to −3 dB FS. As the input amplitude exceeds −3 dB FS, performance begins to degrade. At −2 dB FS, the SNR is about 2 dB worse than with a −3 dB FS input. With a −1.4 dB FS input, the SNR is about 6 dB worse. With a −0.66 dB FS input, the SNR drops by more than 10 dB from the −3 dB FS input case. *Figure 6* illustrates the typical degradation in the dynamic performance of the ADC16071/ADC16471 as the input amplitude approaches full scale. At higher temperatures, the nonlinearities may be a factor at slightly lower input amplitudes, but overload noise and distortion shouldn't be experienced over the entire −40°C to +85°C temperature range with input amplitudes of −6 dB FS or less.

ANALOG INTERFACE AMPLIFIER CONSIDERATIONS

The input impedance of the ADC16071/ADC16471, due to the effective resistance of the switched capacitor input, varies as follows:

$$Z_{IN} = \frac{10^{12}}{2.35 \bullet (f_{CLK}/2)}$$

where f_{CLK} is the frequency of the clock applied to the ADC16071/ADC16471's CLK pin.

The current required during the act of switching, or connecting, the input sampling capacitors between the source circuitry and the ADC16071/ADC16471's modulator input can cause momentary instability in amplifiers with limited gain-bandwidth. To overcome this problem, amplifiers used to drive the inputs of the ADC16071/ADC16471 must be able to recover quickly from the transient current requirements of the switched capacitor input. The capacitors used in the recommended anti-aliasing filter configuration *(Figure 2)* help by acting as charge reservoirs for these current spikes, but it is still recommended that amplifiers be used that have a minimum gain bandwidth of one half the frequency of the clock. For example, when the clock frequency is 24.576 MHz, the gain-bandwidth of any op-amps driving the inputs of the ADC16071/ADC16471 should be at least 13 MHz. The LM6218 and the LM833 are good choices for buffering or amplifying signals applied to the ADC16071/ADC16471. These amplifiers have sufficient bandwidth and slew rate and produce sufficiently low distortion and noise. Additionally, they are available in a dual package, saving board space and component count.

To help source amplifiers settle faster, a series resistance (50Ω to 100Ω) may be placed between the amplifier's output and the ADC16071/ADC16471's inputs. This is already accomplished when the passive low-pass network as shown in *Figure 2* is connected between the amplifier's output and the ADC16071/ADC16471's inputs.

SINGLE-ENDED BIPOLAR INPUT TO BALANCED UNIPOLAR OUTPUT BUFFER

The ADC16071/ADC16471 exhibits the best distortion performance when a balanced AC signal is applied to its analog inputs that has a common mode offset at or below V_{MID}. The circuit in *Figure 7* can be used to convert a single-ended, bipolar signal centered about ground to a balanced signal centered about V_{MID}.

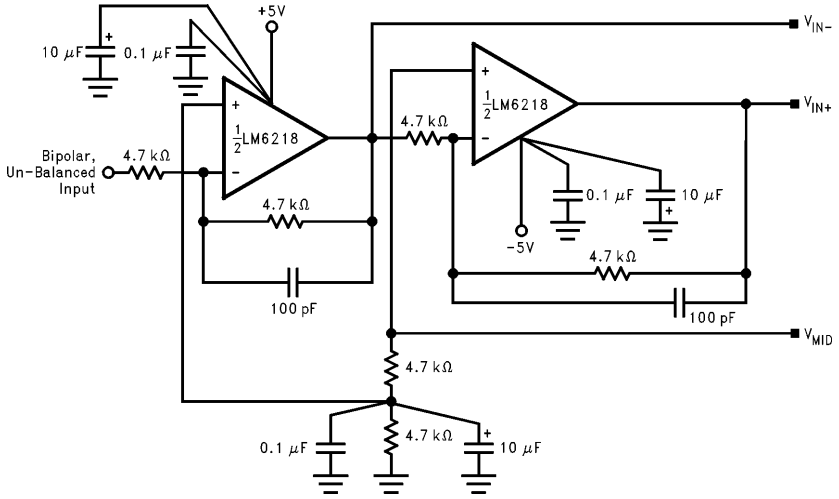

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FIGURE 7. Unbalanced-to-Balanced Buffer

This circuit's level shifting is accomplished using the ADC16071/ADC16471's on-chip one-half supply voltage output, V_{MID}. The V_{MID} output voltage is divided in half and applied to the non-inverting input of the circuit's first inverting buffer. V_{MID} is divided in half because the difference between the DC offset at the input to the circuit (0V) and the voltage at the non-inverting input of the first buffer ($V_{MID}/2$) will see a gain of two. This results in an offset voltage equal to V_{MID} at the output of the first inverting buffer. V_{MID} is also applied to the non-inverting input of the circuit's second inverting buffer. The outputs are two 180° out-of-phase signals (V_{IN+} and V_{IN-}) that swing above and below the V_{MID} voltage.

It is important to note that because of the difference in potential between the inverting input of the first buffer and the common mode output of the signal source, the signal source will have to sink an average of about 270 μA and up to a peak of about 540 μA. An alternate approach is to connect a coupling capacitor between the output of the signal source and the input to the circuit in *Figure 7.*

When the ADC16071/ADC16471 is driven by a balanced signal, the conversion process will cancel out common mode noise and reduce harmonic distortion. *Figure 8* shows an output spectrum from an ADC16071 with a single-ended input signal centered around V_{MID}. *Figure 9* shows the output spectrum from the same ADC16071 with same signal source (without the V_{MID} offset) after it has been converted to a balanced signal using the circuit in *Figure 7.* The distortion performance (THD) improves by more than 25 dB when the input is converted to a balanced signal.

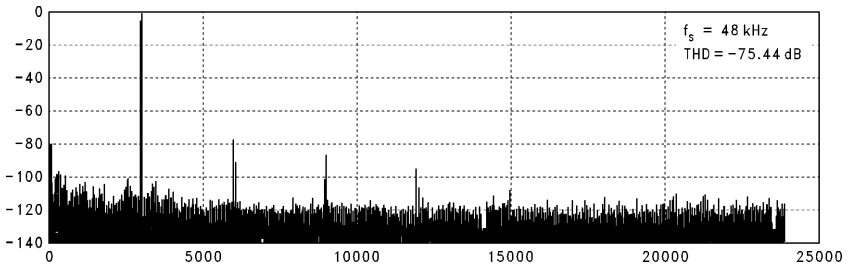

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FIGURE 8. Output Spectrum with Single-Ended Input

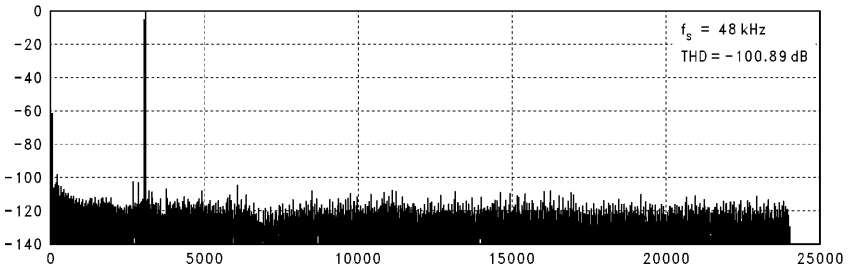

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FIGURE 9. Output Spectrum with Balanced Input

BALANCED BIPOLAR INPUT TO BALANCED UNIPOLAR OUTPUT BUFFER

The circuit shown in *Figure 10* simply buffers and level shifts a balanced analog signal centered about ground. The ADC16071/ADC16471's V_{MID} output voltage is divided in half and applied to the non-inverting inputs of each of the inverting buffers. To maintain the input signal's original phase, the positive inverting buffer's output is applied to V_{IN-} and the negative inverting buffer output is applied to V_{IN+}.

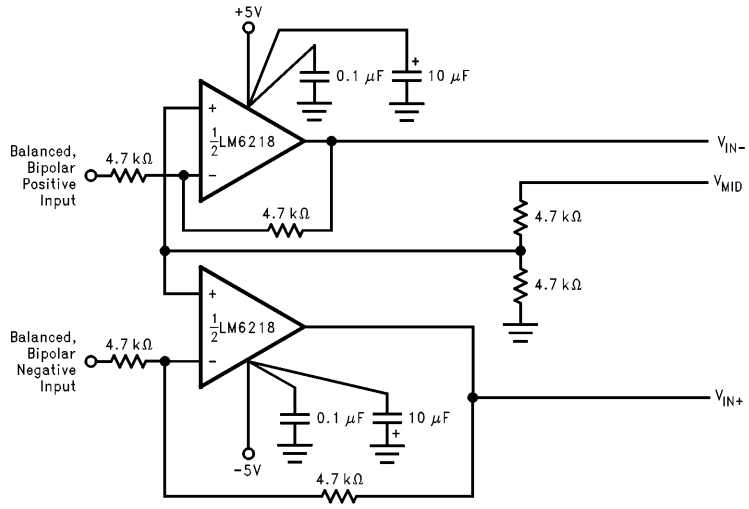

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FIGURE 10. Balanced Bipolar to Unipolar Buffer

REFERENCE VOLTAGE GENERATION FOR THE ADC16071

The ADC16071 requires an external reference voltage source. It must have low output noise and be stable. A suggested circuit that generates a stable reference voltage that can be adjusted between 1.9V and 2.6V is shown in *Figure 11.* It uses the LM4041-ADJ adjustable shunt bandgap reference. The potentiometer, R_P, adjusts the output between 1.9V and 2.6V. If a fixed output is desired, replace the R_1, R_P, and R_2 resistor string with the fixed resistor string shown in *Figure 12.* Use the equation in *Figure 12* to determine the fixed resistor values.

POWER SUPPLY VOLTAGES FOR IMPROVED PERFORMANCE

While adequate performance will be achieved by operating the ADC16071/ADC16471 with +5V connected to V_{A+}, V_{M+} and V_{D+}, dynamic performance, as indicated by SINAD, can be further enhanced by changing V_{D+} to a voltage lower than V_{A+} and V_{M+}. By setting V_{D+} to 3.5V and V_{A+} and V_{M+} to 5.5V, improvements of up to 5 dB will be seen in both noise floor and harmonic performance. The improved performance can be attributed to the reduction of digital switching noise due to the lower digital supply voltage.

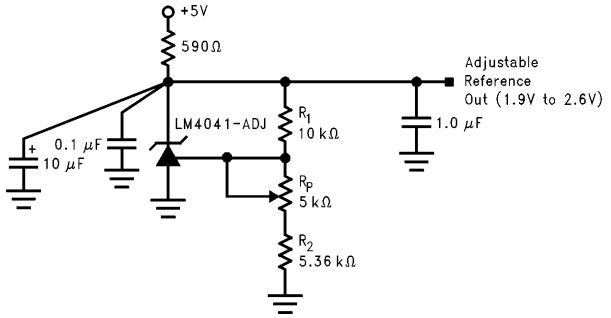

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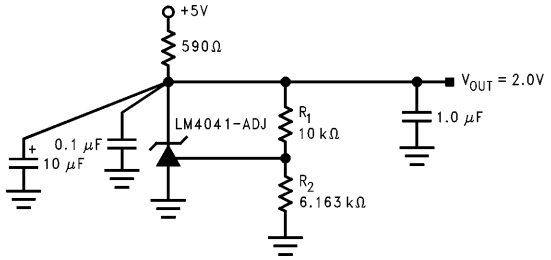
FIGURE 11. 1.9V to 2.6V Adjustable Reference for the ADC16071



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From the LM4041-ADJ datasheet:

$$\frac{R2}{R1} = \frac{V_{OUT}}{1.24 - (1.3 \times 10^{-3})\, V_{OUT}} - 1$$

FIGURE 12. 2.0V Fixed Reference for the ADC16071

PRINTED CIRCUIT BOARD CONSIDERATIONS

Ground Planes and Signal Trace Layers

Analog and digital ground planes are essential in extracting the best performance from high-resolution delta-sigma converters. Ground planes reduce ground return impedances to low levels, ensuring that power supply bypass capacitors have the lowest AC-resistance path possible. The ADC16071/ADC16471's conversion performance is optimized using separate analog and digital ground planes. The ground planes should be connected together at a single point, the power supply ground connection.

Best performance is achieved by ensuring that the trace/ground plane association integrity is maintained. All analog and digital traces are placed over, or within, their associated ground plane.

In a multilayer printed circuit board with separate ground and trace layers, the supply and signal trace layers should be ''sandwiched'' between the analog and digital ground plane layers *(Figure 13).* The outer ground plane layers act as shields, attenuating noise from external sources and from internal digital switching.

Analog signal, digital control signal, and power supply traces should be separated from each other. If the physical board layout prevents adequate separation of the digital, analog, and power supply traces, they should be placed on different circuit board layers and cross at right angles.

INPUT NETWORK LAYOUT AND ROUTING

Careful consideration must be observed concerning the layout and placement of the input network connected to the two balanced inputs, V_{IN+} and V_{IN-}. The layout should be balanced and symmetrical with respect to the V_{IN+} and V_{IN-} pins. All associated traces should have equal trace length and width dimensions. This symmetry should be extended back to the outputs of circuitry that drives V_{IN+} and V_{IN-}.

CLOCK SIGNAL GENERATION AND ROUTING

The ADC16071/ADC16471 requires a low jitter clock signal applied to its CLK pin that is free of ringing (over/undershoot of no more than 100 mV_{PP}) and has rise and fall times in the range of 3 ns–10 ns (10%–90%). The Ecliptek (EC1100 series) and SaRonix (NCH060 and NCH080 series) are recommended crystal clock oscillators for driving the CLK input of the ADC16071/ADC16471. Both of these families use HCMOS logic circuitry for fast rise and fall times.

Overshoot and ringing on the clock-signal edge that a converter uses to internally clock its operation will result in increased noise and distortion. The effects of overshoot and ringing can be minimized by using a series damping resistor between the output of the clock-signal source and the ADC16071/ADC16471's CLK pin. The value of the resistor used is dependent on the board layout, and usually ranges from 25Ω to 150Ω. A typical starting value is 50Ω.

SOCKET CONSIDERATIONS FOR IMPROVED POWER SUPPLY BYPASSING

The ADC16071/ADC16471 is clocked at very high frequencies. This high frequency clocking produces high frequency current spikes and glitches on the power supply lines. If not attenuated, these power supply perturbations will degrade the ADC16071/ADC16471's conversion performance.

For all integrated circuits, the power supply inputs should always be viewed as signal inputs. The internal circuit will treat any AC signal appearing on the power supply voltage as another input signal.

The ADC16071/ADC16471's power supply rejection (PSR) is high at low frequencies and usually decreases as frequency increases. Thus, at the high frequencies used to clock the ADC16071/ADC16471, the PSR is low. Therefore, external power supply bypass capacitors are needed to provide the ADC16071/ADC16471's transient current requirements and to improve the PSR by attenuating the high frequency noise created by high speed digital switching.

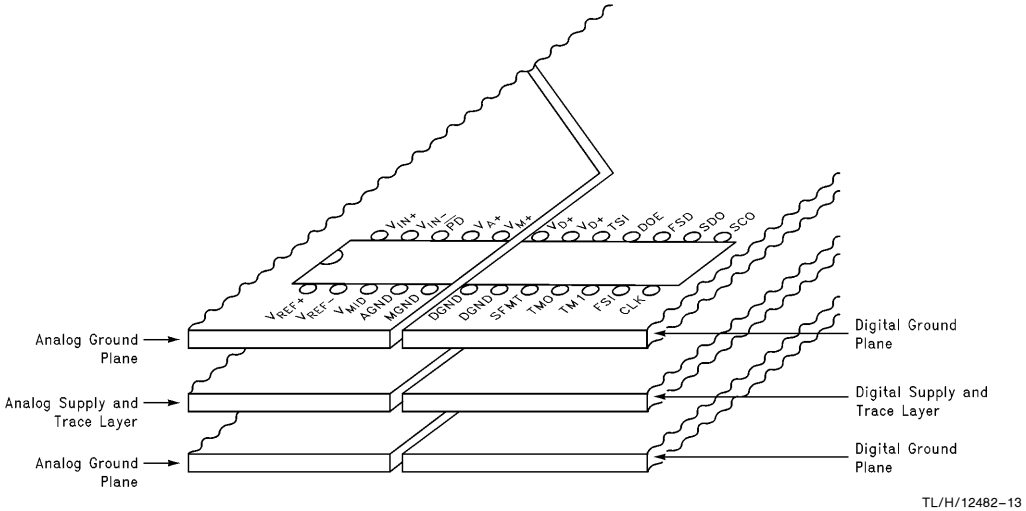

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FIGURE 13. PCB Layout with ''Sandwiched'' Power Supply and Trace Layers

As the distance between the ADC16071/ADC16471 and its bypass capacitors increases, so do the bypass capacitor lead inductances. Increased lead inductances result in decreased high frequency attenuation. At the frequencies used to clock the ADC16071/ADC16471 (f_{CLK} = 24.576 MHz), even a typical lead-length (bond wires, package lead, and capacitors leads) of 10mm has an inductance of 20 nH or 3Ω impedance. This impedance reduces the efficiency of the bypass capacitors. Spikes and glitches riding on the DC supply voltage are most efficiently attenuated when power supply bypass capacitors are placed as close as possible to the power supply pins.

Ideally the ADC16071/16471 should be soldered directly to the printed circuit board. This minimizes lead length between power supply and ground pins and power supply bypass components. Even a lead-length increase of 0.125″ can degrade SINAD performance by 5 dB–15 dB.

When using the ADC16071/ADC16471 in the molded Dual-in-Line Package (DIP), mounting the ADC in a modified ''socket'', allows surface-mount capacitors to be placed directly under the package and between the pins using the shortest possible trace lengths *(Figure 14).* This ''socket'' is created by using individual machined socket-pins. These pins require a hole size of 58 mils. This hole size ensures that only the topmost portion of the pin remains above the circuit board. These ''socket'' pins will tightly grip the ADC16071/ADC16471 plastic package's pins, further reducing a possible source of performance degradation caused by loose fitting sockets.

Suggested power-supply bypassing consists of surface-mount 0.1 μF monolithic ceramic and 10 μF tantalum capacitors. When using the ADC16071/ADC16471 in the DIP package, the bypass capacitors' size is limited by the distance between the DIP package pins. When placed under an ADC16071/ADC16471 DIP package using a modified ''socket'' as in *Figure 14,* the 0.1 μF SMD capacitor's physical size is limited to package number 0805. The 10 μF SMD capacitor's physical size is limited to package number 1210.

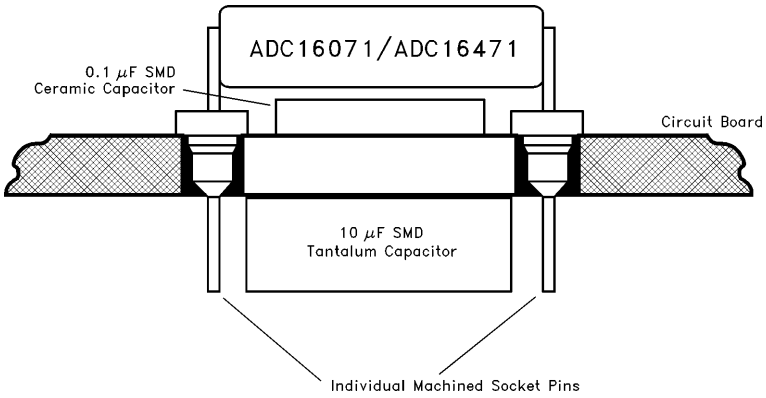
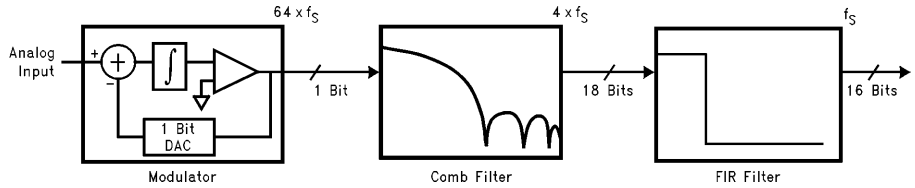


FIGURE 14. ADC16071/ADC16471 PCB Mounting and Bypass Capacitor Positioning

APPENDIX

NOISE SHAPING IN DELTA SIGMA MODULATORS



f_S = Output Data Rate

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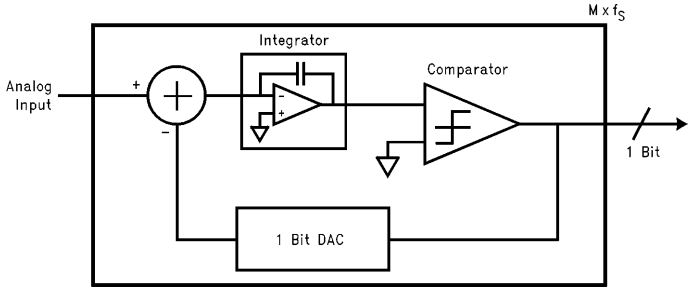
FIGURE A. Delta Sigma ADC Block Diagram



M = Oversampling Ratio

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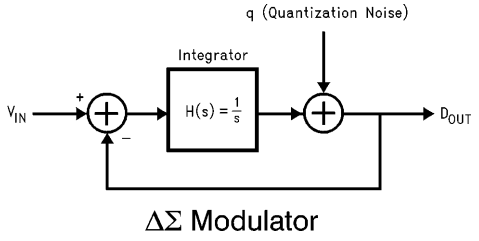
FIGURE B. Block Diagram of a 1-Bit, First Order Delta Sigma Modulator

A delta-sigma converter consists of a $\Delta\Sigma$ modulator that is essentially a high speed, low resolution ADC, and a DSP block that trades time for resolution (i.e., 64 • f_S with 1-bit to f_S with 16 bits) and filters the output of the modulator. The DSP block typically consists of a comb filter, sometimes called a decimator, and an FIR filter that has a ''brick wall'' low-pass characteristic.

Figure B is a block diagram of a 1-bit, first order modulator. The difference (Δ) between the analog input and the comparator's previous output is integrated (Σ) in such a manner that the *average* of the digital output is equal to the analog input.

The ones and zeros at the modulator's output represent the comparator's positive and negative full scale, respectively. For example, a modulator output of: 1,0,1,1,1,1,0,0,0,1,0, represents an analog input halfway between positive and negative full scale (5 out of a possible 10 ones).

Because of the crude approximation made by the comparator of a $\Delta\Sigma$ modulator (it is quantizing with only 1-bit of resolution), a large amount of quantization noise is introduced into the system. But because of the noise ''shaping'' characteristic that is inherent to the design of $\Delta\Sigma$ modulators, much of the quantization noise introduced by the modulator's comparators is pushed beyond the frequency band of interest (f_{BB}), where it may be filtered digitally.



$$D_{OUT} = (V_{IN} - D_{OUT}) \bullet H(s) + q$$

$$D_{OUT} \bullet (1 + H(s)) = V_{IN} + q$$

$$D_{OUT} = \frac{V_{IN} \bullet H(s)}{1 + H(s)} + \frac{q}{1 + H(s)} \qquad H(s) = \frac{1}{s}$$

$$\therefore D_{OUT} = \frac{V_{IN}}{1 + s} + \frac{q \bullet s}{1 + s}$$

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FIGURE C. Noise Shaping in Delta Sigma Modulator

If we make the approximation that the comparator of *Figure B* can be treated as the addition of quantization noise (q) that has a ''white'' spectral distribution (uniform energy at all frequencies) and uncorrelated to the analog input, then the substitution shown in the block diagram of *Figure C* may be made. From this block diagram, the output of the modulator may be equated to the difference between the quantized output, D_{OUT}, and the analog input, V_{IN}, times the transfer function of the integrator, H(s), plus the quantization noise, q. From the resulting transfer function for D_{OUT} in terms of the analog input and the quantization noise, it can be shown that quantization noise is filtered through a high-pass filter

$$\left(\frac{q \bullet s}{s + 1}\right),$$

while the input signal passes unattenuated at low frequencies ($f < f_{BB} << M \bullet f_S$). This high-pass function ''shapes'' the quantization noise out of the baseband, f_{BB} to higher frequencies where it will be cut off by the digital filtering within the ADC.

By increasing the order of a ΔΣ modulator (adding more integrators to the modulator), the noise shaping effect is enhanced. *Figure D's* curves show how the flat quantization noise is ''shaped'' into first-, second-, and third-order modulator characteristics.

ΔΣ modulators further reduce the amount of quantization noise in the baseband by oversampling the input signal. The quantization noise is assumed to be spread out equally from DC up to the sample rate of the modulator. As the oversampling ratio is increased, so is the range over which the quantization noise is spread. The total noise does not decrease, but the density per frequency band does. With a first order modulator, the theoretical maximum signal-to-quantization-noise ratio in the baseband can be shown to increase by 9 dB with each doubling of the oversampling ratio.

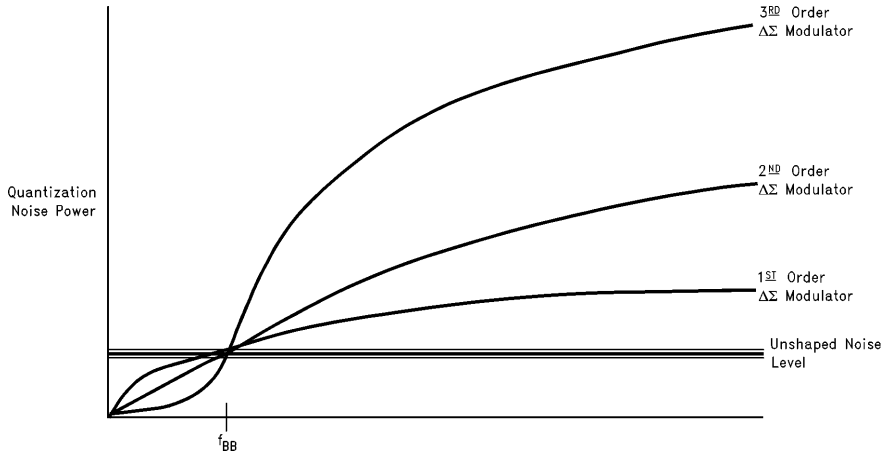

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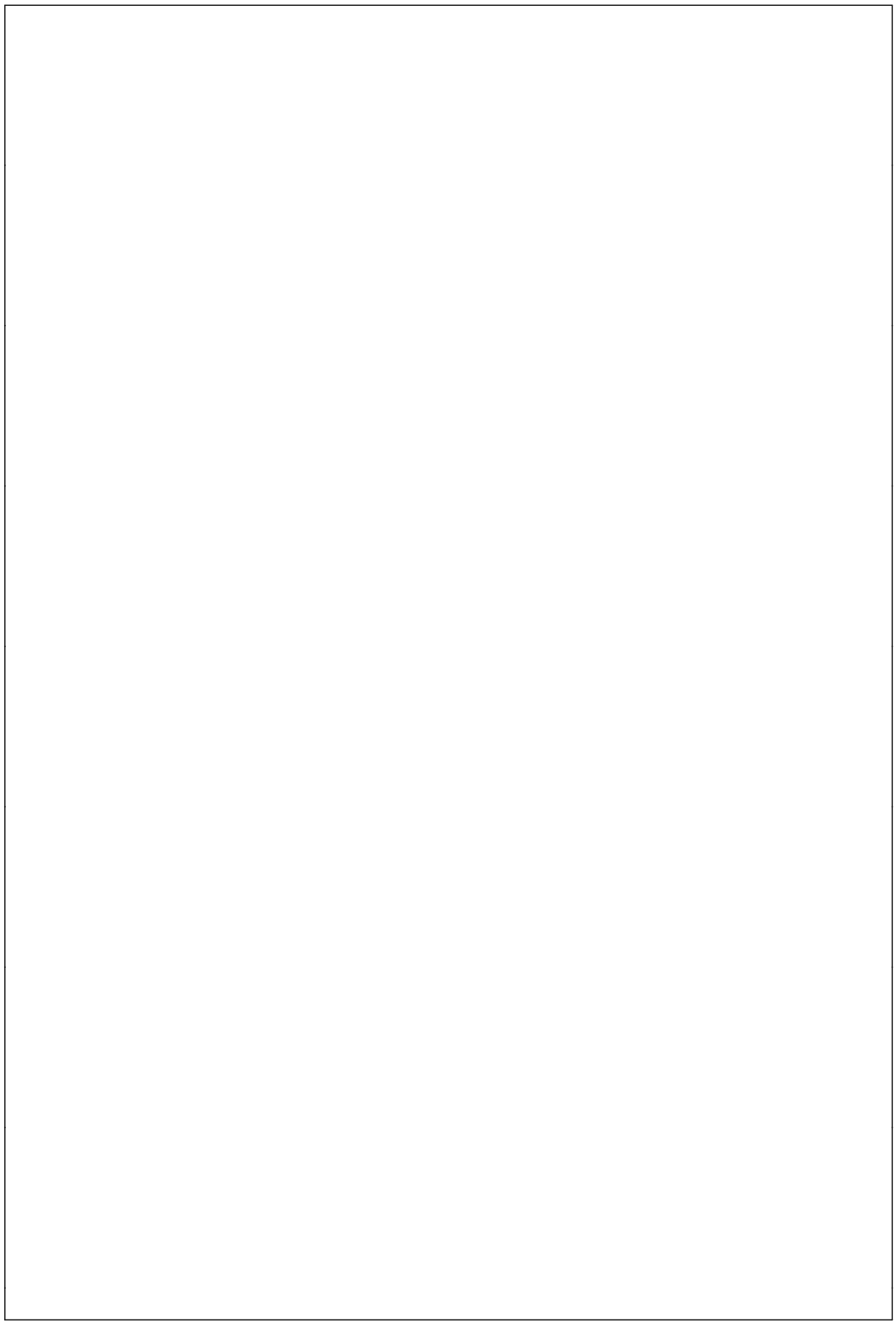
FIGURE D. Noise Shaping Characteristic Curves



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