

LV04EVK01

Channel Link to Channel Link II Converter Evaluation Kit

Rev 0.0
Aug, 2010

General Description

The LV04EVK01 is designed to allow for easy evaluation of the DS92LV0421 and DS92LV0422 Channel Link II Ser/Des. This kit allows for 2 basic methods of evaluation:

- 1) Users may apply application data in the Channel Link LVDS fashion, 4 data + clock, and evaluate the power, jitter and cable performance of the Ser/Des.
- 2) Apply a parallel LVDS clock and enable BIST mode. This allows the user to easily evaluate the serial link and check device feature functionality such as transmit de-emphasis, receive equalization, SSCG, etc.

The LV04EVK01 boards use a space saving 20-position header pin bank as the Channel Link inputs/outputs and USB connectors as the serial Channel Link II inputs/outputs. SMA connectors can also be attached and configured for serial input/output if other types of the cable are desired.

Features

- 10 – 75 MHz support for 240 Mbps – 1.8 Gbps application payload (280 Mbps to 2.1 Gbps Serial Link)
- Low EMI 5 LVDS Channel (4 data + 1 clock) Channel Link inputs/outputs for parallel bus
- AC Coupled STP Interconnect up to 10 meters in length
- Selectable output VOD, adjustable de-emphasis and receive equalization
- Integrated serial terminations
- @ Speed link BIST Mode and reporting pin
- Optional I2C compatible Serial Control Bus
- RGB888 + VS, HS, DE serialized to 1 pair
- Power down mode minimizes power dissipation
- Randomized, DC-balanced and Scrambled data stream
- >8 kV HBM
- Backward compatible mode for operation with older generation devices

Applications

- Industrial Displays
- Machine Vision
- Medical Imaging

Ordering Information

PART: LV04EVK01

Demo boards:

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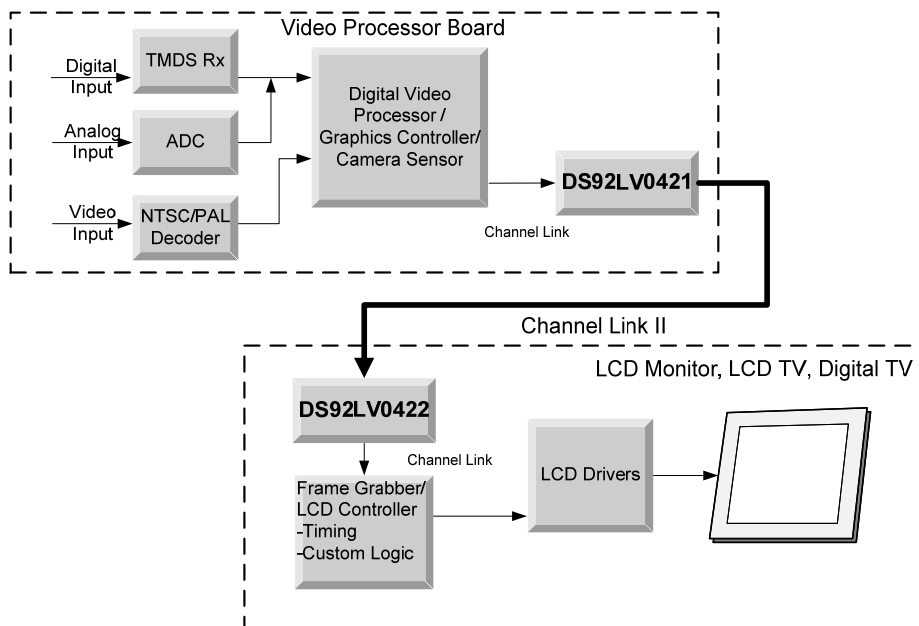
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Tx: DS92LV0421-EVK
Rx: DS92LV0422-EVK

Typical Configuration



Quick Start Guide:

DS92LV0421 Tx Board:

1. Connect 3.3V DC power to the left header pin of JP1 and ground to the right header pin of JP1. Connect 1.8V DC power to J3 and ground to J4.
2. Attach the USB cable to the TX board (DS92LV0421) output and to an RX board (DS92LV0422 supplied) input. The default cable connector on the TX board is P3, which is mounted to the bottom of the evaluation board.
3. Attach parallel LVDS clock and data to the TX board at connector J1. This is typically done with a flat ribbon cable (not supplied).
4. Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the board. See text on Configuration Settings and datasheet for more details.

DS92LV0422 Rx Board

Quick Start Guide:

5. Connect 3.3V DC power to the left header pin of JP1 and ground to the right header pin JP1. Connect 1.8V DC power to J4 and ground to J5.
6. Attach the USB cable to the RX board (DS92LV0422) input from a TX board (DS92LV0421) output. The default cable connector on the RX board is J2.
7. Attach the parallel LVDS clock and data outputs to the desired test equipment or other external hardware. This is typically done with a flat ribbon cable (not supplied).
8. Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the board. See text on Configuration Settings and datasheet for more details.

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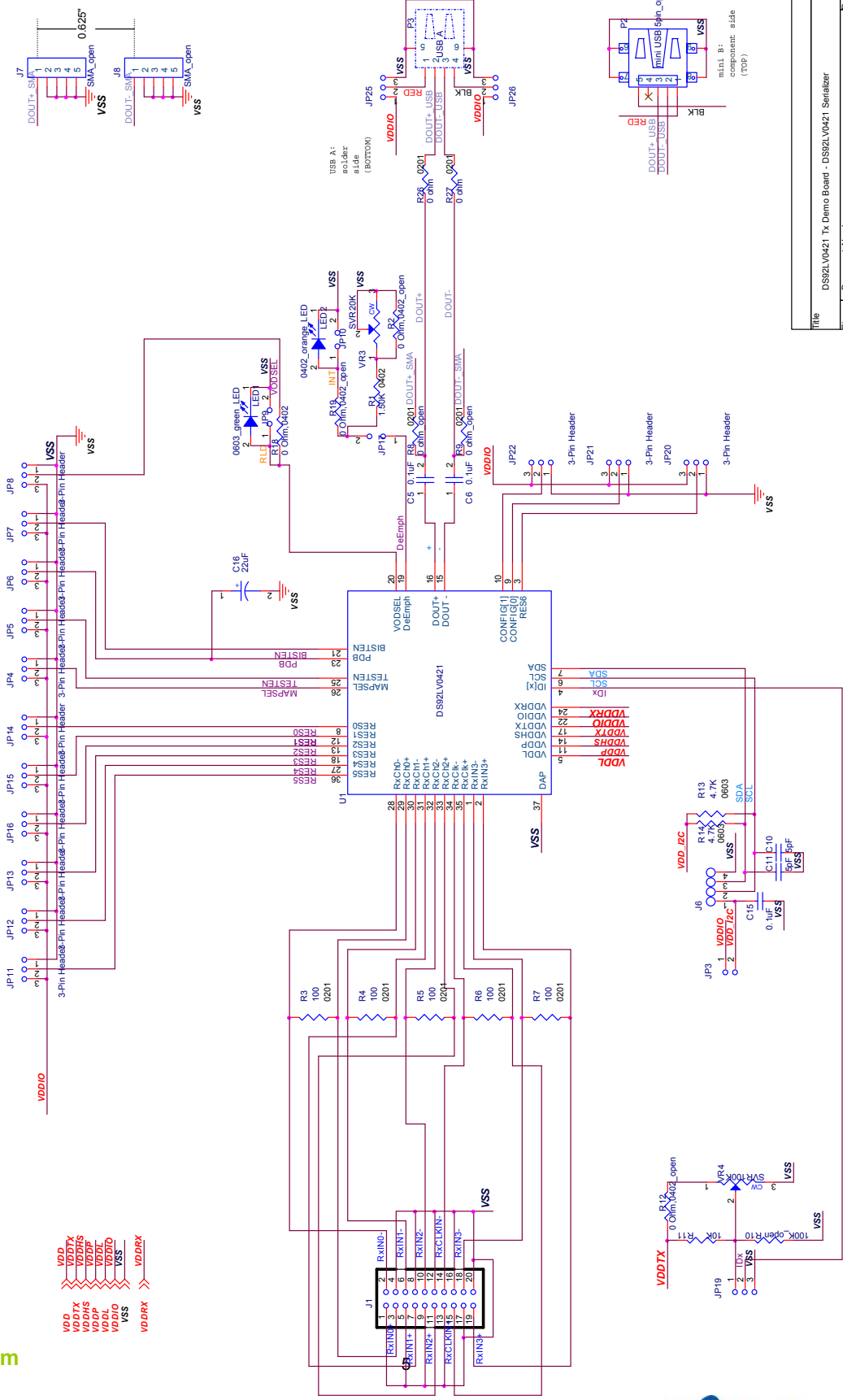
Tx Board Configuration Settings

Component	Name	Function
Power Connections		
J3	1.8V DC	1.8V VDD Power.
JP1	3.3V DC	3.3V VDD Power.
J4	VSS	Ground.
JP2	VDDI	Always connect to 3.3V.
JP18	VDDL	Always connect to 1.8V.
JP23	VDDP	Always connect to 1.8V.
JP24	VDDHS	Always connect to 1.8V.
Input and Output Connections		
J1	20 position wall header	Connect to Channel Link input.
J7 and J8	SMA Connectors	Connect to Channel Link II output. (When using these connectors, R8 and R9 should be placed with 0Ω resistors, the traces from R8 and R9 to the P1 should be cut).
P3	USB Connector	Connect to Channel Link II output. (default)
JP25 and JP26	Power Wire in USB cable through P3	Connect to VSS is recommended.
Control Connections		
JP4	MAPSEL	Connect it to "L" or "H" for the Channel Link mapping select. See datasheet for detail information.
JP5	TESTEN	NSC test mode. Always connect it to "L" or leave it unconnected.
JP6	PDB	Connect it to "L" for the power down mode. Connect it to "H" for the enable mode. See datasheet for detail information.
JP7	BISTEN	Connect it to "H" for the BIST enable mode. See datasheet for detail information.
JP8	VODSEL	Connect it to "L" or "H" for the Channel Link II VOD level select. See datasheet for detail information.
JP21 and JP22	CONFIG	Configuration select. See datasheet for detail information.
JP17 and VR3	DEEMPH	Leave JP17 unconnected to disable the CHANNEL Link II output de-emphasis feature. Connect JP17, Adjust VR3 value to select de-emphasis level.
JP19 and VR4	ID[x]	Connect JP19 to VSS to have the default device PHY address (h'EC). Connect JP19 to VR4; then adjust VR4 value to select desired device PHY address. See datasheet for detail information.
JP3 and J6	I2C Interface	Connect JP3 if the I2C power is not supplied on J6. Otherwise, leave it unconnected.

Tx Board Bill of Materials

Item	Quantity	Reference	Comments	Digi-key P/N	Part number
1	2	C1,C13	CAPACITOR TANT 2.2UF 20V 10% SMD	399-3714-1-ND	T491B225K020AT
2	2	C2,C14	CAP .10UF 50V CERAMIC X7R 1206	399-1249-1-ND	C1206C104K5RACTU
3	4	C3,C4,C7,C8	CAP TANTALUM 10UF 16V 20% SMD. Optional.	493-2365-1-ND	F931C106MBA_open
4	2	C5,C6	CAP CERAMIC .1UF25V X5R 0402	445-4964-1-ND	C1005X5R1E104K
5	2	C9,C12	CAP TANTALUM 22UF 25V 20% SMD	493-2391-1-ND	F931E226MNC
6	2	C10,C11	CAP CERAMIC 5.0PF 25V NP0 0201	PCC2107CT-ND	ECJ-ZEC1E050C
7	7	C15,C20,C23,C24,C27,C30,C32	CAP .1UF ±10% 25V CERAMIC X7R 0603	PCC2277CT-ND	ECJ-1VB1E104K
8	7	C16,C17,C18,C19,C28,C33,C34	CAPACITOR TANT 22UF 16V 20% SMD	399-3835-1-ND	T494B226M016AT
9	6	C21,C22,C25,C26,C29,C31	CAP CERAMIC .01UF 100V X7R 0603	399-3189-1-ND	C0603C103K1RACTU
10	3	JP1,JP3,JP17	CONN HEADER VERT .100 2POS 30AU	A26542-ND	87220-2
11	14	JP2,JP4,JP5,JP6,JP7,JP8,JP18,JP19,JP21,JP22,JP23,JP24,JP25,JP26	CONN HEADER VERT .100 3POS 15AU	A26545-ND	87224-3
12	1	J1	CONN HEADER 20 POS STRGHT GOLD.	MHC20K-ND	N2520-6002RB
13	1	J2	CONN POWER JACK 2.1MM. Optional.	CP-002A-ND_open	PJ-002A_open
14	2	J3,J4	BANANA-female (non-insulated)	J147-ND	108-0740-001
15	1	J5	CONN HDR DUAL 8POS .100 SRT AU. Optional.	WM26808-ND	10-89-7082_open
16	1	J6	CONN HEADER 4POS .100 VERT GOLD End Launch Jack Receptacle - Tab Contact.	WM2702-ND	22-11-2042
17	2	J7,J8	Optional.	J658-ND_open	142-0701-851_open
18	1	P1	Automotive HSD Conn - Right Angle Plug Optional.		D4S20B-40ML5-Y_open
19	1	P2	CONN RECEPT MINI USB2.0 5POS. Optional.	H2959CT-ND	UX60-MB-5ST_open
20	1	P3	CONN USB RECEPT R/A TYPE A 4POS.	A31726-ND	292303-1
21	1	R1	RES 1.50K OHM 1/16W 1% 0402 SMD	P1.50KLCT-ND	ERJ-2RKF1501X
22	2	R2,R12	RES ZERO OHM 1/16W 5% 0402 SMD. Optional.	P0.0JTR-ND_open	ERJ-2GEJ0R00X_open
23	5	R3,R4,R5,R6,R7	RES 100 OHM 0201 SMD. 1/20W .5%	RR03P100DCT-ND	RR0306P-101-D
24	2	R8,R9	RES 0 OHM 0201 SMD. Optional.	P0.0AGCT-ND P100KHCT-ND_open	ERJ-1GE0R00C
25	1	R10	RES 100K OHM 1/10W 1% 0603 SMD. Optional.	P10.0KHCT-ND	ERJ-3EKF1003V_open
26	1	R11	RES 10.0K OHM 1/10W 1% 0603 SMD	P10.0KHCT-ND	ERJ-3EKF1002V
27	2	R13,R14	RES 4.7K OHM 1/10W 5% 0603 SMD	P4.7KGCT-ND	ERJ-3GEYJ472V
28	2	R15,R16	RES 82.5 OHM 1/10W 1% 0603 SMD. Optional.	P82.5HCT-ND	ERJ-3EKF82R5V_open
29	1	R17	RES 100 OHM 1/10W 1% 0603 SMD. Optional.	P100HCT-ND	ERJ-3EKF1000V_open
30	7	R18,R20,R21,R22,R23,R24,R25	RES ZERO OHM 1/16W 5% 0402 SMD	P0.0JTR-ND	ERJ-2GEJ0R00X
31	2	R26,R27	RES 0.0 OHM 1/20W 5% 0201 SMD	P0.0AGCT-ND	ERJ-1GE0R00C
32	1	U1	DO NOT PURCHASE, National will supply.		DS92LV0421
33	2	U2,U3	IC REG ADJ 800MA LDO SOT-223.	LM1117IMP-ADJ/NOPB	LM1117IMP-ADJ/NOPB_open
34	2	VR1,VR2	TRIMPOT 100 OHM 4MM TOP ADJ SMD.	3214W-101ETR-ND	3214W-1-101E_open
35	1	VR3	11-Turn Trimming Potentiometer; Top Adjust	3224W-203ECT-ND	3224W-1-203E
36	1	VR4	11-Turn Trimming Potentiometer; Top Adjust	3224W-1-104ECT-ND	3224W-1-104E

Tx Board Schematics

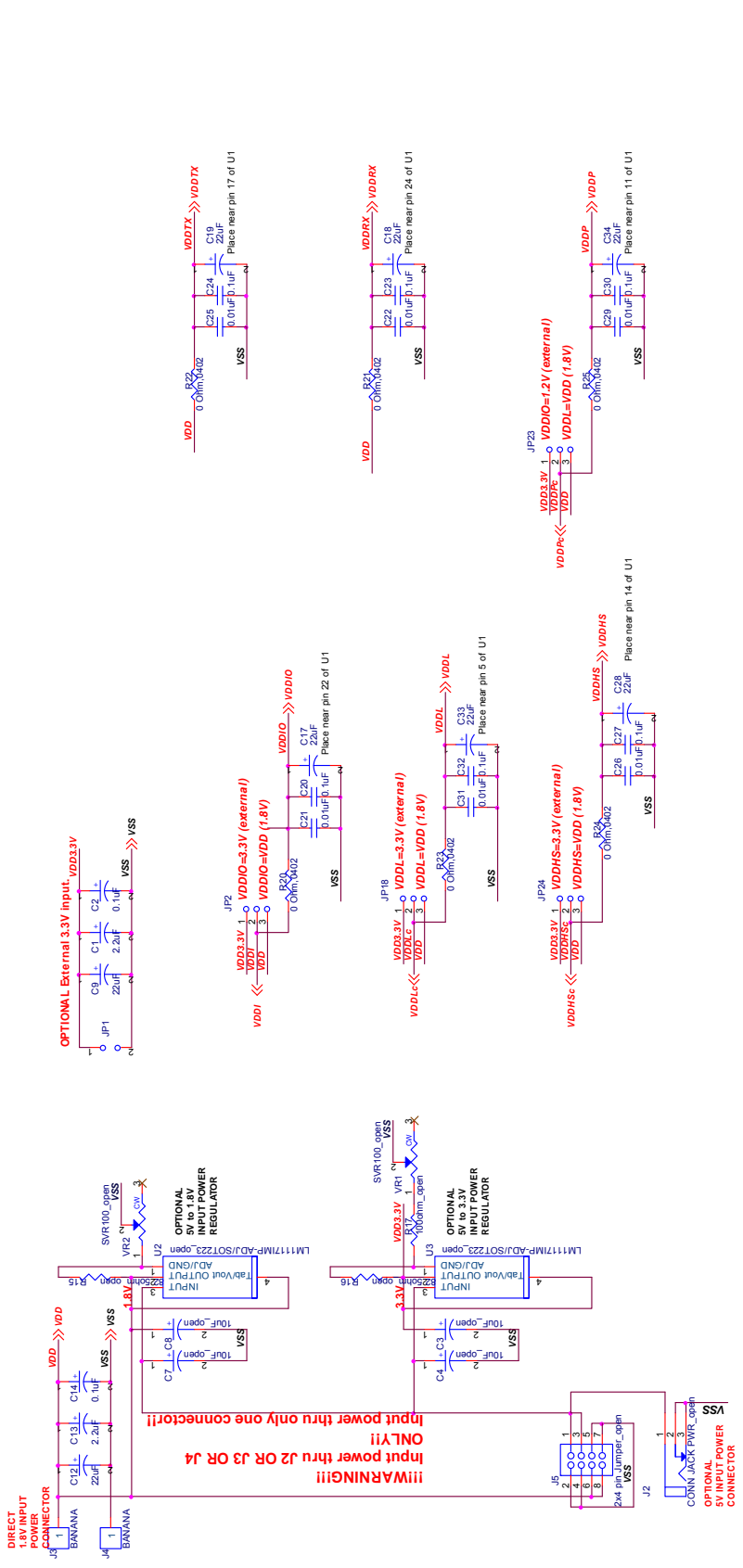


VDD
 VDDTX
 VDDHS
 VDDP
 VDDL
 VDDI
 VDDIO
 VSS
 VDDRX

Title	DS92LV0421 Tx Demo Board - DS92LV0421 Serializer
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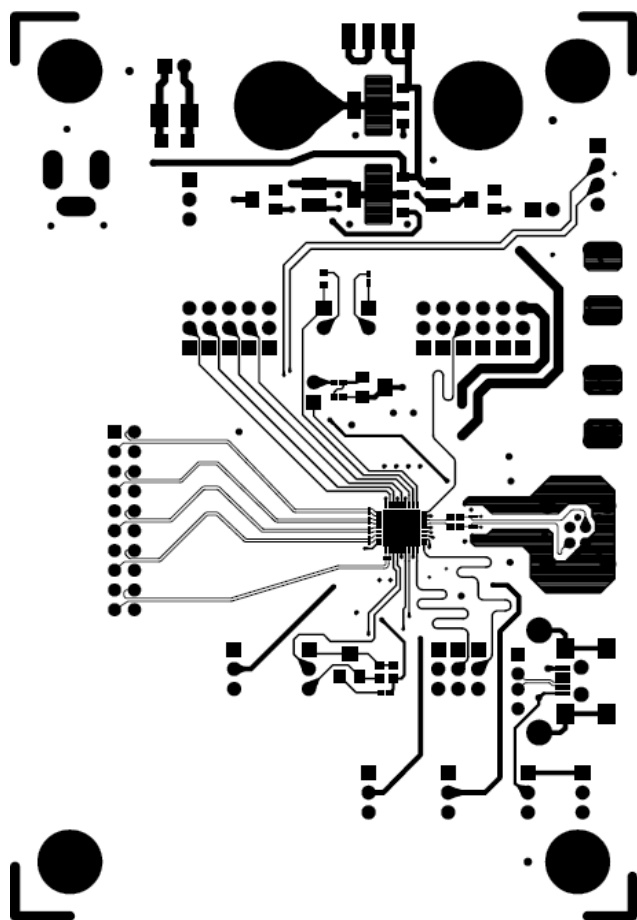


FEATURES/OPTIONS ON THE DEMO BOARD:

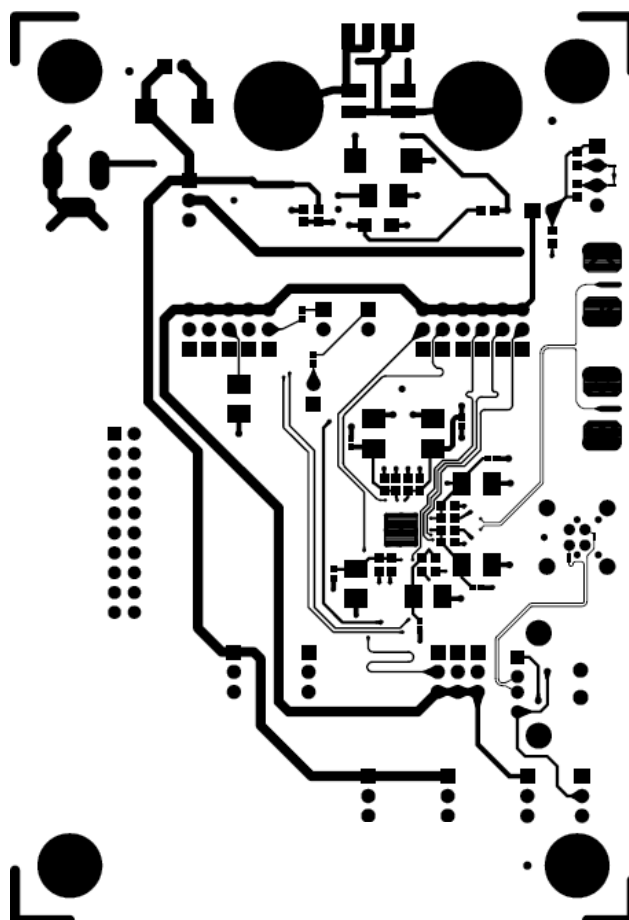
- R33, R34, R37, R38, R39 series 0402 size pads
- 1) Provided for easy separation of each VDD domain (not a user requirement).
- 2) This allows low individual I_{DD} current measurements, loaded with 0 ohm resistors
- 3) This also allows low individual I_{DD} current measurements, loaded with 0 ohm resistors, for noise reduction experimentation.
- C13-C27 decoupling capacitors 0603 and B size pads
- 1) It is not a requirement that the user must have all these capacitors and power separations in the user layout.
- 2) It is not a requirement that the user must have all these capacitors and power separations in the user layout.
- 3) It is easier to un-populate than to add capacitors and pads after the fact.
- 4) See "Typical Connection Diagram Tx - User Reference" for recommended minimum power grouping and decoupling.

Title	DS92LV0421 Tx Demo Board - Power and Decoupling
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Tx Board Reference Layout



Top Layer



Bottom Layer

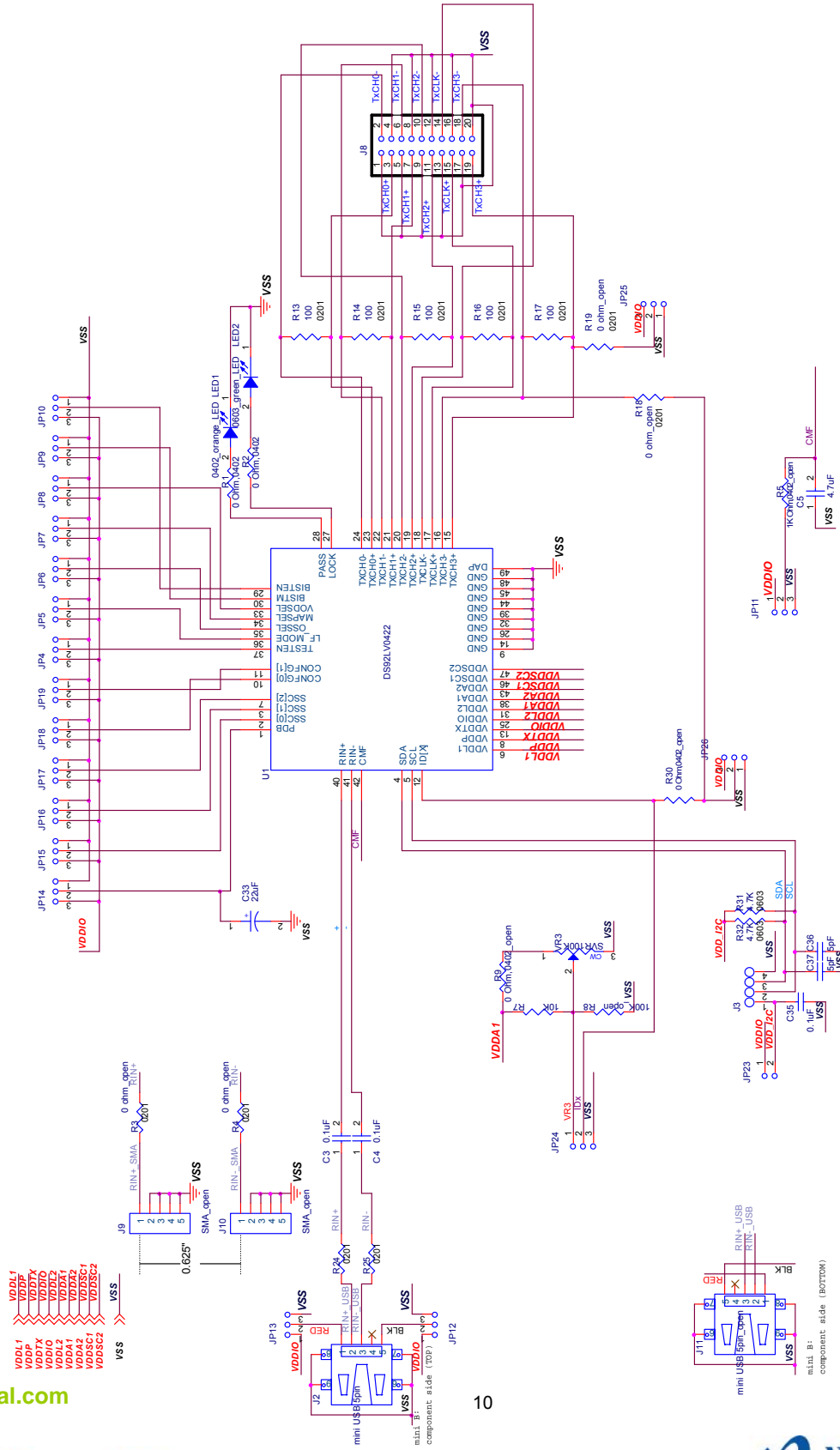
Rx Board Configuration Settings

Component	Name	Function
Power Connections		
J4	1.8V DC	1.8V VDD Power.
JP1	3.3V DC	3.3V VDD Power.
J5	VSS	Ground.
JP2	VDDIO	Connect to 3.3V or 1.8V.
JP3	VDDA2	Always connect to 1.8V.
-	VDDPC	Always connect to 1.8V.
-	VDDL	Always connect to 1.8V.
-	VDDTXC	Always connect to 3.3V.
Input and Output Connections		
J8	20 position wall header	Connect to Channel Link output.
J9 and J10	SMA Connector	Connect to Channel Link II input. (When using these connectors, R3 and R4 should be placed with 0Ω resistors, the traces from R3 and R4 to the J1 should be cut).
J2	USB Connector	Connect to Channel Link II input. (default)
JP12 and JP13	Power Wire in USB cable through J2	Connect to VSS is recommended.
Control Connections		
JP4	TESTEN	NSC test mode. Always connect it to "L" or leave it unconnected.
JP5	LF_MODE	Connect to "L" or "H" for the PCLK frequency select. See datasheet for detail information.
JP6	OSSEL	Connect to "L" or "H" for the Output State select. See datasheet for detail information.
JP7	MAPSEL	Connect it to "L" or "H" for the FPD Link mapping select. See datasheet for detail information.
JP8	VODSEL	Connect it to "L" or "H" for the FPD-Link VOD level select. See datasheet for detail information.
JP9	OEN	Connect it to "L" or "H" for the Output Enable select. See datasheet for detail information.
JP10	BISTEN	Connect it to "H" for the BIST enable mode. See datasheet for detail information.
-	PDB	Connect it to "L" for the power down mode. Connect it to "H" for the enable mode. See datasheet for detail information.
-	SSC[2:0]	Connect them to "L" or "H" for the SSCG selection.
-	CONFIG	Configuration select. See datasheet for detail information.
JP24 and VR3	ID[x]	Connect JP24 to VSS to have the default device PHY address (h'DC). Connect JP24 to VR3; then adjust VR3 value to select desired device PHY address. See datasheet for detail information.
J3 and JP23	I2C Interface	Connect JP23 if the I2C power is not supplied on J6. Otherwise, leave it unconnected.
Others		
LED1	PASS	PASS output. "ON" when PASS is "H"
LED2	LOCK	LOCK output. "ON" when LOCK is "H"
JP11, JP25, JP26	Other options	Do not connect

Rx Board Bill of Materials

Item	Quantity	Reference	Part	Comments	Digi-Key P/N	Part Number
1	2	C3,C4	0.1uF	CAP CERAMIC .1UF25V X5R 0402	445-4964-1-ND	C1005X5R1E104K
2	1	C5	4.7uF	CAP .1UF 16V CERAMIC Y5V 0402.	PCC1731CT-ND	ECJ-0EF1C104Z
3	9	C6,C18,C20,C22,C25,C26, C27,C28,C29	0.01uF	CAP CERAMIC .01UF 100V X7R 0603	399-3189-1-ND	C0603C103K1RACTU
4	10	C7,C17,C19,C21,C23,C24, C30,C31,C32,C35	0.1uF	CAP .1UF 20% 25V CERAMIC X7R 0603	PCC2277CT-ND	ECJ-1VB1E104K
5	2	C10,C13	22uF	CAP TANTALUM 22UF 25V 20% SMD	493-2391-1-ND	F931E226MNC
6	2	C11,C14	2.2uF	CAPACITOR TANT 2.2UF 20V 10% SMD	399-3714-1-ND	T491B225K020AT
7	2	C12,C15	0.1uF	CAP .10UF 50V CERAMIC X7R 1206	399-1249-1-ND	C1206C104K5RACTU
8	3	C16,C33,C34	22uF	CAPACITOR TANT 22UF 16V 20% SMD	399-3835-1-ND	T494B226M016AT
9	2	JP1,JP23	2-Pin Header	CONN HEADER VERT .100 2POS 30AU	A26542-ND	87220-2
10	24	JP2,JP3,JP4,JP5,JP6,JP7, JP8,JP9,JP10,JP12, JP13,JP14,JP15,JP16,JP17, JP18,JP19,JP20,JP21,JP22, JP24	3-Pin Header	CONN HEADER VERT .100 3POS 15AU	A26545-ND	87224-3
11	1	J2	mini USB 5pin	CONN RECEPT MINI USB2.0 5POS.	H2959CT-ND	UX60-MB-5ST
12	1	J3	IDC1X4	CONN HEADER 4POS .100 VERT GOLD	WM2702-ND	22-11-2042
13	2	J4,J5	BANANA	BANANA-female (non-insulated) CONN HEADER 20 POS STRGHT	J147-ND	108-0740-001
14	1	J8	2X10-Pin Header	GOLD. End Launch Jack Receptacle - Tab Contact.	MHC20K-ND	N2520-6002RB
15	2	J9,J10	SMA	LED ORN/CLEAR 610NM 0402 SMD	J658-ND	142-0701-851
16	1	LED1	0402_orange_LED	LED GREEN CLEAR THIN 0603 SMD	67-1879-1-ND	SML-LX0402SOC-TR
17	1	LED2	0603_green_LED	SMD	160-1446-1-ND	LTST-C191KGKT
18	2	R1,R2	0 Ohm,0402	RES ZERO OHM 1/16W 5% 0402 SMD.	P0.0JTR-ND	ERJ-2GEJ0R00X
19	9	R6,R20,R21,R22,R23,R26, R27,R28,R29	0 Ohm,0402	RES ZERO OHM 1/16W 5% 0402 SMD	P0.0JTR-ND	ERJ-2GEJ0R00X
20	1	R7	10K	RES 10.0K OHM 1/10W 1% 0402 SMD	P10.0KHCT-ND	ERJ-3EKF1002V
21	2	R10,R11	82.5ohm	RES 82.5 OHM 1/10W 1% 0603 SMD	P82.5HCT-ND	ERJ-3EKF82R5V
22	5	R13,R14,R15,R16,R17	100	RES 100 OHM 0201 SMD. 1/20W .5%	RR03P100DCT- ND	RR0306P-101-D
23	2	R31,R32	4.7K	RES 4.7K OHM 1/10W 5% 0603 SMD	P4.7KGCT-ND	ERJ-3GEYJ472V
24	1	U1	DS92LV0422	11-Turn Trimming Potentiometer; Top Adjust	3224W-1- 104ECT-ND	DS92LV0422
25	1	VR3	SVR100K			3224W-1-104E

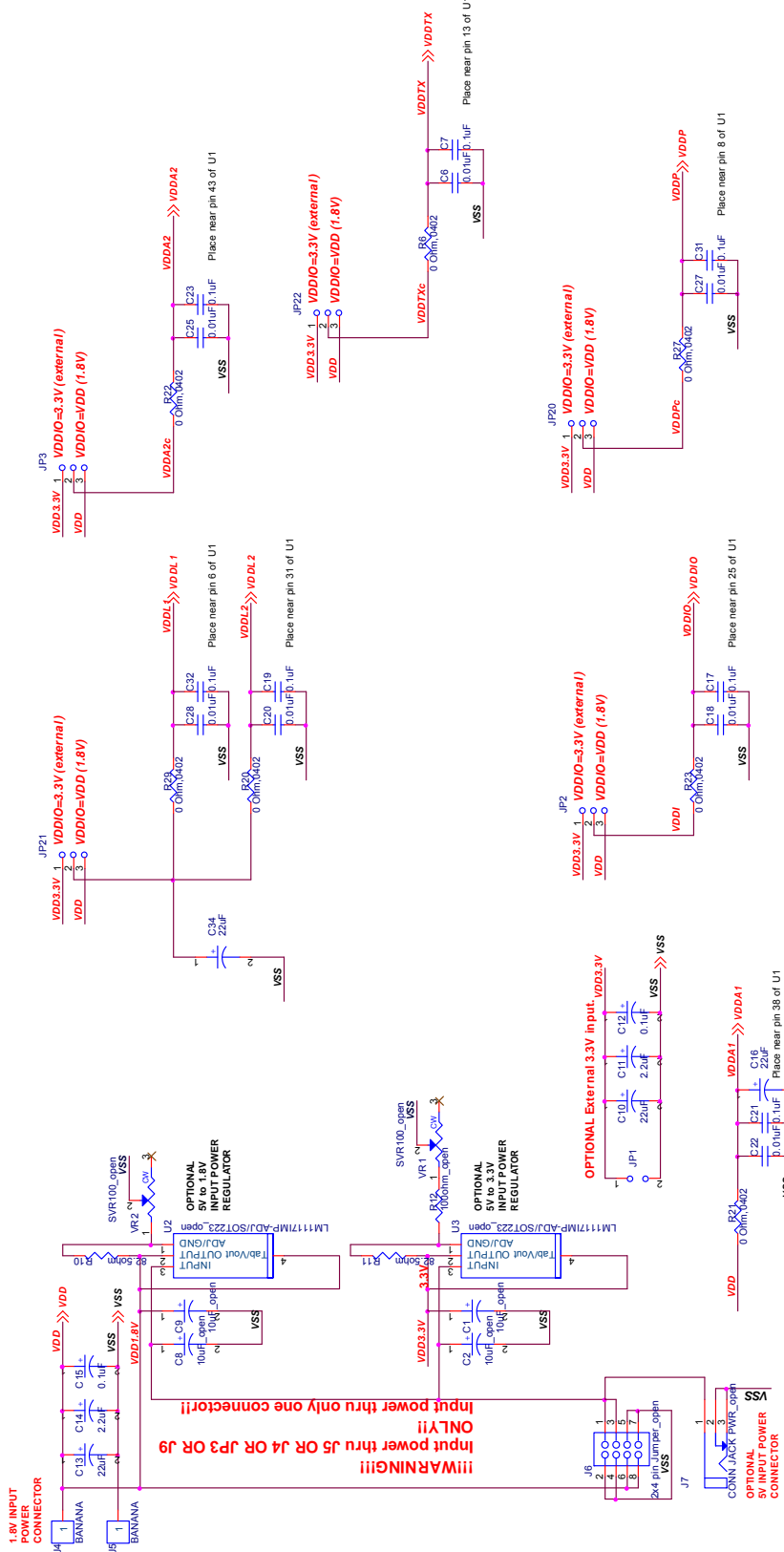
Rx Board Schematics



Title	DS92LV422 Rx Demo Board - DS92LV422 Deserializer
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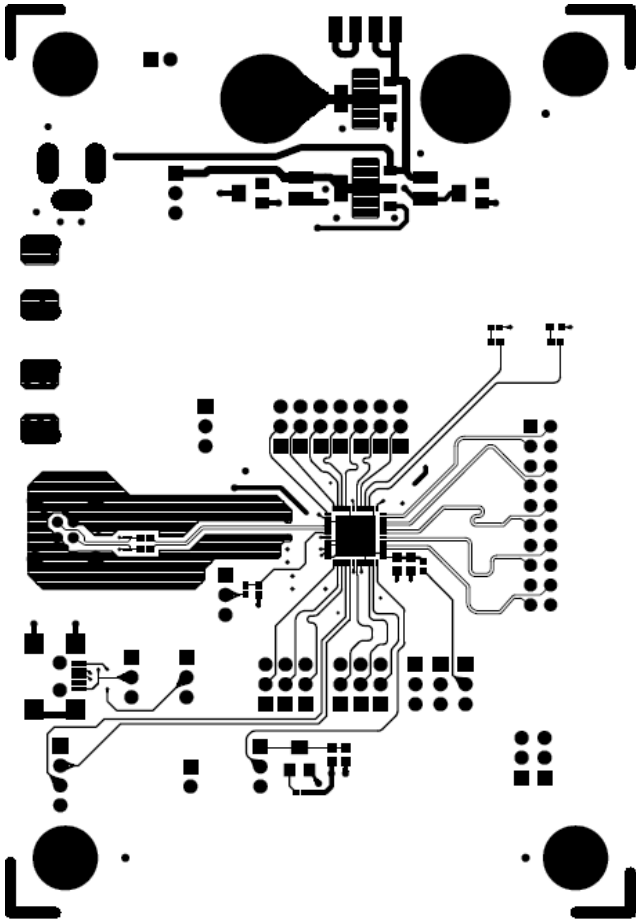
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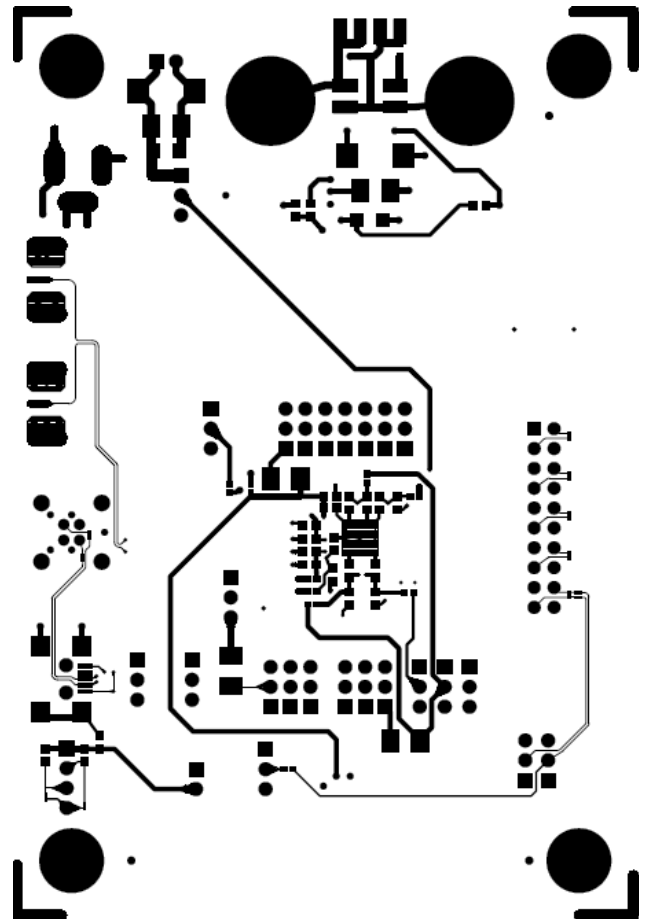


Title	DSS12V0422 Rx Demo Board - Power and Decoupling
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Rx Board Reference Layout



Top Layer



Bottom Layer

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