Application Report

Applications of Low-Voltage Differential Signaling (LVDS) in LED Walls

ABSTRACT

Industrial systems like LED wall applications often include data paths where data must be passed between multiple units in the system. This creates concerns for designers including noise, EMI, number of interface lanes, and power consumption while communicating between these units. This document will examine how the different units in LED wall systems communicate with each other, with a particular focus on where LVDS or similar signaling is applicable.

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Trademarks

1 Introduction

LVDS (Low Voltage Differential Signaling) is a differential signaling technology that uses very low amplitude signals (100 mv ~ 350 mV) to transmit data through a pair of parallel PCB traces or balanced cables, as shown in Figure 1-1.

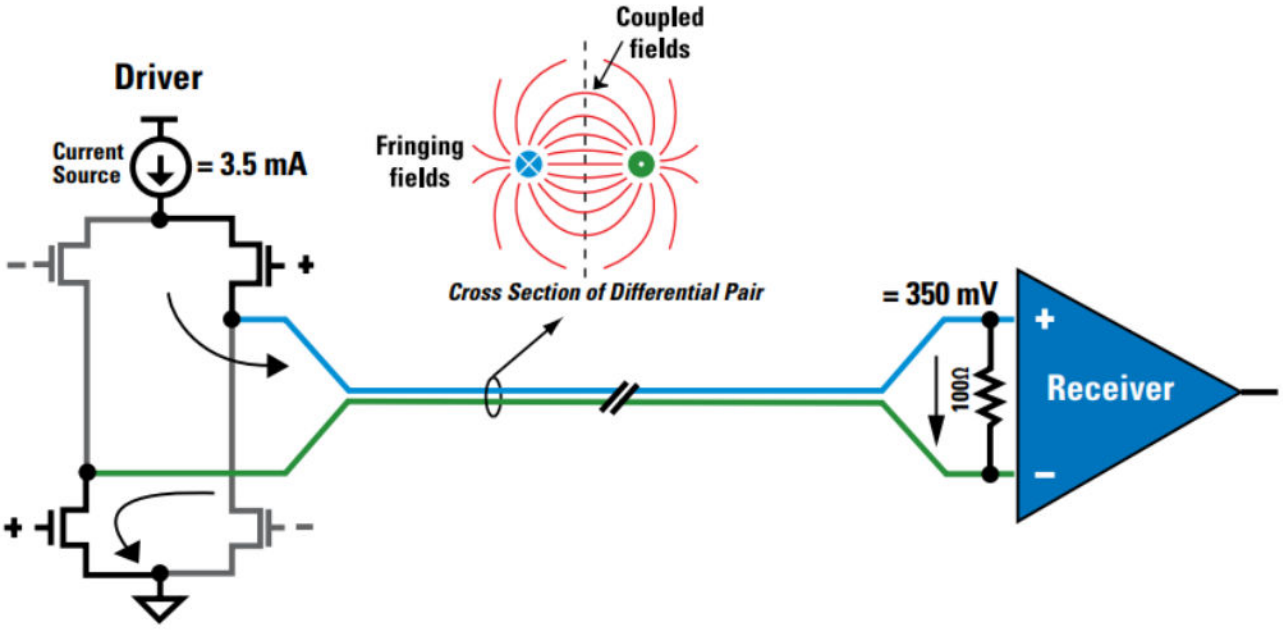

Figure 1-1. LVDS Architecture

The driver consists of a constant current source (usually 3.5 mA) driving a pair of differential signal lines. There is high DC input impedance at the receiver (almost no current consumption), so virtually all of the driver current will flow through a 100 Ω termination resistor to generate about 350 mV amplitude at the receiver input.

Noise from the system or environment will likely be coupled onto both lines at the same time, but the receiving end only cares about the difference between the two signals so the noise is effectively cancelled out. Since the electromagnetic fields around the two signal lines also cancel each other out, the differential signal transmission electromagnetic radiation is much smaller than the single-ended signal transmission electromagnetic radiation. In addition, the transmission standard adopts current mode to drive the output, so it does not generate peak signals caused by ringing and signal switching, and has good EMI (electromagnetic interference) characteristics.

Since LVDS technology reduces noise concerns, lower signal voltage amplitudes can be used. This feature is important because it makes it possible to increase the data transmission rate and reduce power consumption. Also, since the driver is a constant current source, power consumption will not change significantly with frequency.

2 LED Wall Signal Path and LVDS Applications

Figure 2-1 depicts a functional breakdown of an LED wall system. It is a generalized block diagram so it may not exactly match all systems. However, the general concept for the data path should be similar.

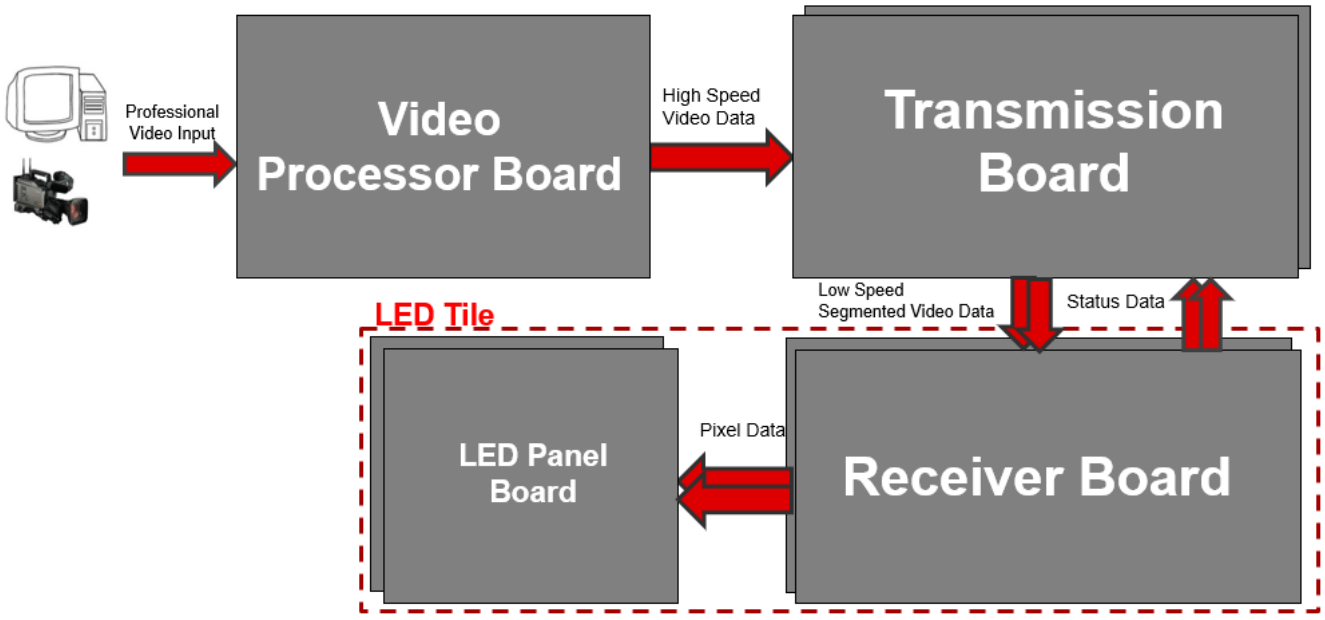

Figure 2-1. LED Wall Functional Block Diagram

A conceptual data path for an LED wall system begins with high speed video data from a source. The data then must be processed, segmented, and synchronized before being sent to the LED tiles.

Let's take a look at each subsystem individually. The Figure 2-2 depicts the processor board.

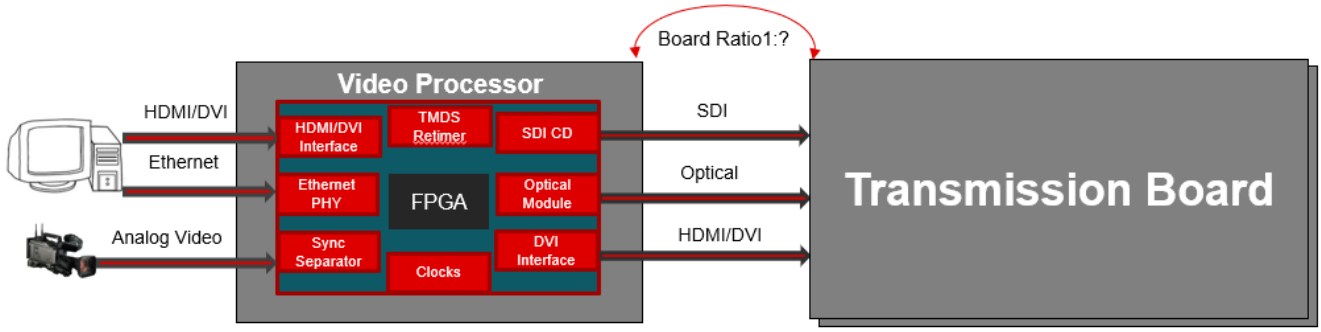

Figure 2-2. Processor Board

A typical system will begin with a video source. This will either be HDMI/DVI, Ethernet, or analog video. The video data is first sent to the processor board. An FPGA on the processor board does the heavy lifting of the processing, and is used to reformat, split, and sync video to multiple subsystems at the original resolution.

After processing the data is sent to the transmission board shown in Figure 2-3:

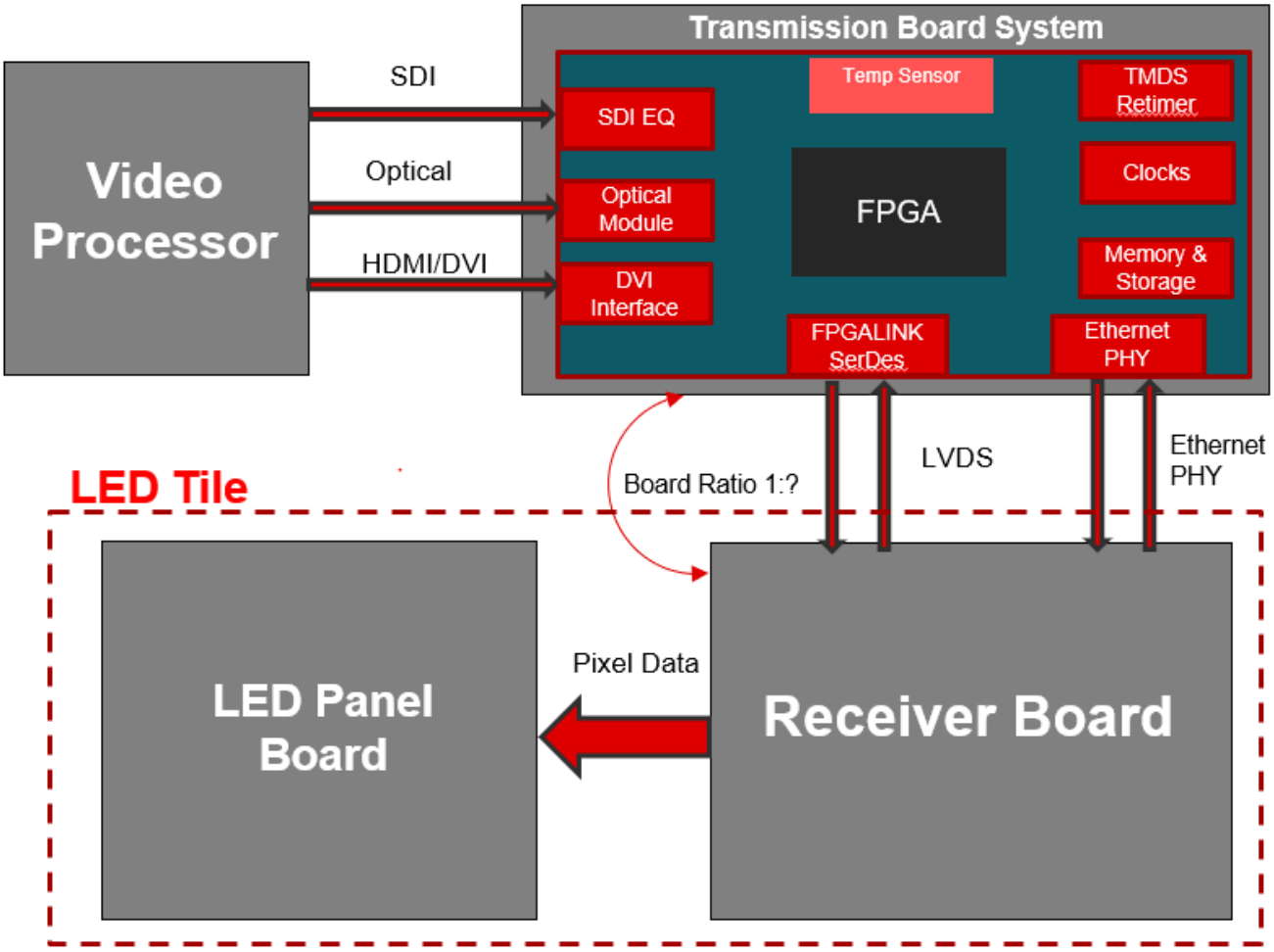

Figure 2-3. Transmission Board

One transmission board then sends the data to multiple receiver boards or LED tiles. There are many ways this can be done depending on the system architecture, but the most common way is by daisy chaining a transmission board to multiple receiver boards. Many first-generation systems send data with single-ended interfaces like LVTTL or LVCMOS. This communication method requires large connectors and cables. Additionally, the large amount of parallel data lanes leads to EMI issues, less PCB board space, significant power dissipation, and increased cost.

To remedy this, TI recommends using LVDS SerDes (serializers + deserializers) instead. The DS32ELX0421 is a serializer that takes 5 LVDS data lanes + 1 LVDS clock lane and serializes them onto 1 differential pair that can be directly connected to the DS32ELX0124 deserializer or an FPGA. The DS32EL0X124 deserializer also provides a retimed output of the data it receives on its input differential pair that can be connected to another deserializer. This can be done repeatedly to daisy chain one transmission board to multiple receiver boards, as shown in Figure 2-4.

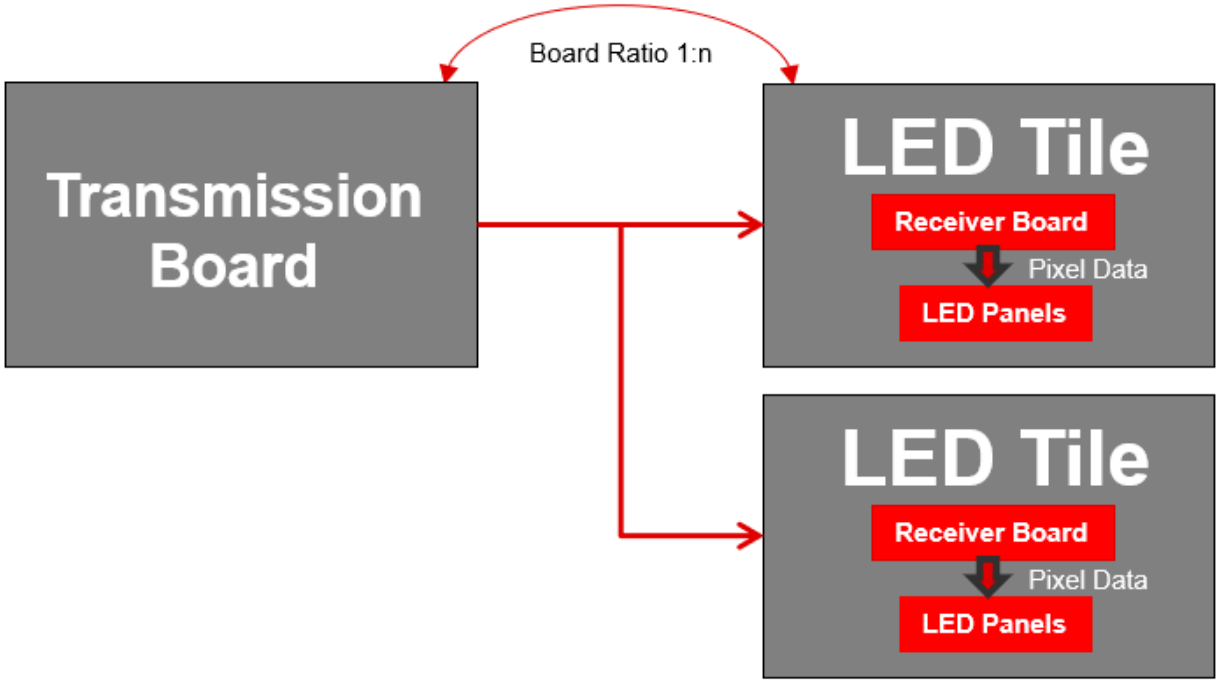

Figure 2-4. Daisy Chained Transmission Board

After additional processing and synchronizing by the receiver board, the data is then sent to the LED panels. This can be done with single-ended signaling, but again, TI recommends the use of LVDS SerDes for data transmission as shown in Figure 2-5.

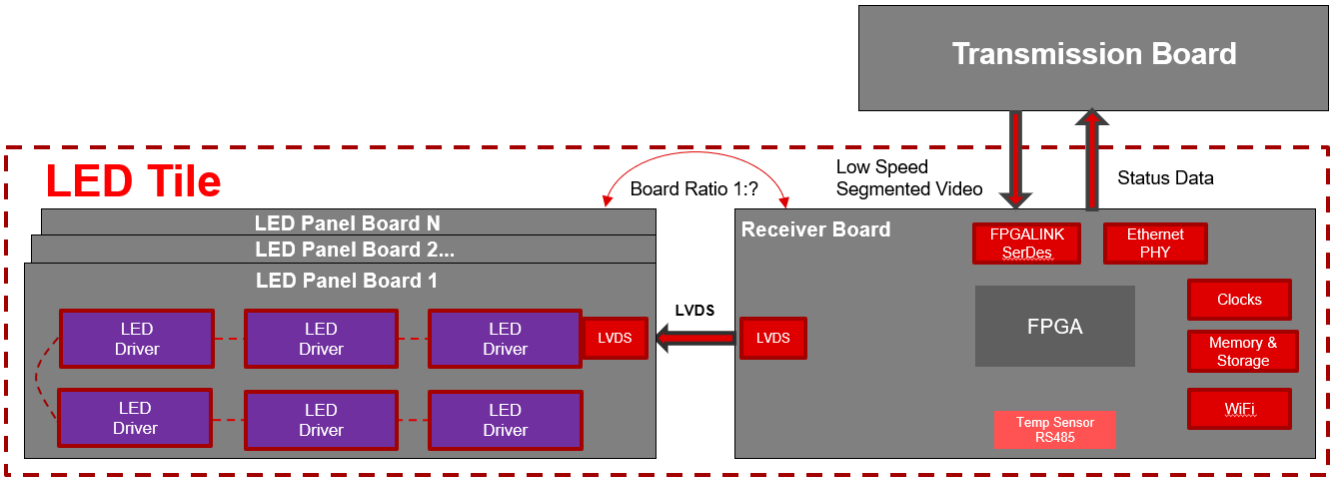

Figure 2-5. Receiver Board

The DS92LV2421 + DS92LV2422 SerDes pair can be used here. The DS92LV2421 is a generation 2 LVDS serializer takes 24-bit parallel RGB data + clock on its input and serializes them onto a single differential pair. The DS92LV2422 is a generation 2 deserializer that takes the differential pair on its input and converts it back into parallel data + clock. With this solution, you can avoid using large cables and connectors to transmit the parallel data and the problems that come with single-ended signaling.

The low amplitude (~350 mV) of the differential pair in the LVDS SerDes ensures lower power dissipation than 3.3 V LVTTL and LVCMOS single-ended signaling. Additionally, at higher data rates, parallel single-ended signaling can present serious EMI (electromagnetic interference) issues. The low amplitude, decreased number of communication lanes, and the differential nature of the differential signal in the LVDS SerDes can significantly reduce EMI.

For control data that is sent between boards, discrete LVDS drivers and receivers like the DS90LV011A and DS90LV012A can be used to transmit longer distances as well as reduce EMI. Additionally, if SPI is the interface used for the control data, it can also be sent over LVDS with the DS90LV011A, DS90LV012A, SN65LVDS31, or SN65LVDS33. TI has a reference design for transmitting SPI signals over LVDS here. LVDS SerDes like the SN65LV1023A + SN65LV1224B can also be used to serialize/deserialize the control signals to reduce the size of the interconnect if desired. For bi-directional communication and multidrop, TI suggests M-LVDS with the SN65MLVD203B or SN65MLVD204B.

In addition to LVDS, TI offers many solutions for the video interfaces in an LED wall system. For HDMI/DVI there is the TFP401, which receives HDMI/DVI and translates it to parallel 24-bit RGB. Conversely there is the TFP410, which receives parallel 24-bit RGB and translates it to HDMI/DVI. There is also the SN75DP159 and TMDS181, HDMI2.0 retimers suitable for resolutions up to 4k. For SDI, there is the LMH1228, a 12G UHD-SDI dual output cable driver, and the LMH1219, a 12G UHD adaptive cable equalizer. For Ethernet there is the DP83867, an Ethernet physical layer transceiver.

3 Summary

In summary, LVDS SerDes and LVDS drivers/receivers are a preferred method of communication when transmitting high-speed data over longer distances. In LED wall systems, concerns about EMI, power consumption/dissipation, and cable/PCB cost can be addressed with LVDS.

4 References

- LVDS Owner's Manual
- Transmitting SPI Signals Over LVDS Interface Reference Design
- LVDS Fundamentals

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