Application Report
SNLA105A–September 2008–Revised April 2013

AN-1854 DP83848C PHYTER Single to DP83848J/M PHYTER Mini System Rollover Document

ABSTRACT

This application report provides points to be considered when migrating an existing 10/100 Mb/s Ethernet design using the Texas Instruments DP83848C PHYTER™ product to the smaller DP83848J or DP83848M products.

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1 Purpose

Both the DP83848C and the DP83848J/M feature the following:

- Support 10/100 MII interface
- Operation over the commercial temperature range
- Compliant with IEEE 802.3 specification

This application report compares differences including feature set, pin functions, package and pinout, and possible register operation differences between DP83848C and DP83848J/M to simplify end user setup and help ensure a better user experience. The impact to a design is dependant on features used and their implementation.

2 Required Changes

This section documents the hardware changes required to transition from the DP83848C to the DP83848J or DP83848M. The required changes for proper operation include package, pinout, bias and termination connections.

2.1 Package

The DP83848C is available in a 48 pin LQFP package. The DP83848J/M comes in a 40 pin LLP package. The differences in package between DP83848C and DP83848J/M are shown in Table 1. For more information on the DP83848 packages, please visit Packaging Information.

Table 1. Packaging Differences

	DP83848C	DP83848J/M
Package	48-LQFP	LLP 40
Footprint	7 × 7 mm	6 × 6 mm
Package Drawing	VBH48A	SQA40A

2.2 Pinout

The DP83848C has 48 pins while the DP83848J/M have a reduced pin count. The LLP package used on the DP83848J/M also has an exposed DAP pad. Please see Appendix A for the pin mapping between DP83848C and DP83848J/M, as well as pins not applicable in the DP83848J/M.

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2.3 PCB Modification

This section describes the DP83848C circuit modifications required to use the DP83848J/M in a similar design.

2.3.1 PFBOUT

Both the DP83848C and DP83848J/M devices require similar connection of the Power Feedback circuit. Parallel capacitors (10uF Tantalum and 0.1uF ceramic) should be placed close to PFBOUT, the output of the regulator. PFBIN1 and PFBIN2 should be externally connected to PFBOUT as shown in Figure 1. A small 0.1uF capacitor should be placed close to the PFBIN1 and PFBIN2 pins. The pin assignment differences between the DP83848C and DP83848J/M are summarized in Table 2.

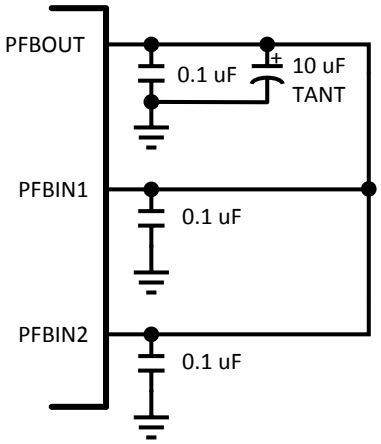

Figure 1. PFBOUT Connection

Table 2. Power Feedback Connections

Signal Name	DP83848C	DP83848J/M
PFBOUT	23	19
PFBIN1	18	16
PFBIN2	37	30

2.3.2 Bias Resistor

Internal circuitry biasing for the devices is accomplished in a similar manner. The only difference is the bias connection pin number, see Table 3.

The 4.87 kΩ connects to pin 24 on the DP83848C and pin 20 on the DP83848J/M.

Table 3. Bias Resistor Values

	DP83848C	DP83848J/M
Bias Resistor Value	4.87 kΩ	4.87 kΩ
Bias Pin	24	20

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2.3.3 Termination and PMD Biasing

The DP83848C and DP83848J/M PMD interface require two pair of 49.9 Ω resistors, biased to VDD of the device. This matching of the termination resistors and common biasing between the receiver and transmitter accommodates the Auto-MDIX feature. Refer to Figure 2 for a graphic explanation of this.

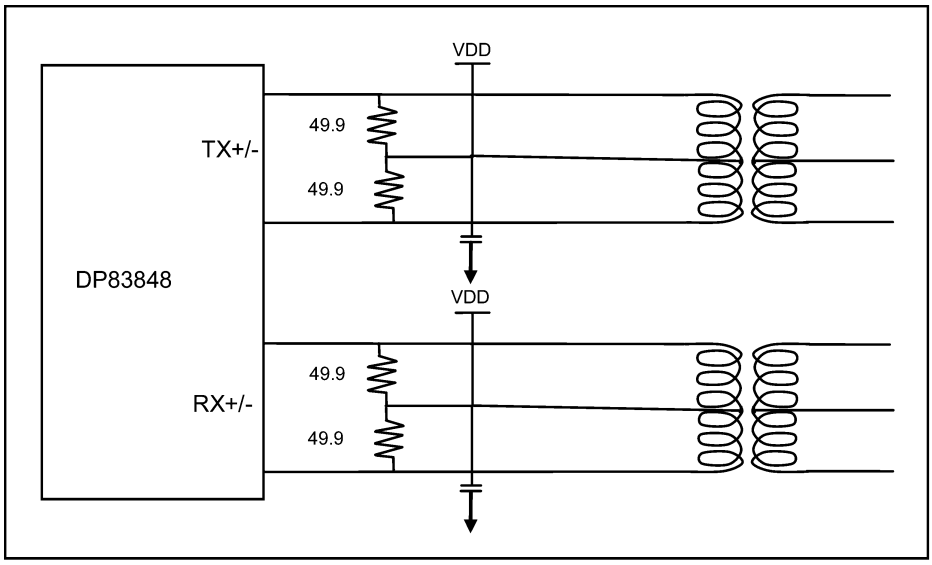

Figure 2. DP83848 PMD Connections (Termination)

3 Potential Changes

The following section describes the specific changes that may be necessary to convert to a DP83848J/M based design.

3.1 MII Interface

The MII interface is used to connect the PHY to the MAC in 10/100 Mb/s systems. For a 5 V MII application, it is recommended to use 33 Ω series resistors between the MAC and DP83848. The MII interface is a nibble-wide interface consisting of transmit data, receive data and control signals.

The transmit interface is comprised of the following signals:

- Transmit data bus, TXD[0:3] (pins 4, 5, 6, and 7 in DP83848J/M)
- Transmit enable signal, TX_EN (pin 3 in DP83848J/M)
- Transmit clock, TX_CLK (pin 2 in DP83848J/M) which runs at 2.5 MHz in 10 Mb/s mode and 25 MHz in 100 Mb/s mode

The receive interface is comprised of the following signals:

- Receive data bus, RXD[0:3] (pin 36, 37, 38, and 39 in DP83848J/M)
- Receive error signal, RX_ER (pin 34 in DP83848J/M)
- Receive data valid, RX_DV (pin 32 in DP83848J/M)
- Receive clock, RX_CLK (pin 31 in DP83848J/M) for synchronous data transfer which runs at 2.5 MHz in 10 Mb/s mode and 25 MHz in 100 Mb/s mode

Refer to Appendix A for a DP83848C to DP83848J/M pin mapping.

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3.2 PHY Address

In a given system, multiple PHYs may be controlled by a single MII management interface. In order to support this, each PHY must have a unique address. DP83848 facilitates this with PHY address strap options.

In the DP83848, RXD[0:3] and COL are also used at power-up or reset time to set the PHY address. Pin COL has a weak internal pull-up and RXD[0:3] have weak internal pull-downs. Hence, the default PHY address setting in the DP83848C and DP83848J/M is 01h. To change the PHY address, from the default, add external 2.2 kΩ pull-ups or pull-downs to the appropriate pin(s).

3.3 Physical Layer ID Register

The PHYsical Layer ID (PHYID) register allows system software to determine applicability of device specific software based on the vendor model number. The vendor model number is represented by bits 9 to 4 in PHYIDR2. The vendor model number in DP83848C is 001001b. For the DP83848J/M, the vendor model number is also 001001b.

Table 4. Register Change for Vendor Model Number

Register Address	Register Name	Register Description	Device	
			DP83848C	DP83848J/M
03h	PHYIDR2	PHY ID 2	5C90h	5C90h

3.4 Auto-Negotiation and LED Pins

The DP83848C has 3 multifunction pins to configure the Auto-Negotiation capabilities, see Table 5. At power-up or reset time they strap the media mode and during normal operation they provide status LED indications. Pin 26 has multiple LED functions, Activity or Collision status, as well as enabling Auto-Negotiation. Pin 27 indicates speed status and controls the advertised and forced mode (AN1) of DP83848C. Pin 28 indicates link status and controls the advertised or forced mode (AN0) of DP83848C.

Due to the reduced pin count in the DP83848J/M, the strapping options for Auto-Negotiation are reduced. For the DP83848J, the ability to strap a forced mode is not available. The DP83848M has an additional limitation of not being able to advertise 10 Base-T or 100 Base-TX only modes. The available Auto-Negotiation strapping modes are summarized in Table 6, Table 7, and Table 8. The full range of operating mode options are still available through register access.

Table 5. DP83848 Pins for Auto-Negotiation and LED

DP83848C Pin Number	Auto-Negotiation Function	LED Function
26	Auto-Negotiation enable	Activity and collision status
27	Controls the advertised and forced mode (AN1)	Speed status
28	Controls the advertised and forced mode (AN0)	Link status

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Table 6. DP83848C Auto-Negotiation Modes

AN_EN	AN0	AN1	Mode
Forced Mode:			
0	0	0	10 Base-T, Half-Duplex
0	0	1	10 Base-T, Full-Duplex
0	1	0	100 Base-TX, Half-Duplex
0	1	1	100 Base-TX, Full-Duplex
Advertised Mode:			
1	0	0	10 Base-T, Half/Full-Duplex
1	0	1	100 Base-TX, Half/Full-Duplex
1	1	0	10 Base-T, Half-Duplex
			100 Base-TX, Half-Duplex
1	1	1	10 Base-T, Half/Full-Duplex
			100 Base-TX, Half/Full-Duplex

Table 7. DP83848J Auto-Negotiation Modes

AN0	AN1	Advertised Mode
0	0	10 Base-T, Half/Full-Duplex
0	1	100 Base-TX, Half/Full-Duplex
1	0	10 Base-T, Half-Duplex
		100 Base-TX, Half-Duplex
1	1	10 Base-T, Half/Full-Duplex
		100 Base-TX, Half/Full-Duplex

Table 8. DP83848M Auto-Negotiation Modes

AN0	Advertised Mode
0	10 Base-T, Half-Duplex
	100 Base-TX, Half-Duplex
1	10 Base-T, Half/Full-Duplex
	100 Base-TX, Half/Full-Duplex

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4 Informational Changes

This section compares the features offered in the DP83848C and DP83848J/M and the changes required to implement them. See Table 9.

Table 9. DP83848C to DP83848J/M Feature Comparison

	DP83848C	DP83848J/M
System Interfaces:		
RMII	Yes	Yes
SNI	Yes	No
JTAG	No	No
Features:		
Auto-MDIX	Yes	Yes
Energy Detect	Yes	Yes
LED Outputs	3	2 (J) 1 (M)
CLK-to-MAC Output	Yes	No (J) Yes (M)
Power Down/Interrupt	Yes	No
Temperature Range	0 to 70 °C	0 to 70 °C
Power Consumption:		
Active Power (Typ)	264mW	264mW

4.1 RMII Interface

The RMII interface can be used to connect the MAC to the PHY in 10/100 Mb/s systems using a reduced number of pins. By utilizing this feature, significant PCB space savings can be realized within the system, especially a design with a large number of physical layer devices.

DP83848 uses an external 50 MHz clock (X1) as reference for both transmit and receive in the RMII mode. The 50 MHz is provided by an external oscillator. To enable RMII mode, RX_DV should be pulled high using a 2.2 kΩ resistor. See Figure 3.

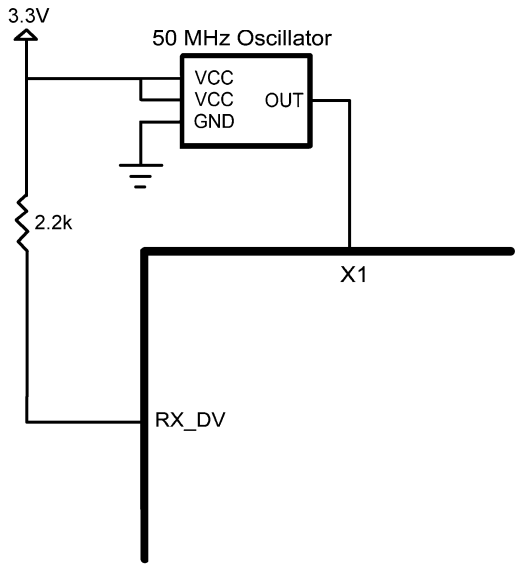

Figure 3. RMII Selection

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4.2 SNI Mode

DP83848C incorporates a 10 Mb/s Serial Network Interface (SNI) that allows a simple data interface for 10 Mb/s only system. While there is no defined standard for this interface, the interface is based on the earlier Texas Instruments 10 Mb/s physical layer devices. The DP83848J/M devices do not support SNI mode. The following pins are used in SNI mode:

- TX_CLK
- TX_EN
- TXD_0
- RX_CLK
- RXD_0
- CRS
- COL

4.3 Auto_MDIX Setting

Auto-MDIX removes cabling complications and simplifies end customer applications by allowing either a straight or a crossover cable to be used without changing the system configuration. When enabled, this function utilizes Auto-Negotiation to determine the proper configuration for transmission and reception of data and subsequently selects the appropriate MDI pair for MDI/MDIX operation. Auto-MDIX is enabled by default in the DP83848C, DP83848J and DP83848M. To disable Auto-MDIX, RX_ER should be pulled to ground using a 2.2 kΩ resistor. See Figure 4.

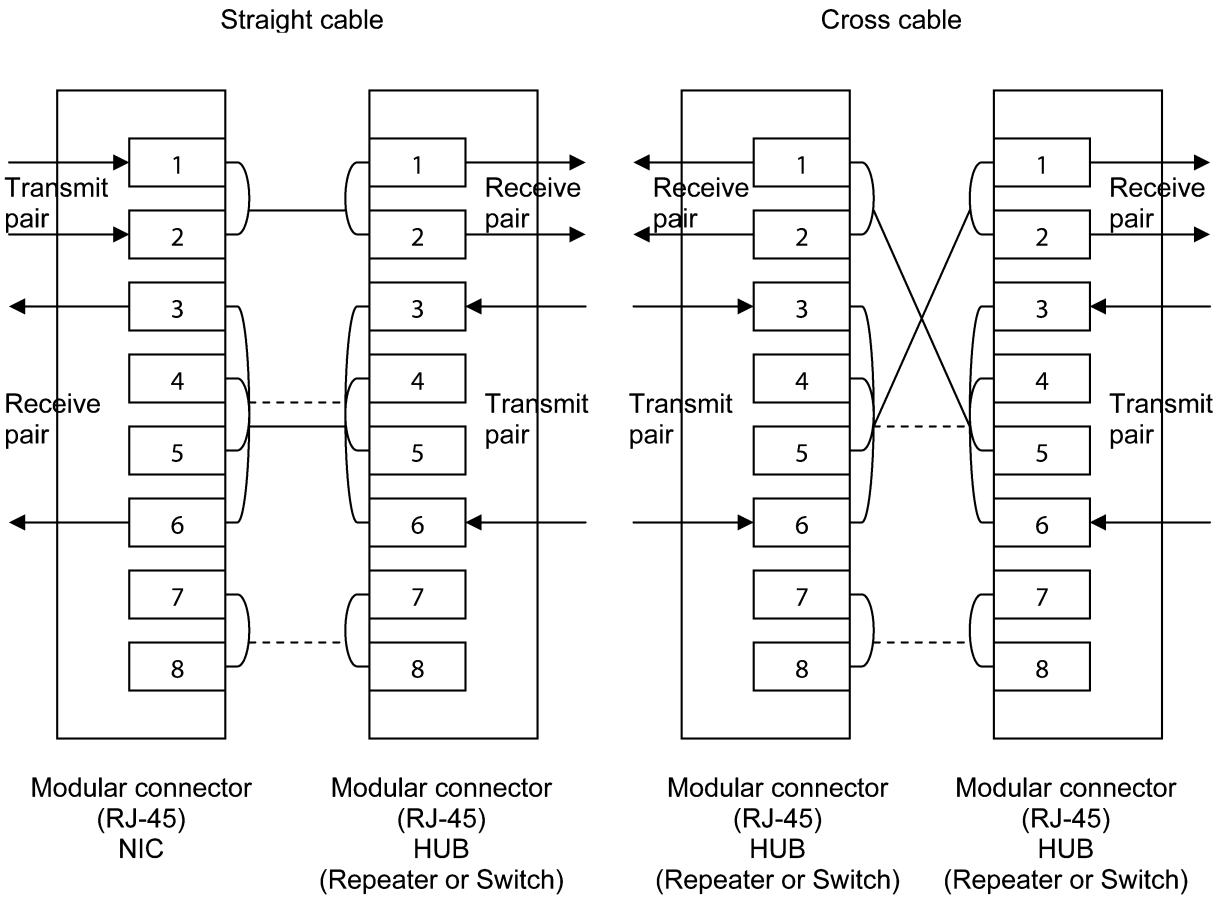

Figure 4. Auto-MDIX Operation

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4.4 Energy Detect

Energy Detect facilitates flexible and automatic power management based on detection of a signal on the cable. This enables an application to use an absolute minimum amount of power over time. Energy Detect functionality is controlled via the Energy Detect Control Register (EDCR), address 1Dh. When Energy detect is enabled and there is no activity on the cable, the PHY will remain in a low power mode while monitoring the receive pair in the transmission line. Activity on the line will cause the PHY to return to the normal power mode.

4.5 CLK_to_MAC Output

DP83848C offers a clock output that may be routed directly to the MAC and act as the MAC reference clock, eliminating the need, and hence space and cost, of an additional MAC clock source. In MII mode, the clock output is 25 MHz and in RMII mode, it is 50 MHz clock. The DP83848M has a 25MHz_OUT pin, while the DP83848J does not.

4.6 Power Down and Interrupt

DP83848C offers a separate, multifunction pin to allow the system to power down the device, or to indicate an interrupt. In Power_Down mode, the PWR_DOWN/INT pin (pin 7) may be asserted low to put the device in a power down state. In Interrupt mode, this pin is an open drain output and will be asserted low when an interrupt condition occurs, based on various criteria defined by the MISR and MICR registers. It is recommended to use an external pull-up resistor for proper operation of the interrupt function.

The interrupt functionality is not available in the DP83848J/M. The Power Down functionality is only available through register access in the DP83848J/M.

5 References

For additional information on these devices, please refer to the applicable datasheet(s).

- *DP83848C PHYTER Commercial Temperature Single Port 10/100 Mb/s Ethernet Physical Layer Transceiver* (SNOSAT2)
- *DP83848J PHYTER Mini LS Commercial Temperature Single Port 10/100 Mb/s Ethernet Transceiver* (SNLS250)
- *DP83848M PHYTER Mini - Commercial Temperature Single 10/100 Ethernet Transceiver* (SNLS227)

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Appendix A Pin Map

Table 10. DP83848C and DP83848J/M Pin Map

Signal Name	DP83848C Pin #	DP83848J/M Pin #	Description
MII Interface Pins:			
MDC	31	25	MGMT DATA CLOCK
MDIO	30	24	MGMT DATA I/O
RXD0:3/PHYAD1:4	43,44,45,46	36,37,38,39	MII RX DATA
RX_CLK	38	31	MII RX CLOCK
RX_ER/MDIX_EN	41	34	MII RX ERROR
RX_DV/MII_MODE	39	32	MII RX DATA VALID
TXD0:3	3,4,5,6	4,5,6,7	MII TX DATA
TX_CLK	1	2	MII TX CLOCK
TX_EN	2	3	MII TX ENABLE
COL/PHYAD0	42	35	MII COL DETECT
CRS/LED_CFG	40	33	MII CARRIER SENSE
PMD Interface Pins:			
RD ±	13,14	11,12	RX DATA
TD ±	16,17	14,15	TX DATA
Clock Interface Pins:			
X1	34	28	XTAL/OSC INPUT
X2	33	27	XTAL OUTPUT
LED Interface Pins:			
LED_ACT/COL/AN_EN	26	n/a	COL LED STATUS
LED_ACT/COL/AN_EN	26	n/a	DUPLEX LED STATUS
LED_LINK/AN_0	28	22	LINK LED STATUS
LED_SPEED/AN_1	27	21 (J) n/a (M)	SPEED LED STATUS
LED_ACT/COL/AN_EN	26	n/a	ACT LED STATUS
JTAG Interface Pins:			
TCK	8	n/a	TEST CLOCK
TDO	9	n/a	TEST DATA OUTPUT
TMS	10	n/a	TEST MODE SELECT
TRST	11	n/a	TEST RESET
TDI	12	n/a	TEST DATA INPUT
Reset Function Pin:			
RESET_N	29	23	RESET
Strap Pins:			
PHYAD0:4	42,43,44,45,46	35,36,37,38,39	PHY ADDRESS
MDIX_EN/RX_ER	41	34	AUTO MDIX ENABLE
MII_MODE/RX_DV	39	32	MII MODE SELECT
SNI_MODE/TXD3	6	n/a	MII MODE SELECT
LED_CFG/CRS	40	20	LED CONFIGURATION
Bias Function Pin:			
RBIAS	24	20	BIAS RESISTOR CONNECTION

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Table 10. DP83848C and DP83848J/M Pin Map (continued)

Signal Name	DP83848C Pin #	DP83848J/M Pin #	Description
Test Mode Pins:			
AN_0/LED_LINK	28	22	TEST MODE SELECT
AN_1/LED_SPEED	27	21 (J) n/a (M)	TEST MODE SELECT
AN_EN/LED_ACT/COL	26	n/a	TEST MODE SELECT
Special Function Pins:			
25MHz_OUT	25	n/a (J) 21 (M)	25 MHz CLOCK OUTPUT
PWR_DOWN/INT	7	n/a	POWER DOWN/INT
PFBIN1	18	16	POWER FEEDBACK IN
PFBIN2	37	30	POWER FEEDBACK IN
PFBOUT	23	19	POWER FEEDBACK OUT
Supply Pins:			
VDD	22,32,48	1,18,26	3.3 V
GND	15,19,35,36,47	13,17,29,40	GROUND
Reserved Pins:			
RESERVED	8,9,10,11,12,20	8,9,10	RESERVED

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Appendix B Register Differences

This appendix covers differences between the registers in DP83848C and DP83848J/M applicable to software configuration of these devices.

IEEE specified registers of Texas Instruments Physical Layer devices comply with the respective IEEE standards. Only vendor specific registers have functions that may vary from device to device. If no vendor specific registers are modified for operation in the system application, the devices will have similar operation. Specific functions of these vendor defined registers may be available in another register or possibly in a different bit within the same register location.

Table 11. Register Bit Definitions

Register Address	Register Name	Register Description	Device	
			DP83848C	DP83848J/M
10h	PHYSTS	PHY Status Register	Bit 7 MII Interrupt	Bit 7 Reserved
11h	MICR	MII Interrupt Control Register	Bit 2 TINT	Bit 2 Reserved
			Bit 1 INTEN	Bit 1 Reserved
			Bit 0 INT_OE	Bit 0 Reserved
12h	MISR	MII Interrupt Status Register	Bit 14 ED_INT	Bit 14 Reserved
			Bit 13 LINK_INT	Bit 13 Reserved
			Bit 12 SPD_INT	Bit 12 Reserved
			Bit 11 DUP_INT	Bit 11 Reserved
			Bit 10 ANC_INT	Bit 10 Reserved
			Bit 9 FHF_INT	Bit 9 Reserved
			Bit 8 RHF_INT	Bit 8 Reserved
			Bit 6 UNMSK_ED	Bit 6 Reserved
			Bit 5 UNMSK_LINK	Bit 5 Reserved
			Bit 4 UNMSK_JAB	Bit 4 Reserved
			Bit 3 UNMSK_RF	Bit 3 Reserved
			Bit 2 UNMSK_ANC	Bit 2 Reserved
			Bit 1 UNMSK_FHF	Bit 1 Reserved
			Bit 0 UNMSK_RHF	Bit 0 Reserved
16h	PCSR	PCS Sub-Layer Configuration and Status Register	bit 12 BYP_4B5B	Bit 12 Reserved
18h	LEDCR	LED Direct Control Register	Bit 5 DRV_SPDLED	Bit 5 Reserved (M)
			Bit 3 DRV_ACTLED	Bit 3 Reserved
			Bit 2 SPDLED	Bit 2 Reserved (M)
			Bit 0 ACTLED	Bit 0 Reserved
19h	PHYCR	PHY Control Register	Bit 6 LEDCNFG[1]	Bit 6 Reserved
1Ah	10BT_SERIAL	10Base-T Status/Control Register	Bit 15 10BT_SERIAL	Bit 15 Reserved
			Bit 14 REJECT 100 BASE T	Bit 14 Reserved
			Bits 13:12 ERROR RANGE	Bits 13:12 Reserved

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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