User's Guide

LMK04368EPEVM User's Guide

ABSTRACT

The LMK04368EPEVM (EVM) is designed to evaluate the performance and features of the LMK04368-EP high performance Ultra-Low-Noise JESD204B Dual-Loop Clock Jitter Cleaner from Texas Instruments. The user's guide describes how to set up and operate the EVM. The LMK04368-EP device on each EVM is an Engineering Model, intended for engineering evaluation only.

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Trademarks

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1 Evaluation Board Kit Contents

Table 1-1 lists the components found in the evaluation board kit.

Table 1-1. EVM Contents

HSDC141	
Evaluation Board	LMK04368EPEVM Evaluation Board with VCXO (1)
USB cable	USB Cable A Plug to Micro B Plug cable (1)

2 Quick Start

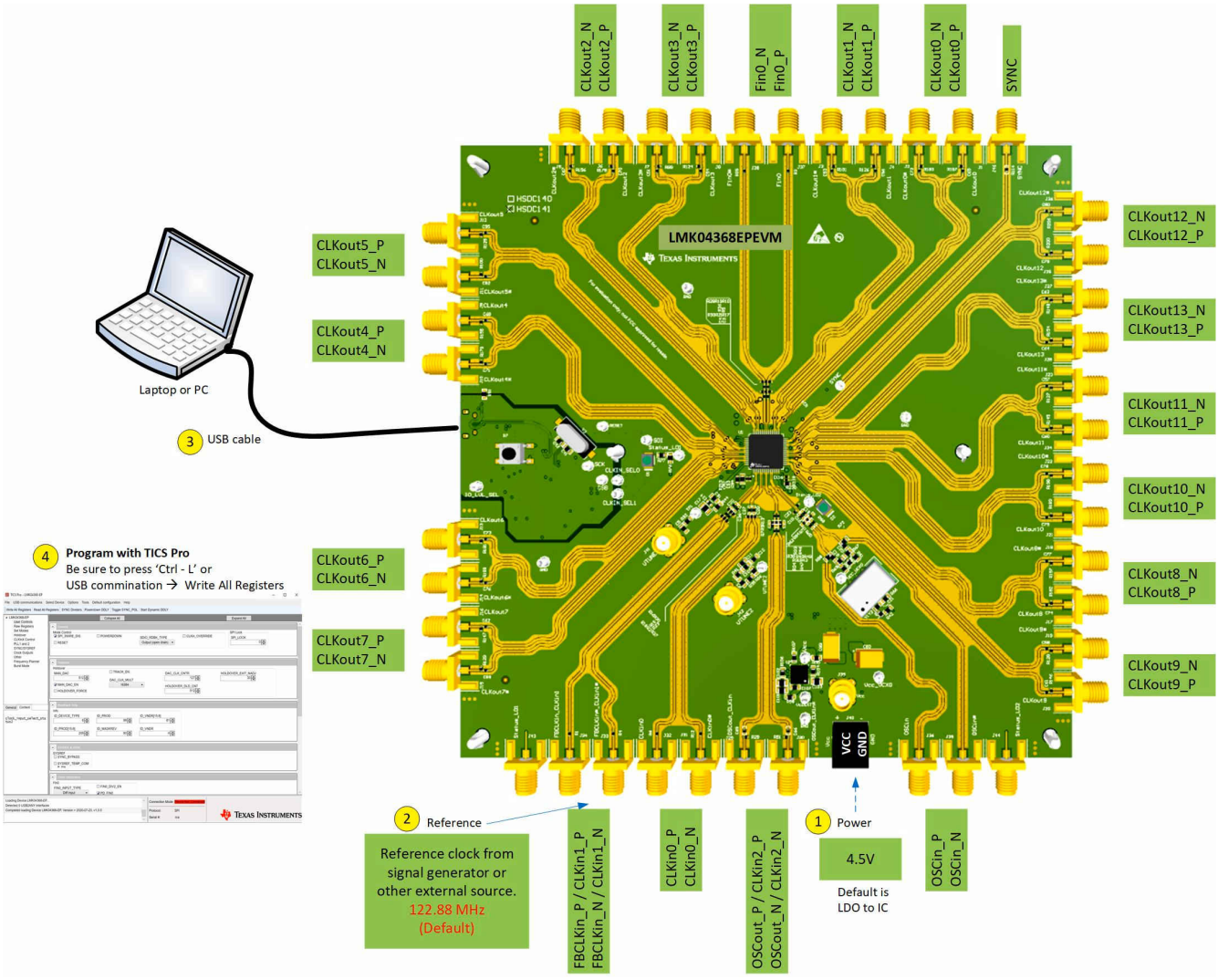

Figure 2-1. Quick Start Diagram

Related information: http://www.ti.com/tool/ticspro-sw

2.1 Quick Start Description

The LMK04368EP EVM allows full verification of the device functionality and performance specifications. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 2-1.

1. Connect a voltage of 4.5 V to the V_{CC} SMA connector or terminal block. The LMK04368-EP and onboard VCXO operate at 3.3 V provided by the onboard TPS7A4701-EP LDO and LP5900 LDO, respectively.

2. Connect a reference clock to the CLKin1* port from a signal generator or other source. Use 122.88 MHz for the default configuration.
3. Connect a USB Cable A Plug to Micro B Plug cable to a PC and the USB connector (J45) at EVM.
4. Program the device with TICS Pro. TICS Pro is available for download at: http://www.ti.com/tool/ticspro-sw.
   a. Select *LMK04368-EP* from the *Select Device* menu. Click *Select Device → Clock Generator/Jitter Cleaner (Dual Loop)*.
   b. Select *USB2ANY mode* from the *Communication Setup* window. To access this, select *USB communications → Interface*. Click *Identify* to confirm that the PC to USB communication is working. A blinking green LED on the USB2ANY indicates the PC is able to communicate through the USB2ANY.
   c. Select a default mode from the *Default Configuration* menu. For the quick start, use: CLKin1 122.88 MHz, OSCin 122.88 MHz, VCO1 2949.12 MHz.
   d. Press *Ctrl+L* at least once to load all registers. Alternatively, click the *USB communications → Write All Registers* menu, the *Write All Registers* button on toolbar, or the *Raw Registers* page (see Section 11.3).
5. Measurements may be made at an active CLKout port through the SMA connector.

2.1.1 Clock Outputs Page Description

Clock outputs are grouped in pairs. This description applies for all clock outputs on the *Clock Outputs* page of the TICS Pro GUI (see Section 11.9).

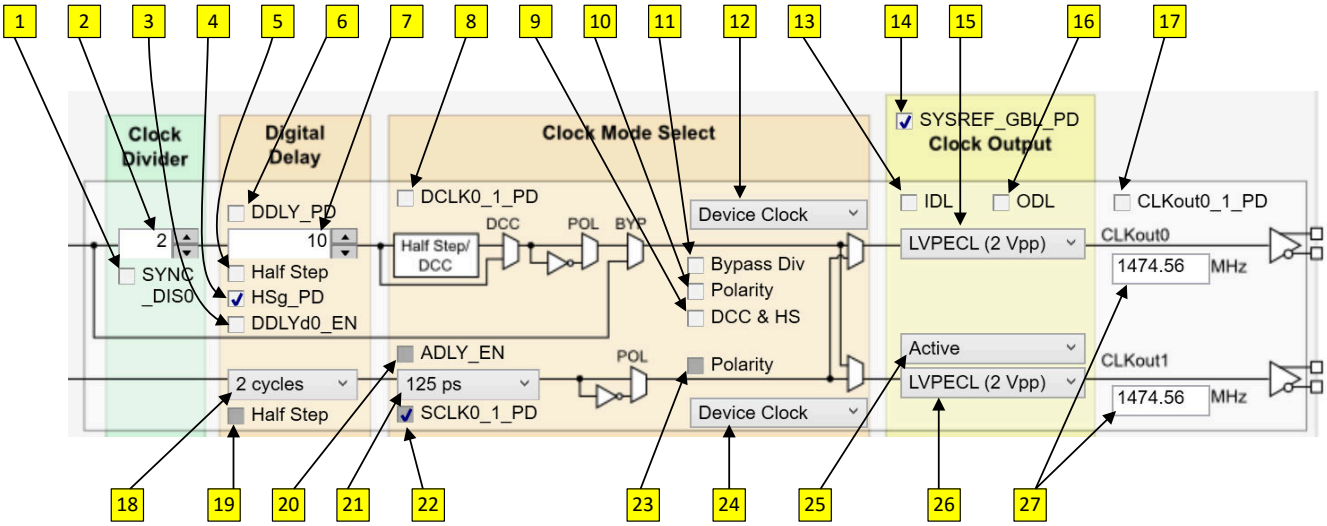

Figure 2-2. Clock Outputs Page Description Diagram

1. SYNC_DISX: Prevent the divider from being reset by SYNC/SYSREF path.
2. DCLKX_Y_DIV: Divide value for the device clock. If set to 1, then DCLKX_Y_DCC (DCC & HS) must = 1.
3. DDLYdX_EN: Enable dynamic digital delay for this divider.
4. DCLKX_Y_HSg_PD: If clear, glitchless half-step adjustments are enabled.
5. DCLKX_Y_HS: Set half step for this divider. DCLKX_Y_DCC (DCC & HS) must = 1.
6. DCLKX_Y_DDLY_PD: If clear, the digital delay value is assured when a SYNC occurs.
7. DCLKX_Y_DDLY: The digital delay value to be used when a SYNC occurs.
8. DCLKX_Y_PD: Power down the device clock divider and path.
9. DCLKX_Y_DCC: Enable duty cycle correct and half-step for this device clock divider.
10. DCLKX_Y_POL: If set, polarity of device clock is inverted.
11. DCLKX_Y_BYP: If set, the device clock divider is bypassed for CLKoutX and #15 must be CML.
12. CLKoutX_SRC_MUX: Select device clock or SYSREF clock path for CLKoutX.
13. CLKoutX_Y_IDL: Increase input drive level to improve noise floor at cost of power (approximately 2 mA).
14. SYSREF_GBL_PD: Set the conditional for SCLKX_Y_DIS_MODE registers.
15. CLKoutX_FMT: Set the clock output format for CLKoutX.
16. CLKoutX_Y_ODL: Increase output drive level to improve noise floor at cost of power (approximately 3 mA). No effect for CLKoutX in bypass mode.
17. CLKoutX_Y_PD: Power down the entire CLKoutX_Y clock pair.
18. SCLKX_Y_DDLY: The SYSREF clock digital delay setting.

19. SCLKX_Y_HS: Set half step for the SYSREF output.
20. SCLKX_Y_ADLY_EN: Enable analog delay for the SYSREF clock path.
21. SCLKX_Y_ADLY: If enabled, set the analog delay for the SYSREF clock path.
22. SCLKX_Y_PD: Power down the SYSREF clock path.
23. SCLKX_Y_POL: If set, polarity of SYSREF output clock is inverted.
24. CLKoutY_SRC_MUX: Select device clock or SYSREF clock path for CLKoutY.
25. SCLKX_Y_DIS_MODE: Set the output state of output clock drivers for the SYSREF clock. For values of 1 and 2 works in conjunction with control on this list #14, SYSREF_GBL_PD.
26. CLKoutY_FMT: Set the clock output format for CLKoutY.
27. Clock output frequency for CLKoutX and CLKoutY.

2.1.2 TICS Pro Tips

Mousing over different controls will display a help prompt with the register address, the data bit location and length, and a brief register description in the lower-left *Context* help pane.

You can set a register equal to 0 or uncheck a register's checkbox to perform the same action. Similarly, setting a register equal to 1 is the same as checking that register's checkbox.

3 PLL Loop Filters and Loop Parameters

In jitter cleaning applications that use a cascaded or dual PLL architecture, the first PLL's purpose is to substitute the phase noise of a low-noise oscillator (VCXO) for the phase noise of a dirty reference clock. The first PLL is typically configured with a narrow loop bandwidth to minimize the impact of the reference clock phase noise. The reference clock consequently serves only as a frequency reference rather than a phase reference.

The loop filters on the LMK04368EPEVM evaluation board are set up using the approach above. The loop filter for PLL1 has been configured for a narrow loop bandwidth (< 1 kHz). The specific loop bandwidth values depend on the phase noise performance of the oscillator mounted on the board. Table 3-1 and Table 3-2 contain the parameters for PLL1 and PLL2 for each oscillator option.

TI's PLLatinum™ Simulation tool can be used to optimize PLL phase noise/jitter for given specifications. See http://www.ti.com/tool/pllatinumsim-sw for more information.

3.1 PLL1 Loop Filter

Table 3-1. PLL1 Loop Filter Parameters for Crystek 122.88 MHz VCXO

122.88 MHz VCXO PLL(1)			
Phase Margin	50°	Kφ (Charge Pump)	450 µA
Loop Bandwidth	14 Hz	Phase Detector Freq	1.024 MHz
		VCO Gain	2.5 kHz/V
Reference Clock Frequency	122.88 MHz	Output Frequency	122.88 MHz (To PLL 2)
Loop Filter Components	LF1_C1 (C31) = 100 nF	LF1_C2 (C14) = 680 nF	LF1_R2 (R44) = 39 kΩ

(1) Loop Bandwidth is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N will change the loop bandwidth.

3.2 PLL2 Loop Filter

Table 3-2. Integrated VCO PLL

PARAMETER(1)	LMK04368-EP		UNIT
	VCO0	VCO1	
LF2_C1 (C12)	0.047		nF
LF2_C2 (C10)	3.9		nF
C3 (internal)	0.03		nF
C4 (internal)	0.01		nF
LF2_R2 (R41)	0.62		kΩ
R3 (internal)	0.2		kΩ
R4 (internal)	0.2		kΩ
Charge Pump Current, Kφ	3.2		mA

Table 3-2. Integrated VCO PLL (continued)

PARAMETER(1)	LMK04368-EP		UNIT
	VCO0	VCO1	
Phase Detector Frequency	122.88		MHz
Frequency	2457.6	2949.12	MHz
Kvco	13.0	25.0	MHz/V
N	20	24	
Phase Margin	68	71	degrees
Loop Bandwidth	210	326	kHz

(1) PLL Loop Bandwidth is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N will change the loop bandwidth.

4 Default TICS Pro Mode

TICS Pro saves the state of the selected LMK04368-EP device when exiting the software. Table 4-1 lists the default mode for the software. To ensure a common starting point, go to the *Default Configuration* menu and select the appropriate device configuration for your device.

Table 4-1. Default TICS Pro Modes for the LMK04368-EP

DEFAULT TICS PRO MODE	DEVICE MODE	CLKin FREQUENCY	OSCin FREQUENCY
CLKin1 122.88 MHz, OSCin 122.88 MHz, VCO1 2949.12 MHz	Dual PLL, Internal VCO	122.88 MHz	122.88 MHz

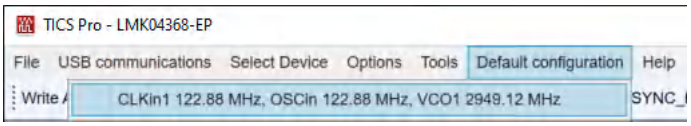

Figure 4-1. Selecting a Default Mode for the LMK04368-EP Device

5 Using TICS Pro to Program the LMK04368-EP

This section will demonstrate how to use TICS Pro. For more information on using TICS Pro, refer to Appendix A. TICS Pro is available for download at http://www.ti.com/tool/ticspro-sw.

Before proceeding, be sure to follow the instructions in Section 2 to ensure proper hardware connections.

5.1 Start TICS Pro Application

Click *Start* → *Programs* → *Texas Instruments* → *TICS Pro*.

The TICS Pro program is installed by default to the Texas Instruments application group.

5.2 Select Device

Click *Select Device* → *Clock Generator/Jitter Cleaner (Dual Loop)* → *LMK04368-EP*.

After start-up, the TICS Pro will load to the last used device. A recent history of used devices can be quickly accessed under the *File* menu. To load a new device, click *Select Device* from the menu bar, select the subgroup, then select the device to load.

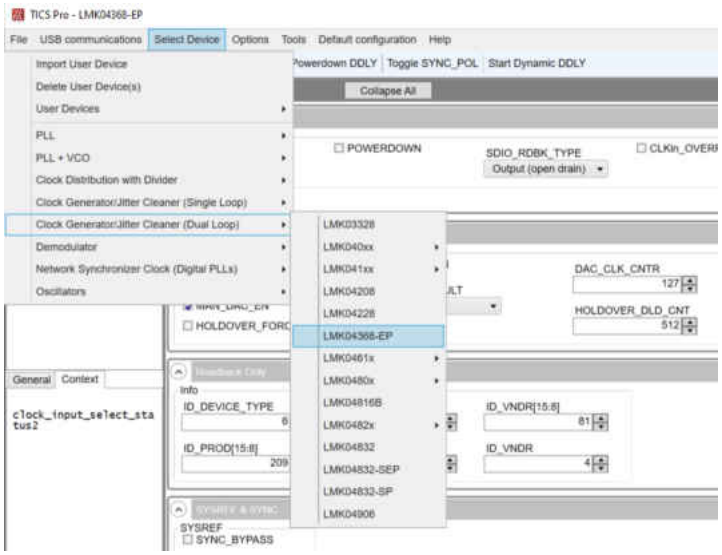

Figure 5-1. Selecting the LMK04368-EP

5.3 Program the Device

To program, press *Ctrl+L*.

Alternatively, click *USB communications* → *Write All Registers* from the menu to program the device to the current state of the register map to the device. *Ctrl+L* is the accelerator key assigned to the *Write All Registers* option and is very convenient.

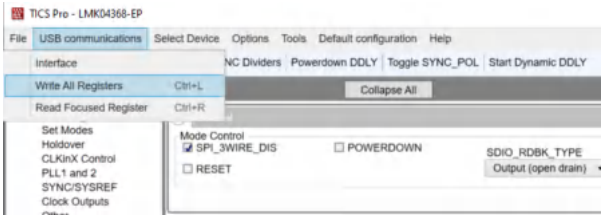

Figure 5-2. Loading the Device

After the device is initially loaded, TICS Pro will automatically program changed registers, so it is not necessary to reload the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the *Options* → *AutoUpdate*.

A default mode will be restored in the next step, therefore this step is not necessary. It is included, however, to emphasize the importance of pressing Ctrl+L to load the device at least once after starting TICS Pro, restoring a mode, or restoring a saved setup using the *File* menu.

See TICS Pro instructions located at http://www.ti.com/tool/ticspro-sw/.

5.4 Restoring a Default Mode

Click *Default configuration* → *CLKin1 122.88 MHz, OSCin 122.88 MHz, VCO1 2949.12 MHz*. Press *Ctrl+L* to restore the default configuration.

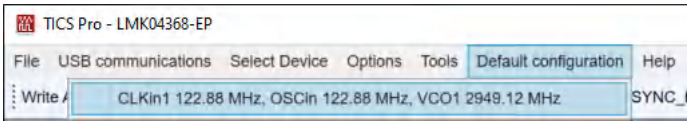

Figure 5-3. Setting the Default Configuration for LMK04368-EP

For the purpose of this walkthrough, a default mode will be loaded to ensure a common starting point. This is important because when TICS Pro is closed, the software remembers the last settings used for a particular device. Again, remember to press *Ctrl+L* as the first step after loading a default mode.

5.5 Visual Confirmation of Frequency Lock

After a default mode is restored and loaded, LED D1 and D2 must illuminate when PLL1 and PLL2 are locked to the reference clock applied to CLKin1. This assumes PLL1_LD_MUX = PLL1_DLD, PLL2_LD_MUX = PLL2_DLD, and PLLX_LD_TYPE = Output (Push-Pull).

5.6 Enable Clock Outputs

The LMK04368-EP offers programmable clock output buffer formats, the evaluation board is shipped with pre-configured output terminations. Refer to Table 6-1 to see the list of output formats available and what output formats your hardware is configured for out of the factory.

To measure phase noise at one of the clock outputs (for example, CLKout0):

1. Go to the *Clock Outputs* page (Section 11.9).
2. Uncheck *CLKoutX_Y_PD* in the *Clock Output* box to enable the channel.
3. Set the following as needed:
    a. For Device Clock:
        i. DCLKX_Y_PD = 0 in *Clock Mode Select* box
        ii. Set Bypass Div (DCLKX_Y_BYP) or Clock Divider (DCLK0_1_DIV) as desired for device clock frequency:
            1. If bypass mode is set, CLKoutX must be set to a CML output format. Bypass mode is not available on CLKoutY.
            2. If Clock Divider = 1, then DCLKX_Y_DCC must be set for clock output.
        iii. Phase of the device clock can be adjusted with:
            1. Static Digital delay (DCLKX_Y_DDLY) after a SYNC. Digital Delay (DCLKX_Y_DDLY_PD) must be powered up.
            2. Dynamic Digital delay (DDLYdX_EN), then programming DDLYd_STEP_CNT. Digital Delay (DCLKX_Y_DDLY_PD) must be powered up. Press the *Send* button at top-right of *Clock Outputs* window to program the DDLYd_STEP_CNT field multiple times.
            3. Half Step bit (DCLKX_Y_HS) if DCC & HS (DCLKX_Y_DCC) is set.
            4. The Polarity bit (DCLKX_Y_POL)
        iv. Select the device clock for CLKoutX or CLKoutY with CLKout#_SRC_MUX = 0 (Device Clock) as desired.
    b. While the phase noise of a SYSREF Clock is typically not of concern, to configure an output for SYSREF:
        i. SCLKX_Y_PD = 0 in *Clock Mode Select* box
        ii. Phase of the SYSREF clock can be adjusted:
            1. Local digital delay can be set with SCLKX_Y_DDLY.
            2. Local analog delay can be set by enabling with ADLY_EN = 1 (SCLKX_Y_ADLY_EN) and then setting SCLKX_Y_ADLY to the desired time delay.
            3. Global digital delay can be set with SYSREF_DDLY, but this delay change will take effect only after a SYNC.
        iii. Enable SYSREF outputs globally. The necessary bits depend upon the type of SYSREF to be enabled. For a simple continuous SYSREF (not recommended in final application due to extra power consumption and crosstalk), set SYSREF_PD = 0, SYSREF_MUX = 0x03 (Continuous), and SYNC_DISSYSREF = 1.

iv. Select the SYSREF clock for CLKoutX or CLKoutY with CLKout#_SRC_MUX = 1 (SYSREF) as desired.

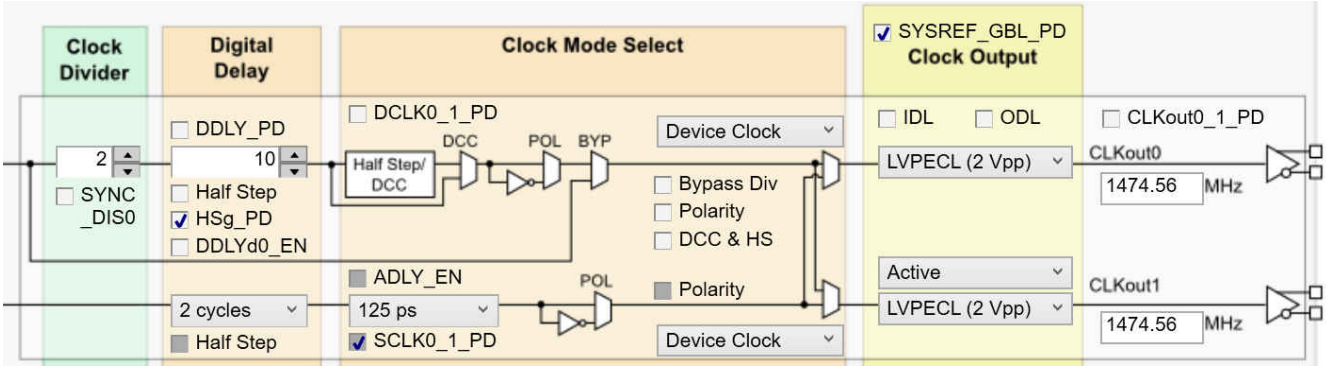

Figure 5-4. Setting Digital Delay, Clock Divider, Analog Delay, and Output Format

4. Depending on the configured output type, the clock output SMAs can be interfaced to a test instrument with a single-ended, 50-Ω input as follows:
   a. For LVDS:
      i. A balun (like ADT2-1T or a high-quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
   b. For LVPECL:
      i. A balun can be used, or
      ii. One side of the LVPECL signal can be terminated with a 50-Ω load and the other side can be run single-ended to the instrument.
   c. For HSDS:
      i. A balun (like ADT2-1T or high-quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
   d. For CML:
      i. A balun can be used, or
      ii. One side of the CML signal can be terminated with a 50-Ω load and the other side can be run single-ended to the instrument.
   e. For LVCMOS:
      i. Connect the LVCMOS signal to measurement equipment as desired. If an output of a pair is not used, TI recommends leaving the output floating close to the IC. Alternatively, place a 50-Ω termination at the end of an unused trace.
5. The phase noise may be measured with a spectrum analyzer or signal source analyzer.

6 Evaluation Board Inputs and Outputs

Table 6-1 contains descriptions of the inputs and outputs for the evaluation board. Additionally, some applicable TICS Pro programming controls are noted for convenience.

Table 6-1. Description of Evaluation Board Inputs and Outputs

<table>
<tr><th>CONNECTOR NAME</th><th>SIGNAL TYPE, INPUT/OUTPUT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="2">Clock Outputs
Populated:
CLKout0_P(J1),
CLKout0_N(J2),
CLKout1_P(J3),
CLKout1_N(J4),
CLKout2_P(J6),
CLKout2_N(J5),
CLKout3_P(J8),
CLKout3_N(J7),
CLKout4_P(J9),
CLKout4_N(J10),
CLKout5_P(J12),
CLKout5_N(J11),
CLKout6_P(J13),
CLKout6_N(J14),
CLKout7_P(J16),
CLKout7_N(J15),
CLKout8_P(J17),
CLKout8_N(J18),
CLKout9_P(J20),
CLKout9_N(J19)</td><td rowspan="2">Analog, Output</td><td colspan="2">Clock outputs with programmable output buffers.
The output terminations by default on the evaluation board are shown here:
Clock Output Pair | Default Board Termination
CLKout0 | LVPECL / LCPECL, 240 Ω
CLKout1 | LVPECL / LCPECL, 240 Ω
CLKout2 | LVPECL / LCPECL, 120 Ω
CLKout3 | LVPECL / LCPECL, 120 Ω
CLKout4 | CML, 68 nH - 20 Ω
CLKout5 | CML, 50 Ω to Vcc
CLKout6 | CML, 68 nH - 20 Ω
CLKout7 | CML, 50 Ω to Vcc
CLKout8 | LVDS / HSDS
CLKout9 | LVDS / HSDS</td></tr>
<tr><td>Not Populated:
CLKout10_P(J21),
CLKout10_N(J22),
CLKout11_P(J24),
CLKout11_N(J23),
CLKout12_P(J25),
CLKout12_N(J26),
CLKout13_P(J28),
CLKout13_N(J27)</td><td colspan="2">Each CLKout pair has a programmable LVDS, LVPECL, LCPECL, HSDS, CML, or LVCMOS buffer. The output buffer type can be selected in the TICS Pro under the Clock Outputs page (Section 11.9) through the CLKoutX_FMT control. All clock outputs are AC-coupled to allow safe testing with RF test equipment. If an output pair is programmed to LVCMOS, each output can be independently configured (normal, inverted, or off/tri-state). Best performance/EMI reduction is achieved by using a complementary output mode like Norm/Inv. TI does NOT recommend using Norm/Norm or Inv/Inv mode.</td></tr>
<tr><td>OSCout
OSCout_P(J29)
OSCout_N(J30)</td><td>Analog, Output</td><td colspan="2">Buffered outputs of OSCin port.
The output terminations on the evaluation board are shown here.:
OSC Output Pair | Default Board Termination
OSCout | LVPECL, 240 Ω
OSCout has a programmable LVDS, LVPECL, or LVCMOS output buffer. The OSCout buffer type can be selected in the TICS Pro under the Clock Outputs page (Section 11.9) through the OSCout_FMT control.
OSCout is AC-coupled to allow safe testing with RF test equipment. If OSCout is programmed as LVCMOS, each output can be independently configured (normal, inverted, inverted, and off/tri-state). Best performance/EMI reduction is achieved by using a complementary output mode like Norm/Inv. TI does NOT recommend using Norm/Norm or Inv/Inv mode.</td></tr>
</table>

Table 6-1. Description of Evaluation Board Inputs and Outputs (continued)

CONNECTOR NAME	SIGNAL TYPE, INPUT/OUTPUT	DESCRIPTION
Power VccEXT(J39/J40/TP13) Vcc(TP12)	Power, Input	Main power supply input for the evaluation board. The LMK04368EPEVM default is setup to use the TPS7A4701-EP voltage regulator. This is a space grade (SEP) voltage regulator. 0-Ω resistors R93, R98 and R104 can be re-configured to route power through the on-board EP grade LDO, the TPS7A4701-EP. The LMK04368-EP contains internal voltage regulators for the VCO and other internal blocks. The clock outputs do not have an internal regulator, so a clean power supply with sufficient output current capability is required for optimal performance. If using an external voltage please ensure the voltage is filtered to get the best performance on the outputs. Apply power to either Vcc SMA(J39) or terminal block(J40), but not both.
Clock Inputs CLKin0_P(J32), CLKin0_N(J31), CLKin1_P(J34), CLKin1_N(J33) OSCout_P(J29), OSCout_N(J30) Fin0_P(J37), Fin0_N(J38)	Analog, Input	Reference Clock Inputs for PLL1 or PLL1 (CLKin0, CLKin1, CLKin2) CLKin1_N is configured by default for a single-ended reference clock input from a 50-Ω source. The non-driven input pin CLKin1_P can be configured as R15 - DNI and R216 replace with 0-Ω resistor. CLKin0 is configured by default for a differential reference clock input from a 50-Ω source. CLKin1 is the default reference clock input selected in the TICS Pro. If OSCout is to be used as a CLKin2, then the PCB must be updated to operate as an input instead of an output.
		Clock Distribution with Fin0 or CLKin1/Fin1 Fin0 and CLKin1 (Fin1) are shared for use as an RF Input for Clock Distribution mode or for an external VCO mode.
		External Feedback Input (FBCLKin) for 0-Delay CLKin1 is shared for use as an external feedback clock input (FBCLKin) to PLL1 N or PLL2 N for 0-delay mode. Refer to the LMK04368-EP data sheet for more details on using 0-delay mode with the evaluation board and the evaluation board software.
OSCin, PLL2 reference/PLL1 feedback OSCin_P(J36), OSCin_N(J35)	Analog, Input	Feedback VCXO clock input to PLL1 and Reference clock input to PLL2. The single-ended output of the onboard VCXO (Y1/Y2) drives the OSCin_N input of the device and the OSCin_P input of the device is connected to GND with 0.1 µF. VCXO Y1 and Y2 may also be used with differential VCXOs. An external VCXO may be optionally attached through these SMA connectors with minor modification to the components going to the OSCin pins of device. A single-ended or differential signal may be used to drive the OSCin pins and must be AC coupled. If operated in single-ended mode, the unused input must be connected to GND with 0.1 µF. Refer to the LMK04368-EP data sheet *Electrical Characteristics* table for PLL2 Reference Input (OSCin) specifications.
VCO Tuning Voltages VTUNE1 (TP1/J41) VTUNE2 (TP2/J42)	Analog, Input/Output	Tuning voltage output from the loop filter for PLL1 and PLL2 of the LMK04368-EP. If an external VCXO is used, this tuning voltage can be connected to the voltage control pin of the external VCXO. The default board does not come with J41 and J42 populated.

Table 6-1. Description of Evaluation Board Inputs and Outputs (continued)

<table>
<tr><th>CONNECTOR NAME</th><th>SIGNAL TYPE, INPUT/OUTPUT</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="6">USB Connector
USB connector (J45)
SPI / GPIO Test points
SDIO (TP11),
SCK (TP8),
CS* (TP4),
CLKin_SEL0(TP9),
CL Kin_SEL1(TP5).
RESET(TP16),</td><td rowspan="6">CMOS, Input/Output</td><td>USB connector to program onboard USB2ANY device and configure the LMK04368-EP device through SPI interface.
SPI signals include SDIO (TP11), SCK (TP8) and CS* (TP4) test points.
The programmable logic I/O signals accessible through this header include: RESET (TP16), SYNC (TP10/J46), CLKin_SEL0 (TP9), and CLKin_SEL1 (TP5).</td></tr>
<tr><td>Input Clock Switching – Pin Select Mode
By default CLKin_SEL0 and CLKin_SEL1 are input pins.
To enable input clock switching, CLKin_SEL_AUTO_EN = 0, CLKin_SEL_PIN_EN = 1, CLKin_SEL_PIN_POL = 0, and Status_CLKinX_TYPE must be 0 to 3 (pin enabled as an input).
When CLKin_SEL_AUTO_EN = 0 and CLKin_SEL_PIN_EN = 1, the Status_CLKinX pins select which clock input is active as follows:</td></tr>
<tr><td><table>
<tr><th>CLKin_SEL1</th><th>CLKin_SEL10</th><th>Active Clock</th></tr>
<tr><td>0</td><td>0</td><td>CLKin0</td></tr>
<tr><td>0</td><td>1</td><td>CLKin1</td></tr>
<tr><td>1</td><td>0</td><td>CLKin2</td></tr>
<tr><td>1</td><td>1</td><td>Holdover</td></tr>
</table></td></tr>
<tr><td>SYNC
SYNC (TP10/J46)</td><td>CMOS, Input/Output</td><td>Programmable status I/O pin. By default, set as an input pin for synchronize the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC. A SYNC event also causes the digital delay values to take effect.
SYNC/SYSREF_REQ pin forces the SYSREF_MUX into SYSREF Continuous mode (0x03) when SYSREF_REQ_EN = 1.
SYNC/SYSREF_REQ pin can hold outputs in a low state, depending on system configuration. SYNC_POL adjusts for active low or active high control.
A SYNC event can also be programmed by toggling the SYNC_POL_INV bit in the SYNC/SYSREF page (Section 11.8) in the TICS Pro.</td></tr>
<tr><td>Status LEDs
Status_LD1(TP6),
Status_LD2(TP7)</td><td>CMOS, Input/Output</td><td>Programmable status output pin. By default, Status_LD1 and Status_LD2 are set to output the digital lock detect status signal for PLL1 and the digital lock detect status signal for PLL2, respectively. By the default TICS Pro configuration, LEDs will illuminate green when lock is detected (output is high) and turn off when lock is lost (output is low).</td></tr>
</table>

7 Recommended Test Equipment

Power Supply

The power supply must be a low-noise power supply, particularly when the devices on the board are being directly powered (onboard LDO regulators bypassed).

Phase Noise / Spectrum Analyzer

TI recommends that an Agilent E5052 Signal Source Analyzer or comparable test equipment is used to measure phase noise and RMS jitter.

Oscilloscope

To measure the output clocks AC performance, such as rise time or fall time, propagation delay, or skew, TI suggests using a real-time oscilloscope with 8+ GHz analog input bandwidth with 50-Ω inputs. To evaluate clock synchronization or phase alignment between multiple clock outputs, TI recommends using phase-matched, 50-Ω cables to minimize external sources of skew or other errors/distortion that may be introduced if using oscilloscope probes.

8 Schematics

The components on the EVM can be found on the following schematic by searching for their reference designators.

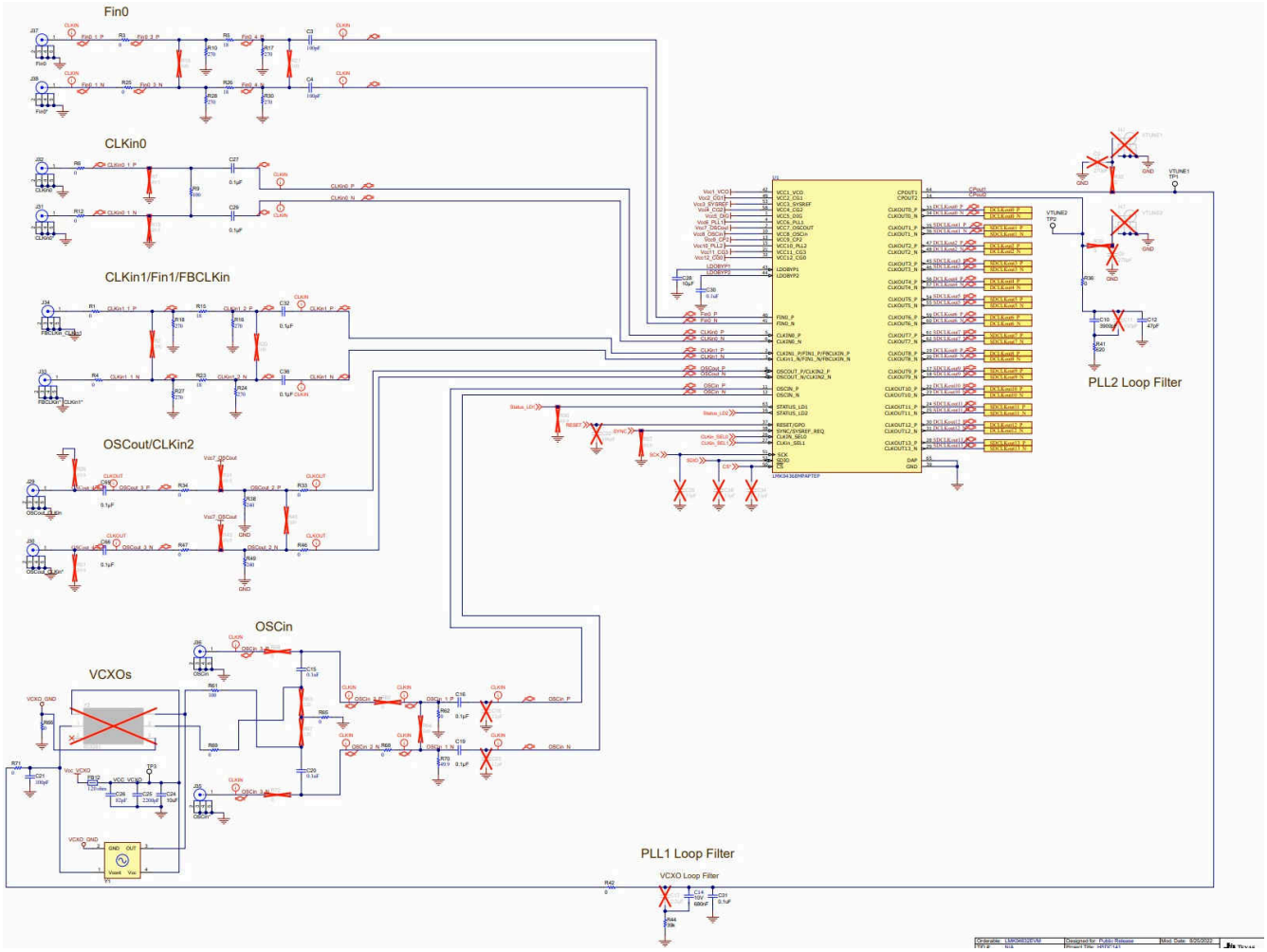

Figure 8-1. Schematic - LMK04368-EP

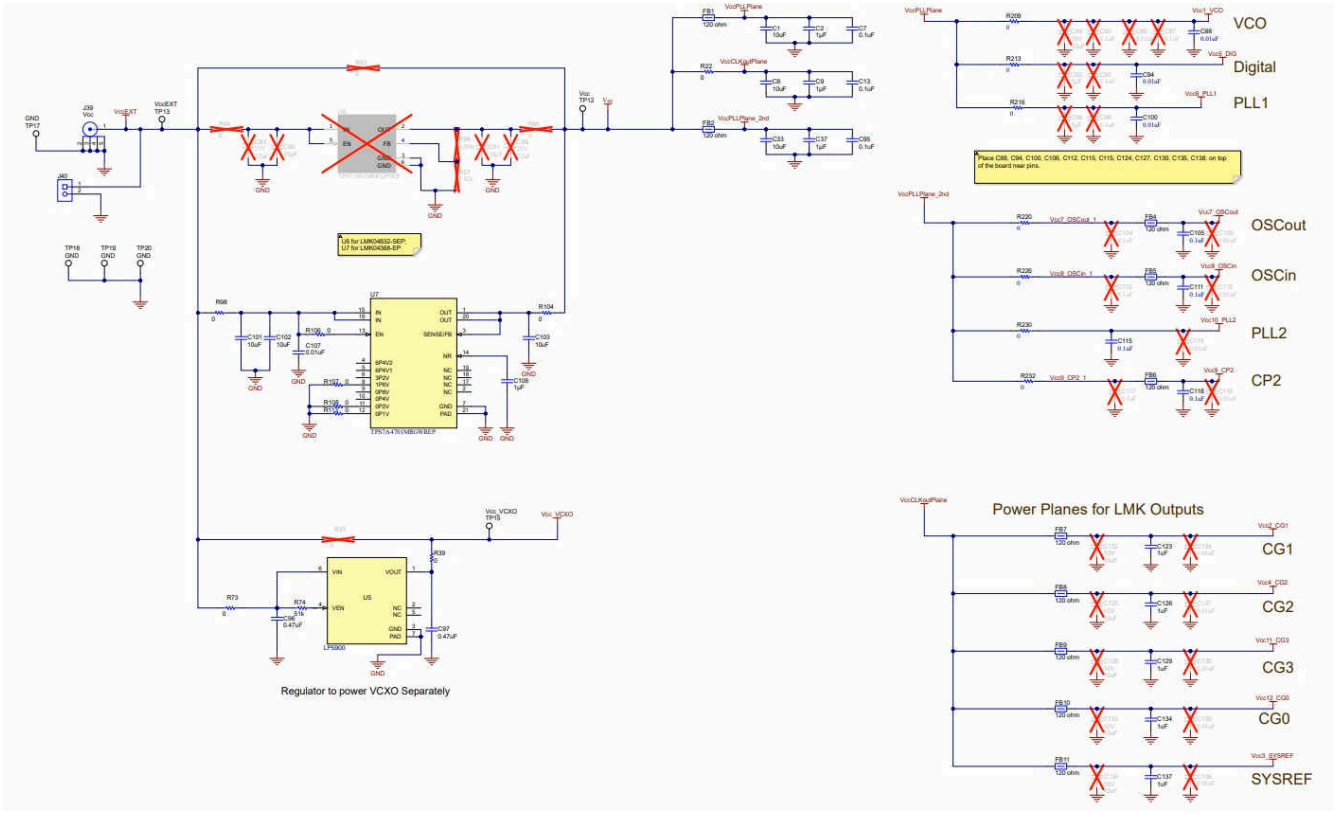

Figure 8-2. Schematic - Power Supply

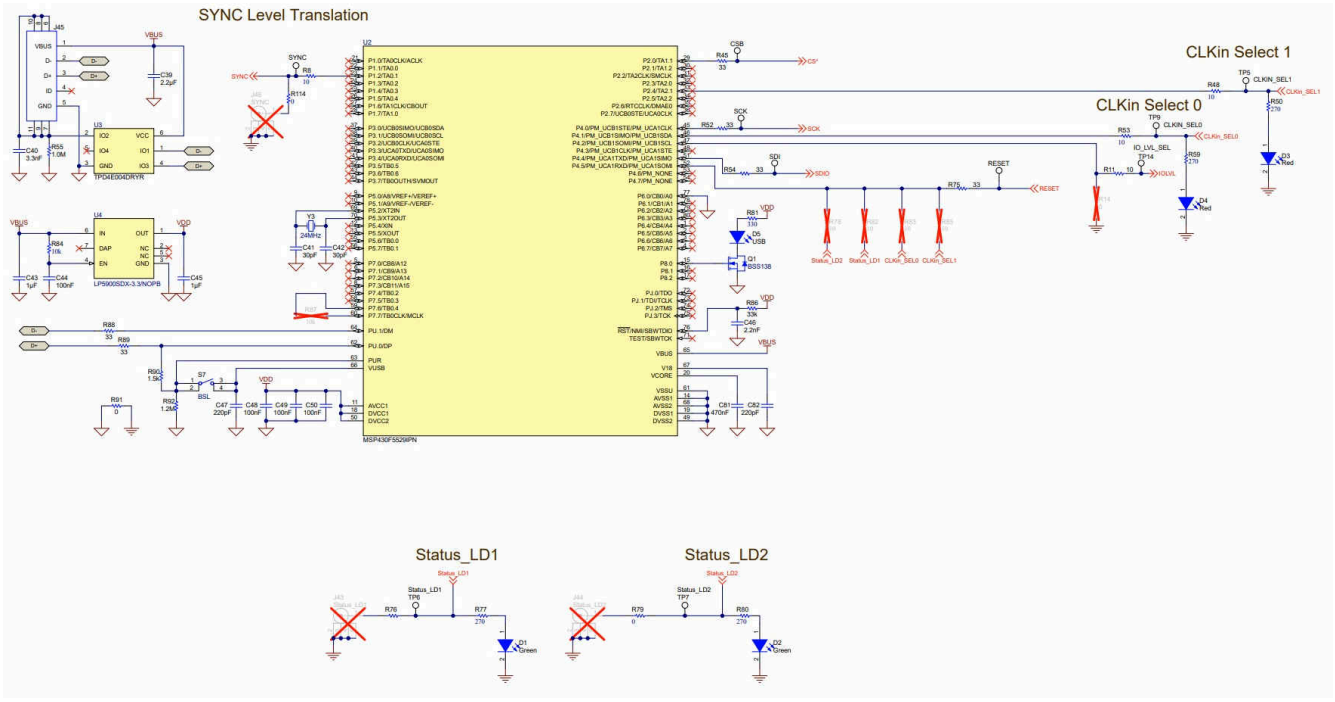

Figure 8-3. Schematic - Digital

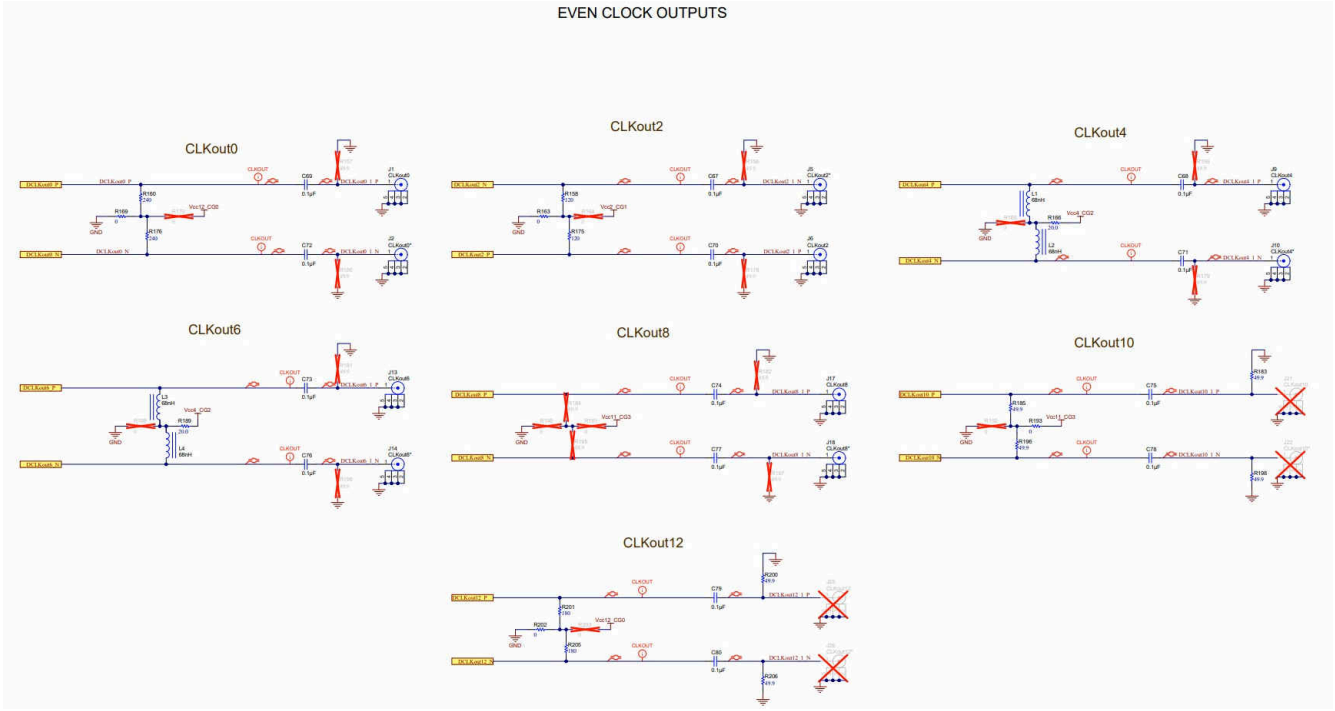

Figure 8-4. Schematic - Clock Outputs 1 of 2

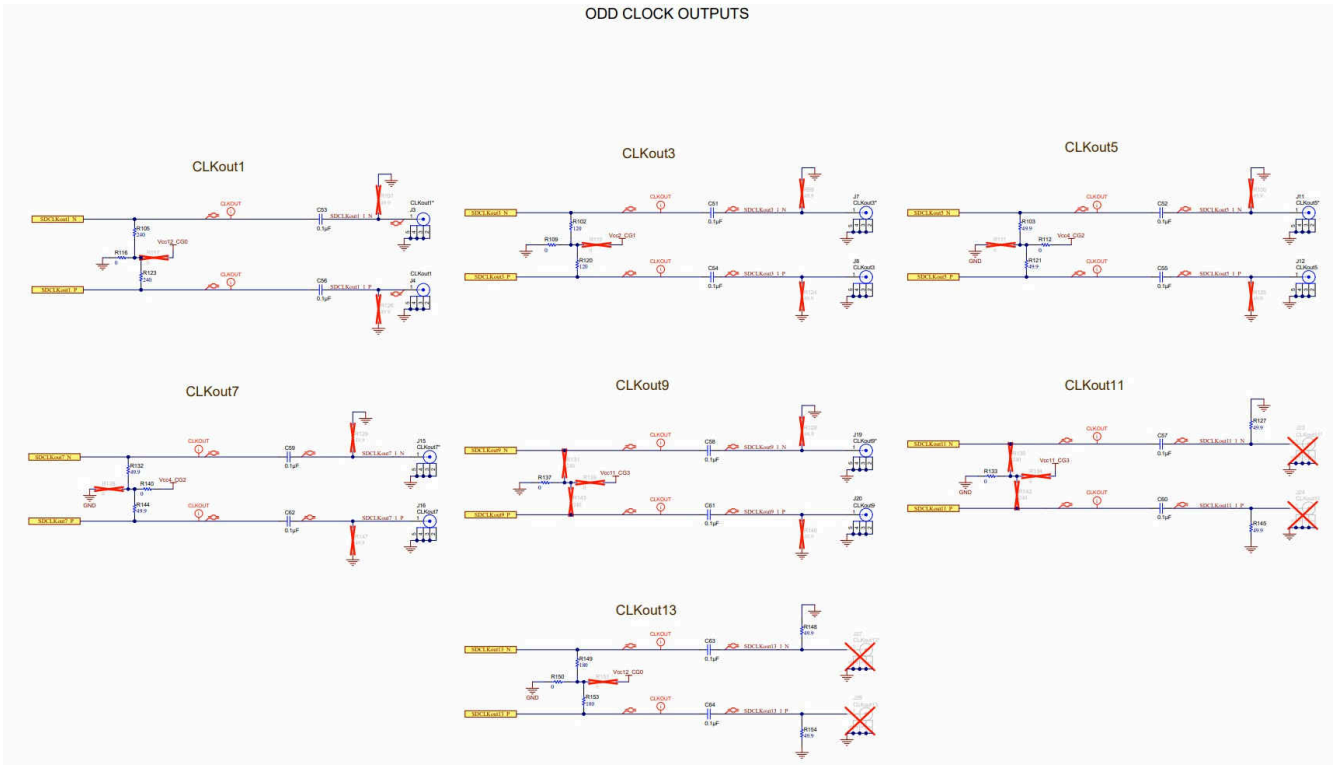

Figure 8-5. Schematic - Clock Outputs 2 of 2

9 Bill of Materials

Table 9-1. Bill of Materials (BOM)

Designator	Description	PartNumber	PackageReference	Manufacturer
C1, C8, C33, C101, C102, C103	CAP, CERM, 10 uF, 16 V, +/- 20%, X7R, 0805	EMK212BB7106MG-T	0805	Taiyo Yuden
C2, C9, C37, C108	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E1X7R1C105K080AC	0603	TDK
C3, C4	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	500R07N101JV4T	0402	MuRata
C7, C13, C20, C30, C31	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	C0603C104J3RACTU	0603	Kemet
C10	CAP, CERM, 3900 pF, 100 V, +/- 5%, X7R, 0603	06031C392JAT2A	0603	AVX
C12	CAP, CERM, 47 pF, 50 V, +/- 5%, C0G/NP0, 0603	C0603C470J5GACTU	0603	Kemet
C14	0.68µF ±10% 10V Ceramic Capacitor X7R 0603 (1608 Metric)	CC0603KRX7R6BB684	0603	Yageo
C15	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	C0603C104K4RACTU	0603	Kemet
C16, C19, C27, C29, C32, C36, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80	CAP, CERM, 0.1 µF, 10 V, +/- 10%, X7R, 0402	C0402C104K8RACTU	0402	Kemet
C21	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	C0603C101J5GACTU	0603	Kemet
C24, C28	CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805	GCM21BR71A106KE22L	0805	MuRata
C25	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	C0603C222K5RACTU	0603	Kemet
C26	CAP, CERM, 82 pF, 50 V, +/- 10%, C0G/NP0, 0603	C0603C820K5GACTU	0603	Kemet
C39	CAP, CERM, 2.2 uF, 16 V, +/- 20%, X5R, 0603	885012106018	0603	Wurth Elektronik

Table 9-1. Bill of Materials (BOM) (continued)

Designator	Description	PartNumber	PackageReference	Manufacturer
C40	CAP, CERM, 3300 pF, 50 V, +/- 10%, X7R, 0603	885012206086	0603	Wurth Elektronik
C41, C42	CAP, CERM, 30 pF, 50 V, +/- 5%, C0G/NP0, 0603	06035A300JAT2A	0603	AVX
C43, C45	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	885012206052	0603	Wurth Elektronik
C44, C48, C49, C50	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	885012206046	0603	Wurth Elektronik
C46	CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0603	885012206036	0603	Wurth Elektronik
C47, C82	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603	06035A221JAT2A	0603	AVX
C81, C96, C97	CAP, CERM, 0.47 uF, 16 V, +/- 10%, X7R, 0603	C0603C474K4RACTU	0603	Kemet
C88, C94, C100	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	GCM155R71E103KA37D	0402	MuRata
C95	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	C0603C104K3RACTU	0603	Kemet
C105, C111, C115, C118	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402	GRM155R71E104KE14D	0402	MuRata
C107	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	C0603C103J5RACTU	0603	Kemet
C123, C126, C129, C134, C137	CAP, CERM, 1 uF, 10 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0402	GCM155C71A105KE38D	0402	MuRata
D1, D2	LED, Green, SMD	150141VS73100	2.8x1.9x3.2mm	Wurth Elektronik
D3, D4	LED, Red, SMD	150141RS73100	SMD, 2-Leads, Body 3.2x3mm	Wurth Elektronik
D5	LED, Green, SMD	LTST-C190GKT	1.6x0.8x0.8mm	Lite-On
FB1, FB2, FB12	Ferrite Bead, 120 ohm @ 100 MHz, 0.5 A, 0603	BLM18AG121SN1D	0603	MuRata
FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11	Ferrite Bead, 120 ohm @ 100 MHz, 0.4 A, 0402	MMZ1005Y121CT000	0402	TDK

Table 9-1. Bill of Materials (BOM) (continued)

Designator	Description	PartNumber	PackageReference	Manufacturer
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38	Connector, End launch SMA, 50 ohm, SMT	142-0701-851	SMA End Launch	Emerson Network Power
J39	Connector, TH, SMA	142-0701-201	SMA	Emerson Network Power
J40	Terminal Block, 5.08mm, 2x1, TH	0395443002	Terminal Block, 5.08mm, 2x1, TH	Molex
J45	Receptacle, USB 2.0, Micro-USB Type B, R/A, SMT	10118194-0001LF	USB-micro B USB 2.0, 0.65mm, 5 Pos, R/A, SMT	FCI
L1, L2, L3, L4	Inductor, Multilayer, Composite, 68 nH, 0.15 A, 1.5 ohm, AEC-Q200 Grade 1, SMD	MLG1005S68NJTD25	0402	TDK
LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	PCB Label 0.650"H x 0.200"W	Brady
Q1	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	BSS138	SOT-23	Fairchild Semiconductor
R1, R3, R4, R6, R12, R25, R33, R34, R46, R47, R62, R68, R109, R112, R114, R116, R133, R137, R140, R150, R163, R169, R193, R202	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0ED	0402	Vishay-Dale
R5, R15, R23, R26	RES, 18, 5%, 0.063 W, 0402	CRCW040218R0JNED	0402	Vishay-Dale
R8, R11, R48, R53	RES, 10, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310R0JNEA	0603	Vishay-Dale
R9	RES, 100, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402100RFKED	0402	Vishay-Dale
R10, R16, R17, R18, R24, R27, R28, R30	RES, 270, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402270RJNED	0402	Vishay-Dale
R22, R36, R39, R42, R65, R66, R69, R71, R73, R76, R79, R91, R98, R104, R106, R107, R108, R113, R209, R213, R216, R220, R226, R230, R232	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA	0603	Vishay-Dale
R38, R49, R105, R123, R160, R176	RES, 240, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402240RJNED	0402	Vishay-Dale

Table 9-1. Bill of Materials (BOM) (continued)

Designator	Description	PartNumber	PackageReference	Manufacturer
R41	RES, 620, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603620RJNEA	0603	Vishay-Dale
R44	RES, 39 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060339K0JNEA	0603	Vishay-Dale
R45, R52, R54, R75, R88, R89	RES, 33, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333R0JNEA	0603	Vishay-Dale
R50, R59, R77, R80	RES, 270, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603270RJNEA	0603	Vishay-Dale
R55	RES, 1.0 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031M00JNEA	0603	Vishay-Dale
R61	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603270RJNEA	0603	Vishay-Dale
R70, R103, R121, R127, R132, R144, R145, R148, R154, R183, R185, R196, R198, R200, R206	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040249R9FKED	0402	Vishay-Dale
R74	RES, 51 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060351K0JNEA	0603	Vishay-Dale
R81	RES, 330, 5%, 0.1 W, 0603	CRCW0603330RJNEA	0603	Vishay-Dale
R84	RES, 10 k, 5%, 0.1 W, 0603	CRCW060310K0JNEA	0603	Vishay-Dale
R86	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333K0JNEA	0603	Vishay-Dale
R90	RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K50JNEA	0603	Vishay-Dale
R92	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031M20JNEA	0603	Vishay-Dale
R102, R120, R158, R175	RES, 120, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402120RJNED	0402	Vishay-Dale
R149, R153, R201, R205	RES, 180, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402180RJNED	0402	Vishay-Dale
R166, R189	RES, 20.0, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040220R0FKED	0402	Vishay-Dale
S1, S2, S3, S4, S5, S6	HEX STANDOFF SPACER, 9.53 mm	TCBS-6-01	7.9x9.5 mm	Richco Plastics

Table 9-1. Bill of Materials (BOM) (continued)

Designator	Description	PartNumber	PackageReference	Manufacturer
S7	Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	FSM4JSMA	SW, SPST 6x6 mm	TE Connectivity
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20	Test Point, Miniature, White, TH	5002	White Miniature Testpoint	Keystone
U1	Enhanced Plastic Grade Ultra-Low-Noise JESD204B Dual-Loop Clock Jitter Cleaner	LMK04368MPAPTEP	TQFP64_PowerPAD	Texas Instruments
U2	25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	MSP430F5529IPN	PN0080A	Texas Instruments
U3	4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	TPD4E004DRYR	DRY0006A	Texas Instruments
U4	Ultra Low Noise, 150mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor, 6-pin LLP, Pb-Free	LP5900SDX-3.3/NOPB	NGF0006A	Texas Instruments
U5	150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	LP5900SD-3.3/NOPB	NGF0006A	Texas Instruments
U7	36-V, 1-A, 4.17-uVRMS, RF LDO Voltage Regulator, RGW0020A (VQFN-20)	TPS7A4701MRGWREP	RGW0020A	Texas Instruments
Y1	VCXO, CMOS 122.880 MHz, 3.3V, SMD	CVHD-950-122.880	CVHD-950-4	Crystek Corporation
Y3	Crystal, 24.000 MHz, 20pF, SMD	ECS-240-20-5PX-TR	Crystal, 11.4x4.3x3.8mm	ECS Inc.

A USB2ANY Firmware Upgrade

When the onboard USB2ANY programmer is first connected, or if the firmware revision used for the onboard USB2ANY programmer does not match the version used by TICS Pro (2.7.0.0), TICS Pro will request a firmware update. Follow the pop-up instructions to complete the update.

1. When the *USB2ANY Firmware Requirement* pop-up window appears, click *OK* to continue.

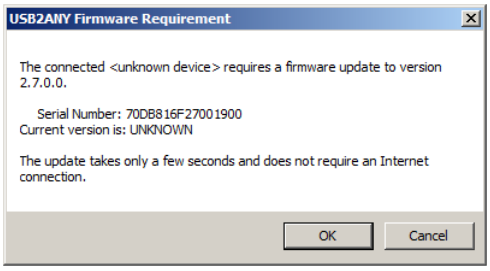

Figure A-1. Firmware Requirement

2. The *Firmware Loader* pop-up window will load. Disconnect the USB cable from the EVM.

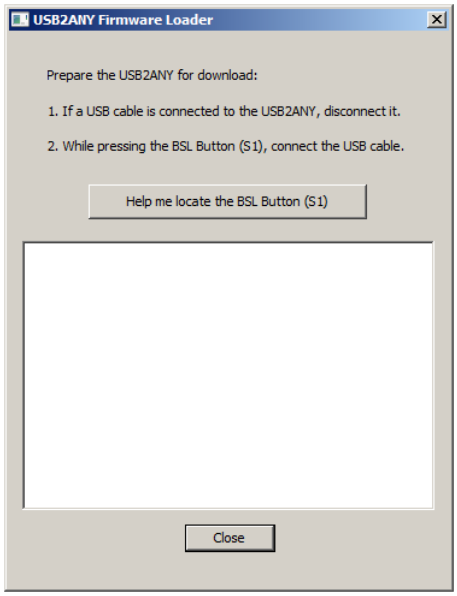

Figure A-2. Firmware Loader

3. Press and hold the BSL button while you connect the USB2ANY cable.

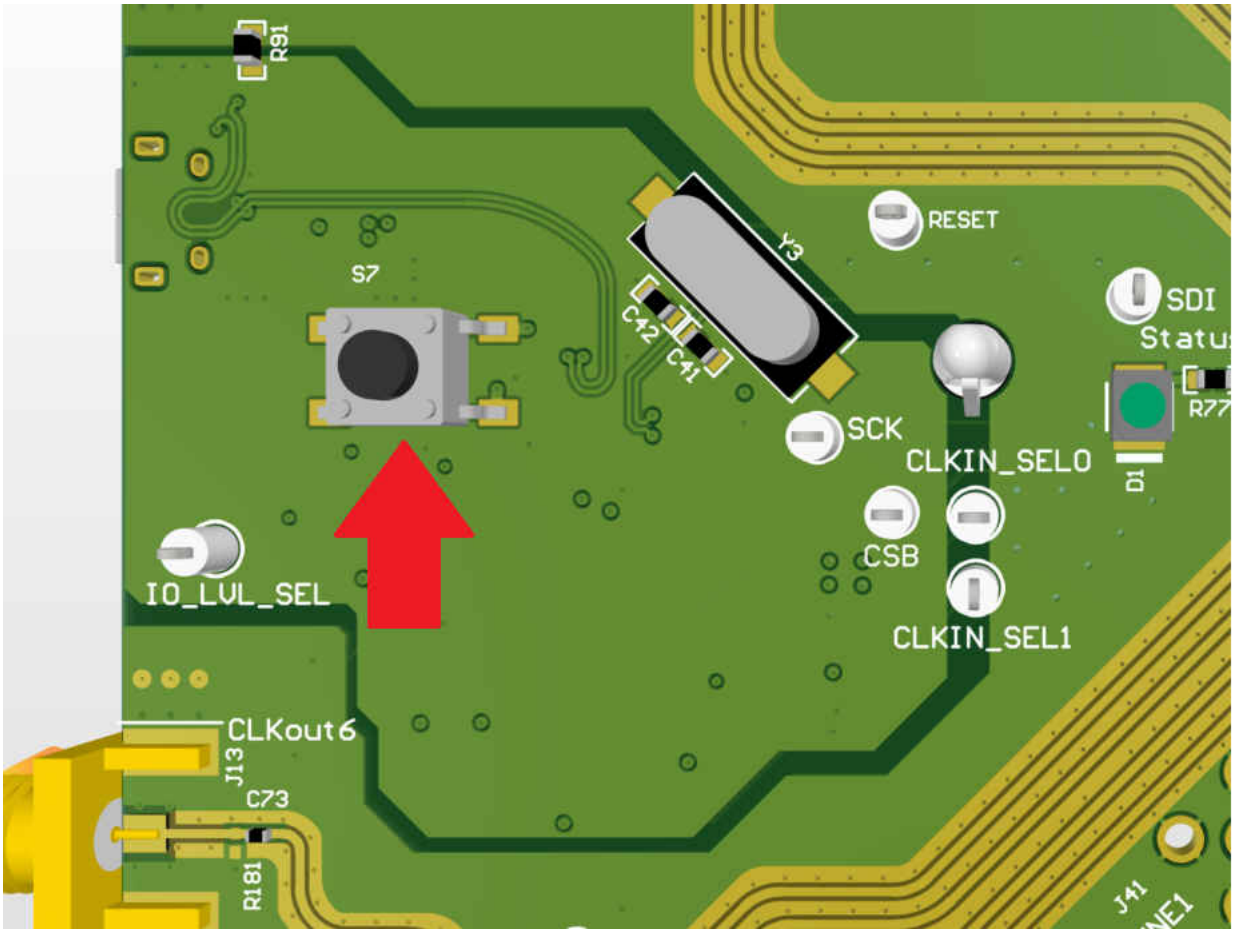

Figure A-3. BSL Button Location

4. The firmware loader should recognize the USB2ANY as a target for programming, and an *Update Firmware* button should appear.

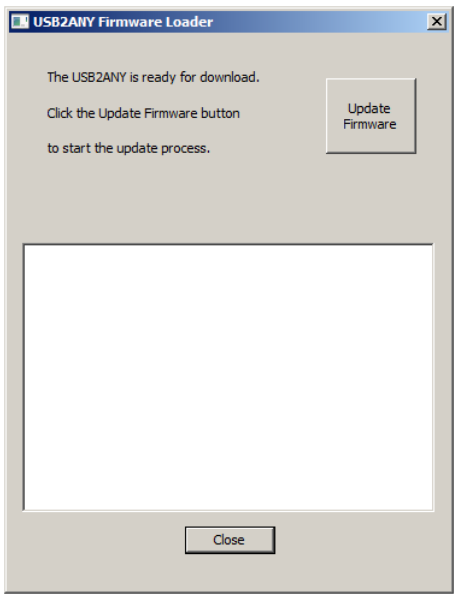

Figure A-4. Update Firmware

5. Click *Upgrade Firmware* to start the firmware upgrade. Click *Close* after the upgrade is complete.

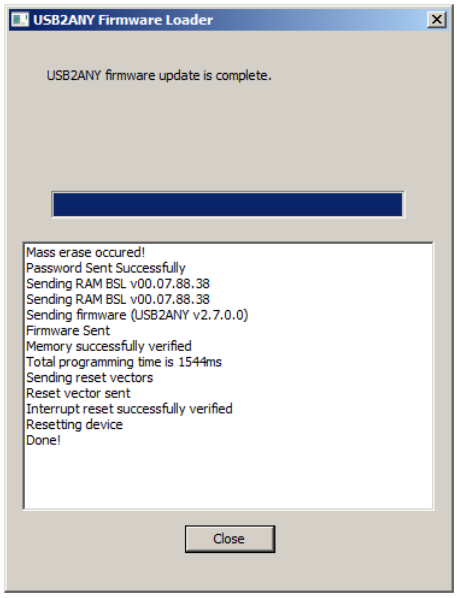

Figure A-5. Firmware Update Complete

6. Go to *USB communications* → *Interface* in the TICS Pro software to check the USB connection. Make sure the *USB Connected* button is green.

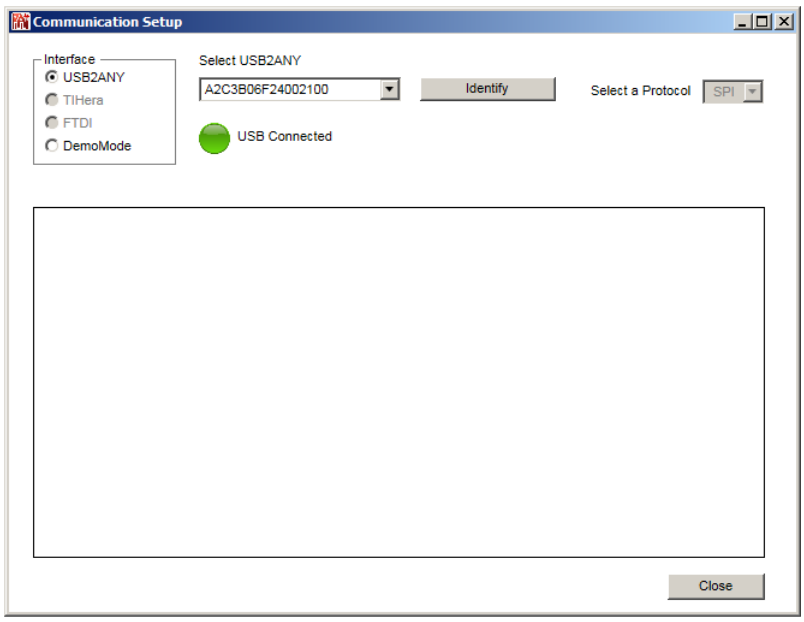

Figure A-6. USB Communications

B TICS Pro Usage

TICS Pro is used to program the evaluation board with the onboard USB2ANY interface (MSP430F5529IPN). TICS Pro can also be used to generate register maps for programming the device and current consumption estimates. This appendix outlines the basic purpose and usage of each page. TICS Pro is available for download at http://www.ti.com/tool/ticspro-sw.

11.1 Communication Setup

The *Communication Setup* window allows you to select the USB2ANY or DemoMode interface. In case you plan to connect multiple evaluation boards to your PC and run multiple instances of the TICS Pro software, the drop-down box will allow you to select specific USB2ANY devices. Press the *Identify* button to determine which USB2ANY is currently selected. Devices used by other instances of TICS Pro will not display in this list.

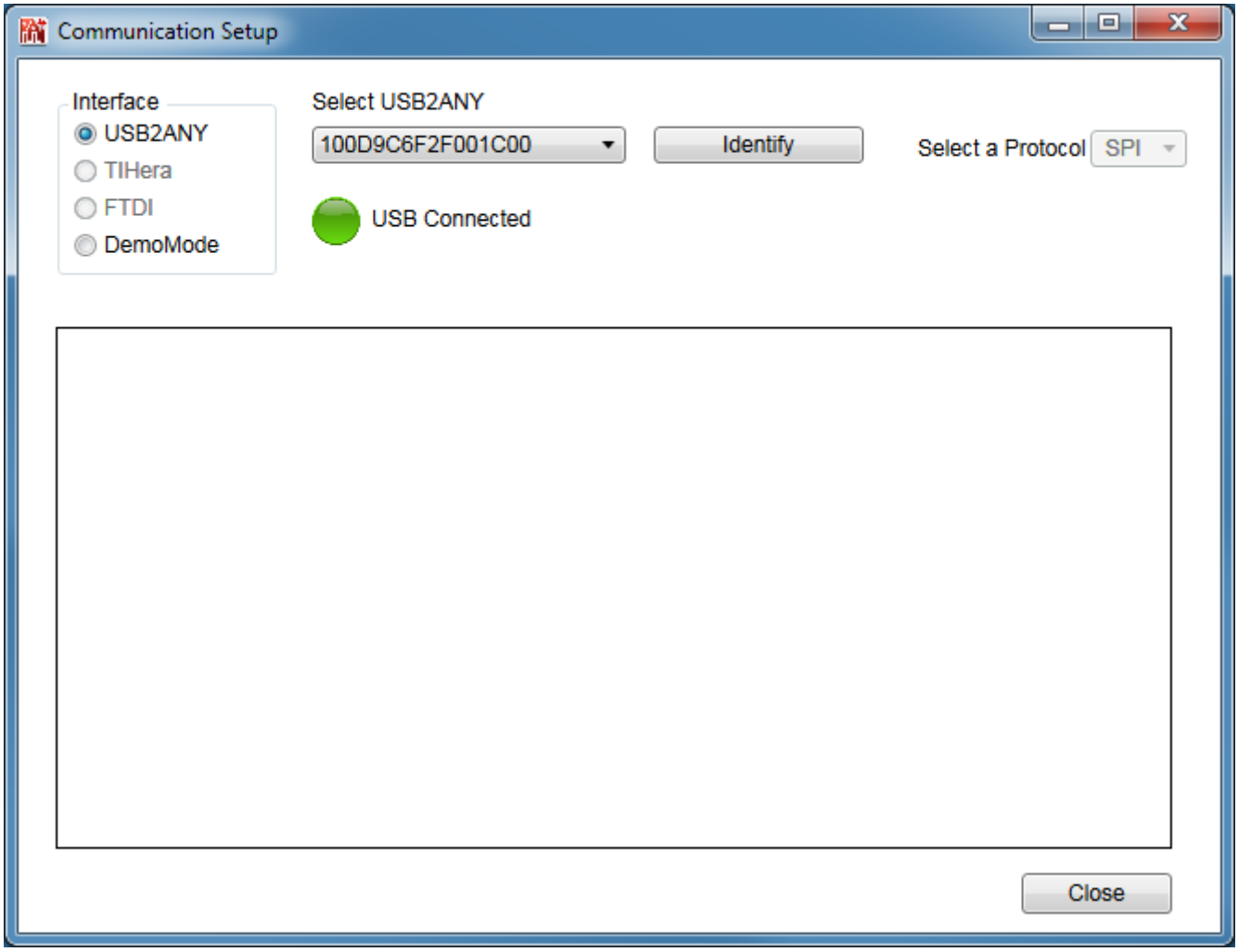

Figure 11-1. TICS Pro - Communication Setup Window

11.2 User Controls

The *User Controls* page has controls typically not included on one of the other dedicated pages.

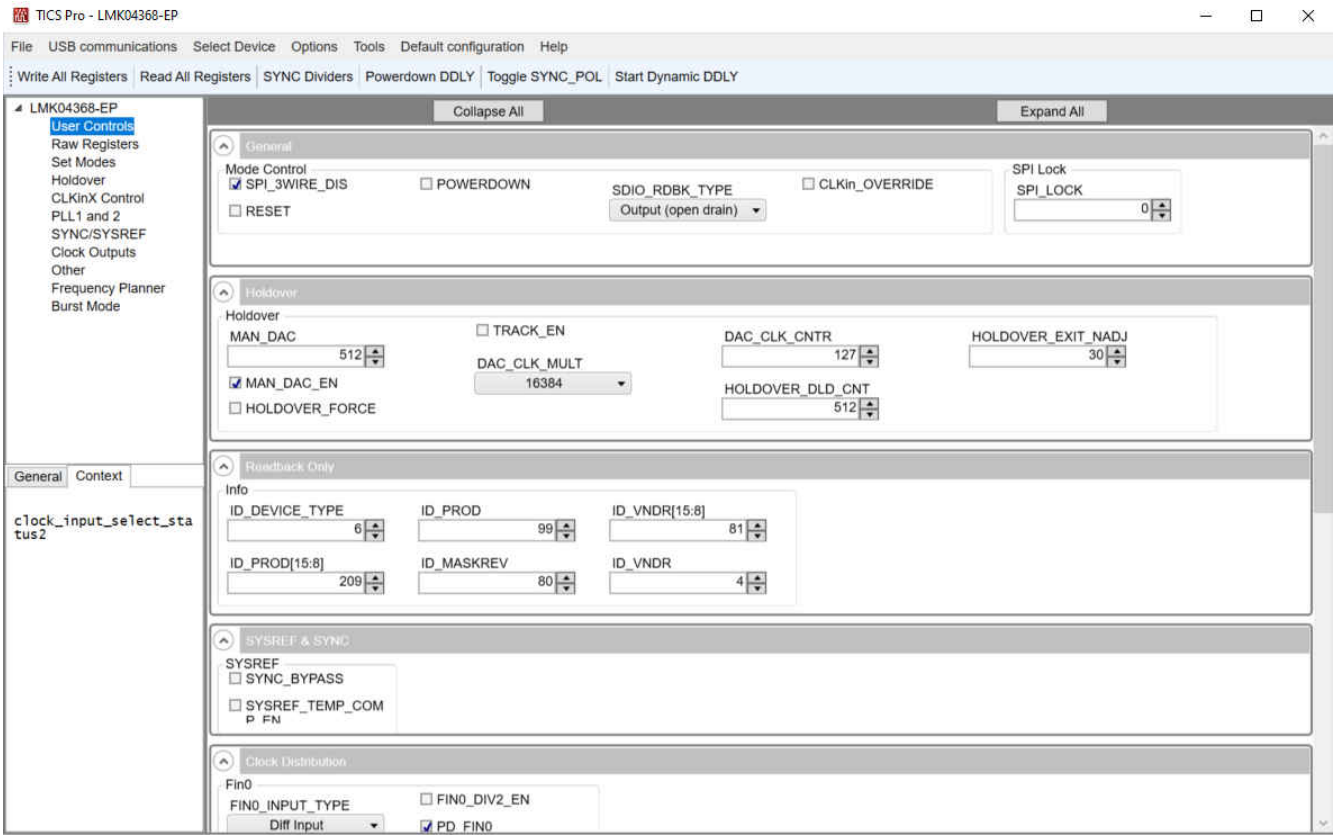

Figure 11-2. TICS Pro - User Controls Page

11.3 Raw Registers Page

The *Raw Register* page displays the register map including address. The address bits have the shaded background and are not editable. The unshaded bits are the data bits. This register map may be directly manipulated by clicking into the bit field, moving around with the arrow keys, and typing 1 or 0 to change a bit.

All registers may be read or written in addition to individual registers. For individual register read or write, the active register is highlighted in the list of registers and displayed in the top right. An individual register or field may be read back by entering the name into the bottom right and clicking the *Read* button.

Register maps may be exported, but also imported. The import format may simply be the address and register data in hex format as illustrated in the address/value column, one register to a line.

Note

Use the *Export Register Map* option to create a text file with the register values for simple re-use of the register configuration.

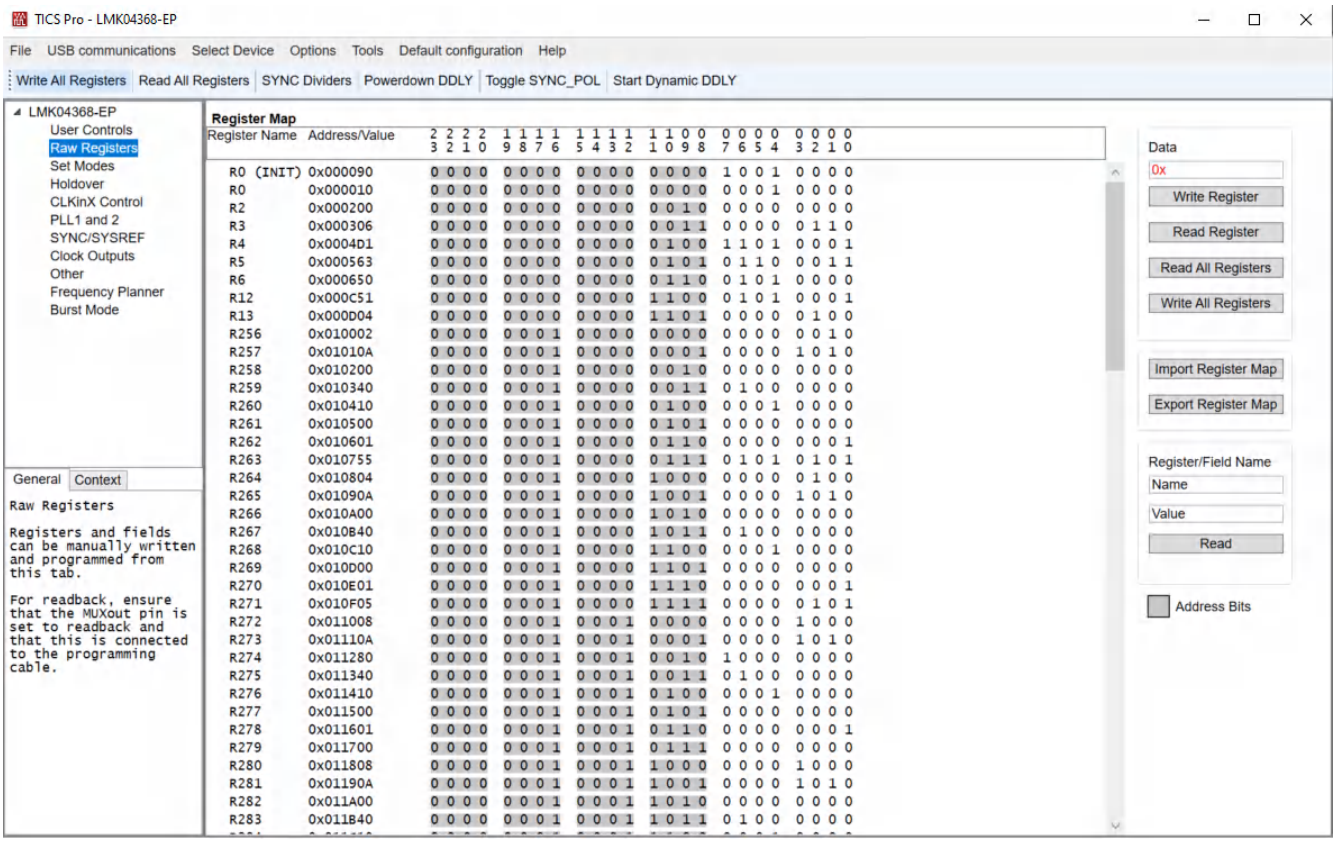

Figure 11-3. TICS Pro - Raw Registers Page

11.4 Set Modes Page

The *Set Modes* page allows the user to quickly configure the LMK04832 into a desired mode. If the LMK04832 is already in the desired mode, or several registers are already programmed as needed, the log will not display any or many register writes.

The top LMK04832 modes section allows the user to set high level usage profiles to allow the device to operate in dual loop, single loop, or distribution mode.

The bottom LMK04832 sub-modes section allows further JESD204B configuration, 0-delay configuration, or clock input configuration which may apply for many of the LMK04832 modes of operation.

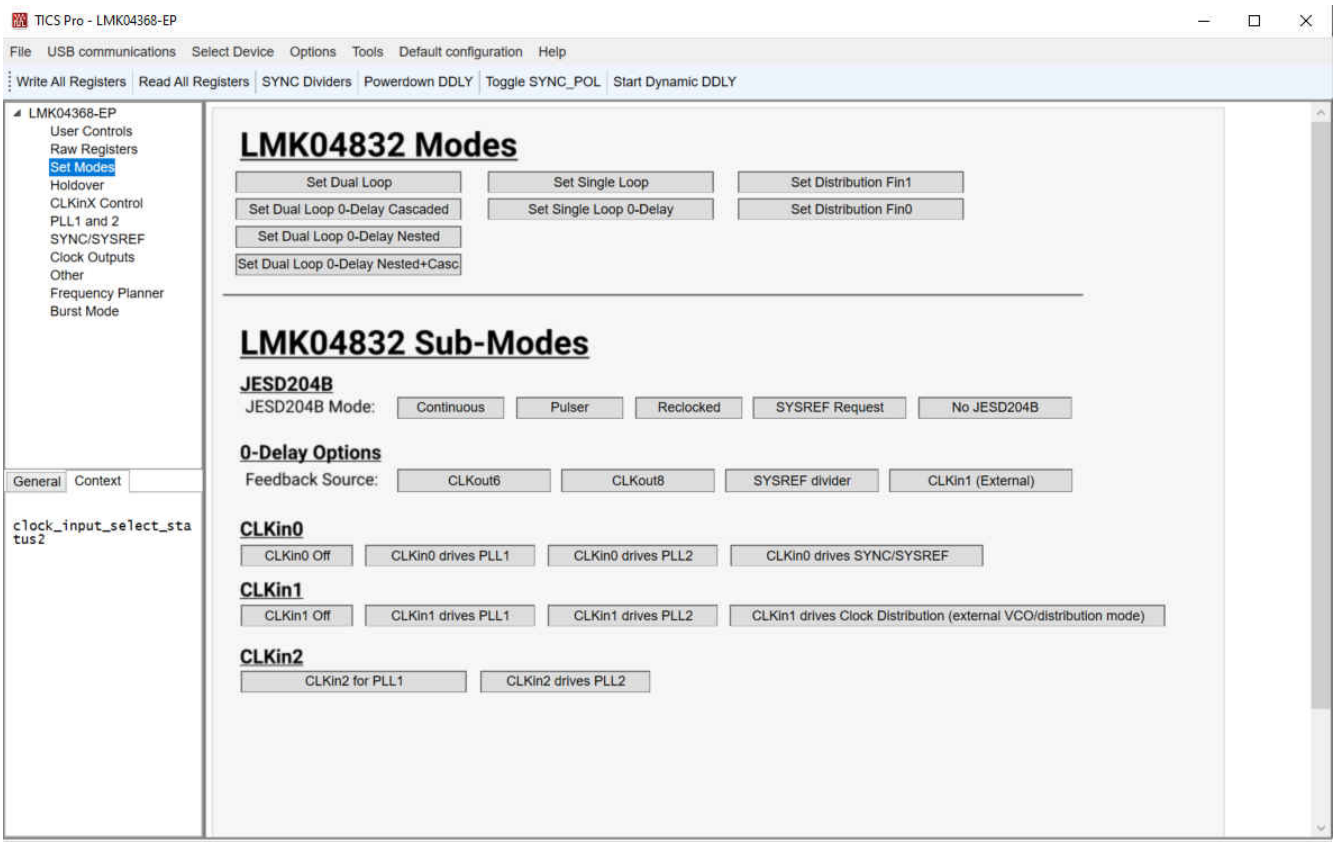

Figure 11-4. TICS Pro - Set Modes Page

11.5 Holdover Page

The *Holdover* page contains many registers pertaining to how the device will enter and exit holdover. To enable holdover and LOS detect for entry and exit of holdover:

- Set HOLDOVER_EN = 1 (checked)
- Set HOLDOVER_EXIT_MODE combo box to 0x00 (Exit based on LOS)
- Set LOS_EN = 1 (checked)
- Set LOS_TIMEOUT combo box to the LOS frequency threshold as desired. For example, if 200 MHz is set as the frequency threshold, the input must be above approximately 200 MHz to lock, otherwise PLL1 will enter holdover. If holdover is not enabled, PLL1 will be prevented from locking if the input frequency is less than the threshold frequency and LOS is enabled.

In addition to the above steps, auto clock selection mode must be used to allow the LMK04832 to automatically switch to holdover when enabled clocks for auto switching (CLKinX_EN) are lost.

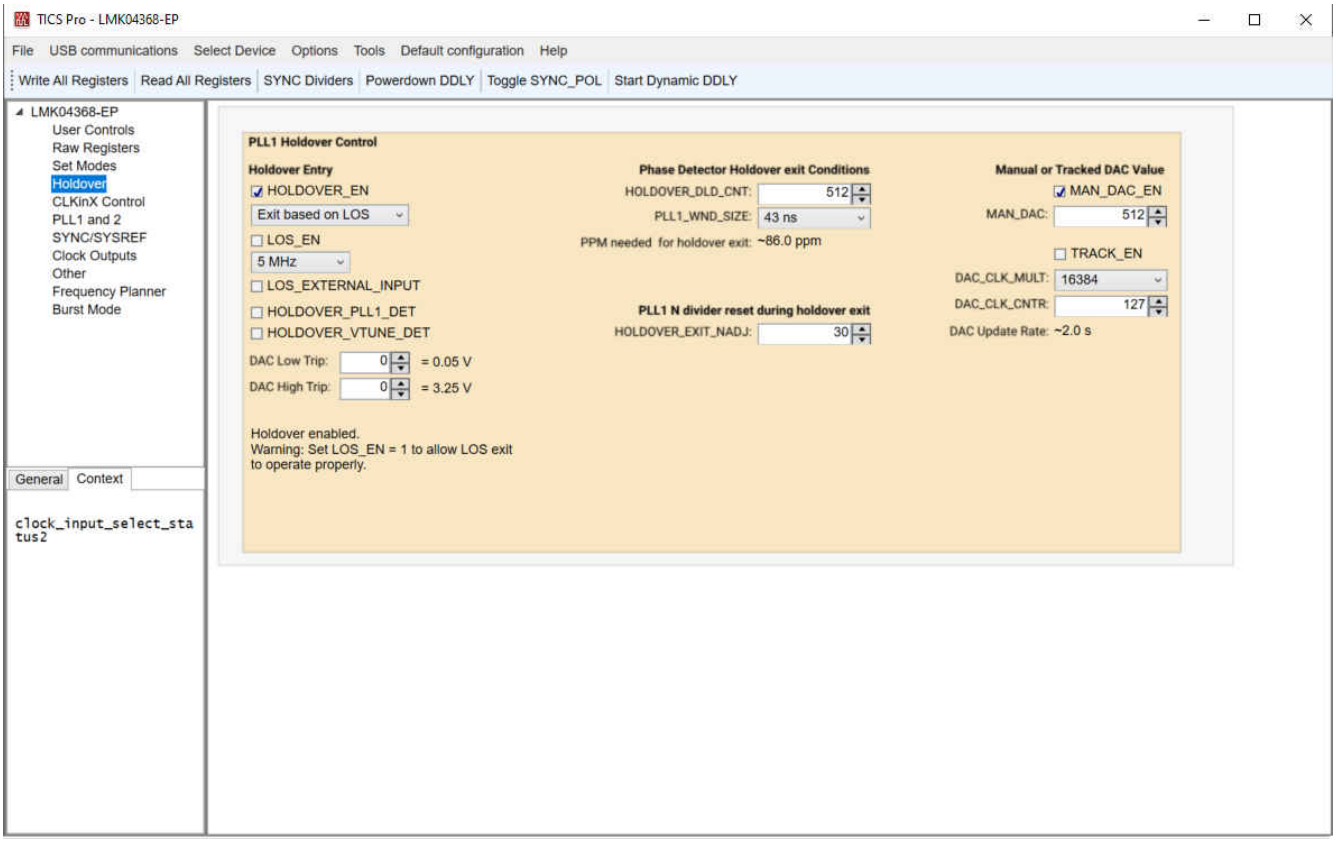

Figure 11-5. TICS Pro - Holdover Page

11.6 CLKinX Control Page

The *CLKinX Control* page allows to the user to enter the input frequency at the different CLKinX pins, change the mode by which the active CLKinX is selected, and change the routing options for the CLKinX inputs.

You can also reset the PLL1 R or PLL2 N divider on this page.

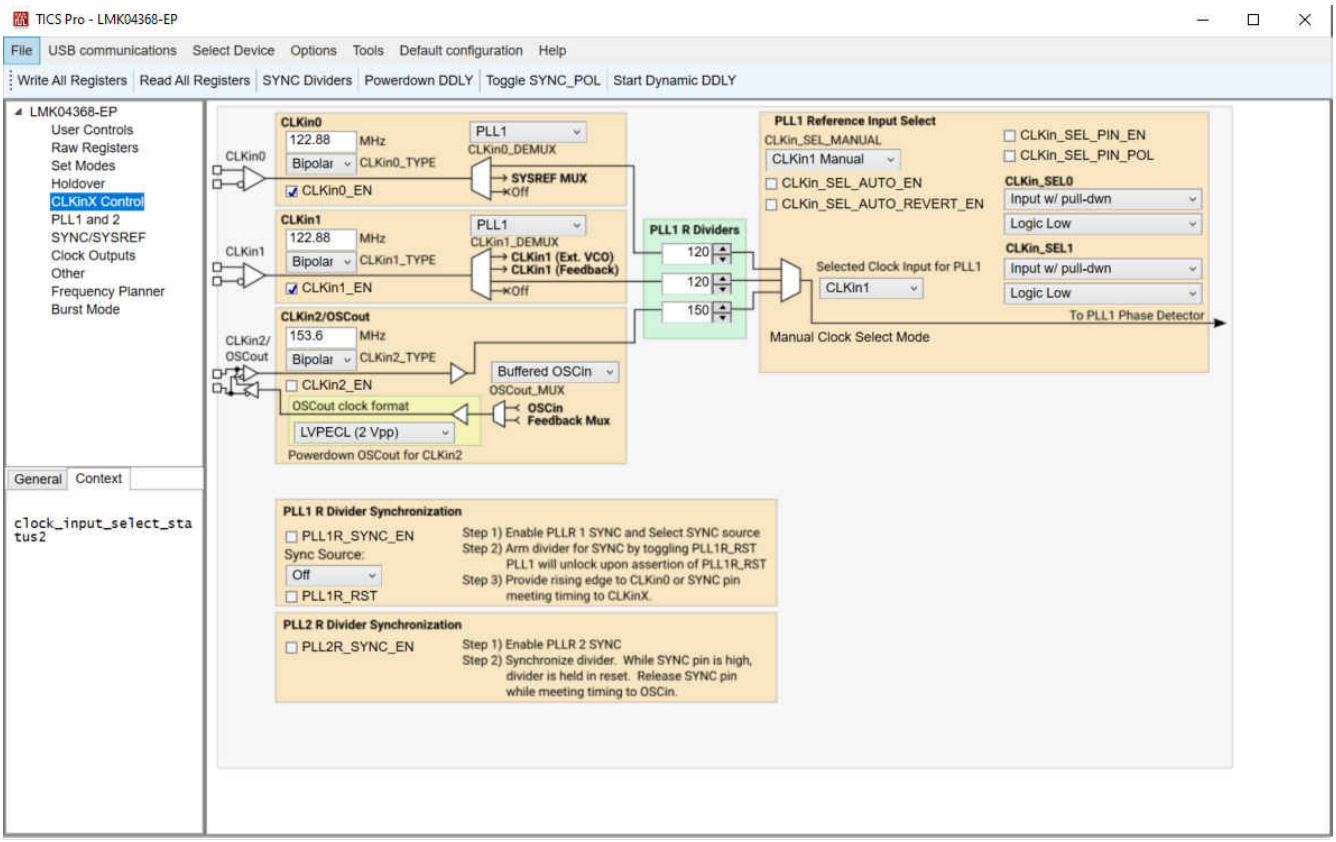

Figure 11-6. TICS Pro - CLKinX Control Page

11.7 PLL1 and 2 Page

The *PLL1 and 2* page shows the operating frequencies of the PLL1 and PLL2. In distribution mode, the CLKin1 frequency will directly be connected to the VCO/clock distribution path frequency. In addition to the basic PLL dividers and controls, when the PLLX_NCLK_MUX selects the feedback mux as a source, 0-delay modes are achieved. When enabling 0-delay red text will help guide the user through properly setting up 0-delay mode.

When using dual PLL mode, the *OSCin Source* combo box can be set to *External VCXO* which links the OSCin frequency with the external VCXO frequency. When using single PLL2 mode, the *OSCin Source* combo box can be set to *Independent* to allow the OSCin frequency to be unlinked from the external VCXO frequency.

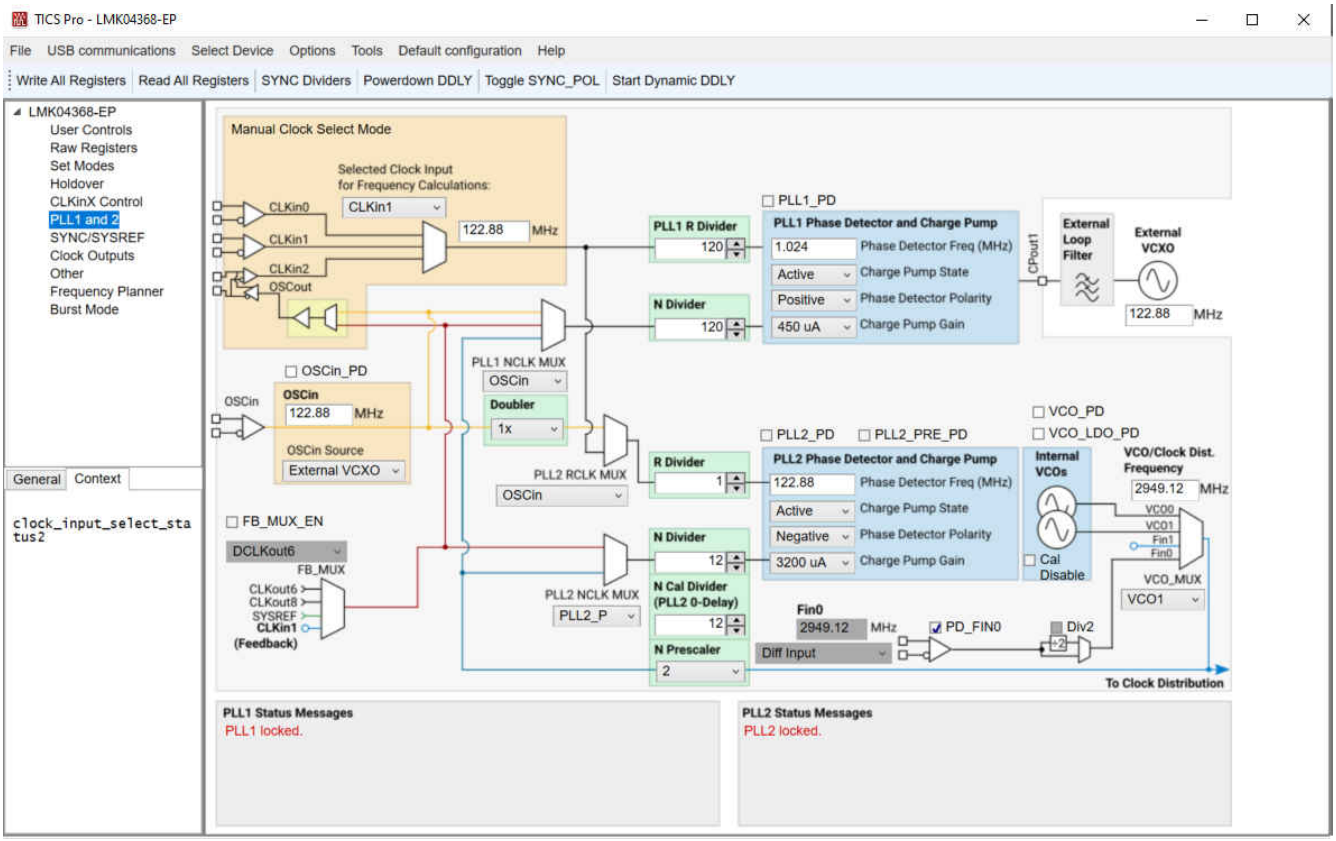

Figure 11-7. TICS Pro - PLL1 and 2 Page

11.8 SYNC / SYSREF Page

The *SYNC / SYSREF* page allows some mode set buttons for JESD204B features. The SYNC dividers button will stop all SYNC inputs, set normal SYNC mode, enable all dividers for SYNC, issue a SYNC by toggling SYNC_POL, set all dividers to ignore SYNC, then return any other changed parameter to its original state. This is a nice feature to ensure all outputs are synchronized together or to be run after changing the digital delay value which requires a SYNC to update. This functionality is also available on any other page through the toolbar as *SYNC Dividers*.

Note

To use SYNC or SYSREF, ensure that SYNC_EN = 1. To use SYSREF in continuous, pulser, or reclocked modes, be sure SYSREF_PD = 0.

The SCLKX_Y_DIS_MODE bits allow the clock outputs to be disabled or set to a low state. Values 1 and 2 are only conditionally set by the SYSREF_GBL_PD bit, therefore it is possible to power up/down several SYSREF outputs by programming only one register. When changing between Active (0x00) and Conditional Low (0x01) states, keep the SYSREF_CLR = 1 during the transition to prevent glitch pulses from the SYSREF output.

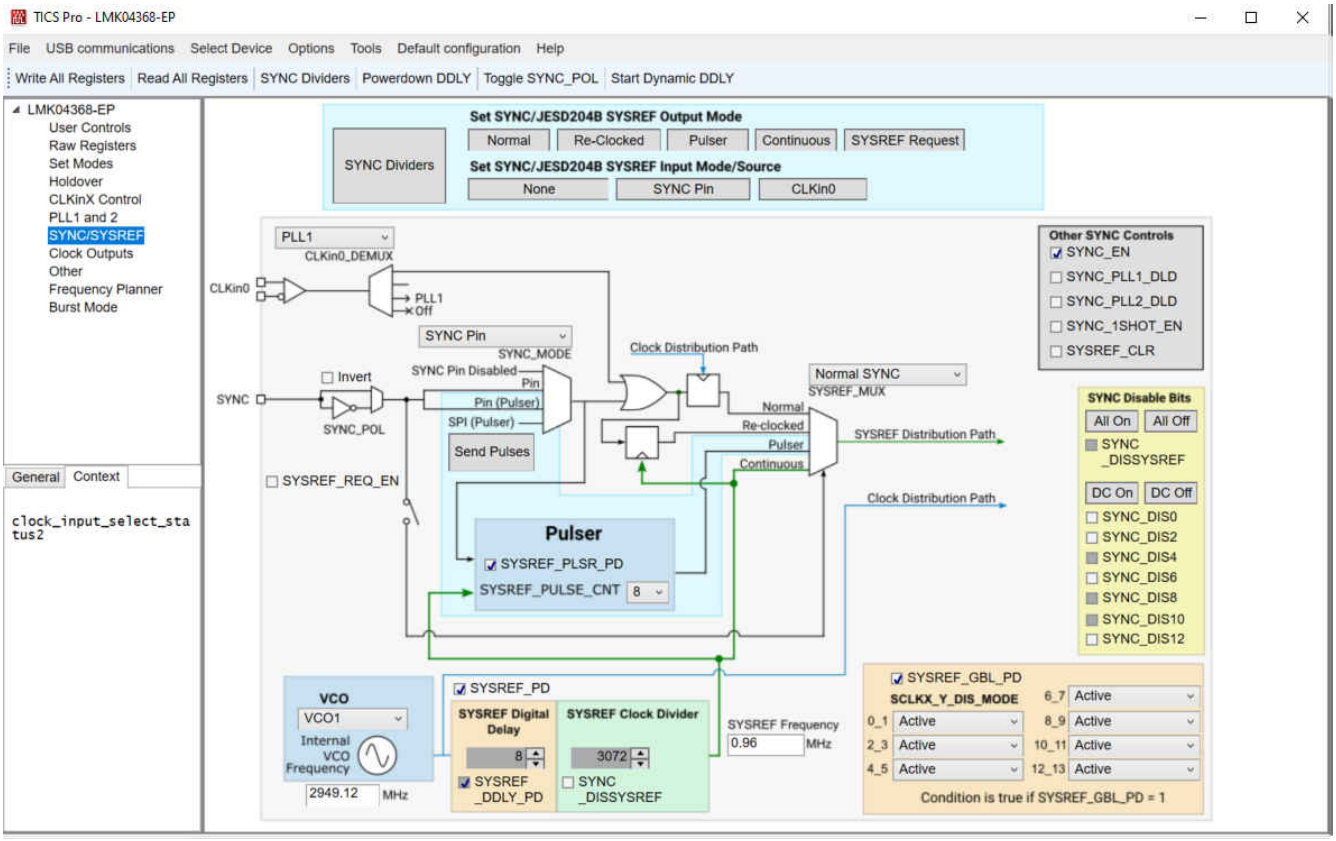

Figure 11-8. TICS Pro - SYNC / SYSREF Page

11.9 Clock Outputs Page

The *Clock Outputs* page allows control of all the clock outputs format and other options relating to the clock outputs. All the clock outputs are paired and allow two device clocks, two SYSREF clocks, or one of each. The naming convention uses X_Y for controls which can impact both CLKoutX (even clock) and CLKoutY (odd clock), X for controls impacting only CLKoutX and Y for controls impacting only CLKoutY.

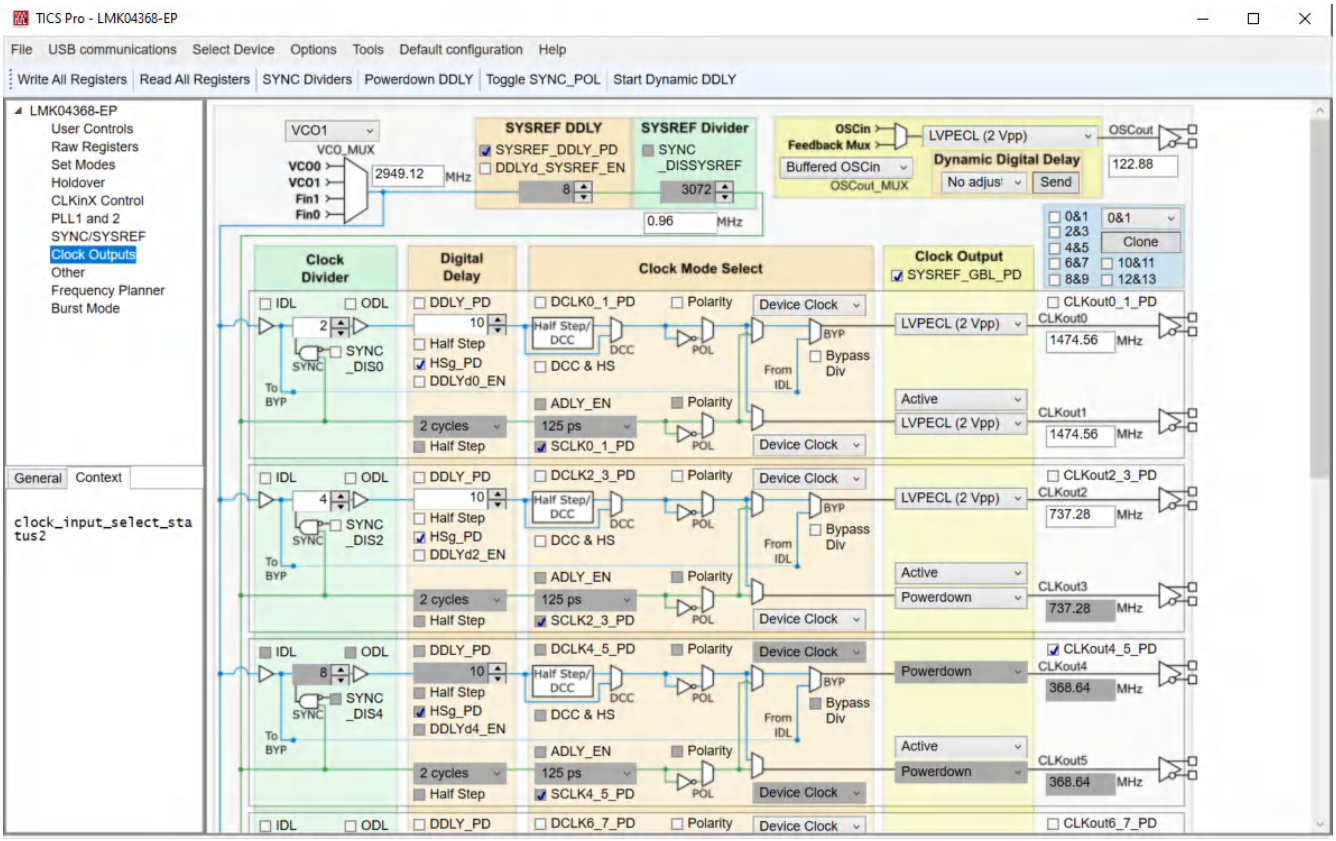

Figure 11-9. TICS Pro - Clock Outputs Page

11.10 Other Page

The *Other* page contains some registers to control the GPIO pins of the LMK04832. Each pin has two fields, the first is the _TYPE field which allows the input or output mode of the pin to be defined. The second is the _MUX field which, when set for output, controls what the pin will output.

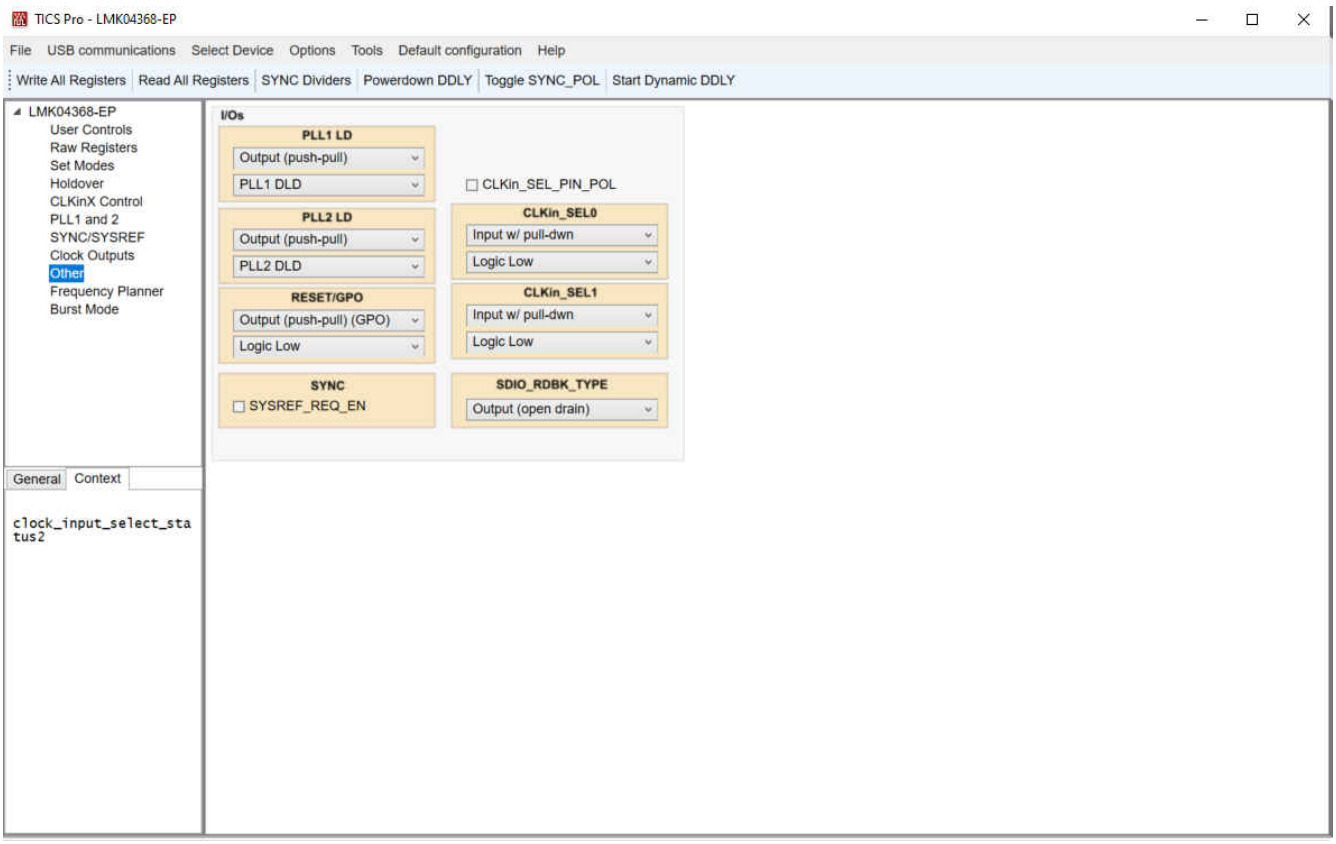

Figure 11-10. TICS Pro - Other Page

11.11 Burst Mode Page

The *Burst* mode page allows the user to program sequences of register programming or pin control.

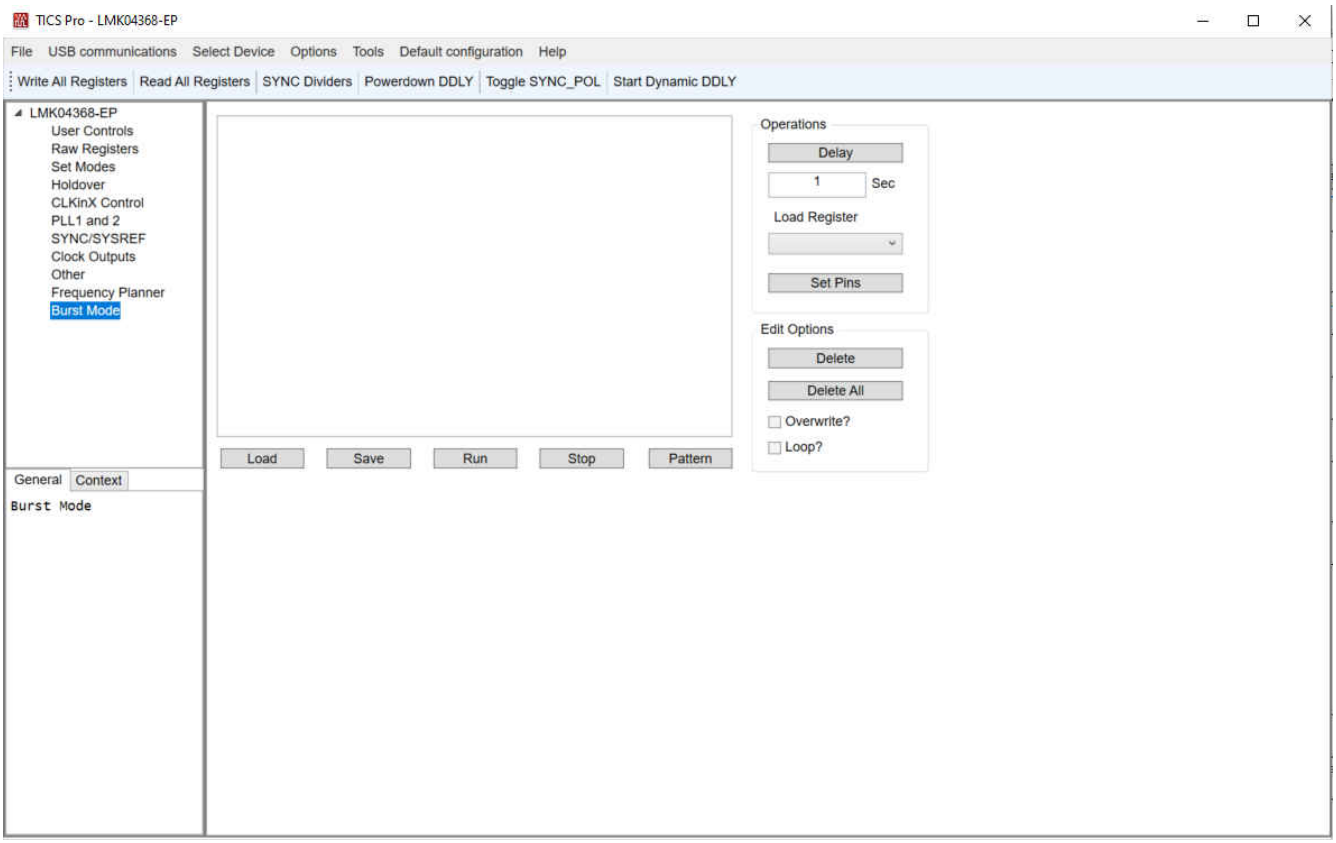

Figure 11-11. TICS Pro - Burst Mode Page

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NOTE:

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CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
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