User's Guide

LMK5B33414 Programmer's Guide

ABSTRACT

This programming guide lists the device registers of the LMK5B33414.

Trademarks

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1 Device Registers

Table 1-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 1-1 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. DEVICE Registers

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0	R0	VNDRID_15:8							
0x1	R1	VNDRID							
0x2	R2	PRODID							
0x3	R3	REVID							
0x10	R16	NVMCNT							
0x12	R18	RESERVED			TARGET_ADR_MSB				
0x13	R19	EEREV							
0x14	R20	ROM_PLUS_EE	EE_ROM_PAGE_SEL				RESERVED		
0x15	R21	SPI_3WIRE_DIS	SYNC_SW	RESERVED					
0x16	R22	RESERVED		DPLL3_EN	APLL3_EN	DPLL2_EN	APLL2_EN	DPLL1_EN	APLL1_EN
0x17	R23	RESERVED	SWRST	RESERVED					
0x18	R24	RESERVED		APLL3_STRT_PRTY		APLL2_STRT_PRTY		APLL1_STRT_PRTY	
0x19	R25	RESERVED							SYNC_EN
0x1A	R26	RESERVED		SYSREF_REQ_MODE		SYSREF_REQ_SEL			SYSREF_REQ_SW
0x1B	R27	TEC_CNTR_39:32							
0x1C	R28	TEC_CNTR_31:24							
0x1D	R29	TEC_CNTR_23:16							
0x1E	R30	TEC_CNTR_15:8							
0x1F	R31	TEC_CNTR							
0x20	R32	RESERVED						TEC_CNTR_TRIG_SEL	TEC_CNTR_EN
0x21	R33	RESERVED				LOL_PLL1	LOL_PLL2	RESERVED	LOS_FDET_XO
0x22	R34	LOPL_DPLL1	LOFL_DPLL1	RESERVED	HLDOVR1	RESERVED			
0x23	R35	LOPL_DPLL2	LOFL_DPLL2	RESERVED	HLDOVR2	RESERVED			
0x24	R36	LOPL_DPLL3	LOFL_DPLL3	RESERVED	HLDOVR3	RESERVED			
0x25	R37	RESERVED				LOL_PLL1_MASK	LOL_PLL2_MASK	RESERVED	LOS_FDET_XO_MASK
0x26	R38	LOPL_DPLL1_MASK	LOFL_DPLL1_MASK	HIST1_MASK	HLDOVR1_MASK	REFSWITCH1_MASK	LOR_MISSCLK1_MASK	LOR_FREQ1_MASK	LOR_PH1_MASK
0x27	R39	LOPL_DPLL2_MASK	LOFL_DPLL2_MASK	HIST2_MASK	HLDOVR2_MASK	REFSWITCH2_MASK	LOR_MISSCLK2_MASK	LOR_FREQ2_MASK	LOR_PH2_MASK
0x28	R40	LOPL_DPLL3_MASK	LOFL_DPLL3_MASK	HIST3_MASK	HLDOVR3_MASK	REFSWITCH3_MASK	LOR_MISSCLK3_MASK	LOR_FREQ3_MASK	LOR_PH3_MASK
0x29	R41	RESERVED				LOL_PLL1_POL	LOL_PLL2_POL	RESERVED	LOS_FDET_XO_POL
0x2A	R42	LOPL_DPLL1_POL	LOFL_DPLL1_POL	HIST1_POL	HLDOVR1_POL	REFSWITCH1_POL	LOR_MISSCLK1_POL	LOR_FREQ1_POL	LOR_PH1_POL
0x2B	R43	LOPL_DPLL2_POL	LOFL_DPLL2_POL	HIST2_POL	HLDOVR2_POL	REFSWITCH2_POL	LOR_MISSCLK2_POL	LOR_FREQ2_POL	LOR_PH2_POL
0x2C	R44	LOPL_DPLL3_POL	LOFL_DPLL3_POL	HIST3_POL	HLDOVR3_POL	REFSWITCH3_POL	LOR_MISSCLK3_POL	LOR_FREQ3_POL	LOR_PH3_POL

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2D	R45	RESERVED				LOL_PLL1_INTR	LOL_PLL2_INTR	RESERVED	LOS_FDET_XO_INTR
0x2E	R46	LOPL_DPLL1_INTR	LOFL_DPLL1_INTR	HIST1_INTR	HLDOVR1_INTR	REFSWITCH1_INTR	LOR_MISSCLK1_INTR	LOR_FREQ1_INTR	LOR_PH1_INTR
0x2F	R47	LOPL_DPLL2_INTR	LOFL_DPLL2_INTR	HIST2_INTR	HLDOVR2_INTR	REFSWITCH2_INTR	LOR_MISSCLK2_INTR	LOR_FREQ2_INTR	LOR_PH2_INTR
0x30	R48	LOPL_DPLL3_INTR	LOFL_DPLL3_INTR	HIST3_INTR	HLDOVR3_INTR	REFSWITCH3_INTR	LOR_MISSCLK3_INTR	LOR_FREQ3_INTR	LOR_PH3_INTR
0x31	R49	RESERVED				INT_LATCH_OR_LIVE	INT_AND_OR	INT_EN	INT_CLR
0x32	R50	RESERVED				REF3_VALID_STATUS	REF2_VALID_STATUS	REF1_VALID_STATUS	REF0_VALID_STATUS
		RESERVED							
0x33	R51	RESERVED		REF3_PH_STATUS	RESERVED	REF3_FDET_STATUS	REF2_PH_STATUS	RESERVED	REF2_FDET_STATUS
0x34	R52	RESERVED		REF1_PH_STATUS	RESERVED	REF1_FDET_STATUS	REF0_PH_STATUS	RESERVED	REF0_FDET_STATUS
0x35	R53	RESERVED			TEC_CNTR_HELD	RESERVED			
0x36	R54	RESERVED	GPIO0_IN_FLT_EN	GPIO0_MODE					
0x37	R55	RESERVED	GPIO1_IN_FLT_EN	GPIO1_MODE					
0x38	R56	RESERVED	GPIO2_IN_FLT_EN	GPIO2_MODE					
0x39	R57	RESERVED	GPIO0_SEL						
0x3A	R58	RESERVED	GPIO1_SEL						
0x3B	R59	RESERVED	GPIO2_SEL						
0x3C	R60	RESERVED		GPIO0_OPEND	GPIO1_OPEND	GPIO2_OPEND	GPIO0_POL	GPIO1_POL	GPIO2_POL
0x3D	R61	RESERVED			GPIO_SYSREF_SEL			MUTE_DPLL3_PHLOCK	MUTE_DPLL3_FRLOCK
0x3E	R62	RESERVED	MUTE_APLL3_LOCK	MUTE_DPLL2_PHLOCK	MUTE_DPLL2_FRLOCK	MUTE_APLL2_LOCK	MUTE_DPLL1_PHLOCK	MUTE_DPLL1_FRLOCK	MUTE_APLL1_LOCK
0x3F	R63	RESERVED			XO_FDET_BYP	XO_ITYPE			
0x40	R64	RESERVED			XO_OUT_BUF_EN				
0x41	R65	RESERVED				REF3_ITYPE			
0x42	R66	RESERVED				REF2_ITYPE			
0x43	R67	RESERVED			REF1_DC_COUPLED_EN	REF1_ITYPE			
0x44	R68	RESERVED			REF0_DC_COUPLED_EN	REF0_ITYPE			
0x46	R70	RESERVED							STATUS_MUX_DIV2_EN
0x4B	R75	RESERVED	TDC3_ZDM_BYPASS_FB_DIV	TDC3_ZDM_FB_PRE_BYP	TDC3_IN_SEL	TDC3_IN_DRV_SEL			
0x4C	R76	RESERVED	TDC2_ZDM_BYPASS_FB_DIV	TDC2_ZDM_FB_PRE_BYP	TDC2_IN_SEL	TDC2_IN_DRV_SEL			

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4D	R77	RESERVED	TDC1_ZDM_BYPASS_FB_DIV	TDC1_ZDM_FB_PRE_BYP	TDC1_IN_SEL		TDC1_IN_DRV_SEL		
0x4E	R78	RESERVED		REF_OUT01_EN	REF_OUT01_SEL				
0x4F	R79	RESERVED		REF0_EARLY_DET_EN	REF0_PH_VALID_EN	REF0_VALTMR_EN	REF0_PPM_EN	REF0_MISSCLK_EN	RESERVED
0x50	R80	RESERVED		REF1_EARLY_DET_EN	REF1_PH_VALID_EN	REF1_VALTMR_EN	REF1_PPM_EN	REF1_MISSCLK_EN	RESERVED
0x51	R81	RESERVED		REF2_EARLY_DET_EN	REF2_PH_VALID_EN	REF2_VALTMR_EN	REF2_PPM_EN	REF2_MISSCLK_EN	RESERVED
0x52	R82	RESERVED		REF3_EARLY_DET_EN	REF3_PH_VALID_EN	REF3_VALTMR_EN	REF3_PPM_EN	REF3_MISSCLK_EN	RESERVED
0x53	R83	REF3_DET_CLK_DIV		REF2_DET_CLK_DIV		REF1_DET_CLK_DIV		REF0_DET_CLK_DIV	
0x54	R84	RESERVED		REF0_MISSCLK_DIV_21:16					
0x55	R85	REF0_MISSCLK_DIV_15:8							
0x56	R86	REF0_MISSCLK_DIV							
0x57	R87	RESERVED		REF1_MISSCLK_DIV_21:16					
0x58	R88	REF1_MISSCLK_DIV_15:8							
0x59	R89	REF1_MISSCLK_DIV							
0x5A	R90	RESERVED		REF2_MISSCLK_DIV_21:16					
0x5B	R91	REF2_MISSCLK_DIV_15:8							
0x5C	R92	REF2_MISSCLK_DIV							
0x5D	R93	RESERVED		REF3_MISSCLK_DIV_21:16					
0x5E	R94	REF3_MISSCLK_DIV_15:8							
0x5F	R95	REF3_MISSCLK_DIV							
0x60	R96	RESERVED							REF0_MISSCLK_VCOSEL
0x61	R97	RESERVED		REF0_EARLY_CLK_DIV_21:16					
0x62	R98	REF0_EARLY_CLK_DIV_15:8							
0x63	R99	REF0_EARLY_CLK_DIV							
0x64	R100	RESERVED		REF1_EARLY_CLK_DIV_21:16					
0x65	R101	REF1_EARLY_CLK_DIV_15:8							
0x66	R102	REF1_EARLY_CLK_DIV							
0x67	R103	RESERVED		REF2_EARLY_CLK_DIV_21:16					
0x68	R104	REF2_EARLY_CLK_DIV_15:8							
0x69	R105	REF2_EARLY_CLK_DIV							
0x6A	R106	RESERVED		REF3_EARLY_CLK_DIV_21:16					
0x6B	R107	REF3_EARLY_CLK_DIV_15:8							
0x6C	R108	REF3_EARLY_CLK_DIV							
0x6D	R109	RESERVED	REF0_PPM_MIN_14:8						
0x6E	R110	REF0_PPM_MIN							
0x6F	R111	RESERVED	REF0_PPM_MAX_14:8						
0x70	R112	REF0_PPM_MAX							
0x71	R113	RESERVED	REF1_PPM_MIN_14:8						
0x72	R114	REF1_PPM_MIN							
0x73	R115	RESERVED	REF1_PPM_MAX_14:8						
0x74	R116	REF1_PPM_MAX							
0x75	R117	RESERVED	REF2_PPM_MIN_14:8						

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x76	R118	REF2_PPM_MIN							
0x77	R119	RESERVED	REF2_PPM_MAX_14:8						
0x78	R120	REF2_PPM_MAX							
0x79	R121	RESERVED	REF3_PPM_MIN_14:8						
0x7A	R122	REF3_PPM_MIN							
0x7B	R123	RESERVED	REF3_PPM_MAX_14:8						
0x7C	R124	REF3_PPM_MAX							
0x8D	R141	RESERVED	REF2_PH_VALID_CNT_MSB			REF2_CNTSTRT_27:24			
0x8E	R142	REF2_CNTSTRT_23:16							
0x8F	R143	REF2_CNTSTRT_15:8							
0x90	R144	REF2_CNTSTRT							
0x91	R145	RESERVED				REF2_HOLD_CNTSTRT_27:24			
0x92	R146	REF2_HOLD_CNTSTRT_23:16							
0x93	R147	REF2_HOLD_CNTSTRT_15:8							
0x94	R148	REF2_HOLD_CNTSTRT							
0x95	R149	RESERVED	REF3_PH_VALID_CNT_MSB			REF3_CNTSTRT_27:24			
0x96	R150	REF3_CNTSTRT_23:16							
0x97	R151	REF3_CNTSTRT_15:8							
0x98	R152	REF3_CNTSTRT							
0x99	R153	RESERVED				REF3_HOLD_CNTSTRT_27:24			
0x9A	R154	REF3_HOLD_CNTSTRT_23:16							
0x9B	R155	REF3_HOLD_CNTSTRT_15:8							
0x9C	R156	REF3_HOLD_CNTSTRT							
0x9D	R157	RESERVED			REF0VLDTMR				
0x9E	R158	RESERVED			REF1VLDTMR				
0x9F	R159	RESERVED			REF2VLDTMR				
0xA0	R160	RESERVED			REF3VLDTMR				
0xA1	R161	RESERVED		REF0_PH_VALID_THR_13:8					
0xA2	R162	REF0_PH_VALID_THR							
0xA3	R163	RESERVED		REF1_PH_VALID_THR_13:8					
0xA4	R164	REF1_PH_VALID_THR							
0xA5	R165	RESERVED		REF2_PH_VALID_THR_13:8					
0xA6	R166	REF2_PH_VALID_THR							
0xA7	R167	RESERVED		REF3_PH_VALID_THR_13:8					
0xA8	R168	REF3_PH_VALID_THR							
0xAA	R170	NVMSCRC							
0xAB	R171	RESERVED	REGCOMMIT	NVMCRCERR	RESERVED		NVMBUSY	NVMERASE	NVMPROG
0xAD	R173	RESERVED			MEMADR_12:8				
0xAE	R174	MEMADR							
0xB0	R176	RAMDAT							
0xB4	R180	NVMUNLK							
0xDF	R223	RESERVED		DPLL1_REF0_AUTO_PRTY			DPLL1_REF1_AUTO_PRTY		
0xE0	R224	RESERVED		DPLL1_REF2_AUTO_PRTY			DPLL1_REF3_AUTO_PRTY		
0xE1	R225	RESERVED		DPLL1_REF4_AUTO_PRTY			DPLL1_REF5_AUTO_PRTY		
0xE2	R226	RESERVED		DPLL1_MAN_REFSEL			DPLL1_MAN_SWITCH_PIN_MODE	DPLL1_SWITCH_MODE	

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xE3	R227	RESERVED		DPLL1_REFSEL_STAT					
0xE4	R228	DPLL1_LOCKDET_PPM_EN	DPLL1_LOCKDET_PPM_MAX_14:8						
0xE5	R229	DPLL1_LOCKDET_PPM_MAX							
0xE6	R230	RESERVED	DPLL1_UNLOCKDET_PPM_MAX_14:8						
0xE7	R231	DPLL1_UNLOCKDET_PPM_MAX							
0xE8	R232	RESERVED		DPLL1_LOCKDET2_PPM_CNTSTRT_29:24					
0xE9	R233	DPLL1_LOCKDET2_PPM_CNTSTRT_23:16							
0xEA	R234	DPLL1_LOCKDET2_PPM_CNTSTRT_15:8							
0xEB	R235	DPLL1_LOCKDET2_PPM_CNTSTRT							
0xEC	R236	RESERVED		DPLL1_LOCKDET_PPM_CNTSTRT_29:24					
0xED	R237	DPLL1_LOCKDET_PPM_CNTSTRT_23:16							
0xEE	R238	DPLL1_LOCKDET_PPM_CNTSTRT_15:8							
0xEF	R239	DPLL1_LOCKDET_PPM_CNTSTRT							
0xF0	R240	RESERVED		DPLL1_LOCKDET_VCO_PPM_CNTSTRT_29:24					
0xF1	R241	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_23:16							
0xF2	R242	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_15:8							
0xF3	R243	DPLL1_LOCKDET_VCO_PPM_CNTSTRT							
0xF4	R244	RESERVED							DPLL1_STATUS_PPM_LOCK
0xF7	R247	DPLL1_LOOP_EN	DPLL1_PHASE_CANCEL_EN	RESERVED	DPLL1_PHS1_EN	DPLL1_ZDM_EN	DPLL1_HIST_EN	DPLL1_PHASE_CANCEL_ALWAYS	RESERVED
0xF8	R248	DPLL1_HOLD_SLEW_LIM_EN	RESERVED				DPLL1_CLK_DIV_SRC_SEL	RESERVED	
0xFA	R250	RESERVED			DPLL1_PH_OFFSET_44:40				
0xFB	R251	DPLL1_PH_OFFSET_39:32							
0xFC	R252	DPLL1_PH_OFFSET_31:24							
0xFD	R253	DPLL1_PH_OFFSET_23:16							
0xFE	R254	DPLL1_PH_OFFSET_15:8							
0xFF	R255	DPLL1_PH_OFFSET							
0x100	R256	DPLL1_FREE_RUN_39:32							
0x101	R257	DPLL1_FREE_RUN_31:24							
0x102	R258	DPLL1_FREE_RUN_23:16							
0x103	R259	DPLL1_FREE_RUN_15:8							
0x104	R260	DPLL1_FREE_RUN							
0x122	R290	RESERVED							DPLL1_LCK_TIMER_9:8
0x123	R291	DPLL1_LCK_TIMER							
0x124	R292	RESERVED							DPLL1_HIST_TIMER_9:8
0x125	R293	DPLL1_HIST_TIMER							
0x126	R294	RESERVED							DPLL1_HOLD_TIMER_9:8
0x127	R295	DPLL1_HOLD_TIMER							
0x128	R296	RESERVED							DPLL1_PHS1_TIMER_9:8
0x129	R297	DPLL1_PHS1_TIMER							
0x12E	R302	RESERVED			DPLL1_HIST_GAIN				
0x12F	R303	RESERVED		DPLL1_PL_THRESH					

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x130	R304	RESERVED		DPLL1_PL_UNLK_THRESH					
0x131	R305	RESERVED		DPLL1_PHS1_THRESH					
0x134	R308	RESERVED		DPLL1_HOLD_SLEW_STEP					
0x136	R310	RESERVED		DPLL1_STATUS_PL	RESERVED				
0x137	R311	RESERVED			DPLL1_DCO_SLEW_ACTIVE	RESERVED			
0x13A	R314	RESERVED							DPLL1_FB_DIV_32:32
0x13B	R315	DPLL1_FB_DIV_31:24							
0x13C	R316	DPLL1_FB_DIV_23:16							
0x13D	R317	DPLL1_FB_DIV_15:8							
0x13E	R318	DPLL1_FB_DIV							
0x13F	R319	DPLL1_FB_NUM_39:32							
0x140	R320	DPLL1_FB_NUM_31:24							
0x141	R321	DPLL1_FB_NUM_23:16							
0x142	R322	DPLL1_FB_NUM_15:8							
0x143	R323	DPLL1_FB_NUM							
0x144	R324	DPLL1_FB_DEN_39:32							
0x145	R325	DPLL1_FB_DEN_31:24							
0x146	R326	DPLL1_FB_DEN_23:16							
0x147	R327	DPLL1_FB_DEN_15:8							
0x148	R328	DPLL1_FB_DEN							
0x149	R329	RESERVED							DPLL1_FB2_DIV_32:32
0x14A	R330	DPLL1_FB2_DIV_31:24							
0x14B	R331	DPLL1_FB2_DIV_23:16							
0x14C	R332	DPLL1_FB2_DIV_15:8							
0x14D	R333	DPLL1_FB2_DIV							
0x14E	R334	DPLL1_FB2_NUM_39:32							
0x14F	R335	DPLL1_FB2_NUM_31:24							
0x150	R336	DPLL1_FB2_NUM_23:16							
0x151	R337	DPLL1_FB2_NUM_15:8							
0x152	R338	DPLL1_FB2_NUM							
0x153	R339	DPLL1_FB2_DEN_39:32							
0x154	R340	DPLL1_FB2_DEN_31:24							
0x155	R341	DPLL1_FB2_DEN_23:16							
0x156	R342	DPLL1_FB2_DEN_15:8							
0x157	R343	DPLL1_FB2_DEN							
0x158	R344	RESERVED		DPLL1_REF5_FB_SEL	DPLL1_REF4_FB_SEL	DPLL1_REF3_FB_SEL	DPLL1_REF2_FB_SEL	DPLL1_REF1_FB_SEL	DPLL1_REF0_FB_SEL
0x159	R345	RESERVED					DPLL1_FB_MASH_ORDER		
0x15A	R346	RESERVED		DPLL1_FB_FDEV_37:32					
0x15B	R347	DPLL1_FB_FDEV_31:24							
0x15C	R348	DPLL1_FB_FDEV_23:16							
0x15D	R349	DPLL1_FB_FDEV_15:8							
0x15E	R350	DPLL1_FB_FDEV							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x15F	R351	RESERVED							DPLL1_FB_FDEV_UPDATE
0x160	R352	RESERVED							DPLL1_FB_FDEV_EN
0x161	R353	DPLL1_FB_NUM_STAT_39:32							
0x162	R354	DPLL1_FB_NUM_STAT_31:24							
0x163	R355	DPLL1_FB_NUM_STAT_23:16							
0x164	R356	DPLL1_FB_NUM_STAT_15:8							
0x165	R357	DPLL1_FB_NUM_STAT							
0x166	R358	RESERVED				DPLL1_REF0_DBLR_EN	DPLL1_REF1_DBLR_EN	DPLL1_REF2_DBLR_EN	DPLL1_REF3_DBLR_EN
0x167	R359	DPLL1_REF0_RDIV_15:8							
0x168	R360	DPLL1_REF0_RDIV							
0x169	R361	DPLL1_REF1_RDIV_15:8							
0x16A	R362	DPLL1_REF1_RDIV							
0x16B	R363	DPLL1_REF2_RDIV_15:8							
0x16C	R364	DPLL1_REF2_RDIV							
0x16D	R365	DPLL1_REF3_RDIV_15:8							
0x16E	R366	DPLL1_REF3_RDIV							
0x16F	R367	DPLL1_REF4_RDIV_15:8							
0x170	R368	DPLL1_REF4_RDIV							
0x171	R369	DPLL1_REF5_RDIV_15:8							
0x172	R370	DPLL1_REF5_RDIV							
0x175	R373	RESERVED		DPLL2_REF0_AUTO_PRTY			DPLL2_REF1_AUTO_PRTY		
0x176	R374	RESERVED		DPLL2_REF2_AUTO_PRTY			DPLL2_REF3_AUTO_PRTY		
0x177	R375	RESERVED		DPLL2_REF4_AUTO_PRTY			DPLL2_REF5_AUTO_PRTY		
0x178	R376	RESERVED		DPLL2_MAN_REFSEL			DPLL2_MAN_SWITCH_PIN_MODE	DPLL2_SWITCH_MODE	
0x179	R377	RESERVED		DPLL2_REFSEL_STAT					
0x17A	R378	DPLL2_LOCKDET_PPM_EN	DPLL2_LOCKDET_PPM_MAX_14:8						
0x17B	R379	DPLL2_LOCKDET_PPM_MAX							
0x17C	R380	RESERVED	DPLL2_UNLOCKDET_PPM_MAX_14:8						
0x17D	R381	DPLL2_UNLOCKDET_PPM_MAX							
0x17E	R382	RESERVED		DPLL2_LOCKDET2_PPM_CNTSTRT_29:24					
0x17F	R383	DPLL2_LOCKDET2_PPM_CNTSTRT_23:16							
0x180	R384	DPLL2_LOCKDET2_PPM_CNTSTRT_15:8							
0x181	R385	DPLL2_LOCKDET2_PPM_CNTSTRT							
0x182	R386	RESERVED		DPLL2_LOCKDET_PPM_CNTSTRT_29:24					
0x183	R387	DPLL2_LOCKDET_PPM_CNTSTRT_23:16							
0x184	R388	DPLL2_LOCKDET_PPM_CNTSTRT_15:8							
0x185	R389	DPLL2_LOCKDET_PPM_CNTSTRT							
0x186	R390	RESERVED		DPLL2_LOCKDET_VCO_PPM_CNTSTRT_29:24					
0x187	R391	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_23:16							
0x188	R392	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_15:8							
0x189	R393	DPLL2_LOCKDET_VCO_PPM_CNTSTRT							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x18A	R394	RESERVED							DPLL2_STATUS_PPM_LOCK
0x18D	R397	DPLL2_LOOP_EN	DPLL2_PHASE_CANCEL_EN	RESERVED	DPLL2_PHS1_EN	DPLL2_ZDM_EN	DPLL2_HIST_EN	DPLL2_PHASE_CANCEL_ALWAYS	RESERVED
0x18E	R398	DPLL2_HOLD_SLEW_LIM_EN	RESERVED						
0x190	R400	RESERVED			DPLL2_PH_OFFSET_44:40				
0x191	R401	DPLL2_PH_OFFSET_39:32							
0x192	R402	DPLL2_PH_OFFSET_31:24							
0x193	R403	DPLL2_PH_OFFSET_23:16							
0x194	R404	DPLL2_PH_OFFSET_15:8							
0x195	R405	DPLL2_PH_OFFSET							
0x196	R406	DPLL2_FREE_RUN_39:32							
0x197	R407	DPLL2_FREE_RUN_31:24							
0x198	R408	DPLL2_FREE_RUN_23:16							
0x199	R409	DPLL2_FREE_RUN_15:8							
0x19A	R410	DPLL2_FREE_RUN							
0x1B8	R440	RESERVED						DPLL2_LCK_TIMER_9:8	
0x1B9	R441	DPLL2_LCK_TIMER							
0x1BA	R442	RESERVED						DPLL2_HIST_TIMER_9:8	
0x1BB	R443	DPLL2_HIST_TIMER							
0x1BC	R444	RESERVED						DPLL2_HOLD_TIMER_9:8	
0x1BD	R445	DPLL2_HOLD_TIMER							
0x1BE	R446	RESERVED						DPLL2_PHS1_TIMER_9:8	
0x1BF	R447	DPLL2_PHS1_TIMER							
0x1C4	R452	RESERVED			DPLL2_HIST_GAIN				
0x1C5	R453	RESERVED		DPLL2_PL_THRESH					
0x1C6	R454	RESERVED		DPLL2_PL_UNLK_THRESH					
0x1C7	R455	RESERVED		DPLL2_PHS1_THRESH					
0x1CA	R458	RESERVED		DPLL2_HOLD_SLEW_STEP					
0x1CC	R460	RESERVED		DPLL2_STATUS_PL	RESERVED				
0x1CD	R461	RESERVED			DPLL2_DCO_SLEW_ACTIVE	RESERVED			
0x1D0	R464	RESERVED							DPLL2_FB_DIV_32:32
0x1D1	R465	DPLL2_FB_DIV_31:24							
0x1D2	R466	DPLL2_FB_DIV_23:16							
0x1D3	R467	DPLL2_FB_DIV_15:8							
0x1D4	R468	DPLL2_FB_DIV							
0x1D5	R469	DPLL2_FB_NUM_39:32							
0x1D6	R470	DPLL2_FB_NUM_31:24							
0x1D7	R471	DPLL2_FB_NUM_23:16							
0x1D8	R472	DPLL2_FB_NUM_15:8							
0x1D9	R473	DPLL2_FB_NUM							
0x1DA	R474	DPLL2_FB_DEN_39:32							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1DB	R475	DPLL2_FB_DEN_31:24							
0x1DC	R476	DPLL2_FB_DEN_23:16							
0x1DD	R477	DPLL2_FB_DEN_15:8							
0x1DE	R478	DPLL2_FB_DEN							
0x1DF	R479	RESERVED							DPLL2_FB2_DIV_32:32
0x1E0	R480	DPLL2_FB2_DIV_31:24							
0x1E1	R481	DPLL2_FB2_DIV_23:16							
0x1E2	R482	DPLL2_FB2_DIV_15:8							
0x1E3	R483	DPLL2_FB2_DIV							
0x1E4	R484	DPLL2_FB2_NUM_39:32							
0x1E5	R485	DPLL2_FB2_NUM_31:24							
0x1E6	R486	DPLL2_FB2_NUM_23:16							
0x1E7	R487	DPLL2_FB2_NUM_15:8							
0x1E8	R488	DPLL2_FB2_NUM							
0x1E9	R489	DPLL2_FB2_DEN_39:32							
0x1EA	R490	DPLL2_FB2_DEN_31:24							
0x1EB	R491	DPLL2_FB2_DEN_23:16							
0x1EC	R492	DPLL2_FB2_DEN_15:8							
0x1ED	R493	DPLL2_FB2_DEN							
0x1EE	R494	RESERVED		DPLL2_REF5_FB_SEL	RESERVED	DPLL2_REF3_FB_SEL	DPLL2_REF2_FB_SEL	DPLL2_REF1_FB_SEL	DPLL2_REF0_FB_SEL
0x1EF	R495	RESERVED					DPLL2_FB_MASH_ORDER		
0x1F0	R496	RESERVED		DPLL2_FB_FDEV_37:32					
0x1F1	R497	DPLL2_FB_FDEV_31:24							
0x1F2	R498	DPLL2_FB_FDEV_23:16							
0x1F3	R499	DPLL2_FB_FDEV_15:8							
0x1F4	R500	DPLL2_FB_FDEV							
0x1F5	R501	RESERVED							DPLL2_FB_FDEV_UPDATE
0x1F6	R502	RESERVED							DPLL2_FB_FDEV_EN
0x1F7	R503	DPLL2_FB_NUM_STAT_39:32							
0x1F8	R504	DPLL2_FB_NUM_STAT_31:24							
0x1F9	R505	DPLL2_FB_NUM_STAT_23:16							
0x1FA	R506	DPLL2_FB_NUM_STAT_15:8							
0x1FB	R507	DPLL2_FB_NUM_STAT							
0x1FC	R508	RESERVED				DPLL2_REF0_DBLR_EN	DPLL2_REF1_DBLR_EN	DPLL2_REF2_DBLR_EN	DPLL2_REF3_DBLR_EN
0x1FD	R509	DPLL2_REF0_RDIV_15:8							
0x1FE	R510	DPLL2_REF0_RDIV							
0x1FF	R511	DPLL2_REF1_RDIV_15:8							
0x200	R512	DPLL2_REF1_RDIV							
0x201	R513	DPLL2_REF2_RDIV_15:8							
0x202	R514	DPLL2_REF2_RDIV							
0x203	R515	DPLL2_REF3_RDIV_15:8							
0x204	R516	DPLL2_REF3_RDIV							
0x205	R517	DPLL2_REF4_RDIV_15:8							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x206	R518	DPLL2_REF4_RDIV							
0x207	R519	DPLL2_REF5_RDIV_15:8							
0x208	R520	DPLL2_REF5_RDIV							
0x20B	R523	RESERVED		DPLL3_REF0_AUTO_PRTY			DPLL3_REF1_AUTO_PRTY		
0x20C	R524	RESERVED		DPLL3_REF2_AUTO_PRTY			DPLL3_REF3_AUTO_PRTY		
0x20D	R525	RESERVED		DPLL3_REF4_AUTO_PRTY			DPLL3_REF5_AUTO_PRTY		
0x20E	R526	RESERVED		DPLL3_MAN_REFSEL			DPLL3_MAN_SWITCH_PIN_MODE	DPLL3_SWITCH_MODE	
0x20F	R527	RESERVED		DPLL3_REFSEL_STAT					
0x210	R528	DPLL3_LOCKDET_PPM_EN	DPLL3_LOCKDET_PPM_MAX_14:8						
0x211	R529	DPLL3_LOCKDET_PPM_MAX							
0x212	R530	RESERVED	DPLL3_UNLOCKDET_PPM_MAX_14:8						
0x213	R531	DPLL3_UNLOCKDET_PPM_MAX							
0x214	R532	RESERVED		DPLL3_LOCKDET2_PPM_CNTSTRT_29:24					
0x215	R533	DPLL3_LOCKDET2_PPM_CNTSTRT_23:16							
0x216	R534	DPLL3_LOCKDET2_PPM_CNTSTRT_15:8							
0x217	R535	DPLL3_LOCKDET2_PPM_CNTSTRT							
0x218	R536	RESERVED		DPLL3_LOCKDET_PPM_CNTSTRT_29:24					
0x219	R537	DPLL3_LOCKDET_PPM_CNTSTRT_23:16							
0x21A	R538	DPLL3_LOCKDET_PPM_CNTSTRT_15:8							
0x21B	R539	DPLL3_LOCKDET_PPM_CNTSTRT							
0x21C	R540	RESERVED		DPLL3_LOCKDET_VCO_PPM_CNTSTRT_29:24					
0x21D	R541	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_23:16							
0x21E	R542	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_15:8							
0x21F	R543	DPLL3_LOCKDET_VCO_PPM_CNTSTRT							
0x220	R544	RESERVED							DPLL3_STATUS_PPM_LOCK
0x223	R547	DPLL3_LOOP_EN	DPLL3_PHASE_CANCEL_EN	DPLL3_FASTLOCK_ALWAYS	DPLL3_PHS1_EN	DPLL3_ZDM_EN	DPLL3_HIST_EN	DPLL3_PHASE_CANCEL_ALWAYS	RESERVED
0x224	R548	DPLL3_HOLD_SLEW_LIM_EN	RESERVED						
0x226	R550	RESERVED			DPLL3_PH_OFFSET_44:40				
0x227	R551	DPLL3_PH_OFFSET_39:32							
0x228	R552	DPLL3_PH_OFFSET_31:24							
0x229	R553	DPLL3_PH_OFFSET_23:16							
0x22A	R554	DPLL3_PH_OFFSET_15:8							
0x22B	R555	DPLL3_PH_OFFSET							
0x22C	R556	DPLL3_FREE_RUN_39:32							
0x22D	R557	DPLL3_FREE_RUN_31:24							
0x22E	R558	DPLL3_FREE_RUN_23:16							
0x22F	R559	DPLL3_FREE_RUN_15:8							
0x230	R560	DPLL3_FREE_RUN							
0x231	R561	DPLL3_PPM_REF_SEL	RESERVED						

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x24E	R590	RESERVED						DPLL3_LCK_TIMER_9:8	
0x24F	R591	DPLL3_LCK_TIMER							
0x250	R592	RESERVED						DPLL3_HIST_TIMER_9:8	
0x251	R593	DPLL3_HIST_TIMER							
0x252	R594	RESERVED						DPLL3_HOLD_TIMER_9:8	
0x253	R595	DPLL3_HOLD_TIMER							
0x254	R596	RESERVED						DPLL3_PHS1_TIMER_9:8	
0x255	R597	DPLL3_PHS1_TIMER							
0x25A	R602	RESERVED			DPLL3_HIST_GAIN				
0x25B	R603	RESERVED		DPLL3_PL_THRESH					
0x25C	R604	RESERVED		DPLL3_PL_UNLK_THRESH					
0x25D	R605	RESERVED		DPLL3_PHS1_THRESH					
0x262	R610	RESERVED		DPLL3_STATUS_PL	RESERVED				
0x263	R611	RESERVED			DPLL3_DCO_SLEW_ACTIVE	RESERVED			
0x266	R614	RESERVED							DPLL3_FB_DIV_32:32
0x267	R615	DPLL3_FB_DIV_31:24							
0x268	R616	DPLL3_FB_DIV_23:16							
0x269	R617	DPLL3_FB_DIV_15:8							
0x26A	R618	DPLL3_FB_DIV							
0x26B	R619	DPLL3_FB_NUM_39:32							
0x26C	R620	DPLL3_FB_NUM_31:24							
0x26D	R621	DPLL3_FB_NUM_23:16							
0x26E	R622	DPLL3_FB_NUM_15:8							
0x26F	R623	DPLL3_FB_NUM							
0x270	R624	DPLL3_FB_DEN_39:32							
0x271	R625	DPLL3_FB_DEN_31:24							
0x272	R626	DPLL3_FB_DEN_23:16							
0x273	R627	DPLL3_FB_DEN_15:8							
0x274	R628	DPLL3_FB_DEN							
0x275	R629	RESERVED							DPLL3_FB2_DIV_32:32
0x276	R630	DPLL3_FB2_DIV_31:24							
0x277	R631	DPLL3_FB2_DIV_23:16							
0x278	R632	DPLL3_FB2_DIV_15:8							
0x279	R633	DPLL3_FB2_DIV							
0x27A	R634	DPLL3_FB2_NUM_39:32							
0x27B	R635	DPLL3_FB2_NUM_31:24							
0x27C	R636	DPLL3_FB2_NUM_23:16							
0x27D	R637	DPLL3_FB2_NUM_15:8							
0x27E	R638	DPLL3_FB2_NUM							
0x27F	R639	DPLL3_FB2_DEN_39:32							
0x280	R640	DPLL3_FB2_DEN_31:24							
0x281	R641	DPLL3_FB2_DEN_23:16							
0x282	R642	DPLL3_FB2_DEN_15:8							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x283	R643	DPLL3_FB2_DEN							
0x284	R644	RESERVED		DPLL3_REF5_FB_SEL	DPLL3_REF4_FB_SEL	DPLL3_REF3_FB_SEL	DPLL3_REF2_FB_SEL	DPLL3_REF1_FB_SEL	DPLL3_REF0_FB_SEL
0x285	R645	RESERVED					DPLL3_FB_MASH_ORDER		
0x286	R646	RESERVED		DPLL3_FB_FDEV_37:32					
0x287	R647	DPLL3_FB_FDEV_31:24							
0x288	R648	DPLL3_FB_FDEV_23:16							
0x289	R649	DPLL3_FB_FDEV_15:8							
0x28A	R650	DPLL3_FB_FDEV							
0x28B	R651	RESERVED							DPLL3_FB_FDEV_UPDATE
0x28C	R652	RESERVED							DPLL3_FB_FDEV_EN
0x28D	R653	DPLL3_FB_NUM_STAT_39:32							
0x28E	R654	DPLL3_FB_NUM_STAT_31:24							
0x28F	R655	DPLL3_FB_NUM_STAT_23:16							
0x290	R656	DPLL3_FB_NUM_STAT_15:8							
0x291	R657	DPLL3_FB_NUM_STAT							
0x292	R658	RESERVED				DPLL3_REF0_DBLR_EN	DPLL3_REF1_DBLR_EN	DPLL3_REF2_DBLR_EN	DPLL3_REF3_DBLR_EN
0x293	R659	DPLL3_REF0_RDIV_15:8							
0x294	R660	DPLL3_REF0_RDIV							
0x295	R661	DPLL3_REF1_RDIV_15:8							
0x296	R662	DPLL3_REF1_RDIV							
0x297	R663	DPLL3_REF2_RDIV_15:8							
0x298	R664	DPLL3_REF2_RDIV							
0x299	R665	DPLL3_REF3_RDIV_15:8							
0x29A	R666	DPLL3_REF3_RDIV							
0x29B	R667	DPLL3_REF4_RDIV_15:8							
0x29C	R668	DPLL3_REF4_RDIV							
0x29D	R669	DPLL3_REF5_RDIV_15:8							
0x29E	R670	DPLL3_REF5_RDIV							
0x2C3	R707	PLL1_CP_PU_R							
0x2C4	R708	RESERVED						PLL1_CPG	
0x2C5	R709	RESERVED		PLL1_LF_R2					
0x2C6	R710	RESERVED		PLL1_LF_R3					
0x2C7	R711	RESERVED		PLL1_LF_R4					
0x2C8	R712	PLL1_DISABLE_3RD4TH		PLL1_LF_C3			PLL1_LF_C4		
0x2C9	R713	RESERVED							PLL1_RDIV_8:8
0x2CA	R714	PLL1_RDIV							
0x2CB	R715	RESERVED			PLL1_RDIV_XO_EN	PLL1_RDIV_XO_DBLR_EN	PLL1_RDIV_BYPASS_EN	PLL1_RDIV_MUX_SEL	
0x2CC	R716	RESERVED							PLL1_NDIV_8:8
0x2CD	R717	PLL1_NDIV							
0x2CE	R718	PLL1_NUM_MSB							
0x2CF	R719	PLL1_NUM_39:32							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2D0	R720	PLL1_NUM_31:24							
0x2D1	R721	PLL1_NUM_23:16							
0x2D2	R722	PLL1_NUM_15:8							
0x2D3	R723	PLL1_NUM							
0x2D4	R724	RESERVED		PLL1_DTHRMODE		PLL1_ORDER			PLL1_MODE
0x2D5	R725	APLL1_NUM_STAT_39:32							
0x2D6	R726	APLL1_NUM_STAT_31:24							
0x2D7	R727	APLL1_NUM_STAT_23:16							
0x2D8	R728	APLL1_NUM_STAT_15:8							
0x2D9	R729	APLL1_NUM_STAT							
0x2DB	R731	PLL1_PRI_DIV_SYNC_EN	PLL1_PRI_DIV_EN	PLL1_PRI_DIV			PLL1_PRI_DIV_DRVR_EN		
0x2DC	R732	PLL1_SEC_DIV_SYNC_EN	PLL1_SEC_DIV_EN	PLL1_SEC_DIV			PLL1_SEC_DIV_DRVR_EN		
0x2DD	R733	PLL1_VCO_BUF_EN	PLL1_VCO_BUF_2REF_EN		PLL1_VCO_BUF_2DPLL_EN	RESERVED	PLL1_VCO_BUF_PPM_CHECK_EN	PLL1_VCO_BUF_FB_TDC_EN	
0x2E0	R736	RESERVED				PLL1_RDIV_TEST_EN	RESERVED		
0x2E5	R741	RESERVED		PLL1_VM_INSIDE	PLL1_VM_HI	RESERVED			
0x2E9	R745	RESERVED		PLL1_NDIV_TEST_EN	RESERVED				
0x2EA	R746	RESERVED							PLL1_VCO_PREBUF_EN
0x305	R773	RESERVED							
0x309	R777	PLL2_CP_PU_R							
0x30A	R778	RESERVED			PLL2_CP_PU_DIS	PLL2_CPG			
0x30B	R779	PLL2_LF_R2							
0x30C	R780	RESERVED		PLL2_LF_R3					
0x30D	R781	RESERVED		PLL2_LF_R4					
0x30E	R782	PLL2_DISABLE_3RD4TH		PLL2_LF_C3		PLL2_LF_C4			
0x30F	R783	RESERVED							PLL2_RDIV_8:8
0x310	R784	PLL2_RDIV							
0x311	R785	RESERVED			PLL2_RDIV_XO_EN	PLL2_RDIV_XO_DBLR_EN	PLL2_RDIV_BYPASS_EN	PLL2_RDIV_MUX_SEL	
0x312	R786	RESERVED							PLL2_NDIV_8:8
0x313	R787	PLL2_NDIV							
0x314	R788	PLL2_NUM_MSB							
0x315	R789	PLL2_NUM_39:32							
0x316	R790	PLL2_NUM_31:24							
0x317	R791	PLL2_NUM_23:16							
0x318	R792	PLL2_NUM_15:8							
0x319	R793	PLL2_NUM							
0x31A	R794	RESERVED		PLL2_DTHRMODE		PLL2_ORDER			PLL2_MODE

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x31B	R795	APLL2_NUM_STAT_39:32							
0x31C	R796	APLL2_NUM_STAT_31:24							
0x31D	R797	APLL2_NUM_STAT_23:16							
0x31E	R798	APLL2_NUM_STAT_15:8							
0x31F	R799	APLL2_NUM_STAT							
0x323	R803	RESERVED			PLL2_VCO_BUF_EN	PLL2_VCO_BUF_2REF_EN		PLL2_VCO_BUF_2DPLL_EN	PLL2_VCO_BUF_2WNDDET_EN
0x324	R804	RESERVED		PLL2_VCO_DIV_SYNC_EN	PLL2_VCO_DIV_EN	PLL2_VCO_DIV			
0x325	R805	RESERVED	PLL2_VCO_BUF_FB_TDC_EN		PLL2_VCO_DIV_DRVR_EN				
0x328	R808	RESERVED				PLL2_RDIV_TEST_EN	RESERVED		
0x32D	R813	RESERVED		PLL2_VM_INSIDE	PLL2_VM_HI	RESERVED			
0x332	R818	RESERVED		PLL2_NDIV_TEST_EN	RESERVED				
0x333	R819	RESERVED							PLL2_VCO_PREBUF_EN
0x348	R840	PLL3_CPBAW_BLEED							
0x349	R841	RESERVED			PLL3_CP_PU_DIS	PLL3_CPG			
0x34A	R842	RESERVED		PLL3_LF_R2					
0x34B	R843	RESERVED		PLL3_LF_R3					
0x34C	R844	RESERVED		PLL3_LF_R4					
0x34D	R845	RESERVED		PLL3_LF_C3			PLL3_LF_C4		
0x34E	R846	RESERVED							PLL3_RDIV_8:8
0x34F	R847	PLL3_RDIV							
0x350	R848	RESERVED			PLL3_RDIV_XO_EN	PLL3_RDIV_XO_DBLR_EN	PLL3_RDIV_BYPASS_EN	PLL3_RDIV_MUX_SEL	
0x351	R849	RESERVED							PLL3_NDIV_8:8
0x352	R850	PLL3_NDIV							
0x353	R851	PLL3_NUM_MSB							
0x354	R852	PLL3_NUM_39:32							
0x355	R853	PLL3_NUM_31:24							
0x356	R854	PLL3_NUM_23:16							
0x357	R855	PLL3_NUM_15:8							
0x358	R856	PLL3_NUM							
0x359	R857	RESERVED		PLL3_DTHRMODE		PLL3_ORDER			PLL3_MODE
0x35A	R858	APLL3_NUM_STAT_39:32							
0x35B	R859	APLL3_NUM_STAT_31:24							
0x35C	R860	APLL3_NUM_STAT_23:16							
0x35D	R861	APLL3_NUM_STAT_15:8							
0x35E	R862	APLL3_NUM_STAT							
0x360	R864	PLL3_VCO_BUF_OUT_EN				PLL3_VCO_DIV_SYNC_EN	PLL3_PRI_DIV		

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x361	R865	PLL3_VCO_DIV_SEL		PLL3_VCO_CHAN_DRVR_IN_EN	PLL3_CHAN_EN				
0x362	R866	RESERVED			PLL3_VCO_BUF_2REF_EN		PLL3_WIN_DET_DRVR_EN	PLL3_VCO_BUF_FB_TDC_EN	
0x368	R872	RESERVED			PLL3_NCLK_TEST_EN	PLL3_RDIV_TEST_EN	RESERVED		
0x3C1	R961	RESERVED	OUT_0_EN	OUT_0_VCM			OUT_0_VOD		
0x3C2	R962	OUT_0_CAP_EN	OUT_0_STATIC_LOW	OUT_0_P_CMOS_EN	OUT_0_N_CMOS_EN	OUT_0_P_INVERT_POLARITY	OUT_0_N_INVERT_POLARITY	OUT_0_P_FORCELOW	OUT_0_N_FORCELOW
0x3C3	R963	OUT_0_CONFIGURATION							
0x3C4	R964	RESERVED	OUT_1_EN	OUT_1_VCM			OUT_1_VOD		
0x3C5	R965	OUT_1_CAP_EN	OUT_1_STATIC_LOW	OUT_1_P_CMOS_EN	OUT_1_N_CMOS_EN	OUT_1_P_INVERT_POLARITY	OUT_1_N_INVERT_POLARITY	OUT_1_P_FORCELOW	OUT_1_N_FORCELOW
0x3C6	R966	OUT_1_CONFIGURATION							
0x3C7	R967	RESERVED						OUT_0_1_CMOS_OUT_VOLTAGE_SEL	OUT_0_1_CMOS_OUT_LDO_EN
0x3C8	R968	RESERVED				OUT_0_1_ZDM_TDC_SEL			OUT_0_1_ZDM_EN
0x3C9	R969	RESERVED	OUT_0_1_DIV_MUTE_EN	OUT_0_1_DIV_SYNC_EN	OUT_0_1_SR_DIV_SYNC_EN	OUT_0_1_CH0_CHAN_POL_SEL	OUT_0_1_CH1_CHAN_POL_SEL	OUT_0_1_CH0_DIV_EN	OUT_0_1_CH1_DIV_EN
0x3CC	R972	RESERVED						OUT_0_1_CH0_CH_DIV_SR_MUX_CLK_SEL	RESERVED
0x3CD	R973	OUT_0_1_CLK_IN_FANOUT						RESERVED	
0x3CE	R974	RESERVED				OUT_0_1_CH0_CH_STATIC_OFFSET_11:8			
0x3CF	R975	OUT_0_1_CH0_CH_STATIC_OFFSET							
0x3D0	R976	RESERVED				OUT_0_1_CH1_CH_STATIC_OFFSET_11:8			
0x3D1	R977	OUT_0_1_CH1_CH_STATIC_OFFSET							
0x3D2	R978	RESERVED				OUT_0_1_CH0_CH_DIV_11:8			
0x3D3	R979	OUT_0_1_CH0_CH_DIV							
0x3D4	R980	RESERVED				OUT_0_1_CH1_CH_DIV_11:8			
0x3D5	R981	OUT_0_1_CH1_CH_DIV							
0x3D6	R982	RESERVED			OUT_0_1_SR_ANA_DELAY				
0x3D7	R983	RESERVED		OUT_0_1_SR_ANA_DELAY_DIV2_SEL	OUT_0_1_SR_ANA_DELAY_EN	OUT_0_1_SR_ANA_DELAY_SMALL_STEP_EN	OUT_0_1_SR_ANA_DELAY_RANGE		
0x3D8	R984	RESERVED			OUT_0_1_SR_DDLY				
0x3D9	R985	RESERVED				OUT_0_1_SR_DIV_19:16			
0x3DA	R986	OUT_0_1_SR_DIV_15:8							
0x3DB	R987	OUT_0_1_SR_DIV							
0x3DC	R988	RESERVED	OUT_0_1_SR_DIV_STATIC_OFFSET_14:8						
0x3DD	R989	OUT_0_1_SR_DIV_STATIC_OFFSET							
0x3DE	R990	OUT_0_1_SR_REQ_MODE	OUT_0_1_SR_GPIO_EN	RESERVED	OUT_0_1_PULSE_COUNT			OUT_0_1_SR_MODE	

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x3DF	R991	RESERVED		OUT_0_1_SR_CH0_DIV_BYPASS	RESERVED				
0x400	R1024	RESERVED	OUT_2_EN	OUT_2_VCM			OUT_2_VOD		
0x401	R1025	RESERVED				OUT_2_CAP_EN	OUT_2_CONFIGURATION		
0x402	R1026	OUT_2_CHAN_POL_SEL	OUT_2_CLK_MUX		RESERVED	OUT_2_DIV_EN	OUT_2_CH_MUX_SEL		
0x403	R1027	RESERVED			OUT_2_MUTE_EN	OUT_2_SYNC_EN	RESERVED		
0x404	R1028	RESERVED				OUT_2_CH_STATIC_OFFSET_11:8			
0x405	R1029	OUT_2_CH_STATIC_OFFSET							
0x406	R1030	RESERVED				OUT_2_CH_DIV_11:8			
0x407	R1031	OUT_2_CH_DIV							
0x420	R1056	RESERVED	OUT_3_EN	OUT_3_VCM			OUT_3_VOD		
0x421	R1057	RESERVED				OUT_3_CAP_EN	OUT_3_CONFIGURATION		
0x422	R1058	OUT_3_CHAN_POL_SEL	OUT_3_CLK_MUX		RESERVED	OUT_3_DIV_EN	OUT_3_CH_MUX_SEL		
0x423	R1059	RESERVED			OUT_3_MUTE_EN	OUT_3_SYNC_EN	RESERVED		
0x424	R1060	RESERVED				OUT_3_CH_STATIC_OFFSET_11:8			
0x425	R1061	OUT_3_CH_STATIC_OFFSET							
0x426	R1062	RESERVED				OUT_3_CH_DIV_11:8			
0x427	R1063	OUT_3_CH_DIV							
0x440	R1088	RESERVED					OUT_4_5_SR_ANA_DLY_BIASTRIM		
0x441	R1089	RESERVED	OUT_4_EN	OUT_4_VCM			OUT_4_VOD		
0x442	R1090	RESERVED	OUT_4_CAP_EN	RESERVED	OUT_4_CONFIGURATION				
0x443	R1091	RESERVED	OUT_5_EN	OUT_5_VCM			OUT_5_VOD		
0x444	R1092	RESERVED	OUT_5_CAP_EN	RESERVED	OUT_5_CONFIGURATION				
0x445	R1093	RESERVED		OUT_4_5_DIV_SYNC_EN	OUT_4_5_SR_DIV_SYNC_EN	RESERVED		OUT_4_5_CHAN_POL_SEL	OUT_4_5_DIV_EN
0x446	R1094	OUT_4_5_MUTE_EN	OUT_4_5_ZDM_EN	OUT_4_5_CLK_IN_SEL	OUT_4_5_CH_DIV_SR_MUX_CLK_SEL	OUT_4_5_CH_MUX_SEL			
0x447	R1095	RESERVED				OUT_4_5_CH_STATIC_OFFSET_11:8			
0x448	R1096	OUT_4_5_CH_STATIC_OFFSET							
0x449	R1097	RESERVED				OUT_4_5_CH_DIV_11:8			
0x44A	R1098	OUT_4_5_CH_DIV							
0x44B	R1099	RESERVED			OUT_4_5_SR_ANA_DELAY				
0x44C	R1100	RESERVED		OUT_4_5_SR_ANA_DELAY_DIV2_SEL	OUT_4_5_SR_ANA_DELAY_EN	OUT_4_5_SR_ANA_DELAY_SMALL_STEP_EN	OUT_4_5_SR_ANA_DELAY_RANGE		
0x44D	R1101	RESERVED			OUT_4_5_SR_DDLY				
0x44E	R1102	RESERVED				OUT_4_5_SR_DIV_19:16			
0x44F	R1103	OUT_4_5_SR_DIV_15:8							
0x450	R1104	OUT_4_5_SR_DIV							

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x451	R1105	RESERVED	OUT_4_5_SR_DIV_STATIC_OFFSET_14:8						
0x452	R1106	OUT_4_5_SR_DIV_STATIC_OFFSET							
0x453	R1107	RESERVED	OUT_4_5_SR_REQ_MODE	OUT_4_5_PULSE_COUNT			OUT_4_5_SR_GPIO_EN	OUT_4_5_SR_MODE	
0x454	R1108	RESERVED			OUT_4_5_SR_CH_DIV_BYPASS	RESERVED			
0x461	R1121	RESERVED	OUT_6_EN	OUT_6_VCM			OUT_6_VOD		
0x462	R1122	RESERVED	OUT_6_CAP_EN	RESERVED	OUT_6_CONFIGURATION				
0x463	R1123	RESERVED	OUT_7_EN	OUT_7_VCM			OUT_7_VOD		
0x464	R1124	RESERVED	OUT_7_CAP_EN	RESERVED	OUT_7_CONFIGURATION				
0x465	R1125	RESERVED		OUT_6_7_DIV_SYNC_EN	OUT_6_7_SR_DIV_SYNC_EN	RESERVED		OUT_6_7_CHAN_POL_SEL	OUT_6_7_DIV_EN
0x466	R1126	OUT_6_7_MUTE_EN	RESERVED	OUT_6_7_CLK_IN_SEL	OUT_6_7_CH_DIV_SR_MUX_CLK_SEL	OUT_6_7_CH_MUX_SEL			
0x467	R1127	RESERVED				OUT_6_7_CH_STATIC_OFFSET_11:8			
0x468	R1128	OUT_6_7_CH_STATIC_OFFSET							
0x469	R1129	RESERVED				OUT_6_7_CH_DIV_11:8			
0x46A	R1130	OUT_6_7_CH_DIV							
0x46B	R1131	RESERVED			OUT_6_7_SR_ANA_DELAY				
0x46C	R1132	RESERVED		OUT_6_7_SR_ANA_DELAY_DIV2_SEL	OUT_6_7_SR_ANA_DELAY_EN	OUT_6_7_SR_ANA_DELAY_SMALL_STEP_EN	OUT_6_7_SR_ANA_DELAY_RANGE		
0x46D	R1133	RESERVED			OUT_6_7_SR_DDLY				
0x46E	R1134	RESERVED				OUT_6_7_SR_DIV_19:16			
0x46F	R1135	OUT_6_7_SR_DIV_15:8							
0x470	R1136	OUT_6_7_SR_DIV							
0x471	R1137	RESERVED	OUT_6_7_SR_DIV_STATIC_OFFSET_14:8						
0x472	R1138	OUT_6_7_SR_DIV_STATIC_OFFSET							
0x473	R1139	RESERVED	OUT_6_7_SR_REQ_MODE	OUT_6_7_PULSE_COUNT			OUT_6_7_SR_GPIO_EN	OUT_6_7_SR_MODE	
0x474	R1140	RESERVED			OUT_6_7_SR_CH_DIV_BYPASS	RESERVED			
0x481	R1153	RESERVED	OUT_8_EN	OUT_8_VCM			OUT_8_VOD		
0x482	R1154	RESERVED	OUT_8_CAP_EN	RESERVED	OUT_8_CONFIGURATION				
0x483	R1155	RESERVED	OUT_9_EN	OUT_9_VCM			OUT_9_VOD		
0x484	R1156	RESERVED	OUT_9_CAP_EN	RESERVED	OUT_9_CONFIGURATION				
0x485	R1157	RESERVED		OUT_8_9_DIV_SYNC_EN	OUT_8_9_SR_DIV_SYNC_EN	RESERVED		OUT_8_9_CHAN_POL_SEL	OUT_8_9_DIV_EN
0x486	R1158	OUT_8_9_MUTE_EN	RESERVED	OUT_8_9_CLK_IN_SEL	OUT_8_9_CH_DIV_SR_MUX_CLK_SEL	OUT_8_9_CH_MUX_SEL			

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x487	R1159	RESERVED				OUT_8_9_CH_STATIC_OFFSET_11:8			
0x488	R1160	OUT_8_9_CH_STATIC_OFFSET							
0x489	R1161	RESERVED				OUT_8_9_CH_DIV_11:8			
0x48A	R1162	OUT_8_9_CH_DIV							
0x48B	R1163	RESERVED			OUT_8_9_SR_ANA_DELAY				
0x48C	R1164	RESERVED		OUT_8_9_SR_ANA_DELAY_DIV2_SEL	OUT_8_9_SR_ANA_DELAY_EN	OUT_8_9_SR_ANA_DELAY_SMALL_STEP_EN	OUT_8_9_SR_ANA_DELAY_RANGE		
0x48D	R1165	RESERVED			OUT_8_9_SR_DDLY				
0x48E	R1166	RESERVED				OUT_8_9_SR_DIV_19:16			
0x48F	R1167	OUT_8_9_SR_DIV_15:8							
0x490	R1168	OUT_8_9_SR_DIV							
0x491	R1169	RESERVED	OUT_8_9_SR_DIV_STATIC_OFFSET_14:8						
0x492	R1170	OUT_8_9_SR_DIV_STATIC_OFFSET							
0x493	R1171	RESERVED	OUT_8_9_SR_REQ_MODE	OUT_8_9_PULSE_COUNT			OUT_8_9_SR_GPIO_EN	OUT_8_9_SR_MODE	
0x4A1	R1185	RESERVED	OUT_10_EN	OUT_10_VCM			OUT_10_VOD		
0x4A2	R1186	RESERVED	OUT_10_CAP_EN	RESERVED	OUT_10_CONFIGURATION				
0x4A3	R1187	RESERVED	OUT_11_EN	OUT_11_VCM			OUT_11_VOD		
0x4A4	R1188	RESERVED	OUT_11_CAP_EN	RESERVED	OUT_11_CONFIGURATION				
0x4A5	R1189	RESERVED		OUT_10_11_DIV_SYNC_EN	OUT_10_11_SR_DIV_SYNC_EN	RESERVED		OUT_10_11_CHAN_POL_SEL	OUT_10_11_DIV_EN
0x4A6	R1190	OUT_10_11_MUTE_EN	OUT_10_11_ZDM_EN	OUT_10_11_CLK_IN_SEL	OUT_10_11_CH_DIV_SR_MUX_CLK_SEL	OUT_10_11_CH_MUX_SEL			
0x4A7	R1191	RESERVED				OUT_10_11_CH_STATIC_OFFSET_11:8			
0x4A8	R1192	OUT_10_11_CH_STATIC_OFFSET							
0x4A9	R1193	RESERVED				OUT_10_11_CH_DIV_11:8			
0x4AA	R1194	OUT_10_11_CH_DIV							
0x4AB	R1195	RESERVED			OUT_10_11_SR_ANA_DELAY				
0x4AC	R1196	RESERVED		OUT_10_11_SR_ANA_DELAY_DIV2_SEL	OUT_10_11_SR_ANA_DELAY_EN	OUT_10_11_SR_ANA_DELAY_SMALL_STEP_EN	OUT_10_11_SR_ANA_DELAY_RANGE		
0x4AD	R1197	RESERVED			OUT_10_11_SR_DDLY				
0x4AE	R1198	RESERVED				OUT_10_11_SR_DIV_19:16			
0x4AF	R1199	OUT_10_11_SR_DIV_15:8							
0x4B0	R1200	OUT_10_11_SR_DIV							
0x4B1	R1201	RESERVED	OUT_10_11_SR_DIV_STATIC_OFFSET_14:8						
0x4B2	R1202	OUT_10_11_SR_DIV_STATIC_OFFSET							
0x4B3	R1203	RESERVED	OUT_10_11_SR_REQ_MODE	OUT_10_11_PULSE_COUNT			OUT_10_11_SR_GPIO_EN	OUT_10_11_SR_MODE	
0x4B4	R1204	RESERVED			OUT_10_11_SR_CH_DIV_BYPASS	RESERVED			
0x4C1	R1217	RESERVED	OUT_12_EN	OUT_12_VCM			OUT_12_VOD		

Table 1-1. DEVICE Registers (continued)

Offset	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4C2	R1218	RESERVED	OUT_12_CAP_EN	RESERVED	OUT_12_CONFIGURATION				
0x4C3	R1219	RESERVED	OUT_13_EN	OUT_13_VCM			OUT_13_VOD		
0x4C4	R1220	RESERVED	OUT_13_CAP_EN	RESERVED	OUT_13_CONFIGURATION				
0x4C5	R1221	RESERVED		OUT_12_13_DIV_SYNC_EN	OUT_12_13_SR_DIV_SYNC_EN	RESERVED		OUT_12_13_CHAN_POL_SEL	OUT_12_13_DIV_EN
0x4C6	R1222	OUT_12_13_MUTE_EN	RESERVED	OUT_12_13_CLK_IN_SEL	OUT_12_13_CH_DIV_SR_MUX_CLK_SEL	OUT_12_13_CH_MUX_SEL			
0x4C7	R1223	RESERVED				OUT_12_13_CH_STATIC_OFFSET_11:8			
0x4C8	R1224	OUT_12_13_CH_STATIC_OFFSET							
0x4C9	R1225	RESERVED				OUT_12_13_CH_DIV_11:8			
0x4CA	R1226	OUT_12_13_CH_DIV							
0x4CB	R1227	RESERVED			OUT_12_13_SR_ANA_DELAY				
0x4CC	R1228	RESERVED		OUT_12_13_SR_ANA_DELAY_DIV2_SEL	OUT_12_13_SR_ANA_DELAY_EN	OUT_12_13_SR_ANA_DELAY_SMALL_STEP_EN	OUT_12_13_SR_ANA_DELAY_RANGE		
0x4CD	R1229	RESERVED			OUT_12_13_SR_DDLY				
0x4CE	R1230	RESERVED				OUT_12_13_SR_DIV_19:16			
0x4CF	R1231	OUT_12_13_SR_DIV_15:8							
0x4D0	R1232	OUT_12_13_SR_DIV							
0x4D1	R1233	RESERVED	OUT_12_13_SR_DIV_STATIC_OFFSET_14:8						
0x4D2	R1234	OUT_12_13_SR_DIV_STATIC_OFFSET							
0x4D3	R1235	RESERVED	OUT_12_13_SR_REQ_MODE	OUT_12_13_PULSE_COUNT			OUT_12_13_SR_GPIO_EN	OUT_12_13_SR_MODE	
0x4D4	R1236	RESERVED			OUT_12_13_SR_CH_DIV_BYPASS	RESERVED			

Complex bit access types are encoded to fit into small table cells. Table 1-2 shows the codes that are used for access types in this section.

Table 1-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WSC	W	Write
Reset or Default Value		
-n		Value after reset or the default value

1.1 R0 Register (Offset = 0x0) [Reset = 0x10]

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Table 1-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID_15:8	R	0x10	See Register 1

1.2 R1 Register (Offset = 0x1) [Reset = 0x0B]

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Table 1-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID	R	0xB	Vendor Identification Number. The Vendor Identification Number is a unique 16-bit identification number assigned to I2C/SMBus vendors. ROM=N, EEPROM=N

1.3 R2 Register (Offset = 0x2) [Reset = 0x32]

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Table 1-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODID	R	0x32	Product ID. ROM=N, EEPROM=N

1.4 R3 Register (Offset = 0x3) [Reset = 0x01]

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Table 1-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REVID	R	0x1	Revision ID. LMK5B33216 = 0x01 ROM=N, EEPROM=N

1.5 R16 Register (Offset = 0x10) [Reset = 0x00]

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Table 1-7. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMCNT	R	0x0	NVM Program Count. The NVMCNT increments automatically after every EEPROM Erase/Program Cycle. The NVMCNT value is retrieved automatically after reset, after a NVM Commit operation, or after a Erase/Program cycle. The NVMCNT register will increment until it reaches it's maximum value of 255 after which no further increments will take place. ROM=N, EEPROM=Y

1.6 R18 Register (Offset = 0x12) [Reset = 0x19]

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Table 1-8. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Reserved

Table 1-8. R18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	TARGET_ADR_MSB	R	0x19	I2C/SMBus Target Address. This field holds the 5 MSB bits of the Target Address used to identify this device during I2C/SMBus transactions. The two least significant bits of the Target Address are defined by CSC/ADD/TEC pin upon power-up. This is user-writable to EEPROM only through SRAM register at address 12. ROM=N, EEPROM=Y

1.7 R19 Register (Offset = 0x13) [Reset = 0x00]

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Table 1-9. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EEREV	R/W	0x0	EEPROM Image Revision ID. EEPROM Image Revision is automatically retrieved from EEPROM and stored in the EEREV register after a reset or after a NVM commit operation. This is user-writable to EEPROM only through SRAM register address 13. ROM=N, EEPROM=Y

1.8 R20 Register (Offset = 0x14) [Reset = 0x00]

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Table 1-10. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ROM_PLUS_EE	R/W	0x0	When set, the thin EEPROM settings are loaded. This is user-writable to EEPROM only through SRAM register address 14. ROM=N, EEPROM=Y
6:3	EE_ROM_PAGE_SEL	R/W	0x0	EE_ROM_PAGE_SEL value is added to the GPIO pin value for selecting the start-up ROM. ROM=N, EEPROM=Y
2:0	RESERVED	R/W	0x0	Reserved

1.9 R21 Register (Offset = 0x15) [Reset = 0xA1]

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Table 1-11. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_3WIRE_DIS	R/W	0x1	Disable SPI 3 wire readback. The SDIO pin will remain input at all times. ROM=Y, EEPROM=N 0x0 = 3-wire SPI readback enabled 0x1 = 3-wire SPI readback disabled
6	SYNC_SW	R/W	0x0	Software SYNC Assertion. Writing a '1' to this bit is equivalent to asserting the SYNC pin. SYNC_EN must also be set to 1. ROM=Y, EEPROM=Y
5:0	RESERVED	R/W	0x21	Reserved

1.10 R22 Register (Offset = 0x16) [Reset = 0x35]

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Table 1-12. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-12. R22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DPLL3_EN	R/W	0x1	Enable DPLL3. ROM=Y, EEPROM=N
4	APLL3_EN	R/W	0x1	Enable APLL3. ROM=Y, EEPROM=Y
3	DPLL2_EN	R/W	0x0	Enable DPLL2. ROM=Y, EEPROM=N
2	APLL2_EN	R/W	0x1	Enable APLL2. ROM=Y, EEPROM=Y
1	DPLL1_EN	R/W	0x0	Enable DPLL1. ROM=Y, EEPROM=N
0	APLL1_EN	R/W	0x1	Enable APLL1. ROM=Y, EEPROM=Y

1.11 R23 Register (Offset = 0x17) [Reset = 0x00]

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Table 1-13. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	SWRST	R/W	0x0	Software Reset ALL functions (active low). Writing a '0' will cause the device to return to its power-up state apart from the programmed registers and the configuration controller. The configuration controller is excluded to prevent an re-transfer of EEPROM data to on-chip registers. Not a self clearing field. ROM=N, EEPROM=N
5:0	RESERVED	R-0/W1S	0x0	Reserved

1.12 R24 Register (Offset = 0x18) [Reset = 0x06]

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Table 1-14. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	APLL3_STRT_PRTY	R/W	0x0	APLL3 Start-up Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y
3:2	APLL2_STRT_PRTY	R/W	0x1	APLL2 Start-up Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y
1:0	APLL1_STRT_PRTY	R/W	0x2	APLL1 Start-up Priority. 0 is highest priority. APLLs with the same priority will start simultaneously. ROM=Y, EEPROM=Y

1.13 R25 Register (Offset = 0x19) [Reset = 0x00]

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Table 1-15. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:1	RESERVED	R/W	0x0	Reserved

Table 1-15. R25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SYNC_EN	R/W	0x0	Allows SYNC from SYNC_SW and GPIO pin. For GPIO sync, must be set together with SYNC input for GPIOx_MODE. ROM=Y, EEPROM=Y

1.14 R26 Register (Offset = 0x1A) [Reset = 0x00]

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Table 1-16. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	SYSREF_REQ_MODE	R/W	0x0	SYSREF Request Mode. Determines how a GPIO input is synchronized to generate a SYSREF request. ROM=Y, EEPROM=N 0x0 = Direct SYSREF request 0x1 = Reserved 0x2 = Reserved 0x3 = Resampled SYSREF request
3:1	SYSREF_REQ_SEL	R/W	0x0	SYSREF Request Select. Chooses which output drives the SYSREF_FB_CLK. ROM=Y, EEPROM=N 0x0 = SYSREF0_1_CLK 0x1 = SYSREF6_7_CLK 0x2 = SYSREF4_5_CLK 0x3 = SYSREF8_9_CLK 0x4 = SYSREF10_11_CLK 0x5 = SYSREF12_13_CLK 0x6 = Reserved
0	SYSREF_REQ_SW	R/WSC	0x0	Software SYSREF request trigger ROM=N, EEPROM=N

1.15 R27 Register (Offset = 0x1B) [Reset = 0x00]

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Table 1-17. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_39:32	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.16 R28 Register (Offset = 0x1C) [Reset = 0x00]

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Table 1-18. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_31:24	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.17 R29 Register (Offset = 0x1D) [Reset = 0x00]

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Table 1-19. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_23:16	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.18 R30 Register (Offset = 0x1E) [Reset = 0x00]

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Table 1-20. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR_15:8	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.19 R31 Register (Offset = 0x1F) [Reset = 0x00]

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Table 1-21. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TEC_CNTR	R	0x0	Time Elapsed Counter Readback ROM=N, EEPROM=N

1.20 R32 Register (Offset = 0x20) [Reset = 0x00]

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Table 1-22. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	TEC_CNTR_TRIG_SEL	R/W	0x0	Time Elapsed Counter trigger select. If using GPIO, must also set GPIOx_MODE to provide TEC trigger. ROM=Y, EEPROM=N 0x0 = SPI 0x1 = GPIO
0	TEC_CNTR_EN	R/W	0x0	Time Elapsed Counter counter enable. When transitioning from 0 --> 1, the TEC counter will start from 0. ROM=Y, EEPROM=N

1.21 R33 Register (Offset = 0x21) [Reset = 0x00]

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Table 1-23. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1	R	0x0	Loss of Lock - APLL1 ROM=N, EEPROM=N
2	LOL_PLL2	R	0x0	Loss of Lock - APLL2 ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO	R	0x0	Loss of Source Freq Detection - XO ROM=N, EEPROM=N

1.22 R34 Register (Offset = 0x22) [Reset = 0x00]

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Table 1-24. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1	R	0x0	Loss of Phase Lock - DPLL1 ROM=N, EEPROM=N
6	LOFL_DPLL1	R	0x0	Loss of Frequency Lock - DPLL1 ROM=N, EEPROM=N
5	RESERVED	R	0x0	Reserved
4	HLDOVR1	R	0x0	Holdover event - DPLL1 ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.23 R35 Register (Offset = 0x23) [Reset = 0x00]

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Table 1-25. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2	R	0x0	Loss of Phase Lock - DPLL2 ROM=N, EEPROM=N
6	LOFL_DPLL2	R	0x0	Loss of Frequency Lock - DPLL2 ROM=N, EEPROM=N
5	RESERVED	R	0x0	Reserved
4	HLDOVR2	R	0x0	Holdover event - DPLL2 ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.24 R36 Register (Offset = 0x24) [Reset = 0x00]

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Table 1-26. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3	R	0x0	Loss of Phase Lock - DPLL3 ROM=N, EEPROM=N
6	LOFL_DPLL3	R	0x0	Loss of Frequency Lock - DPLL3 ROM=N, EEPROM=N
5	RESERVED	R	0x0	Reserved
4	HLDOVR3	R	0x0	Holdover event - DPLL3 ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.25 R37 Register (Offset = 0x25) [Reset = 0x00]

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Table 1-27. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1_MASK	R/W	0x0	Masks Loss of Lock - APLL1. When LOL_PLL1_MASK is 1 then the LOL_PLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

Table 1-27. R37 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOL_PLL2_MASK	R/W	0x0	Masks Loss of Lock - APLL2. When LOL_PLL2_MASK is 1 then the LOL_PLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	RESERVED	R/W	0x0	Reserved
0	LOS_FDET_XO_MASK	R/W	0x0	Masks Loss of Source Freq Detection - XO. When LOS_FDET_XO_MASK is 1 then the LOS_FDET_XO interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.26 R38 Register (Offset = 0x26) [Reset = 0xFF]

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Table 1-28. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_MASK	R/W	0x1	Masks Loss of Phase Lock - DPLL1. When LOPL_DPLL1_MASK is 1 then the LOPL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL1_MASK	R/W	0x1	Masks Loss of Freq Lock - DPLL1. When LOFL_DPLL1_MASK is 1 then the LOFL_DPLL1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST1_MASK	R/W	0x1	Masks Tuning word history update - DPLL1. When HIST1_MASK is 1 then the HIST1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR1_MASK	R/W	0x1	Masks Holdover event - DPLL1. When HLDOVR1_MASK is 1 then the HLDOVR1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH1_MASK	R/W	0x1	Masks Reference Switchover - DPLL1. When REFSWITCH1_MASK is 1 then the REFSWITCH1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOR_MISSCLK1_MASK	R/W	0x1	Masks Loss of Active Reference - Missing Clock - DPLL1. When LOR_MISSCLK1_MASK is 1 then the LOR_MISSCLK1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ1_MASK	R/W	0x1	Masks Loss of Active Reference - Frequency - DPLL1. When LOR_FREQ1_MASK is 1 then the LOR_FREQ1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH1_MASK	R/W	0x1	Masks Loss of Active Reference - Phase - DPLL1. When LOR_PH1_MASK is 1 then the LOR_PH1 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.27 R39 Register (Offset = 0x27) [Reset = 0xFF]

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Table 1-29. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_MASK	R/W	0x1	Masks Loss of Phase Lock - DPLL2. When LOPL_DPLL2_MASK is 1 then the LOPL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL2_MASK	R/W	0x1	Masks Loss of Freq Lock - DPLL2. When LOFL_DPLL2_MASK is 1 then the LOFL_DPLL2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST2_MASK	R/W	0x1	Masks Tuning word history update - DPLL2. When HIST2_MASK is 1 then the HIST2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR2_MASK	R/W	0x1	Masks Holdover event - DPLL2. When HLDOVR2_MASK is 1 then the HLDOVR2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH2_MASK	R/W	0x1	Masks Reference Switchover - DPLL2. When REFSWITCH2_MASK is 1 then the REFSWITCH2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
2	LOR_MISSCLK2_MASK	R/W	0x1	Masks Loss of Active Reference - Missing Clock - DPLL2. When LOR_MISSCLK2_MASK is 1 then the LOR_MISSCLK2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ2_MASK	R/W	0x1	Masks Loss of Active Reference - Frequency - DPLL2. When LOR_FREQ2_MASK is 1 then the LOR_FREQ2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH2_MASK	R/W	0x1	Masks Loss of Active Reference - Phase - DPLL2. When LOR_PH2_MASK is 1 then the LOR_PH2 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.28 R40 Register (Offset = 0x28) [Reset = 0x20]

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Table 1-30. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3_MASK	R/W	0x0	Masks Loss of Phase Lock - DPLL3. When LOPL_DPLL3_MASK is 1 then the LOPL_DPLL3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
6	LOFL_DPLL3_MASK	R/W	0x0	Masks Loss of Freq Lock - DPLL3. When LOFL_DPLL3_MASK is 1 then the LOFL_DPLL3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
5	HIST3_MASK	R/W	0x1	Masks Tuning word history update - DPLL3. When HIST3_MASK is 1 then the HIST3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
4	HLDOVR3_MASK	R/W	0x0	Masks Holdover event - DPLL3. When HLDOVR3_MASK is 1 then the HLDOVR3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
3	REFSWITCH3_MASK	R/W	0x0	Masks Reference Switchover - DPLL3. When REFSWITCH3_MASK is 1 then the REFSWITCH3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

Table 1-30. R40 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	LOR_MISSCLK3_MASK	R/W	0x0	Masks Loss of Active Reference - Missing Clock - DPLL3. When LOR_MISSCLK3_MASK is 1 then the LOR_MISSCLK3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
1	LOR_FREQ3_MASK	R/W	0x0	Masks Loss of Active Reference - Frequency - DPLL3. When LOR_FREQ3_MASK is 1 then the LOR_FREQ3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N
0	LOR_PH3_MASK	R/W	0x0	Masks Loss of Active Reference - Phase - DPLL3. When LOR_PH3_MASK is 1 then the LOR_PH3 interrupt source is masked and will not cause the interrupt signal to be activated. ROM=Y, EEPROM=N

1.29 R41 Register (Offset = 0x29) [Reset = 0x00]

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Table 1-31. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1_POL	R/W	0x0	LOL_PLL1 Flag Polarity. When LOL_PLL1_POL = 1,LOL_PLL1 = 0 results in LOL_PLL1_INTR = 1. When LOL_PLL1_POL = 0, LOL_PLL1 = 1 results in LOL_PLL1_INTR = 1. ROM=Y, EEPROM=N
2	LOL_PLL2_POL	R/W	0x0	LOL_PLL2 Flag Polarity. When LOL_PLL2_POL = 1,LOL_PLL2 = 0 results in LOL_PLL2_INTR = 1. When LOL_PLL2_POL = 0, LOL_PLL2 = 1 results in LOL_PLL2_INTR = 1. ROM=Y, EEPROM=N
1	RESERVED	R/W	0x0	Reserved
0	LOS_FDET_XO_POL	R/W	0x0	LOS_FDET_XO Flag Polarity. When LOS_FDET_XO_POL = 1, LOS_FDET_XO = 0 results in LOS_FDET_XO_INTR = 1. When LOS_FDET_XO_POL = 0, LOS_FDET_XO = 1 results in LOS_FDET_XO_INTR = 1. ROM=Y, EEPROM=N

1.30 R42 Register (Offset = 0x2A) [Reset = 0x00]

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Table 1-32. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_POL	R/W	0x0	LOPL_DPLL1 Flag Polarity. When LOPL_DPLL1_POL = 1, LOPL_DPLL1 = 0 results in LOPL_DPLL1_INTR = 1. When LOPL_DPLL1_POL = 0, LOPL_DPLL1 = 1 results in LOPL_DPLL1_INTR = 1. ROM=Y, EEPROM=N
6	LOFL_DPLL1_POL	R/W	0x0	LOFL_DPLL1 Flag Polarity. When LOFL_DPLL1_POL = 1, LOFL_DPLL1 = 0 results in LOFL_DPLL1_INTR = 1. When LOFL_DPLL1_POL = 0, LOFL_DPLL1 = 1 results in LOFL_DPLL1_INTR = 1. ROM=Y, EEPROM=N
5	HIST1_POL	R/W	0x0	HIST1 Flag Polarity. When HIST1_POL = 1, HIST1 = 0 results in HIST1_INTR = 1. When HIST1_POL = 0, HIST1 = 1 results in HIST1_INTR = 1. ROM=Y, EEPROM=N

Table 1-32. R42 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	HLDOVR1_POL	R/W	0x0	HLDOVR1 Flag Polarity. When HLDOVR1_POL = 1, HLDOVR1 = 0 results in HLDOVR1_INTR = 1. When HLDOVR1_POL = 0, HLDOVR1 = 1 results in HLDOVR1_INTR = 1. ROM=Y, EEPROM=N
3	REFSWITCH1_POL	R/W	0x0	REFSWITCH1 Flag Polarity. When REFSWITCH1_POL = 1, REFSWITCH1 = 0 results in REFSWITCH1_INTR = 1. When REFSWITCH1_POL = 0, REFSWITCH1 = 1 results in REFSWITCH1_INTR = 1. ROM=Y, EEPROM=N
2	LOR_MISSCLK1_POL	R/W	0x0	LOR_MISSCLK1 Flag Polarity. When LOR_MISSCLK1_POL = 1, LOR_MISSCLK1 = 0 results in LOR_MISSCLK1_INTR = 1. When LOR_MISSCLK1_POL = 0, LOR_MISSCLK1 = 1 results in LOR_MISSCLK1_INTR = 1. ROM=Y, EEPROM=N
1	LOR_FREQ1_POL	R/W	0x0	LOR_FREQ1 Flag Polarity. When LOR_FREQ1_POL = 1, LOR_FREQ1 = 0 results in LOR_FREQ1_INTR = 1. When LOR_FREQ1_POL = 0, LOR_FREQ1 = 1 results in LOR_FREQ1_INTR = 1. ROM=Y, EEPROM=N
0	LOR_PH1_POL	R/W	0x0	LOR_PH1 Flag Polarity. When LOR_PH1_POL = 1, LOR_PH1 = 0 results in LOR_PH1_INTR = 1. When LOR_PH1_POL = 0, LOR_PH1 = 1 results in LOR_PH1_INTR = 1. ROM=Y, EEPROM=N

1.31 R43 Register (Offset = 0x2B) [Reset = 0x00]

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Table 1-33. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_POL	R/W	0x0	LOPL_DPLL2 Flag Polarity. When LOPL_DPLL2_POL = 1, LOPL_DPLL2 = 0 results in LOPL_DPLL2_INTR = 1. When LOPL_DPLL2_POL = 0, LOPL_DPLL2 = 1 results in LOPL_DPLL2_INTR = 1. ROM=Y, EEPROM=N
6	LOFL_DPLL2_POL	R/W	0x0	LOFL_DPLL2 Flag Polarity. When LOFL_DPLL2_POL = 1, LOFL_DPLL2 = 0 results in LOFL_DPLL2_INTR = 1. When LOFL_DPLL2_POL = 0, LOFL_DPLL2 = 1 results in LOFL_DPLL2_INTR = 1. ROM=Y, EEPROM=N
5	HIST2_POL	R/W	0x0	HIST2 Flag Polarity. When HIST2_POL = 1, HIST2 = 0 results in HIST2_INTR = 1. When HIST2_POL = 0, HIST2 = 1 results in HIST2_INTR = 1. ROM=Y, EEPROM=N
4	HLDOVR2_POL	R/W	0x0	HLDOVR2 Flag Polarity. When HLDOVR2_POL = 1, HLDOVR2 = 0 results in HLDOVR2_INTR = 1. When HLDOVR2_POL = 0, HLDOVR2 = 1 results in HLDOVR2_INTR = 1. ROM=Y, EEPROM=N
3	REFSWITCH2_POL	R/W	0x0	REFSWITCH2 Flag Polarity. When REFSWITCH2_POL = 1, REFSWITCH2 = 0 results in REFSWITCH2_INTR = 1. When REFSWITCH2_POL = 0, REFSWITCH2 = 1 results in REFSWITCH2_INTR = 1. ROM=Y, EEPROM=N
2	LOR_MISSCLK2_POL	R/W	0x0	LOR_MISSCLK2 Flag Polarity. When LOR_MISSCLK2_POL = 1, LOR_MISSCLK2 = 0 results in LOR_MISSCLK2_INTR = 1. When LOR_MISSCLK2_POL = 0, LOR_MISSCLK2 = 1 results in LOR_MISSCLK2_INTR = 1. ROM=Y, EEPROM=N

Table 1-33. R43 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LOR_FREQ2_POL	R/W	0x0	LOR_FREQ2 Flag Polarity. When LOR_FREQ2_POL = 1, LOR_FREQ2 = 0 results in LOR_FREQ2_INTR = 1. When LOR_FREQ2_POL = 0, LOR_FREQ2 = 1 results in LOR_FREQ2_INTR = 1. ROM=Y, EEPROM=N
0	LOR_PH2_POL	R/W	0x0	LOR_PH2 Flag Polarity. When LOR_PH2_POL = 1, LOR_PH2 = 0 results in LOR_PH2_INTR = 1. When LOR_PH2_POL = 0, LOR_PH2 = 1 results in LOR_PH2_INTR = 1. ROM=Y, EEPROM=N

1.32 R44 Register (Offset = 0x2C) [Reset = 0x00]

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Table 1-34. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3_POL	R/W	0x0	LOPL_DPLL3 Flag Polarity. When LOPL_DPLL3_POL = 1, LOPL_DPLL3 = 0 results in LOPL_DPLL3_INTR = 1. When LOPL_DPLL3_POL = 0, LOPL_DPLL3 = 1 results in LOPL_DPLL3_INTR = 1. ROM=Y, EEPROM=N
6	LOFL_DPLL3_POL	R/W	0x0	LOFL_DPLL3 Flag Polarity. When LOFL_DPLL3_POL = 1, LOFL_DPLL3 = 0 results in LOFL_DPLL3_INTR = 1. When LOFL_DPLL3_POL = 0, LOFL_DPLL3 = 1 results in LOFL_DPLL3_INTR = 1. ROM=Y, EEPROM=N
5	HIST3_POL	R/W	0x0	HIST3 Flag Polarity. When HIST3_POL = 1, HIST3 = 0 results in HIST3_INTR = 1. When HIST3_POL = 0, HIST3 = 1 results in HIST3_INTR = 1. ROM=Y, EEPROM=N
4	HLDOVR3_POL	R/W	0x0	HLDOVR3 Flag Polarity. When HLDOVR3_POL = 1, HLDOVR3 = 0 results in HLDOVR3_INTR = 1. When HLDOVR3_POL = 0, HLDOVR3 = 1 results in HLDOVR3_INTR = 1. ROM=Y, EEPROM=N
3	REFSWITCH3_POL	R/W	0x0	REFSWITCH3 Flag Polarity. When REFSWITCH3_POL = 1, REFSWITCH3 = 0 results in REFSWITCH3_INTR = 1. When REFSWITCH3_POL = 0, REFSWITCH3 = 1 results in REFSWITCH3_INTR = 1. ROM=Y, EEPROM=N
2	LOR_MISSCLK3_POL	R/W	0x0	LOR_MISSCLK3 Flag Polarity. When LOR_MISSCLK3_POL = 1, LOR_MISSCLK3 = 0 results in LOR_MISSCLK3_INTR = 1. When LOR_MISSCLK3_POL = 0, LOR_MISSCLK3 = 1 results in LOR_MISSCLK3_INTR = 1. ROM=Y, EEPROM=N
1	LOR_FREQ3_POL	R/W	0x0	LOR_FREQ3 Flag Polarity. When LOR_FREQ3_POL = 1, LOR_FREQ3 = 0 results in LOR_FREQ3_INTR = 1. When LOR_FREQ3_POL = 0, LOR_FREQ3 = 1 results in LOR_FREQ3_INTR = 1. ROM=Y, EEPROM=N
0	LOR_PH3_POL	R/W	0x0	LOR_PH3 Flag Polarity. When LOR_PH3_POL = 1, LOR_PH3 = 0 results in LOR_PH3_INTR = 1. When LOR_PH3_POL = 0, LOR_PH3 = 1 results in LOR_PH3_INTR = 1. ROM=Y, EEPROM=N

1.33 R45 Register (Offset = 0x2D) [Reset = 0x00]

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Table 1-35. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	LOL_PLL1_INTR	R	0x0	LOL_PLL1 Interrupt. The LOL_PLL1_INTR bit is set when a level of the correct polarity is detected on the LOL_PLL1 interrupt source. The LOL_PLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOL_PLL2_INTR	R	0x0	LOL_PLL2 Interrupt. The LOL_PLL2_INTR bit is set when a level of the correct polarity is detected on the LOL_PLL2 interrupt source. The LOL_PLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	LOS_FDET_XO_INTR	R	0x0	LOL_FDET_XO Interrupt. The LOL_FDET_XO_INTR bit is set when a level of the correct polarity is detected on the LOL_FDET_XO interrupt source. The LOL_FDET_XO_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.34 R46 Register (Offset = 0x2E) [Reset = 0x00]

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Table 1-36. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL1_INTR	R	0x0	LOPL_DPLL1 Interrupt. The LOPL_DPLL1_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL1 interrupt source. The LOPL_DPLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL1_INTR	R	0x0	LOFL_DPLL1 Interrupt. The LOFL_DPLL1_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL1 interrupt source. The LOFL_DPLL1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST1_INTR	R	0x0	HIST1 Interrupt. The HIST1_INTR bit is set when a level of the correct polarity is detected on the HIST1 interrupt source. The HIST1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
4	HLDOVR1_INTR	R	0x0	HLDOVR1 Interrupt. The HLDOVR1_INTR bit is set when a level of the correct polarity is detected on the HLDOVR1 interrupt source. The HLDOVR1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH1_INTR	R	0x0	REFSWITCH1 Interrupt. The REFSWITCH1_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH1 interrupt source. The REFSWITCH1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK1_INTR	R	0x0	LOR_MISSCLK1 Interrupt. The LOR_MISSCLK1_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK1 interrupt source. The LOR_MISSCLK1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ1_INTR	R	0x0	LOR_FREQ1 Interrupt. The LOR_FREQ1_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ1 interrupt source. The LOR_FREQ1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH1_INTR	R	0x0	LOR_PH1 Interrupt. The LOR_PH1_INTR bit is set when a level of the correct polarity is detected on the LOR_PH1 interrupt source. The LOR_PH1_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.35 R47 Register (Offset = 0x2F) [Reset = 0x00]

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Table 1-37. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL2_INTR	R	0x0	LOPL_DPLL2 Interrupt. The LOPL_DPLL2_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL2 interrupt source. The LOPL_DPLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL2_INTR	R	0x0	LOFL_DPLL2 Interrupt. The LOFL_DPLL2_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL2 interrupt source. The LOFL_DPLL2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST2_INTR	R	0x0	HIST2 Interrupt. The HIST2_INTR bit is set when a level of the correct polarity is detected on the HIST2 interrupt source. The HIST2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
4	HLDOVR2_INTR	R	0x0	HLDOVR2 Interrupt. The HLDOVR2_INTR bit is set when a level of the correct polarity is detected on the HLDOVR2 interrupt source. The HLDOVR2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH2_INTR	R	0x0	REFSWITCH2 Interrupt. The REFSWITCH2_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH2 interrupt source. The REFSWITCH2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK2_INTR	R	0x0	LOR_MISSCLK2 Interrupt. The LOR_MISSCLK2_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK2 interrupt source. The LOR_MISSCLK2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ2_INTR	R	0x0	LOR_FREQ2 Interrupt. The LOR_FREQ2_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ2 interrupt source. The LOR_FREQ2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH2_INTR	R	0x0	LOR_PH2 Interrupt. The LOR_PH2_INTR bit is set when a level of the correct polarity is detected on the LOR_PH2 interrupt source. The LOR_PH2_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.36 R48 Register (Offset = 0x30) [Reset = 0x00]

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Table 1-38. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL3_INTR	R	0x0	LOPL_DPLL3 Interrupt. The LOPL_DPLL3_INTR bit is set when a level of the correct polarity is detected on the LOPL_DPLL3 interrupt source. The LOPL_DPLL3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
6	LOFL_DPLL3_INTR	R	0x0	LOFL_DPLL3 Interrupt. The LOFL_DPLL3_INTR bit is set when a level of the correct polarity is detected on the LOFL_DPLL3 interrupt source. The LOFL_DPLL3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
5	HIST3_INTR	R	0x0	HIST3 Interrupt. The HIST3_INTR bit is set when a level of the correct polarity is detected on the HIST3 interrupt source. The HIST3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

Table 1-38. R48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	HLDOVR3_INTR	R	0x0	HLDOVR3 Interrupt. The HLDOVR3_INTR bit is set when a level of the correct polarity is detected on the HLDOVR3 interrupt source. The HLDOVR3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
3	REFSWITCH3_INTR	R	0x0	REFSWITCH3 Interrupt. The REFSWITCH3_INTR bit is set when a level of the correct polarity is detected on the REFSWITCH3 interrupt source. The REFSWITCH3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
2	LOR_MISSCLK3_INTR	R	0x0	LOR_MISSCLK3 Interrupt. The LOR_MISSCLK3_INTR bit is set when a level of the correct polarity is detected on the LOR_MISSCLK3 interrupt source. The LOR_MISSCLK3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
1	LOR_FREQ3_INTR	R	0x0	LOR_FREQ3 Interrupt. The LOR_FREQ3_INTR bit is set when a level of the correct polarity is detected on the LOR_FREQ3 interrupt source. The LOR_FREQ3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N
0	LOR_PH3_INTR	R	0x0	LOR_PH3 Interrupt. The LOR_PH3_INTR bit is set when a level of the correct polarity is detected on the LOR_PH3 interrupt source. The LOR_PH3_INTR bit is cleared by writing a 1 to INT_CLR. ROM=N, EEPROM=N

1.37 R49 Register (Offset = 0x31) [Reset = 0x02]

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Table 1-39. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	INT_LATCH_OR_LIVE	R/W	0x0	Interrupt GPIO Output Type Selection. When set to 0, flag interrupts are fed into the reduction AND / reduction OR logic. When set to 1, live interrupts are fed into the reduction AND / reduction OR logic. ROM=Y, EEPROM=N 0x0 = Latch Mode 0x1 = Live Mode
2	INT_AND_OR	R/W	0x0	Interrupt AND/OR Combination. If INT_AND_OR is 1, then the interrupts are combined in an AND structure, in which case ALL un-masked interrupt flags must be active in order to generate the interrupt. If INT_AND_OR is 0, then the interrupts are combined in an OR structure, in which case ANY un-masked interrupt flags can generate the interrupt. ROM=Y, EEPROM=N 0x0 = OR 0x1 = AND
1	INT_EN	R/W	0x1	Interrupt Enable. If INT_EN is 1 then the interrupt circuit is enabled. If INT_EN is 0 the interrupt circuit is disabled. When INT_EN is 0, interrupts cannot be signaled on the GPIOx pins, and the flag registers (*_INTR) will not be updated; however, the live status registers will still reflect the current state of the internal interrupt source signals. To provide an interrupt on a pin, a GPIOx pin must also be configured as interrupt output. Interrupts may be enabled without providing a GPIOx output to allow sticky bits to be set. ROM=Y, EEPROM=N
0	INT_CLR	R/WSC	0x0	Clears all interrupt flag (*_INTR) registers ROM=N, EEPROM=N

1.38 R50 Register (Offset = 0x32) [Reset = 0x00]

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Table 1-40. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	REF3_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN3 ROM=N, EEPROM=N
2	REF2_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN2 ROM=N, EEPROM=N
1	REF1_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN1 ROM=N, EEPROM=N
0	REF0_VALID_STATUS	R	0x0	Status of Reference Input Validation for IN0 ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.39 R51 Register (Offset = 0x33) [Reset = 0x00]

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Table 1-41. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF3_PH_STATUS	R	0x0	Status of Reference 3 Phase Validation ROM=N, EEPROM=N
4	RESERVED	R	0x0	Reserved
3	REF3_FDET_STATUS	R	0x0	Status of Reference 3 Frequency Validation ROM=N, EEPROM=N
2	REF2_PH_STATUS	R	0x0	Status of Reference 2 Phase Validation ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	REF2_FDET_STATUS	R	0x0	Status of Reference 2 Frequency Validation ROM=N, EEPROM=N

1.40 R52 Register (Offset = 0x34) [Reset = 0x00]

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Table 1-42. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF1_PH_STATUS	R	0x0	Status of Reference 1 Phase Validation ROM=N, EEPROM=N
4	RESERVED	R	0x0	Reserved
3	REF1_FDET_STATUS	R	0x0	Status of Reference 1 Frequency Validation ROM=N, EEPROM=N
2	REF0_PH_STATUS	R	0x0	Status of Reference 0 Phase Validation ROM=N, EEPROM=N
1	RESERVED	R	0x0	Reserved
0	REF0_FDET_STATUS	R	0x0	Status of Reference 0 Frequency Validation ROM=N, EEPROM=N

1.41 R53 Register (Offset = 0x35) [Reset = 0x00]

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Table 1-43. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	TEC_CNTR_HELD	R	0x0	TEC Held. Reading back a 1 indicates GPIO or SPI event has latched a holdover value. Will clear to 0 after TEC CNTR LSB is read. ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.42 R54 Register (Offset = 0x36) [Reset = 0x00]

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Table 1-44. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO0_IN_FLT_EN	R/W	0x0	Enable GPIO0 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-44. R54 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO0_MODE	R/W	0x0	Select GPIO0 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/INTERRUPT) 0x1 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL3, Selects input 0 or input 1 for DPLL3 0x4 = INSEL23_DPLL1, Selects input 2 or input 3 for DPLL1 0x5 = INSEL23_DPLL2, Selects input 2 or input 3 for DPLL2 0x6 = INSEL23_DPLL3, Selects input 2 or input 3 for DPLL3 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = INSEL12_DPLL1, Selects input 1 or input 2 for DPLL1 0xE = INSEL12_DPLL2, Selects input 1 or input 2 for DPLL2 0xF = INSEL12_DPLL3, Selects input 1 or input 2 for DPLL3 0x10 = INSEL03_DPLL1, Selects input 0 or input 3 for DPLL1 0x11 = INSEL03_DPLL2, Selects input 0 or input 3 for DPLL2 0x12 = INSEL03_DPLL3, Selects input 0 or input 3 for DPLL3 0x13 = INSEL02_DPLL1, Selects input 0 or input 2 for DPLL1 0x14 = INSEL02_DPLL2, Selects input 0 or input 2 for DPLL2 0x15 = INSEL02_DPLL3, Selects input 0 or input 2 for DPLL3 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = INSEL13_DPLL1, Selects input 1 or input 3 for DPLL1 0x1A = INSEL13_DPLL2, Selects input 1 or input 3 for DPLL2 0x1B = INSEL13_DPLL3, Selects input 1 or input 3 for DPLL3 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL3, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL3 0x24 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x26 = FDEV_DIR_DPLL3, FDEV_DIR_DPLL3 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x27 = TEC_TRIG_SEL

1.43 R55 Register (Offset = 0x37) [Reset = 0x00]

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Table 1-45. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO1_IN_FLT_EN	R/W	0x0	Enable GPIO1 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-45. R55 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO1_MODE	R/W	0x0	Select GPIO1 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/INTERRUPT) 0x1 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL3, Selects input 0 or input 1 for DPLL3 0x4 = INSEL23_DPLL1, Selects input 2 or input 3 for DPLL1 0x5 = INSEL23_DPLL2, Selects input 2 or input 3 for DPLL2 0x6 = INSEL23_DPLL3, Selects input 2 or input 3 for DPLL3 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = INSEL12_DPLL1, Selects input 1 or input 2 for DPLL1 0xE = INSEL12_DPLL2, Selects input 1 or input 2 for DPLL2 0xF = INSEL12_DPLL3, Selects input 1 or input 2 for DPLL3 0x10 = INSEL03_DPLL1, Selects input 0 or input 3 for DPLL1 0x11 = INSEL03_DPLL2, Selects input 0 or input 3 for DPLL2 0x12 = INSEL03_DPLL3, Selects input 0 or input 3 for DPLL3 0x13 = INSEL02_DPLL1, Selects input 0 or input 2 for DPLL1 0x14 = INSEL02_DPLL2, Selects input 0 or input 2 for DPLL2 0x15 = INSEL02_DPLL3, Selects input 0 or input 2 for DPLL3 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = INSEL13_DPLL1, Selects input 1 or input 3 for DPLL1 0x1A = INSEL13_DPLL2, Selects input 1 or input 3 for DPLL2 0x1B = INSEL13_DPLL3, Selects input 1 or input 3 for DPLL3 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL3, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL3 0x24 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x26 = FDEV_DIR_DPLL3, FDEV_DIR_DPLL3 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x27 = TEC_TRIG_SEL

1.44 R56 Register (Offset = 0x38) [Reset = 0x00]

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Table 1-46. R56 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	GPIO2_IN_FLT_EN	R/W	0x0	Enable GPIO2 Input Pin Deglitch Filter ROM=Y, EEPROM=N

Table 1-46. R56 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	GPIO2_MODE	R/W	0x0	Select GPIO2 Pin Operating Mode. ROM=Y, EEPROM=N 0x0 = STATUS or INT, Acts as status or interrupt outputs (See section on STATUS/INTERRUPT) 0x1 = INSEL01_DPLL1, Selects input 0 or input 1 for DPLL1 0x2 = INSEL01_DPLL2, Selects input 0 or input 1 for DPLL2 0x3 = INSEL01_DPLL3, Selects input 0 or input 1 for DPLL3 0x4 = INSEL23_DPLL1, Selects input 2 or input 3 for DPLL1 0x5 = INSEL23_DPLL2, Selects input 2 or input 3 for DPLL2 0x6 = INSEL23_DPLL3, Selects input 2 or input 3 for DPLL3 0x7 = Reserved 0x8 = Reserved 0x9 = Reserved 0xA = Reserved 0xB = Reserved 0xC = Reserved 0xD = INSEL12_DPLL1, Selects input 1 or input 2 for DPLL1 0xE = INSEL12_DPLL2, Selects input 1 or input 2 for DPLL2 0xF = INSEL12_DPLL3, Selects input 1 or input 2 for DPLL3 0x10 = INSEL03_DPLL1, Selects input 0 or input 3 for DPLL1 0x11 = INSEL03_DPLL2, Selects input 0 or input 3 for DPLL2 0x12 = INSEL03_DPLL3, Selects input 0 or input 3 for DPLL3 0x13 = INSEL02_DPLL1, Selects input 0 or input 2 for DPLL1 0x14 = INSEL02_DPLL2, Selects input 0 or input 2 for DPLL2 0x15 = INSEL02_DPLL3, Selects input 0 or input 2 for DPLL3 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved 0x19 = INSEL13_DPLL1, Selects input 1 or input 3 for DPLL1 0x1A = INSEL13_DPLL2, Selects input 1 or input 3 for DPLL2 0x1B = INSEL13_DPLL3, Selects input 1 or input 3 for DPLL3 0x1C = Reserved 0x1D = Reserved 0x1E = Reserved 0x1F = SYNC, Synchronizes selected outputs on a low-to-high pulse. "1" is normal state for outputs. "0" sets outputs in SYNC. 0x20 = SYSREF_REQ, Can request SYSREF pulses on appropriate output channels via low-to-high pulse. 0x21 = FDEV_TRIG_DPLL1, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL1 0x22 = FDEV_TRIG_DPLL2, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL2 0x23 = FDEV_TRIG_DPLL3, A rising edge will trigger a frequency change based on the FDEV_DIR_DPLL3 0x24 = FDEV_DIR_DPLL1, FDEV_DIR_DPLL1 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x25 = FDEV_DIR_DPLL2, FDEV_DIR_DPLL2 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x26 = FDEV_DIR_DPLL3, FDEV_DIR_DPLL3 will determine the direction of the FDEV trigger. 0 = Positive and 1 = Negative 0x27 = TEC_TRIG_SEL

1.45 R57 Register (Offset = 0x39) [Reset = 0x0C]

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Table 1-47. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-47. R57 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO0_SEL	R/W	0xC	GPIO0 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = APLL1 Loss of Lock (LOL) 0x2 = APLL2 Loss of Lock (LOL) 0x3 = APLL3 Loss of Lock (LOL) 0x4 = DPLL1 Loss of Phase Lock (LOPL) 0x5 = DPLL1 Loss of Frequency Lock (LOFL) 0x6 = PLL1 LOL | DPLL1 LOPL | DPLL1 LOFL 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL | DPLL2 LOPL | DPLL2 LOFL 0xA = DPLL3 Loss of Phase Lock (LOPL) 0xB = DPLL3 Loss of Frequency Lock (LOFL) 0xC = PLL3 LOL | DPLL3 LOPL | DPLL3 LOFL 0xD = DPLL1 | DPLL2 | DPLL3 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = DPLL1 REF0 Selected 0x16 = DPLL1 REF1 Selected 0x17 = DPLL1 REF2 Selected 0x18 = DPLL1 REF3 Selected 0x19 = Reserved 0x1A = DPLL1 Holdover Active 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = DPLL2 REF2 Selected 0x1E = DPLL2 REF3 Selected 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL3 REF0 Selected 0x22 = DPLL3 REF1 Selected 0x23 = DPLL3 REF2 Selected 0x24 = DPLL3 REF3 Selected 0x25 = Reserved 0x26 = DPLL3 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = REF2 Frequency Monitor 0x2A = REF3 Frequency Monitor 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = REF2 Missing Clock Monitor 0x2F = REF3 Missing Clock Monitor 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor 0x3D = REF2 Phase Validation Monitor 0x3E = REF3 Phase Validation Monitor 0x3F = Reserved 0x40 = Reserved 0x41 = Reserved

Table 1-47. R57 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = Reserved 0x47 = Reserved 0x48 = Reserved 0x49 = Reserved 0x4A = Reserved 0x4B = Reserved 0x4C = Reserved 0x4D = Reserved 0x4E = Reserved 0x4F = Reserved 0x50 = PLL1 N-Divider Divided By 2 0x51 = PLL2 N-Divider Divided By 2 0x52 = PLL3 N-Divider Divided By 2 0x53 = PLL1 R-Divider Divided By 2 0x54 = PLL2 R-Divider Divided By 2 0x55 = PLL3 R-Divider Divided By 2 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = REF0 Monitor Divider Output Divided By 2 0x5A = REF1 Monitor Divider Output Divided By 2 0x5B = REF2 Monitor Divider Output Divided By 2 0x5C = REF3 Monitor Divider Output Divided By 2 0x5D = Reserved 0x5E = Reserved 0x5F = Reserved 0x60 = Reserved 0x61 = Reserved 0x62 = Reserved 0x63 = Reserved 0x64 = Reserved 0x65 = Reserved 0x66 = Reserved 0x67 = Reserved 0x68 = Reserved 0x69 = Reserved 0x6A = Reserved 0x6B = Reserved 0x6C = Reserved 0x6D = Reserved 0x6E = Reserved 0x6F = Reserved 0x70 = Reserved 0x71 = Reserved 0x72 = Reserved

1.46 R58 Register (Offset = 0x3A) [Reset = 0x0F]

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Table 1-48. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-48. R58 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO1_SEL	R/W	0xF	GPIO1 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = APLL1 Loss of Lock (LOL) 0x2 = APLL2 Loss of Lock (LOL) 0x3 = APLL3 Loss of Lock (LOL) 0x4 = DPLL1 Loss of Phase Lock (LOPL) 0x5 = DPLL1 Loss of Frequency Lock (LOFL) 0x6 = PLL1 LOL | DPLL1 LOPL | DPLL1 LOFL 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL | DPLL2 LOPL | DPLL2 LOFL 0xA = DPLL3 Loss of Phase Lock (LOPL) 0xB = DPLL3 Loss of Frequency Lock (LOFL) 0xC = PLL3 LOL | DPLL3 LOPL | DPLL3 LOFL 0xD = DPLL1 | DPLL2 | DPLL3 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = DPLL1 REF0 Selected 0x16 = DPLL1 REF1 Selected 0x17 = DPLL1 REF2 Selected 0x18 = DPLL1 REF3 Selected 0x19 = Reserved 0x1A = DPLL1 Holdover Active 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = DPLL2 REF2 Selected 0x1E = DPLL2 REF3 Selected 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL3 REF0 Selected 0x22 = DPLL3 REF1 Selected 0x23 = DPLL3 REF2 Selected 0x24 = DPLL3 REF3 Selected 0x25 = Reserved 0x26 = DPLL3 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = REF2 Frequency Monitor 0x2A = REF3 Frequency Monitor 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = REF2 Missing Clock Monitor 0x2F = REF3 Missing Clock Monitor 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor 0x3D = REF2 Phase Validation Monitor 0x3E = REF3 Phase Validation Monitor 0x3F = Reserved 0x40 = DPLL1 Phase Cancellation Active 0x41 = Reserved

Table 1-48. R58 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = Reserved 0x47 = Reserved 0x48 = Reserved 0x49 = Reserved 0x4A = Reserved 0x4B = Reserved 0x4C = Reserved 0x4D = Reserved 0x4E = Reserved 0x4F = Reserved 0x50 = PLL1 N-Divider Divided By 2 0x51 = PLL2 N-Divider Divided By 2 0x52 = PLL3 N-Divider Divided By 2 0x53 = PLL1 R-Divider Divided By 2 0x54 = PLL2 R-Divider Divided By 2 0x55 = PLL3 R-Divider Divided By 2 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = REF0 Monitor Divider Output Divided By 2 0x5A = REF1 Monitor Divider Output Divided By 2 0x5B = REF2 Monitor Divider Output Divided By 2 0x5C = REF3 Monitor Divider Output Divided By 2 0x5D = Reserved 0x5E = Reserved 0x5F = Reserved 0x60 = Reserved 0x61 = Reserved 0x62 = Reserved 0x63 = Reserved 0x64 = Reserved 0x65 = Reserved 0x66 = Reserved 0x67 = Reserved 0x68 = Reserved 0x69 = Reserved 0x6A = Reserved 0x6B = Reserved 0x6C = Reserved 0x6D = Reserved 0x6E = Reserved 0x6F = Reserved 0x70 = Reserved 0x71 = Reserved 0x72 = Reserved 0x73 = Continuous SYSREF / 1-PPS from selected SYSREF DIV

1.47 R59 Register (Offset = 0x3B) [Reset = 0x0E]

Return to the Summary Table.

Table 1-49. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-49. R59 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	GPIO2_SEL	R/W	0xE	GPIO2 Status Signal Select. ROM=Y, EEPROM=N 0x0 = XO Loss of Signal (LOS) 0x1 = APLL1 Loss of Lock (LOL) 0x2 = APLL2 Loss of Lock (LOL) 0x3 = APLL3 Loss of Lock (LOL) 0x4 = DPLL1 Loss of Phase Lock (LOPL) 0x5 = DPLL1 Loss of Frequency Lock (LOFL) 0x6 = PLL1 LOL | DPLL1 LOPL | DPLL1 LOFL 0x7 = DPLL2 Loss of Phase Lock (LOPL) 0x8 = DPLL2 Loss of Frequency Lock (LOFL) 0x9 = PLL2 LOL | DPLL2 LOPL | DPLL2 LOFL 0xA = DPLL3 Loss of Phase Lock (LOPL) 0xB = DPLL3 Loss of Frequency Lock (LOFL) 0xC = PLL3 LOL | DPLL3 LOPL | DPLL3 LOFL 0xD = DPLL1 | DPLL2 | DPLL3 LOL 0xE = Interrupt (INTR). Derived from INT_FLAG register bits. 0xF = SPI Readback Data (SDO) 0x10 = Reserved 0x11 = Reserved 0x12 = Reserved 0x13 = Reserved 0x14 = Reserved 0x15 = DPLL1 REF0 Selected 0x16 = DPLL1 REF1 Selected 0x17 = DPLL1 REF2 Selected 0x18 = DPLL1 REF3 Selected 0x19 = Reserved 0x1A = DPLL1 Holdover Active 0x1B = DPLL2 REF0 Selected 0x1C = DPLL2 REF1 Selected 0x1D = DPLL2 REF2 Selected 0x1E = DPLL2 REF3 Selected 0x1F = Reserved 0x20 = DPLL2 Holdover Active 0x21 = DPLL3 REF0 Selected 0x22 = DPLL3 REF1 Selected 0x23 = DPLL3 REF2 Selected 0x24 = DPLL3 REF3 Selected 0x25 = Reserved 0x26 = DPLL3 Holdover Active 0x27 = REF0 Frequency Monitor 0x28 = REF1 Frequency Monitor 0x29 = REF2 Frequency Monitor 0x2A = REF3 Frequency Monitor 0x2B = Reserved 0x2C = REF0 Missing Clock Monitor 0x2D = REF1 Missing Clock Monitor 0x2E = REF2 Missing Clock Monitor 0x2F = REF3 Missing Clock Monitor 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = REF0 Phase Validation Monitor 0x3C = REF1 Phase Validation Monitor 0x3D = REF2 Phase Validation Monitor 0x3E = REF3 Phase Validation Monitor 0x3F = Reserved 0x40 = DPLL1 Phase Cancellation Active 0x41 = Reserved

Table 1-49. R59 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = Reserved 0x47 = Reserved 0x48 = Reserved 0x49 = Reserved 0x4A = Reserved 0x4B = Reserved 0x4C = Reserved 0x4D = Reserved 0x4E = Reserved 0x4F = Reserved 0x50 = PLL1 N-Divider Divided By 2 0x51 = PLL2 N-Divider Divided By 2 0x52 = PLL3 N-Divider Divided By 2 0x53 = PLL1 R-Divider Divided By 2 0x54 = PLL2 R-Divider Divided By 2 0x55 = PLL3 R-Divider Divided By 2 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = REF0 Monitor Divider Output Divided By 2 0x5A = REF1 Monitor Divider Output Divided By 2 0x5B = REF2 Monitor Divider Output Divided By 2 0x5C = REF3 Monitor Divider Output Divided By 2 0x5D = Reserved 0x5E = Reserved 0x5F = Reserved 0x60 = Reserved 0x61 = Reserved 0x62 = Reserved 0x63 = Reserved 0x64 = Reserved 0x65 = Reserved 0x66 = Reserved 0x67 = Reserved 0x68 = Reserved 0x69 = Reserved 0x6A = Reserved 0x6B = Reserved 0x6C = Reserved 0x6D = Reserved 0x6E = Reserved 0x6F = Reserved 0x70 = Reserved 0x71 = Reserved 0x72 = Reserved 0x73 = Continuous SYSREF / 1-PPS from selected SYSREF DIV

1.48 R60 Register (Offset = 0x3C) [Reset = 0x14]

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Table 1-50. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	GPIO0_OPEND	R/W	0x0	GPIO0 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain. External pull-up from 1.8 V to 5.5 V supply rail required.

Table 1-50. R60 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	GPIO1_OPEND	R/W	0x1	GPIO1 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain. External pull-up from 1.8 V to 5.5 V supply rail required.
3	GPIO2_OPEND	R/W	0x0	GPIO2 Open Drain Enable ROM=Y, EEPROM=N 0x0 = CMOS 0x1 = NMOS open drain. External pull-up from 1.8 V to 5.5 V supply rail required.
2	GPIO0_POL	R/W	0x1	GPIO0 Status Output Polarity. The GPIO0_STAT_POL bit defines the polarity of information presented on the GPIO0 output. If GPIO0_STAT_POL is set to 1, then GPIO0 is active high. If GPIO0_STAT_POL is 0, then GPIO0 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low
1	GPIO1_POL	R/W	0x0	GPIO1 Status Output Polarity. The GPIO1_STAT_POL bit defines the polarity of information presented on the GPIO1 output. If GPIO1_STAT_POL is set to 1, then GPIO1 is active high. If GPIO1_STAT_POL is 0, then GPIO1 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low
0	GPIO2_POL	R/W	0x0	GPIO2 Status Output Polarity. The GPIO2_STAT_POL bit defines the polarity of information presented on the GPIO2 output. If GPIO2_STAT_POL is set to 1, then GPIO2 is active high. If GPIO2_STAT_POL is 0, then GPIO2 is active low. ROM=Y, EEPROM=N 0x0 = Active High 0x1 = Active Low

1.49 R61 Register (Offset = 0x3D) [Reset = 0x00]

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Table 1-51. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	GPIO_SYSREF_SEL	R/W	0x0	Select SYSREF divider output for GPIO output. When GPIOx_SEL chooses SYSREF divider, this is the SYSREF divider output on the GPIO. This signal is continuous. This could be used for low frequency outputs such as 1-PPS or 8 kHz as a 3.3-V LVCMOS signal. Select SYSREF divider output after static digital delay but before the analog and digital delay and pulser. ROM=Y, EEPROM=N 0x0 = OUT_0_1 0x1 = OUT_6_7 0x2 = OUT_4_5 0x3 = OUT_8_9 0x4 = OUT_10_11 0x5 = OUT_12_13 0x6 = NA 0x7 = NA
1	MUTE_DPLL3_PHLOCK	R/W	0x0	DPLL3 mute enabled during phase lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
0	MUTE_DPLL3_FRLOCK	R/W	0x0	DPLL3 mute enabled during dpll lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y

1.50 R62 Register (Offset = 0x3E) [Reset = 0x00]

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Table 1-52. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	MUTE_APLL3_LOCK	R/W	0x0	APLL3 mute enabled during PLL lock. APLL3 lock detect is always true. ROM=Y, EEPROM=N
5	MUTE_DPLL2_PHLOCK	R/W	0x0	DPLL2 mute enabled during phase lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
4	MUTE_DPLL2_FRLOCK	R/W	0x0	DPLL2 mute enabled during dpll lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
3	MUTE_APLL2_LOCK	R/W	0x0	APLL2 mute enabled during PLL lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
2	MUTE_DPLL1_PHLOCK	R/W	0x0	DPLL1 mute enabled during phase lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
1	MUTE_DPLL1_FRLOCK	R/W	0x0	DPLL1 mute enabled during dpll lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y
0	MUTE_APLL1_LOCK	R/W	0x0	APLL1 mute enabled during PLL lock. Muted outputs will start clocking glitch free once achieving lock status. ROM=Y, EEPROM=Y

1.51 R63 Register (Offset = 0x3F) [Reset = 0x00]

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Table 1-53. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	XO_FDET_BYP	R/W	0x0	Frequency Detector Bypass. When XO_FDET_BYP is set to 1, the output of the XO frequency detector is ignored. ROM=Y, EEPROM=N
3:0	XO_ITYPE	R/W	0x0	XO interface type control. ROM=Y, EEPROM=Y 0x0 = DC-DIFF (ext. term) 0x1 = AC-DIFF (ext. term) 0x3 = LVDS/HSDS (AC-DIFF, int. 100 Ω) 0x4 = HCSL (DC-DIFF, int. 50 Ω to GND) 0x5 = LVPECL (AC-DIFF, int. 50 Ω to GND) 0x8 = CMOS 0xC = S-E (int. 50 Ω)

1.52 R64 Register (Offset = 0x40) [Reset = 0x09]

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Table 1-54. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-54. R64 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	XO_OUT_BUF_EN	R/W	0x9	Bit position enables XO Output Buffer path to: [0] The XO Freq Detector [1] APLL1 REF [2] APLL2 REF [3] APLL3 REF, and [4] OUT0_1 ROM=Y, EEPROM=Y

1.53 R65 Register (Offset = 0x41) [Reset = 0x00]

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Table 1-55. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3:0	REF3_ITYPE	R/W	0x0	To be updated. REF3 interface type control. ROM=Y, EEPROM=N 0x0 = DC-DIFF (ext. term) 0x1 = AC-DIFF (ext. term) 0x2 = DC-DIFF (int. 100 Ω term) 0x3 = LVDS/HSDS (AC-DIFF, int. 100 Ω) 0x4 = HCSL (DC-DIFF, int. 50 Ω to GND) 0x5 = LVPECL (AC-DIFF, int. 50 Ω to GND) 0x8 = CMOS 0xC = S-E (int. 50 Ω)

1.54 R66 Register (Offset = 0x42) [Reset = 0x00]

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Table 1-56. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3:0	REF2_ITYPE	R/W	0x0	To be updated. REF2 interface type control. ROM=Y, EEPROM=N 0x0 = DC-DIFF (ext. term) 0x1 = AC-DIFF (ext. term) 0x2 = DC-DIFF (int. 100 Ω term) 0x3 = LVDS/HSDS (AC-DIFF, int. 100 Ω) 0x4 = HCSL (DC-DIFF, int. 50 Ω to GND) 0x5 = LVPECL (AC-DIFF, int. 50 Ω to GND) 0x8 = CMOS 0xC = S-E (int. 50 Ω)

1.55 R67 Register (Offset = 0x43) [Reset = 0x00]

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Table 1-57. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved

Table 1-57. R67 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	REF1_DC_COUPLED_EN	R/W	0x0	DC couple input. Eliminates need for hysteresis for low frequency input clocks. ROM=Y, EEPROM=N
3:0	REF1_ITYPE	R/W	0x0	REF1 interface type control. ROM=Y, EEPROM=N 0x0 = DC-DIFF (ext. term) 0x1 = AC-DIFF (ext. term) 0x2 = DC-DIFF (int. 100 Ω term) 0x3 = LVDS/HSDS (AC-DIFF, int. 100 Ω) 0x4 = HCSL (DC-DIFF, int. 50 Ω to GND) 0x5 = LVPECL (AC-DIFF, int. 50 Ω to GND) 0x8 = CMOS 0xC = S-E (int. 50 Ω)

1.56 R68 Register (Offset = 0x44) [Reset = 0x00]

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Table 1-58. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	REF0_DC_COUPLED_EN	R/W	0x0	DC couple input. Eliminates need for hysteresis for low frequency input clocks. ROM=Y, EEPROM=N
3:0	REF0_ITYPE	R/W	0x0	REF0 interface type control. ROM=Y, EEPROM=N 0x0 = DC-DIFF (ext. term) 0x1 = AC-DIFF (ext. term) 0x2 = DC-DIFF (int. 100 Ω term) 0x3 = LVDS/HSDS (AC-DIFF, int. 100 Ω) 0x4 = HCSL (DC-DIFF, int. 50 Ω to GND) 0x5 = LVPECL (AC-DIFF, int. 50 Ω to GND) 0x8 = CMOS 0xC = S-E (int. 50 Ω)

1.57 R70 Register (Offset = 0x46) [Reset = 0x00]

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Table 1-59. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	STATUS_MUX_DIV2_EN	R/W	0x0	Enable all DivideBy2 clocks for Status MUX debug signals ROM=N, EEPROM=N

1.58 R75 Register (Offset = 0x4B) [Reset = 0x1A]

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Table 1-60. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	TDC3_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC3 feedback input source ROM=Y, EEPROM=N 0x0 = Select FB Divider 0x1 = Bypass FB Divider

Table 1-60. R75 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TDC3_ZDM_FB_PRE_BYP	R/W	0x0	Inserts TDC3 feedback divider in series with selected channel divider ROM=Y, EEPROM=N 0x0 = ZDM disabled 0x1 = ZDM enable
4:3	TDC3_IN_SEL	R/W	0x3	Selects TDC3 zero delay input ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = OUT_10_11_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO3 direct (ZDM disabled)
2:0	TDC3_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = ZDM disabled 0x3 = Reserved 0x4 = Reserved 0x5 = ZDM enabled 0x6 = Reserved 0x7 = Reserved

1.59 R76 Register (Offset = 0x4C) [Reset = 0x1A]

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Table 1-61. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	TDC2_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC feedback input. 0=FB_DIV, 1=ZD bypass FBDIV ROM=Y, EEPROM=N 0x0 = Select FB Divider 0x1 = Bypass FB Divider
5	TDC2_ZDM_FB_PRE_BYP	R/W	0x0	Inserts TDC feedback divider in series with selected channel divider ROM=Y, EEPROM=N 0x0 = ZDM disabled 0x1 = ZDM enable
4:3	TDC2_IN_SEL	R/W	0x3	Selects zero delay input ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = OUT_4_5_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO2 direct (ZDM disabled)
2:0	TDC2_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = ZDM disabled 0x3 = Reserved 0x4 = Reserved 0x5 = ZDM enabled 0x6 = Reserved 0x7 = Reserved

1.60 R77 Register (Offset = 0x4D) [Reset = 0x1A]

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Table 1-62. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved

Table 1-62. R77 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TDC1_ZDM_BYPASS_FB_DIV	R/W	0x0	Selects TDC feedback input. 0=FB_DIV, 1=ZD bypass FBDIV ROM=Y, EEPROM=N 0x0 = Select FB Divider 0x1 = Bypass FB Divider
5	TDC1_ZDM_FB_PRE_BYP	R/W	0x0	Inserts TDC feedback divider in series with selected channel divider ROM=Y, EEPROM=N 0x0 = ZDM disabled 0x1 = ZDM enable
4:3	TDC1_IN_SEL	R/W	0x3	Selects which output group to feedback for zero delay mode. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = OUT_0_1_ZD_FB 0x2 = OUT_0_1_ZD_FB 0x3 = VCO1 direct (ZDM disabled)
2:0	TDC1_IN_DRV_SEL	R/W	0x2	Enables zero delay input mux output ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = ZDM disabled 0x3 = Reserved 0x4 = Reserved 0x5 = ZDM enabled 0x6 = Reserved 0x7 = Reserved

1.61 R78 Register (Offset = 0x4E) [Reset = 0x00]

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Table 1-63. R78 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5	REF_OUT01_EN	R/W	0x0	Ref to OUT0_1 Enable. Enables the path for a reference clock (selected by REF_2OUT01_SEL) to be available for selection at OUT0_1. ROM=Y, EEPROM=N
4:0	REF_OUT01_SEL	R/W	0x0	Ref to OUT0_1 Select. Selects one reference clock which will be fed to the input of OUT0_1 (if path enabled by REF_2OUT01_EN). ROM=Y, EEPROM=N 0x0 = OFF 0x1 = REF0 0x2 = REF1 0x4 = REF2 0x8 = REF3

1.62 R79 Register (Offset = 0x4F) [Reset = 0x2E]

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Table 1-64. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF0_EARLY_DET_EN	R/W	0x1	REF0 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF0_PH_VALID_EN	R/W	0x0	REF0 Phase Validation Enable ROM=Y, EEPROM=N
3	REF0_VALTMR_EN	R/W	0x1	REF0 Validation Timer Enable ROM=Y, EEPROM=N

Table 1-64. R79 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	REF0_PPM_EN	R/W	0x1	REF0 Freq ppm Enable ROM=Y, EEPROM=N
1	REF0_MISSCLK_EN	R/W	0x1	REF0 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R/W	0x0	Reserved

1.63 R80 Register (Offset = 0x50) [Reset = 0x2E]

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Table 1-65. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF1_EARLY_DET_EN	R/W	0x1	REF1 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF1_PH_VALID_EN	R/W	0x0	REF1 Phase Validation Enable ROM=Y, EEPROM=N
3	REF1_VALTMR_EN	R/W	0x1	REF1 Validation Timer Enable ROM=Y, EEPROM=N
2	REF1_PPM_EN	R/W	0x1	REF1 Freq ppm Enable ROM=Y, EEPROM=N
1	REF1_MISSCLK_EN	R/W	0x1	REF1 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R/W	0x0	Reserved

1.64 R81 Register (Offset = 0x51) [Reset = 0x00]

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Table 1-66. R81 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF2_EARLY_DET_EN	R/W	0x0	REF2 Early Clock Detect Enable ROM=Y, EEPROM=N
4	REF2_PH_VALID_EN	R/W	0x0	REF2 Phase Validation Enable ROM=Y, EEPROM=N
3	REF2_VALTMR_EN	R/W	0x0	REF2 Validation Timer Enable ROM=Y, EEPROM=N
2	REF2_PPM_EN	R/W	0x0	REF2 Freq ppm Enable ROM=Y, EEPROM=N
1	REF2_MISSCLK_EN	R/W	0x0	REF2 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R/W	0x0	Reserved

1.65 R82 Register (Offset = 0x52) [Reset = 0x00]

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Table 1-67. R82 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	REF3_EARLY_DET_EN	R/W	0x0	REF3 Early Clock Detect Enable ROM=Y, EEPROM=N

Table 1-67. R82 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	REF3_PH_VALID_EN	R/W	0x0	REF3 Phase Validation Enable ROM=Y, EEPROM=N
3	REF3_VALTMR_EN	R/W	0x0	REF3 Validation Timer Enable ROM=Y, EEPROM=N
2	REF3_PPM_EN	R/W	0x0	REF3 Freq ppm Enable ROM=Y, EEPROM=N
1	REF3_MISSCLK_EN	R/W	0x0	REF3 Missing Clock Detect Enable ROM=Y, EEPROM=N
0	RESERVED	R/W	0x0	Reserved

1.66 R83 Register (Offset = 0x53) [Reset = 0xAA]

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Table 1-68. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	REF3_DET_CLK_DIV	R/W	0x2	REF3 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)
5:4	REF2_DET_CLK_DIV	R/W	0x2	REF2 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)
3:2	REF1_DET_CLK_DIV	R/W	0x2	REF1 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)
1:0	REF0_DET_CLK_DIV	R/W	0x2	REF0 Clock Detector Divider. Bit 0 controls the divide value (0=Div4, 1=Div16). Bit 1, if set, causes the divider to be bypassed. ROM=Y, EEPROM=N 0x0 = Div By 4 0x1 = Div By 16 0x2 = Bypass 0x3 = Bypass (Reserved)

1.67 R84 Register (Offset = 0x54) [Reset = 0x00]

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Table 1-69. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_MISSCLK_DIV_21:16	R/W	0x0	See Register 86

1.68 R85 Register (Offset = 0x55) [Reset = 0x00]

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Table 1-70. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_MISSCLK_DIV_15:8	R/W	0x0	See Register 86

1.69 R86 Register (Offset = 0x56) [Reset = 0x36]

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Table 1-71. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_MISSCLK_DIV	R/W	0x36	REF0 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF0 or VCO2/5 to REF0 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.70 R87 Register (Offset = 0x57) [Reset = 0x00]

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Table 1-72. R87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_MISSCLK_DIV_21:16	R/W	0x0	See Register 89

1.71 R88 Register (Offset = 0x58) [Reset = 0x00]

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Table 1-73. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_MISSCLK_DIV_15:8	R/W	0x0	See Register 89

1.72 R89 Register (Offset = 0x59) [Reset = 0x36]

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Table 1-74. R89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_MISSCLK_DIV	R/W	0x36	REF1 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF1 or VCO2/5 to REF1 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.73 R90 Register (Offset = 0x5A) [Reset = 0x00]

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Table 1-75. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-75. R90 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REF2_MISSCLK_DIV_21:16	R/W	0x0	See Register 92

1.74 R91 Register (Offset = 0x5B) [Reset = 0x00]

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Table 1-76. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_MISSCLK_DIV_15:8	R/W	0x0	See Register 92

1.75 R92 Register (Offset = 0x5C) [Reset = 0x36]

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Table 1-77. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_MISSCLK_DIV	R/W	0x36	REF2 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF2 or VCO2/5 to REF2 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.76 R93 Register (Offset = 0x5D) [Reset = 0x00]

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Table 1-78. R93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF3_MISSCLK_DIV_21:16	R/W	0x0	See Register 95

1.77 R94 Register (Offset = 0x5E) [Reset = 0x00]

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Table 1-79. R94 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_MISSCLK_DIV_15:8	R/W	0x0	See Register 95

1.78 R95 Register (Offset = 0x5F) [Reset = 0x36]

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Table 1-80. R95 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_MISSCLK_DIV	R/W	0x36	REF3 Missing Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF3 or VCO2/5 to REF3 (determined by REF0_MISSCLK_VCOSEL selection) with some offset added for upper bound. ROM=Y, EEPROM=N

1.79 R96 Register (Offset = 0x60) [Reset = 0x00]

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Table 1-81. R96 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:1	RESERVED	R/W	0x0	Reserved
0	REF0_MISSCLK_VCOSEL	R/W	0x0	Missing/Early Clock Detector VCO selection for all references. Also selects TEC clock source. ROM=Y, EEPROM=N 0x0 = VCO3 0x1 = VCO2

1.80 R97 Register (Offset = 0x61) [Reset = 0x00]

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Table 1-82. R97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 99

1.81 R98 Register (Offset = 0x62) [Reset = 0x00]

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Table 1-83. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 99

1.82 R99 Register (Offset = 0x63) [Reset = 0x2E]

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Table 1-84. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_EARLY_CLK_DIV	R/W	0x2E	REF0 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF0 or VCO2/5 to REF0 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.83 R100 Register (Offset = 0x64) [Reset = 0x00]

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Table 1-85. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 102

1.84 R101 Register (Offset = 0x65) [Reset = 0x00]

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Table 1-86. R101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 102

1.85 R102 Register (Offset = 0x66) [Reset = 0x2E]

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Table 1-87. R102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_EARLY_CLK_DIV	R/W	0x2E	REF1 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF1 or VCO2/5 to REF1 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.86 R103 Register (Offset = 0x67) [Reset = 0x00]

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Table 1-88. R103 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF2_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 105

1.87 R104 Register (Offset = 0x68) [Reset = 0x00]

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Table 1-89. R104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 105

1.88 R105 Register (Offset = 0x69) [Reset = 0x2E]

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Table 1-90. R105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_EARLY_CLK_DIV	R/W	0x2E	REF2 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF2 or VCO2/5 to REF2 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.89 R106 Register (Offset = 0x6A) [Reset = 0x00]

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Table 1-91. R106 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF3_EARLY_CLK_DIV_21:16	R/W	0x0	See Register 108

1.90 R107 Register (Offset = 0x6B) [Reset = 0x00]

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Table 1-92. R107 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_EARLY_CLK_DIV_15:8	R/W	0x0	See Register 108

1.91 R108 Register (Offset = 0x6C) [Reset = 0x2E]

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Table 1-93. R108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_EARLY_CLK_DIV	R/W	0x2E	REF3 Early Clock Detector Divider. 21-bit divide value. Should be equal to the ratio of either VCO3/2 to REF3 or VCO2/5 to REF3 (determined by REF0_MISSCLK_VCOSEL selection) with some offset subtracted for lower bound. ROM=Y, EEPROM=N

1.92 R109 Register (Offset = 0x6D) [Reset = 0x00]

Return to the Summary Table.

Table 1-94. R109 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF0_PPM_MIN_14:8	R/W	0x0	See Register 110

1.93 R110 Register (Offset = 0x6E) [Reset = 0x0E]

Return to the Summary Table.

Table 1-95. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PPM_MIN	R/W	0xE	REF0 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.94 R111 Register (Offset = 0x6F) [Reset = 0x00]

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Table 1-96. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF0_PPM_MAX_14:8	R/W	0x0	See Register 112

1.95 R112 Register (Offset = 0x70) [Reset = 0x14]

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Table 1-97. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PPM_MAX	R/W	0x14	REF0 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.96 R113 Register (Offset = 0x71) [Reset = 0x00]

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Table 1-98. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF1_PPM_MIN_14:8	R/W	0x0	See Register 114

1.97 R114 Register (Offset = 0x72) [Reset = 0x0E]

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Table 1-99. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PPM_MIN	R/W	0xE	REF1 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.98 R115 Register (Offset = 0x73) [Reset = 0x00]

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Table 1-100. R115 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF1_PPM_MAX_14:8	R/W	0x0	See Register 116

1.99 R116 Register (Offset = 0x74) [Reset = 0x14]

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Table 1-101. R116 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PPM_MAX	R/W	0x14	REF1 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.100 R117 Register (Offset = 0x75) [Reset = 0x00]

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Table 1-102. R117 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF2_PPM_MIN_14:8	R/W	0x0	See Register 118

1.101 R118 Register (Offset = 0x76) [Reset = 0x0E]

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Table 1-103. R118 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_PPM_MIN	R/W	0xE	REF2 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.102 R119 Register (Offset = 0x77) [Reset = 0x00]

Return to the Summary Table.

Table 1-104. R119 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF2_PPM_MAX_14:8	R/W	0x0	See Register 120

1.103 R120 Register (Offset = 0x78) [Reset = 0x14]

Return to the Summary Table.

Table 1-105. R120 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_PPM_MAX	R/W	0x14	REF2 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.104 R121 Register (Offset = 0x79) [Reset = 0x00]

Return to the Summary Table.

Table 1-106. R121 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF3_PPM_MIN_14:8	R/W	0x0	See Register 122

1.105 R122 Register (Offset = 0x7A) [Reset = 0x0E]

Return to the Summary Table.

Table 1-107. R122 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_PPM_MIN	R/W	0xE	REF3 Frequency PPM Lower Limit ROM=Y, EEPROM=N

1.106 R123 Register (Offset = 0x7B) [Reset = 0x00]

Return to the Summary Table.

Table 1-108. R123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	REF3_PPM_MAX_14:8	R/W	0x0	See Register 124

1.107 R124 Register (Offset = 0x7C) [Reset = 0x14]

Return to the Summary Table.

Table 1-109. R124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_PPM_MAX	R/W	0x14	REF3 Frequency PPM Upper Limit ROM=Y, EEPROM=N

1.108 R141 Register (Offset = 0x8D) [Reset = 0x00]

Return to the Summary Table.

Table 1-110. R141 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	REF2_PH_VALID_CNT_MSB	R/W	0x0	REF2 Counter ROM=Y, EEPROM=N
3:0	REF2_CNTSTRT_27:24	R/W	0x0	See Register 144

1.109 R142 Register (Offset = 0x8E) [Reset = 0x01]

Return to the Summary Table.

Table 1-111. R142 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_CNTSTRT_23:16	R/W	0x1	See Register 144

1.110 R143 Register (Offset = 0x8F) [Reset = 0x96]

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Table 1-112. R143 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_CNTSTRT_15:8	R/W	0x96	See Register 144

1.111 R144 Register (Offset = 0x90) [Reset = 0xE7]

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Table 1-113. R144 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_CNTSTRT	R/W	0xE7	REF2 Counter ROM=Y, EEPROM=N

1.112 R145 Register (Offset = 0x91) [Reset = 0x00]

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Table 1-114. R145 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	REF2_HOLD_CNTSTRT_27:24	R/W	0x0	See Register 148

1.113 R146 Register (Offset = 0x92) [Reset = 0x03]

Return to the Summary Table.

Table 1-115. R146 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_HOLD_CNTSTRT_23:16	R/W	0x3	See Register 148

1.114 R147 Register (Offset = 0x93) [Reset = 0x0D]

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Table 1-116. R147 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_HOLD_CNTSTRT_15:8	R/W	0xD	See Register 148

1.115 R148 Register (Offset = 0x94) [Reset = 0x41]

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Table 1-117. R148 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_HOLD_CNTSTRT	R/W	0x41	REF2 Holdover Counter ROM=Y, EEPROM=N

1.116 R149 Register (Offset = 0x95) [Reset = 0x00]

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Table 1-118. R149 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	REF3_PH_VALID_CNT_MSB	R/W	0x0	REF3 Counter ROM=Y, EEPROM=N
3:0	REF3_CNTSTRT_27:24	R/W	0x0	See Register 152

1.117 R150 Register (Offset = 0x96) [Reset = 0x01]

Return to the Summary Table.

Table 1-119. R150 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_CNTSTRT_23:16	R/W	0x1	See Register 152

1.118 R151 Register (Offset = 0x97) [Reset = 0x96]

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Table 1-120. R151 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_CNTSTRT_15:8	R/W	0x96	See Register 152

1.119 R152 Register (Offset = 0x98) [Reset = 0xE7]

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Table 1-121. R152 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_CNTSTRT	R/W	0xE7	REF3 Counter ROM=Y, EEPROM=N

1.120 R153 Register (Offset = 0x99) [Reset = 0x00]

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Table 1-122. R153 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	REF3_HOLD_CNTSTRT_27:24	R/W	0x0	See Register 156

1.121 R154 Register (Offset = 0x9A) [Reset = 0x03]

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Table 1-123. R154 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_HOLD_CNTSTRT_23:16	R/W	0x3	See Register 156

1.122 R155 Register (Offset = 0x9B) [Reset = 0x0D]

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Table 1-124. R155 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_HOLD_CNTSTRT_15:8	R/W	0xD	See Register 156

1.123 R156 Register (Offset = 0x9C) [Reset = 0x41]

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Table 1-125. R156 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_HOLD_CNTSTRT	R/W	0x41	REF3 Holdover Counter ROM=Y, EEPROM=N

1.124 R157 Register (Offset = 0x9D) [Reset = 0x0A]

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Table 1-126. R157 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-126. R157 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF0VLDTMR	R/W	0xA	REF0 Validation Timer. All selected validations must be valid for selected amount of time before the IN0/REF0 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.125 R158 Register (Offset = 0x9E) [Reset = 0x0A]

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Table 1-127. R158 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-127. R158 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF1VLDTMR	R/W	0xA	REF1 Validation Timer. All selected validations must be valid for selected amount of time before the IN1/REF1 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.126 R159 Register (Offset = 0x9F) [Reset = 0x0A]

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Table 1-128. R159 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-128. R159 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF2VLDTMR	R/W	0xA	REF2 Validation Timer. All selected validations must be valid for selected amount of time before the IN2/REF2 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.127 R160 Register (Offset = 0xA0) [Reset = 0x0A]

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Table 1-129. R160 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-129. R160 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	REF3VLDTMR	R/W	0xA	REF3 Validation Timer. All selected validations must be valid for selected amount of time before the IN3/REF3 is considered valid. ROM=Y, EEPROM=N 0x0 = 0.1 ms 0x1 = 0.2 ms 0x2 = 0.4 ms 0x3 = 0.8 ms 0x4 = 1.6 ms 0x5 = 3.2 ms 0x6 = 6.4 ms 0x7 = 12.8 ms 0x8 = 25.6 ms 0x9 = 51.2 ms 0xA = 102.4 ms 0xB = 204.8 ms 0xC = 409.6 ms 0xD = 819.2 ms 0xE = 1.6 s 0xF = 3.3 s 0x10 = 6.6 s 0x11 = 13.1 s 0x12 = 26.2 s 0x13 = 52.4 s 0x14 = 1.7 min 0x15 = 3.5 min 0x16 = 7.0 min 0x17 = 14.0 min 0x18 = 28.0 min 0x19 = 55.9 min 0x1A = 1.9 hr 0x1B = 3.7 hr 0x1C = 7.5 hr 0x1D = 14.9 hr 0x1E = 29.8 hr 0x1F = 59.7 hr

1.128 R161 Register (Offset = 0xA1) [Reset = 0x00]

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Table 1-130. R161 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF0_PH_VALID_THR_13:8	R/W	0x0	REF0 Phase Validation Threshold ROM=Y, EEPROM=N

1.129 R162 Register (Offset = 0xA2) [Reset = 0x00]

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Table 1-131. R162 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF0_PH_VALID_THR	R/W	0x0	REF0 Phase Validation Threshold ROM=Y, EEPROM=N

1.130 R163 Register (Offset = 0xA3) [Reset = 0x00]

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Table 1-132. R163 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF1_PH_VALID_THR_13:8	R/W	0x0	REF1 Phase Validation Threshold ROM=Y, EEPROM=N

1.131 R164 Register (Offset = 0xA4) [Reset = 0x00]

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Table 1-133. R164 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF1_PH_VALID_THR	R/W	0x0	REF1 Phase Validation Threshold ROM=Y, EEPROM=N

1.132 R165 Register (Offset = 0xA5) [Reset = 0x00]

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Table 1-134. R165 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF2_PH_VALID_THR_13:8	R/W	0x0	REF2 Phase Validation Threshold ROM=Y, EEPROM=N

1.133 R166 Register (Offset = 0xA6) [Reset = 0x00]

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Table 1-135. R166 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF2_PH_VALID_THR	R/W	0x0	REF2 Phase Validation Threshold ROM=Y, EEPROM=N

1.134 R167 Register (Offset = 0xA7) [Reset = 0x00]

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Table 1-136. R167 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	REF3_PH_VALID_THR_13:8	R/W	0x0	REF3 Phase Validation Threshold ROM=Y, EEPROM=N

1.135 R168 Register (Offset = 0xA8) [Reset = 0x00]

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Table 1-137. R168 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REF3_PH_VALID_THR	R/W	0x0	REF3 Phase Validation Threshold ROM=Y, EEPROM=N

1.136 R170 Register (Offset = 0xAA) [Reset = 0x00]

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Table 1-138. R170 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMSCRC	R	0x0	NVM Stored CRC ROM=N, EEPROM=N

1.137 R171 Register (Offset = 0xAB) [Reset = 0x00]

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Table 1-139. R171 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	REGCOMMIT	R/WSC	0x0	Copy fields which also exist in SRAM to SRAM memory. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete. Next an EEPROM programming operation may be performed to update NVM EEPROM. When programming to alter an NVM profile, it is suggested to toggle PD# to assure default conditions, change the desired fields, then assert the REGCOMMIT bit. ROM=N, EEPROM=N
5	NVMCRCERR	R	0x0	NVM CRC Error Indication. The NVMCRCERR bit is set to 1 if a CRC Error has been detected when reading back from on-chip EEPROM during device configuration. ROM=N, EEPROM=N
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/WSC	0x0	Reserved
2	NVMBUSY	R	0x0	NVM Program Busy Indication. The NVMBUSY bit is 1 during an on-chip EEPROM Erase/Program cycle. While NVMBUSY is 1 the on-chip EEPROM cannot be accessed. Toggling PD# or removing power while NVMBUSY is asserted will corrupt the EEPROM. ROM=N, EEPROM=N
1	NVMERASE	R/WSC	0x0	NVM Erase Start. The NVMERASE bit is used to begin an on-chip EEPROM Erase cycle. The Erase cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register with the appropriate code. The NVMERASE bit is automatically cleared to 0.
0	NVMPROG	R/WSC	0x0	NVM Program Start. The NVMPROG bit is used to begin an on-chip EEPROM Program cycle. The Program cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register with the appropriate code. The NVMPROG bit is automatically cleared to 0.

1.138 R173 Register (Offset = 0xAD) [Reset = 0x00]

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Table 1-140. R173 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	MEMADR_12:8	R/W	0x0	See Register 174

1.139 R174 Register (Offset = 0xAE) [Reset = 0x00]

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Table 1-141. R174 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MEMADR	R/W	0x0	Memory Address. The MEMADR value determines the starting address for access to the on-chip memories. This same MEMADR value is used for EEPROM and SRAM access which share the same memory map and also ROM access. The NVMDAT field is used to read and write from EEPROM. The RAMDAT field is used to read and write from SRAM. The ROMDAT field is used to read and write from ROM.

1.140 R176 Register (Offset = 0xB0) [Reset = 0x00]

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Table 1-142. R176 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RAMDAT	R/W	0x0	RAM Read/Write Data. The first time an I2C/SMBus read or write transaction accesses the RAMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, a read transaction will return the RAM data located at the address specified by the MEMADR register and a write transaction will cause the current I2C/SMBus data to be written to the address specified by the MEMADR register. Any additional accesses which are part of the same transaction will cause the RAM address to be incremented and a read or write access will take place to the next SRAM address. The I2C/SMBus address will no longer be auto-incremented (that is, the I2C/SMBus address will be locked to the RAMDAT register after the first access). Access to the RAMDAT register will terminate at the end of the current I2C/SMBus transaction. ROM=N, EEPROM=N

1.141 R180 Register (Offset = 0xB4) [Reset = 0x00]

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Table 1-143. R180 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMUNLK	R/W	0x0	NVM Prog Unlock. The NVMUNLK register must be written immediately prior to setting the NVMERASE and NVMPROG bit, otherwise the Erase/Program cycle will not be triggered. NVMUNLK must be written with a value of 0xEA. ROM=N, EEPROM=N

1.142 R223 Register (Offset = 0xDF) [Reset = 0x00]

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Table 1-144. R223 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-144. R223 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	DPLL1_REF0_AUTO_PRTY	R/W	0x0	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL1_REF1_AUTO_PRTY	R/W	0x0	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.143 R224 Register (Offset = 0xE0) [Reset = 0x00]

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Table 1-145. R224 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL1_REF2_AUTO_PRTY	R/W	0x0	REF2 Priority for Automatic Switchover. Sets the priority for REF2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL1_REF3_AUTO_PRTY	R/W	0x0	REF3 Priority for Automatic Switchover. Sets the priority for REF3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.144 R225 Register (Offset = 0xE1) [Reset = 0x00]

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Table 1-146. R225 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL1_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 feedback from APLL2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL1_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 feedback from APLL3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.145 R226 Register (Offset = 0xE2) [Reset = 0x01]

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Table 1-147. R226 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5:3	DPLL1_MAN_REFSEL	R/W	0x0	DPLL1 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = REF2 0x3 = REF3 0x4 = PLL2 0x5 = PLL3
2	DPLL1_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL1 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL1_SWITCH_MODE	R/W	0x1	DPLL1 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto Non-revertive 0x1 = Auto Revertive 0x2 = Manual w/ Fallback 0x3 = Manual w/ Holdover

1.146 R227 Register (Offset = 0xE3) [Reset = 0x00]

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Table 1-148. R227 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_REFSEL_STAT	R	0x0	Reports the DPLL1 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = REF2 0x8 = REF3 0x10 = APLL2 0x20 = APLL3

1.147 R228 Register (Offset = 0xE4) [Reset = 0x00]

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Table 1-149. R228 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_LOCKDET_PPM_EN	R/W	0x0	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL1_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 229

1.148 R229 Register (Offset = 0xE5) [Reset = 0x0A]

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Table 1-150. R229 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_MAX	R/W	0xA	DPLL frequency lock detect in-lock threshold ROM=Y, EEPROM=N

1.149 R230 Register (Offset = 0xE6) [Reset = 0x00]

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Table 1-151. R230 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL1_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 231

1.150 R231 Register (Offset = 0xE7) [Reset = 0x64]

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Table 1-152. R231 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_UNLOCKDET_PPM_MAX	R/W	0x64	DPLL frequency lock detect out-of-lock threshold ROM=Y, EEPROM=N

1.151 R232 Register (Offset = 0xE8) [Reset = 0x00]

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Table 1-153. R232 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET2_PPM_CNTSTRT_29:24	R/W	0x0	See Register 235

1.152 R233 Register (Offset = 0xE9) [Reset = 0x09]

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Table 1-154. R233 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTRT_23:16	R/W	0x9	See Register 235

1.153 R234 Register (Offset = 0xEA) [Reset = 0x27]

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Table 1-155. R234 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTRT_15:8	R/W	0x27	See Register 235

1.154 R235 Register (Offset = 0xEB) [Reset = 0xC0]

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Table 1-156. R235 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET2_PPM_CNTSTRT	R/W	0xC0	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.155 R236 Register (Offset = 0xEC) [Reset = 0x00]

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Table 1-157. R236 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET_PPM_CNTSTRT_29:24	R/W	0x0	See Register 239

1.156 R237 Register (Offset = 0xED) [Reset = 0x22]

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Table 1-158. R237 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT_23:16	R/W	0x22	See Register 239

1.157 R238 Register (Offset = 0xEE) [Reset = 0xA0]

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Table 1-159. R238 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT_15:8	R/W	0xA0	See Register 239

1.158 R239 Register (Offset = 0xEF) [Reset = 0xF3]

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Table 1-160. R239 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_PPM_CNTSTRT	R/W	0xF3	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.159 R240 Register (Offset = 0xF0) [Reset = 0x00]

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Table 1-161. R240 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_29:24	R/W	0x0	See Register 243

1.160 R241 Register (Offset = 0xF1) [Reset = 0x98]

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Table 1-162. R241 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_23:16	R/W	0x98	See Register 243

1.161 R242 Register (Offset = 0xF2) [Reset = 0x96]

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Table 1-163. R242 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNTSTRT_15:8	R/W	0x96	See Register 243

1.162 R243 Register (Offset = 0xF3) [Reset = 0x83]

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Table 1-164. R243 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LOCKDET_VCO_PPM_CNTSTRT	R/W	0x83	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.163 R244 Register (Offset = 0xF4) [Reset = 0x00]

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Table 1-165. R244 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL1_STATUS_PPM_LOCK	R	0x0	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.164 R247 Register (Offset = 0xF7) [Reset = 0x55]

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Table 1-166. R247 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_LOOP_EN	R/W	0x0	Enable DPLL1 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL1_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	RESERVED	R/W	0x0	Reserved
4	DPLL1_PHS1_EN	R/W	0x1	Enable holdover exit phase slew control . ROM=Y, EEPROM=N
3	DPLL1_ZDM_EN	R/W	0x0	Enable Zero Delay ROM=Y, EEPROM=N
2	DPLL1_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1	DPLL1_PHASE_CANCEL_ALWAYS	R/W	0x0	Force phase cancellation to always occur when DPLL is acquiring lock ROM=Y, EEPROM=N
0	RESERVED	R/W	0x1	Reserved

1.165 R248 Register (Offset = 0xF8) [Reset = 0x42]

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Table 1-167. R248 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL1_HOLD_SLEW_LIM_EN	R/W	0x0	Enable slew limiter when entering holdover. Allows slew rate control between current DPLL value before entering holdover and history value. ROM=Y, EEPROM=N
6	RESERVED	R/W	0x1	Reserved
5:3	RESERVED	R	0x0	Reserved
2	DPLL1_CLK_DIV_SRC_SEL	R/W	0x0	DPLL1 cannot be used without DPLL2 or DPLL3 operating. DPLL1 clock select 0x0 = DPLL3 0x1 = DPLL2
1:0	RESERVED	R/W	0x2	Reserved

1.166 R250 Register (Offset = 0xFA) [Reset = 0x00]

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Table 1-168. R250 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL1_PH_OFFSET_44:40	R/W	0x0	See Register 255

1.167 R251 Register (Offset = 0xFB) [Reset = 0x00]

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Table 1-169. R251 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_39:32	R/W	0x0	See Register 255

1.168 R252 Register (Offset = 0xFC) [Reset = 0x00]

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Table 1-170. R252 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_31:24	R/W	0x0	See Register 255

1.169 R253 Register (Offset = 0xFD) [Reset = 0x00]

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Table 1-171. R253 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_23:16	R/W	0x0	See Register 255

1.170 R254 Register (Offset = 0xFE) [Reset = 0x00]

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Table 1-172. R254 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET_15:8	R/W	0x0	See Register 255

1.171 R255 Register (Offset = 0xFF) [Reset = 0x00]

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Table 1-173. R255 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PH_OFFSET	R/W	0x0	Phase offset to adjust and calibrate input to output phase in ZDM. ROM=Y, EEPROM=N

1.172 R256 Register (Offset = 0x100) [Reset = 0x00]

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Table 1-174. R256 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_39:32	R/W	0x0	See Register 260

1.173 R257 Register (Offset = 0x101) [Reset = 0x00]

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Table 1-175. R257 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_31:24	R/W	0x0	See Register 260

1.174 R258 Register (Offset = 0x102) [Reset = 0x00]

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Table 1-176. R258 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_23:16	R/W	0x0	See Register 260

1.175 R259 Register (Offset = 0x103) [Reset = 0x00]

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Table 1-177. R259 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN_15:8	R/W	0x0	See Register 260

1.176 R260 Register (Offset = 0x104) [Reset = 0x00]

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Table 1-178. R260 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FREE_RUN	R/W	0x0	DPLL1 starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.177 R290 Register (Offset = 0x122) [Reset = 0x03]

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Table 1-179. R290 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_LCK_TIMER_9:8	R/W	0x3	See Register 291

1.178 R291 Register (Offset = 0x123) [Reset = 0x09]

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Table 1-180. R291 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_LCK_TIMER	R/W	0x9	Minimum amount of time until DPLL1_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.179 R292 Register (Offset = 0x124) [Reset = 0x01]

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Table 1-181. R292 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_HIST_TIMER_9:8	R/W	0x1	See Register 293

1.180 R293 Register (Offset = 0x125) [Reset = 0x92]

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Table 1-182. R293 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_HIST_TIMER	R/W	0x92	Time interval between history update events. ROM=Y, EEPROM=N

1.181 R294 Register (Offset = 0x126) [Reset = 0x0D]

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Table 1-183. R294 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x3	Reserved
1:0	DPLL1_HOLD_TIMER_9:8	R/W	0x1	See Register 295

1.182 R295 Register (Offset = 0x127) [Reset = 0x42]

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Table 1-184. R295 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.183 R296 Register (Offset = 0x128) [Reset = 0x01]

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Table 1-185. R296 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL1_PHS1_TIMER_9:8	R/W	0x1	See Register 297

1.184 R297 Register (Offset = 0x129) [Reset = 0x40]

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Table 1-186. R297 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_PHS1_TIMER	R/W	0x40	Holdover exit phase slew control. Timer controlling update period. ROM=Y, EEPROM=N

1.185 R302 Register (Offset = 0x12E) [Reset = 0x08]

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Table 1-187. R302 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL1_HIST_GAIN	R/W	0x8	History filter gain ROM=Y, EEPROM=N

1.186 R303 Register (Offset = 0x12F) [Reset = 0x22]

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Table 1-188. R303 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PL_THRESH	R/W	0x22	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.187 R304 Register (Offset = 0x130) [Reset = 0x24]

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Table 1-189. R304 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PL_UNLK_THRESH	R/W	0x24	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.188 R305 Register (Offset = 0x131) [Reset = 0x07]

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Table 1-190. R305 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_PHS1_THRESH	R/W	0x7	Holdover exit phase slew control. Change per timer event. ROM=Y, EEPROM=N

1.189 R308 Register (Offset = 0x134) [Reset = 0x3F]

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Table 1-191. R308 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-191. R308 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DPLL1_HOLD_SLEW_STEP	R/W	0x3F	When DPLL exits holdover, rate of phase change relates to the ratio of DPLLx_HOLD_SLEW_STEP divided by DPLLx_HOLD_TIMER. DPLLx_HOLD_SLEW_STEP is applied to DPLL numerator when exiting holdover or APLL numerator when using APLL relative DCO. ROM=Y, EEPROM=N

1.190 R310 Register (Offset = 0x136) [Reset = 0x00]

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Table 1-192. R310 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL1_STATUS_PL	R	0x0	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.191 R311 Register (Offset = 0x137) [Reset = 0x00]

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Table 1-193. R311 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL1_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.192 R314 Register (Offset = 0x13A) [Reset = 0x00]

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Table 1-194. R314 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB_DIV_32:32	R/W	0x0	See Register 318

1.193 R315 Register (Offset = 0x13B) [Reset = 0x00]

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Table 1-195. R315 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_31:24	R/W	0x0	See Register 318

1.194 R316 Register (Offset = 0x13C) [Reset = 0x00]

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Table 1-196. R316 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_23:16	R/W	0x0	See Register 318

1.195 R317 Register (Offset = 0x13D) [Reset = 0x00]

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Table 1-197. R317 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV_15:8	R/W	0x0	See Register 318

1.196 R318 Register (Offset = 0x13E) [Reset = 0xD3]

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Table 1-198. R318 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DIV	R/W	0xD3	DPLL Feedback Divider N Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.197 R319 Register (Offset = 0x13F) [Reset = 0x81]

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Table 1-199. R319 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_39:32	R/W	0x81	See Register 323

1.198 R320 Register (Offset = 0x140) [Reset = 0xD7]

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Table 1-200. R320 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_31:24	R/W	0xD7	See Register 323

1.199 R321 Register (Offset = 0x141) [Reset = 0xDB]

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Table 1-201. R321 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_23:16	R/W	0xDB	See Register 323

1.200 R322 Register (Offset = 0x142) [Reset = 0xF3]

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Table 1-202. R322 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_15:8	R/W	0xF3	See Register 323

1.201 R323 Register (Offset = 0x143) [Reset = 0xFC]

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Table 1-203. R323 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM	R/W	0xFC	DPLL Feedback Divider Numerator Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.202 R324 Register (Offset = 0x144) [Reset = 0xFF]

Return to the Summary Table.

Table 1-204. R324 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_39:32	R/W	0xFF	See Register 328

1.203 R325 Register (Offset = 0x145) [Reset = 0xFF]

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Table 1-205. R325 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_31:24	R/W	0xFF	See Register 328

1.204 R326 Register (Offset = 0x146) [Reset = 0xFF]

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Table 1-206. R326 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_23:16	R/W	0xFF	See Register 328

1.205 R327 Register (Offset = 0x147) [Reset = 0xFE]

Return to the Summary Table.

Table 1-207. R327 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN_15:8	R/W	0xFE	See Register 328

1.206 R328 Register (Offset = 0x148) [Reset = 0xEC]

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Table 1-208. R328 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_DEN	R/W	0xEC	DPLL Feedback Divider Denominator Value used with DPLL1 feedback configuration 1 ROM=Y, EEPROM=N

1.207 R329 Register (Offset = 0x149) [Reset = 0x00]

Return to the Summary Table.

Table 1-209. R329 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB2_DIV_32:32	R/W	0x0	See Register 333

1.208 R330 Register (Offset = 0x14A) [Reset = 0x00]

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Table 1-210. R330 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_31:24	R/W	0x0	See Register 333

1.209 R331 Register (Offset = 0x14B) [Reset = 0x00]

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Table 1-211. R331 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_23:16	R/W	0x0	See Register 333

1.210 R332 Register (Offset = 0x14C) [Reset = 0x0F]

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Table 1-212. R332 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV_15:8	R/W	0xF	See Register 333

1.211 R333 Register (Offset = 0x14D) [Reset = 0xA0]

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Table 1-213. R333 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DIV	R/W	0xA0	DPLL Feedback Divider N Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.212 R334 Register (Offset = 0x14E) [Reset = 0x00]

Return to the Summary Table.

Table 1-214. R334 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_39:32	R/W	0x0	See Register 338

1.213 R335 Register (Offset = 0x14F) [Reset = 0x00]

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Table 1-215. R335 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_31:24	R/W	0x0	See Register 338

1.214 R336 Register (Offset = 0x150) [Reset = 0x00]

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Table 1-216. R336 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_23:16	R/W	0x0	See Register 338

1.215 R337 Register (Offset = 0x151) [Reset = 0x00]

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Table 1-217. R337 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM_15:8	R/W	0x0	See Register 338

1.216 R338 Register (Offset = 0x152) [Reset = 0x00]

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Table 1-218. R338 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.217 R339 Register (Offset = 0x153) [Reset = 0x00]

Return to the Summary Table.

Table 1-219. R339 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_39:32	R/W	0x0	See Register 343

1.218 R340 Register (Offset = 0x154) [Reset = 0x00]

Return to the Summary Table.

Table 1-220. R340 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_31:24	R/W	0x0	See Register 343

1.219 R341 Register (Offset = 0x155) [Reset = 0x00]

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Table 1-221. R341 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_23:16	R/W	0x0	See Register 343

1.220 R342 Register (Offset = 0x156) [Reset = 0x00]

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Table 1-222. R342 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN_15:8	R/W	0x0	See Register 343

1.221 R343 Register (Offset = 0x157) [Reset = 0x00]

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Table 1-223. R343 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB2_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.222 R344 Register (Offset = 0x158) [Reset = 0x00]

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Table 1-224. R344 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL1_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4	DPLL1_REF4_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF4. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
3	DPLL1_REF3_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
2	DPLL1_REF2_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF2. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
1	DPLL1_REF1_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
0	DPLL1_REF0_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.223 R345 Register (Offset = 0x159) [Reset = 0x02]

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Table 1-225. R345 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R/W	0x0	Reserved
2:0	DPLL1_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N 0x0 = Integer 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.224 R346 Register (Offset = 0x15A) [Reset = 0x00]

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Table 1-226. R346 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL1_FB_FDEV_37:32	R/W	0x0	See Register 350

1.225 R347 Register (Offset = 0x15B) [Reset = 0x00]

Return to the Summary Table.

Table 1-227. R347 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_31:24	R/W	0x0	See Register 350

1.226 R348 Register (Offset = 0x15C) [Reset = 0x00]

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Table 1-228. R348 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_23:16	R/W	0x0	See Register 350

1.227 R349 Register (Offset = 0x15D) [Reset = 0x00]

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Table 1-229. R349 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV_15:8	R/W	0x0	See Register 350

1.228 R350 Register (Offset = 0x15E) [Reset = 0x00]

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Table 1-230. R350 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_FDEV	R/W	0x0	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.229 R351 Register (Offset = 0x15F) [Reset = 0x00]

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Table 1-231. R351 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.230 R352 Register (Offset = 0x160) [Reset = 0x00]

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Table 1-232. R352 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL1_FB_FDEV_EN	R/W	0x0	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.231 R353 Register (Offset = 0x161) [Reset = 0x00]

Return to the Summary Table.

Table 1-233. R353 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_39:32	R	0x0	See Register 357

1.232 R354 Register (Offset = 0x162) [Reset = 0x00]

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Table 1-234. R354 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_31:24	R	0x0	See Register 357

1.233 R355 Register (Offset = 0x163) [Reset = 0x00]

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Table 1-235. R355 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_23:16	R	0x0	See Register 357

1.234 R356 Register (Offset = 0x164) [Reset = 0x00]

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Table 1-236. R356 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT_15:8	R	0x0	See Register 357

1.235 R357 Register (Offset = 0x165) [Reset = 0x00]

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Table 1-237. R357 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_FB_NUM_STAT	R	0x0	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.236 R358 Register (Offset = 0x166) [Reset = 0x00]

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Table 1-238. R358 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL1_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL1_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1	DPLL1_REF2_DBLR_EN	R/W	0x0	DPLL Reference 2 Doubler Enable ROM=Y, EEPROM=N
0	DPLL1_REF3_DBLR_EN	R/W	0x0	DPLL Reference 3 Doubler Enable ROM=Y, EEPROM=N

1.237 R359 Register (Offset = 0x167) [Reset = 0x00]

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Table 1-239. R359 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF0_RDIV_15:8	R/W	0x0	See Register 360

1.238 R360 Register (Offset = 0x168) [Reset = 0x01]

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Table 1-240. R360 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF0_RDIV	R/W	0x1	DPLL REF0 R-divider value ROM=Y, EEPROM=N

1.239 R361 Register (Offset = 0x169) [Reset = 0x00]

Return to the Summary Table.

Table 1-241. R361 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF1_RDIV_15:8	R/W	0x0	See Register 362

1.240 R362 Register (Offset = 0x16A) [Reset = 0x01]

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Table 1-242. R362 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF1_RDIV	R/W	0x1	DPLL REF1 R-divider value ROM=Y, EEPROM=N

1.241 R363 Register (Offset = 0x16B) [Reset = 0x00]

Return to the Summary Table.

Table 1-243. R363 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF2_RDIV_15:8	R/W	0x0	See Register 364

1.242 R364 Register (Offset = 0x16C) [Reset = 0x00]

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Table 1-244. R364 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF2_RDIV	R/W	0x0	DPLL REF2 R-divider value ROM=Y, EEPROM=N

1.243 R365 Register (Offset = 0x16D) [Reset = 0x00]

Return to the Summary Table.

Table 1-245. R365 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF3_RDIV_15:8	R/W	0x0	See Register 366

1.244 R366 Register (Offset = 0x16E) [Reset = 0x00]

Return to the Summary Table.

Table 1-246. R366 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF3_RDIV	R/W	0x0	DPLL REF3 R-divider value ROM=Y, EEPROM=N

1.245 R367 Register (Offset = 0x16F) [Reset = 0x00]

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Table 1-247. R367 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF4_RDIV_15:8	R/W	0x0	See Register 368

1.246 R368 Register (Offset = 0x170) [Reset = 0x00]

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Table 1-248. R368 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF4_RDIV	R/W	0x0	DPLL REF4 R-divider value ROM=Y, EEPROM=N

1.247 R369 Register (Offset = 0x171) [Reset = 0x00]

Return to the Summary Table.

Table 1-249. R369 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF5_RDIV_15:8	R/W	0x0	DPLL REF5 R-divider value. For use when DPLL1 uses output of VCO3 as a reference. ROM=Y, EEPROM=N

1.248 R370 Register (Offset = 0x172) [Reset = 0x00]

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Table 1-250. R370 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL1_REF5_RDIV	R/W	0x0	DPLL REF5 R-divider value. For use when DPLL1 uses output of VCO3 as a reference. ROM=Y, EEPROM=N

1.249 R373 Register (Offset = 0x175) [Reset = 0x00]

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Table 1-251. R373 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_REF0_AUTO_PRTY	R/W	0x0	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL2_REF1_AUTO_PRTY	R/W	0x0	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.250 R374 Register (Offset = 0x176) [Reset = 0x00]

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Table 1-252. R374 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_REF2_AUTO_PRTY	R/W	0x0	REF2 Priority for Automatic Switchover. Sets the priority for REF2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL2_REF3_AUTO_PRTY	R/W	0x0	REF3 Priority for Automatic Switchover. Sets the priority for REF3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.251 R375 Register (Offset = 0x177) [Reset = 0x00]

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Table 1-253. R375 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL2_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 feedback from APLL1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL2_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 feedback from APLL3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.252 R376 Register (Offset = 0x178) [Reset = 0x01]

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Table 1-254. R376 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5:3	DPLL2_MAN_REFSEL	R/W	0x0	DPLL2 Manual Reference Selection ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = REF2 0x3 = REF3 0x4 = PLL1 0x5 = PLL3
2	DPLL2_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL2 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL2_SWITCH_MODE	R/W	0x1	DPLL2 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual fallback 0x3 = Manual Holdover

1.253 R377 Register (Offset = 0x179) [Reset = 0x00]

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Table 1-255. R377 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_REFSEL_STAT	R	0x0	Reads the DPLL2 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = REF2 0x8 = REF3 0x10 = APLL1 0x20 = APLL3

1.254 R378 Register (Offset = 0x17A) [Reset = 0x00]

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Table 1-256. R378 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_LOCKDET_PPM_EN	R/W	0x0	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL2_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 379

1.255 R379 Register (Offset = 0x17B) [Reset = 0x0A]

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Table 1-257. R379 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_MAX	R/W	0xA	DPLL frequency lock detect in-lock threshold ROM=Y, EEPROM=N

1.256 R380 Register (Offset = 0x17C) [Reset = 0x00]

Return to the Summary Table.

Table 1-258. R380 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL2_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 381

1.257 R381 Register (Offset = 0x17D) [Reset = 0x64]

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Table 1-259. R381 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_UNLOCKDET_PPM_MAX	R/W	0x64	DPLL frequency lock detect out-of-lock threshold ROM=Y, EEPROM=N

1.258 R382 Register (Offset = 0x17E) [Reset = 0x00]

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Table 1-260. R382 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET2_PPM_CNTSTRT_29:24	R/W	0x0	See Register 385

1.259 R383 Register (Offset = 0x17F) [Reset = 0x00]

Return to the Summary Table.

Table 1-261. R383 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTRT_23:16	R/W	0x0	See Register 385

1.260 R384 Register (Offset = 0x180) [Reset = 0x09]

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Table 1-262. R384 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTRT_15:8	R/W	0x9	See Register 385

1.261 R385 Register (Offset = 0x181) [Reset = 0xC5]

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Table 1-263. R385 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET2_PPM_CNTSTRT	R/W	0xC5	DPLL frequency lock detect reference count value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.262 R386 Register (Offset = 0x182) [Reset = 0x00]

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Table 1-264. R386 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_LOCKDET_PPM_CNTSTRT_29:24	R/W	0x0	See Register 389

1.263 R387 Register (Offset = 0x183) [Reset = 0x27]

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Table 1-265. R387 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT_23:16	R/W	0x27	See Register 389

1.264 R388 Register (Offset = 0x184) [Reset = 0x75]

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Table 1-266. R388 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT_15:8	R/W	0x75	See Register 389

1.265 R389 Register (Offset = 0x185) [Reset = 0x03]

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Table 1-267. R389 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_PPM_CNTSTRT	R/W	0x3	DPLL frequency lock detect reference count value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.266 R390 Register (Offset = 0x186) [Reset = 0x00]

Return to the Summary Table.

Table 1-268. R390 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-268. R390 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_29:24	R/W	0x0	See Register 393

1.267 R391 Register (Offset = 0x187) [Reset = 0x98]

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Table 1-269. R391 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_23:16	R/W	0x98	See Register 393

1.268 R392 Register (Offset = 0x188) [Reset = 0x96]

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Table 1-270. R392 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT_15:8	R/W	0x96	See Register 393

1.269 R393 Register (Offset = 0x189) [Reset = 0x82]

Return to the Summary Table.

Table 1-271. R393 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LOCKDET_VCO_PPM_CNTSTRT	R/W	0x82	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.270 R394 Register (Offset = 0x18A) [Reset = 0x00]

Return to the Summary Table.

Table 1-272. R394 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL2_STATUS_PPM_LOCK	R	0x0	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.271 R397 Register (Offset = 0x18D) [Reset = 0x55]

Return to the Summary Table.

Table 1-273. R397 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_LOOP_EN	R/W	0x0	Enable DPLL2 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL2_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	RESERVED	R/W	0x0	Reserved

Table 1-273. R397 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DPLL2_PHS1_EN	R/W	0x1	Enable holdover exit phase slew control . ROM=Y, EEPROM=N
3	DPLL2_ZDM_EN	R/W	0x0	Enable Zero Delay ROM=Y, EEPROM=N
2	DPLL2_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1	DPLL2_PHASE_CANCEL_ALWAYS	R/W	0x0	Force phase cancellation to always occur when DPLL is acquiring lock ROM=Y, EEPROM=N
0	RESERVED	R/W	0x1	Reserved

1.272 R398 Register (Offset = 0x18E) [Reset = 0x6E]

Return to the Summary Table.

Table 1-274. R398 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL2_HOLD_SLEW_LIM_EN	R/W	0x0	Enable slew limiter when entering holdover ROM=Y, EEPROM=N
6:0	RESERVED	R/W	0x6E	Reserved

1.273 R400 Register (Offset = 0x190) [Reset = 0x00]

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Table 1-275. R400 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL2_PH_OFFSET_44:40	R/W	0x0	See Register 405

1.274 R401 Register (Offset = 0x191) [Reset = 0x00]

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Table 1-276. R401 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_39:32	R/W	0x0	See Register 405

1.275 R402 Register (Offset = 0x192) [Reset = 0x00]

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Table 1-277. R402 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_31:24	R/W	0x0	See Register 405

1.276 R403 Register (Offset = 0x193) [Reset = 0x00]

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Table 1-278. R403 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_23:16	R/W	0x0	See Register 405

1.277 R404 Register (Offset = 0x194) [Reset = 0x00]

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Table 1-279. R404 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET_15:8	R/W	0x0	See Register 405

1.278 R405 Register (Offset = 0x195) [Reset = 0x00]

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Table 1-280. R405 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PH_OFFSET	R/W	0x0	Phase offset to control input to output phase in ZDM. ROM=Y, EEPROM=N

1.279 R406 Register (Offset = 0x196) [Reset = 0x00]

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Table 1-281. R406 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_39:32	R/W	0x0	See Register 410

1.280 R407 Register (Offset = 0x197) [Reset = 0x00]

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Table 1-282. R407 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_31:24	R/W	0x0	See Register 410

1.281 R408 Register (Offset = 0x198) [Reset = 0x00]

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Table 1-283. R408 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_23:16	R/W	0x0	See Register 410

1.282 R409 Register (Offset = 0x199) [Reset = 0x00]

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Table 1-284. R409 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN_15:8	R/W	0x0	See Register 410

1.283 R410 Register (Offset = 0x19A) [Reset = 0x00]

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Table 1-285. R410 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FREE_RUN	R/W	0x0	DPLL2 starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.284 R440 Register (Offset = 0x1B8) [Reset = 0x03]

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Table 1-286. R440 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_LCK_TIMER_9:8	R/W	0x3	See Register 441

1.285 R441 Register (Offset = 0x1B9) [Reset = 0x09]

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Table 1-287. R441 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_LCK_TIMER	R/W	0x9	Minimum amount of time until DPLL2_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.286 R442 Register (Offset = 0x1BA) [Reset = 0x01]

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Table 1-288. R442 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_HIST_TIMER_9:8	R/W	0x1	See Register 443

1.287 R443 Register (Offset = 0x1BB) [Reset = 0x92]

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Table 1-289. R443 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_HIST_TIMER	R/W	0x92	Time interval between history update events. ROM=Y, EEPROM=N

1.288 R444 Register (Offset = 0x1BC) [Reset = 0x0D]

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Table 1-290. R444 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x3	Reserved
1:0	DPLL2_HOLD_TIMER_9:8	R/W	0x1	See Register 445

1.289 R445 Register (Offset = 0x1BD) [Reset = 0x42]

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Table 1-291. R445 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.290 R446 Register (Offset = 0x1BE) [Reset = 0x01]

Return to the Summary Table.

Table 1-292. R446 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL2_PHS1_TIMER_9:8	R/W	0x1	See Register 447

1.291 R447 Register (Offset = 0x1BF) [Reset = 0x40]

Return to the Summary Table.

Table 1-293. R447 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_PHS1_TIMER	R/W	0x40	Holdover exit phase slew control. Timer controlling update period. ROM=Y, EEPROM=N

1.292 R452 Register (Offset = 0x1C4) [Reset = 0x08]

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Table 1-294. R452 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL2_HIST_GAIN	R/W	0x8	History filter gain ROM=Y, EEPROM=N

1.293 R453 Register (Offset = 0x1C5) [Reset = 0x22]

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Table 1-295. R453 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PL_THRESH	R/W	0x22	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.294 R454 Register (Offset = 0x1C6) [Reset = 0x24]

Return to the Summary Table.

Table 1-296. R454 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PL_UNLK_THRESH	R/W	0x24	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.295 R455 Register (Offset = 0x1C7) [Reset = 0x07]

Return to the Summary Table.

Table 1-297. R455 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_PHS1_THRESH	R/W	0x7	Holdover exit phase slew control. Change per timer event. ROM=Y, EEPROM=N

1.296 R458 Register (Offset = 0x1CA) [Reset = 0x3F]

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Table 1-298. R458 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_HOLD_SLEW_STEP	R/W	0x3F	When DPLL exits holdover, rate of phase change relates to DPLLx_HOLD_SLEW_STEP over DPLLx_HOLD_TIMER. DPLLx_HOLD_SLEW_STEP is applied to DPLL numerator when exiting holdover or APLL numerator when using APLL relative DCO. ROM=Y, EEPROM=N

1.297 R460 Register (Offset = 0x1CC) [Reset = 0x00]

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Table 1-299. R460 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL2_STATUS_PL	R	0x0	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.298 R461 Register (Offset = 0x1CD) [Reset = 0x00]

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Table 1-300. R461 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL2_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.299 R464 Register (Offset = 0x1D0) [Reset = 0x00]

Return to the Summary Table.

Table 1-301. R464 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_DIV_32:32	R/W	0x0	See Register 468

1.300 R465 Register (Offset = 0x1D1) [Reset = 0x00]

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Table 1-302. R465 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_31:24	R/W	0x0	See Register 468

1.301 R466 Register (Offset = 0x1D2) [Reset = 0x00]

Return to the Summary Table.

Table 1-303. R466 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_23:16	R/W	0x0	See Register 468

1.302 R467 Register (Offset = 0x1D3) [Reset = 0x00]

Return to the Summary Table.

Table 1-304. R467 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV_15:8	R/W	0x0	See Register 468

1.303 R468 Register (Offset = 0x1D4) [Reset = 0xE8]

Return to the Summary Table.

Table 1-305. R468 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DIV	R/W	0xE8	DPLL Feedback Divider N Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.304 R469 Register (Offset = 0x1D5) [Reset = 0x08]

Return to the Summary Table.

Table 1-306. R469 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_39:32	R/W	0x8	See Register 473

1.305 R470 Register (Offset = 0x1D6) [Reset = 0x00]

Return to the Summary Table.

Table 1-307. R470 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_31:24	R/W	0x0	See Register 473

1.306 R471 Register (Offset = 0x1D7) [Reset = 0x00]

Return to the Summary Table.

Table 1-308. R471 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_23:16	R/W	0x0	See Register 473

1.307 R472 Register (Offset = 0x1D8) [Reset = 0x00]

Return to the Summary Table.

Table 1-309. R472 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_15:8	R/W	0x0	See Register 473

1.308 R473 Register (Offset = 0x1D9) [Reset = 0x00]

Return to the Summary Table.

Table 1-310. R473 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.309 R474 Register (Offset = 0x1DA) [Reset = 0x00]

Return to the Summary Table.

Table 1-311. R474 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_39:32	R/W	0x0	See Register 478

1.310 R475 Register (Offset = 0x1DB) [Reset = 0x00]

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Table 1-312. R475 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_31:24	R/W	0x0	See Register 478

1.311 R476 Register (Offset = 0x1DC) [Reset = 0x00]

Return to the Summary Table.

Table 1-313. R476 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_23:16	R/W	0x0	See Register 478

1.312 R477 Register (Offset = 0x1DD) [Reset = 0x00]

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Table 1-314. R477 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN_15:8	R/W	0x0	See Register 478

1.313 R478 Register (Offset = 0x1DE) [Reset = 0x00]

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Table 1-315. R478 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL2 feedback configuration 1 ROM=Y, EEPROM=N

1.314 R479 Register (Offset = 0x1DF) [Reset = 0x00]

Return to the Summary Table.

Table 1-316. R479 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB2_DIV_32:32	R/W	0x0	See Register 483

1.315 R480 Register (Offset = 0x1E0) [Reset = 0x00]

Return to the Summary Table.

Table 1-317. R480 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_31:24	R/W	0x0	See Register 483

1.316 R481 Register (Offset = 0x1E1) [Reset = 0x00]

Return to the Summary Table.

Table 1-318. R481 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_23:16	R/W	0x0	See Register 483

1.317 R482 Register (Offset = 0x1E2) [Reset = 0x12]

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Table 1-319. R482 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV_15:8	R/W	0x12	See Register 483

1.318 R483 Register (Offset = 0x1E3) [Reset = 0xC0]

Return to the Summary Table.

Table 1-320. R483 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DIV	R/W	0xC0	DPLL Feedback Divider N Value used with DPLL2 feedback configuration 2. ROM=Y, EEPROM=N

1.319 R484 Register (Offset = 0x1E4) [Reset = 0x00]

Return to the Summary Table.

Table 1-321. R484 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_39:32	R/W	0x0	See Register 488

1.320 R485 Register (Offset = 0x1E5) [Reset = 0x00]

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Table 1-322. R485 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_31:24	R/W	0x0	See Register 488

1.321 R486 Register (Offset = 0x1E6) [Reset = 0x00]

Return to the Summary Table.

Table 1-323. R486 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_23:16	R/W	0x0	See Register 488

1.322 R487 Register (Offset = 0x1E7) [Reset = 0x00]

Return to the Summary Table.

Table 1-324. R487 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM_15:8	R/W	0x0	See Register 488

1.323 R488 Register (Offset = 0x1E8) [Reset = 0x00]

Return to the Summary Table.

Table 1-325. R488 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.324 R489 Register (Offset = 0x1E9) [Reset = 0x00]

Return to the Summary Table.

Table 1-326. R489 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_39:32	R/W	0x0	See Register 493

1.325 R490 Register (Offset = 0x1EA) [Reset = 0x00]

Return to the Summary Table.

Table 1-327. R490 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_31:24	R/W	0x0	See Register 493

1.326 R491 Register (Offset = 0x1EB) [Reset = 0x00]

Return to the Summary Table.

Table 1-328. R491 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_23:16	R/W	0x0	See Register 493

1.327 R492 Register (Offset = 0x1EC) [Reset = 0x00]

Return to the Summary Table.

Table 1-329. R492 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN_15:8	R/W	0x0	See Register 493

1.328 R493 Register (Offset = 0x1ED) [Reset = 0x00]

Return to the Summary Table.

Table 1-330. R493 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB2_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL2 feedback configuration 2 ROM=Y, EEPROM=N

1.329 R494 Register (Offset = 0x1EE) [Reset = 0x00]

Return to the Summary Table.

Table 1-331. R494 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL2_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4	RESERVED	R/W	0x0	Reserved

Table 1-331. R494 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DPLL2_REF3_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
2	DPLL2_REF2_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF2. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
1	DPLL2_REF1_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
0	DPLL2_REF0_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.330 R495 Register (Offset = 0x1EF) [Reset = 0x02]

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Table 1-332. R495 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R/W	0x0	Reserved
2:0	DPLL2_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N 0x0 = Integer 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.331 R496 Register (Offset = 0x1F0) [Reset = 0x00]

Return to the Summary Table.

Table 1-333. R496 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL2_FB_FDEV_37:32	R/W	0x0	See Register 500

1.332 R497 Register (Offset = 0x1F1) [Reset = 0x9D]

Return to the Summary Table.

Table 1-334. R497 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_31:24	R/W	0x9D	See Register 500

1.333 R498 Register (Offset = 0x1F2) [Reset = 0xA3]

Return to the Summary Table.

Table 1-335. R498 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_23:16	R/W	0xA3	See Register 500

1.334 R499 Register (Offset = 0x1F3) [Reset = 0x83]

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Table 1-336. R499 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV_15:8	R/W	0x83	See Register 500

1.335 R500 Register (Offset = 0x1F4) [Reset = 0x41]

Return to the Summary Table.

Table 1-337. R500 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_FDEV	R/W	0x41	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.336 R501 Register (Offset = 0x1F5) [Reset = 0x01]

Return to the Summary Table.

Table 1-338. R501 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_FDEV_UPDATE	R/W	0x1	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.337 R502 Register (Offset = 0x1F6) [Reset = 0x00]

Return to the Summary Table.

Table 1-339. R502 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL2_FB_FDEV_EN	R/W	0x0	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.338 R503 Register (Offset = 0x1F7) [Reset = 0x00]

Return to the Summary Table.

Table 1-340. R503 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_39:32	R	0x0	See Register 507

1.339 R504 Register (Offset = 0x1F8) [Reset = 0x00]

Return to the Summary Table.

Table 1-341. R504 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_31:24	R	0x0	See Register 507

1.340 R505 Register (Offset = 0x1F9) [Reset = 0x00]

Return to the Summary Table.

Table 1-342. R505 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_23:16	R	0x0	See Register 507

1.341 R506 Register (Offset = 0x1FA) [Reset = 0x00]

Return to the Summary Table.

Table 1-343. R506 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT_15:8	R	0x0	See Register 507

1.342 R507 Register (Offset = 0x1FB) [Reset = 0x00]

Return to the Summary Table.

Table 1-344. R507 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_FB_NUM_STAT	R	0x0	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.343 R508 Register (Offset = 0x1FC) [Reset = 0x00]

Return to the Summary Table.

Table 1-345. R508 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL2_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL2_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1	DPLL2_REF2_DBLR_EN	R/W	0x0	DPLL Reference 2 Doubler Enable ROM=Y, EEPROM=N
0	DPLL2_REF3_DBLR_EN	R/W	0x0	DPLL Reference 3 Doubler Enable ROM=Y, EEPROM=N

1.344 R509 Register (Offset = 0x1FD) [Reset = 0x00]

Return to the Summary Table.

Table 1-346. R509 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF0_RDIV_15:8	R/W	0x0	See Register 510

1.345 R510 Register (Offset = 0x1FE) [Reset = 0x01]

Return to the Summary Table.

Table 1-347. R510 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF0_RDIV	R/W	0x1	DPLL Reference 0 R divider value ROM=Y, EEPROM=N

1.346 R511 Register (Offset = 0x1FF) [Reset = 0x00]

Return to the Summary Table.

Table 1-348. R511 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF1_RDIV_15:8	R/W	0x0	See Register 512

1.347 R512 Register (Offset = 0x200) [Reset = 0x01]

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Table 1-349. R512 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF1_RDIV	R/W	0x1	DPLL Reference 1 R divider value ROM=Y, EEPROM=N

1.348 R513 Register (Offset = 0x201) [Reset = 0x00]

Return to the Summary Table.

Table 1-350. R513 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF2_RDIV_15:8	R/W	0x0	See Register 514

1.349 R514 Register (Offset = 0x202) [Reset = 0x00]

Return to the Summary Table.

Table 1-351. R514 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF2_RDIV	R/W	0x0	DPLL Reference 2 R divider value ROM=Y, EEPROM=N

1.350 R515 Register (Offset = 0x203) [Reset = 0x00]

Return to the Summary Table.

Table 1-352. R515 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF3_RDIV_15:8	R/W	0x0	See Register 516

1.351 R516 Register (Offset = 0x204) [Reset = 0x00]

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Table 1-353. R516 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF3_RDIV	R/W	0x0	DPLL Reference 3 R divider value ROM=Y, EEPROM=N

1.352 R517 Register (Offset = 0x205) [Reset = 0x00]

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Table 1-354. R517 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF4_RDIV_15:8	R/W	0x0	See Register 518

1.353 R518 Register (Offset = 0x206) [Reset = 0x00]

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Table 1-355. R518 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF4_RDIV	R/W	0x0	DPLL REF4 R-divider value ROM=Y, EEPROM=N

1.354 R519 Register (Offset = 0x207) [Reset = 0x00]

Return to the Summary Table.

Table 1-356. R519 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF5_RDIV_15:8	R/W	0x0	See Register 520

1.355 R520 Register (Offset = 0x208) [Reset = 0x00]

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Table 1-357. R520 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL2_REF5_RDIV	R/W	0x0	DPLL Reference 3 R divider value ROM=Y, EEPROM=N

1.356 R523 Register (Offset = 0x20B) [Reset = 0x11]

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Table 1-358. R523 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-358. R523 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	DPLL3_REF0_AUTO_PRTY	R/W	0x2	REF0 Priority for Automatic Switchover. Sets the priority for REF0 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL3_REF1_AUTO_PRTY	R/W	0x1	REF1 Priority for Automatic Switchover. Sets the priority for REF1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.357 R524 Register (Offset = 0x20C) [Reset = 0x00]

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Table 1-359. R524 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL3_REF2_AUTO_PRTY	R/W	0x0	REF2 Priority for Automatic Switchover. Sets the priority for REF2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL3_REF3_AUTO_PRTY	R/W	0x0	REF3 Priority for Automatic Switchover. Sets the priority for REF3 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.358 R525 Register (Offset = 0x20D) [Reset = 0x00]

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Table 1-360. R525 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:3	DPLL3_REF4_AUTO_PRTY	R/W	0x0	REF4 Priority for Automatic Switchover. Sets the priority for REF4 feedback from APLL1 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th
2:0	DPLL3_REF5_AUTO_PRTY	R/W	0x0	REF5 Priority for Automatic Switchover. Sets the priority for REF5 feedback from APLL2 used in Automatic Non-Revertive, Automatic Revertive, and Manual Selection with Automatic Fallback switchover modes. ROM=Y, EEPROM=N 0x0 = Not available for selection 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th 0x5 = 5th 0x6 = 6th 0x7 = 7th

1.359 R526 Register (Offset = 0x20E) [Reset = 0x01]

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Table 1-361. R526 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5:3	DPLL3_MAN_REFSEL	R/W	0x0	DPLL3 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = REF0 0x1 = REF1 0x2 = REF2 0x3 = REF3 0x4 = PLL1 0x5 = PLL2
2	DPLL3_MAN_SWITCH_PIN_MODE	R/W	0x0	DPLL3 Manual Reference Selection Mode. Determines how the manually selected reference is chosen. If this is set to a '1', the manually selected reference is taken from a GPIO input pin. If it is set to a '0', the manually selected reference is taken from a register. ROM=Y, EEPROM=N 0x0 = Register 0x1 = Pin
1:0	DPLL3_SWITCH_MODE	R/W	0x1	DPLL3 Reference Switchover Mode. Selects between Automatic Non-revertive, Automatic Revertive, Manual Selection with Automatic Fallback, and Manual Selection with Automatic Holdover. ROM=Y, EEPROM=N 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual fallback 0x3 = Manual Holdover

1.360 R527 Register (Offset = 0x20F) [Reset = 0x01]

Return to the Summary Table.

Table 1-362. R527 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_REFSEL_STAT	R	0x1	Reads the DPLL3 selected reference ROM=N, EEPROM=N 0x0 = Holdover 0x1 = REF0 0x2 = REF1 0x4 = REF2 0x8 = REF3 0x10 = APLL1 0x20 = APLL2

1.361 R528 Register (Offset = 0x210) [Reset = 0x80]

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Table 1-363. R528 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_LOCKDET_PPM_EN	R/W	0x1	DPLL frequency lock detect enable ROM=Y, EEPROM=N
6:0	DPLL3_LOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 529

1.362 R529 Register (Offset = 0x211) [Reset = 0x0A]

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Table 1-364. R529 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_MAX	R/W	0xA	DPLL frequency lock detect in-lock threshold ROM=Y, EEPROM=N

1.363 R530 Register (Offset = 0x212) [Reset = 0x00]

Return to the Summary Table.

Table 1-365. R530 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL3_UNLOCKDET_PPM_MAX_14:8	R/W	0x0	See Register 531

1.364 R531 Register (Offset = 0x213) [Reset = 0x64]

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Table 1-366. R531 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_UNLOCKDET_PPM_MAX	R/W	0x64	DPLL frequency lock detect out-of-lock threshold ROM=Y, EEPROM=N

1.365 R532 Register (Offset = 0x214) [Reset = 0x00]

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Table 1-367. R532 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_LOCKDET2_PPM_CNTSTRT_29:24	R/W	0x0	See Register 535

1.366 R533 Register (Offset = 0x215) [Reset = 0x03]

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Table 1-368. R533 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET2_PPM_CNTSTRT_23:16	R/W	0x3	See Register 535

1.367 R534 Register (Offset = 0x216) [Reset = 0x0D]

Return to the Summary Table.

Table 1-369. R534 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET2_PPM_CNTSTRT_15:8	R/W	0xD	See Register 535

1.368 R535 Register (Offset = 0x217) [Reset = 0x40]

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Table 1-370. R535 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET2_PPM_CNTSTRT	R/W	0x40	DPLL frequency lock detect reference count value used with DPLL1 feedback configuration 2 ROM=Y, EEPROM=N

1.369 R536 Register (Offset = 0x218) [Reset = 0x00]

Return to the Summary Table.

Table 1-371. R536 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_LOCKDET_PPM_CNTSTRT_29:24	R/W	0x0	See Register 539

1.370 R537 Register (Offset = 0x219) [Reset = 0x24]

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Table 1-372. R537 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_CNTSTRT_23:16	R/W	0x24	See Register 539

1.371 R538 Register (Offset = 0x21A) [Reset = 0x9F]

Return to the Summary Table.

Table 1-373. R538 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_CNTSTRT_15:8	R/W	0x9F	See Register 539

1.372 R539 Register (Offset = 0x21B) [Reset = 0x00]

Return to the Summary Table.

Table 1-374. R539 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_PPM_CNTSTRT	R/W	0x0	DPLL frequency lock detect reference count value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.373 R540 Register (Offset = 0x21C) [Reset = 0x00]

Return to the Summary Table.

Table 1-375. R540 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_29:24	R/W	0x0	See Register 543

1.374 R541 Register (Offset = 0x21D) [Reset = 0x98]

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Table 1-376. R541 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_23:16	R/W	0x98	See Register 543

1.375 R542 Register (Offset = 0x21E) [Reset = 0x96]

Return to the Summary Table.

Table 1-377. R542 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT_15:8	R/W	0x96	See Register 543

1.376 R543 Register (Offset = 0x21F) [Reset = 0x80]

Return to the Summary Table.

Table 1-378. R543 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LOCKDET_VCO_PPM_CNTSTRT	R/W	0x80	DPLL frequency lock detect VCO count value ROM=Y, EEPROM=N

1.377 R544 Register (Offset = 0x220) [Reset = 0x00]

Return to the Summary Table.

Table 1-379. R544 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R	0x0	Reserved
0	DPLL3_STATUS_PPM_LOCK	R	0x0	Readback lock indicator from DPLL PPM Checker ROM=N, EEPROM=N

1.378 R547 Register (Offset = 0x223) [Reset = 0xD5]

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Table 1-380. R547 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_LOOP_EN	R/W	0x1	Enable DPLL3 loop filter and R-Div mash engine ROM=Y, EEPROM=N
6	DPLL3_PHASE_CANCEL_EN	R/W	0x1	Enable Phase Cancellation ROM=Y, EEPROM=N
5	DPLL3_FASTLOCK_ALWAYS	R/W	0x0	Always perform fastlock ROM=Y, EEPROM=N
4	DPLL3_PHS1_EN	R/W	0x1	Enable holdover exit phase slew control . ROM=Y, EEPROM=N
3	DPLL3_ZDM_EN	R/W	0x0	Enable Zero Delay mode ROM=Y, EEPROM=N
2	DPLL3_HIST_EN	R/W	0x1	Enable History word to be used during holdover ROM=Y, EEPROM=N
1	DPLL3_PHASE_CANCEL_ALWAYS	R/W	0x0	Force phase cancellation to always occur when DPLL is acquiring lock. ROM=Y, EEPROM=N
0	RESERVED	R/W	0x1	Reserved

1.379 R548 Register (Offset = 0x224) [Reset = 0x56]

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Table 1-381. R548 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_HOLD_SLEW_LIM_EN	R/W	0x0	During holdover enable slew limiter ROM=Y, EEPROM=N
6:0	RESERVED	R/W	0x56	Reserved

1.380 R550 Register (Offset = 0x226) [Reset = 0x00]

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Table 1-382. R550 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL3_PH_OFFSET_44:40	R/W	0x0	See Register 555

1.381 R551 Register (Offset = 0x227) [Reset = 0x00]

Return to the Summary Table.

Table 1-383. R551 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_39:32	R/W	0x0	See Register 555

1.382 R552 Register (Offset = 0x228) [Reset = 0x00]

Return to the Summary Table.

Table 1-384. R552 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_31:24	R/W	0x0	See Register 555

1.383 R553 Register (Offset = 0x229) [Reset = 0x00]

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Table 1-385. R553 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_23:16	R/W	0x0	See Register 555

1.384 R554 Register (Offset = 0x22A) [Reset = 0x00]

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Table 1-386. R554 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET_15:8	R/W	0x0	See Register 555

1.385 R555 Register (Offset = 0x22B) [Reset = 0x00]

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Table 1-387. R555 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PH_OFFSET	R/W	0x0	Phase offset to control input to output phase in ZDM. ROM=Y, EEPROM=N

1.386 R556 Register (Offset = 0x22C) [Reset = 0x00]

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Table 1-388. R556 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_39:32	R/W	0x0	See Register 560

1.387 R557 Register (Offset = 0x22D) [Reset = 0x00]

Return to the Summary Table.

Table 1-389. R557 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_31:24	R/W	0x0	See Register 560

1.388 R558 Register (Offset = 0x22E) [Reset = 0x00]

Return to the Summary Table.

Table 1-390. R558 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_23:16	R/W	0x0	See Register 560

1.389 R559 Register (Offset = 0x22F) [Reset = 0x00]

Return to the Summary Table.

Table 1-391. R559 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN_15:8	R/W	0x0	See Register 560

1.390 R560 Register (Offset = 0x230) [Reset = 0x00]

Return to the Summary Table.

Table 1-392. R560 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FREE_RUN	R/W	0x0	DPLL starting word. Also non-history holdover word. ROM=Y, EEPROM=N

1.391 R561 Register (Offset = 0x231) [Reset = 0x03]

Return to the Summary Table.

Table 1-393. R561 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL3_PPM_REF_SEL	R/W	0x0	PPM Detector Reference Selection. When set to 0, the selected input reference is used. When set to 1, the XO is used. ROM=Y, EEPROM=N 0x0 = DPLL3 DLD 0x1 = APLL3 DLD
6:0	RESERVED	R/W	0x3	Reserved

1.392 R590 Register (Offset = 0x24E) [Reset = 0x03]

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Table 1-394. R590 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL3_LCK_TIMER_9:8	R/W	0x3	See Register 591

1.393 R591 Register (Offset = 0x24F) [Reset = 0x09]

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Table 1-395. R591 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_LCK_TIMER	R/W	0x9	Minimum amount of time until DPLL3_LOPL will be deasserted after starting to lock. Timer begins once device is within valid phase lock window. ROM=Y, EEPROM=N

1.394 R592 Register (Offset = 0x250) [Reset = 0x01]

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Table 1-396. R592 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL3_HIST_TIMER_9:8	R/W	0x1	See Register 593

1.395 R593 Register (Offset = 0x251) [Reset = 0x92]

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Table 1-397. R593 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_HIST_TIMER	R/W	0x92	History timer ROM=Y, EEPROM=N

1.396 R594 Register (Offset = 0x252) [Reset = 0x0D]

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Table 1-398. R594 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x3	Reserved
1:0	DPLL3_HOLD_TIMER_9:8	R/W	0x1	See Register 595

1.397 R595 Register (Offset = 0x253) [Reset = 0x42]

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Table 1-399. R595 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_HOLD_TIMER	R/W	0x42	Rate of change to DPLL or APLL numerator during phase slew control. See DPLLx_HOLD_SLEW_STEP. ROM=Y, EEPROM=N

1.398 R596 Register (Offset = 0x254) [Reset = 0x01]

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Table 1-400. R596 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved

Table 1-400. R596 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	DPLL3_PHS1_TIMER_9:8	R/W	0x1	See Register 597

1.399 R597 Register (Offset = 0x255) [Reset = 0x40]

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Table 1-401. R597 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_PHS1_TIMER	R/W	0x40	Holdover exit phase slew control. Timer controlling update period. ROM=Y, EEPROM=N

1.400 R602 Register (Offset = 0x25A) [Reset = 0x08]

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Table 1-402. R602 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL3_HIST_GAIN	R/W	0x8	History filter gain ROM=Y, EEPROM=N

1.401 R603 Register (Offset = 0x25B) [Reset = 0x22]

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Table 1-403. R603 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_PL_THRESH	R/W	0x22	Phase lock in-lock threshold ROM=Y, EEPROM=N

1.402 R604 Register (Offset = 0x25C) [Reset = 0x24]

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Table 1-404. R604 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_PL_UNLK_THRESH	R/W	0x24	Phase lock out-of-lock threshold ROM=Y, EEPROM=N

1.403 R605 Register (Offset = 0x25D) [Reset = 0x07]

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Table 1-405. R605 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_PHS1_THRESH	R/W	0x7	Holdover exit phase slew control. Change per timer event. ROM=Y, EEPROM=N

1.404 R610 Register (Offset = 0x262) [Reset = 0x00]

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Table 1-406. R610 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	DPLL3_STATUS_PL	R	0x0	Readback the phase lock status ROM=N, EEPROM=N
4:0	RESERVED	R	0x0	Reserved

1.405 R611 Register (Offset = 0x263) [Reset = 0x00]

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Table 1-407. R611 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	DPLL3_DCO_SLEW_ACTIVE	R	0x0	Readback DCO slew status ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.406 R614 Register (Offset = 0x266) [Reset = 0x00]

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Table 1-408. R614 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB_DIV_32:32	R/W	0x0	See Register 618

1.407 R615 Register (Offset = 0x267) [Reset = 0x00]

Return to the Summary Table.

Table 1-409. R615 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV_31:24	R/W	0x0	See Register 618

1.408 R616 Register (Offset = 0x268) [Reset = 0x00]

Return to the Summary Table.

Table 1-410. R616 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV_23:16	R/W	0x0	See Register 618

1.409 R617 Register (Offset = 0x269) [Reset = 0x00]

Return to the Summary Table.

Table 1-411. R617 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV_15:8	R/W	0x0	See Register 618

1.410 R618 Register (Offset = 0x26A) [Reset = 0x64]

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Table 1-412. R618 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DIV	R/W	0x64	DPLL Feedback Divider N Value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.411 R619 Register (Offset = 0x26B) [Reset = 0x00]

Return to the Summary Table.

Table 1-413. R619 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_39:32	R/W	0x0	See Register 623

1.412 R620 Register (Offset = 0x26C) [Reset = 0x00]

Return to the Summary Table.

Table 1-414. R620 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_31:24	R/W	0x0	See Register 623

1.413 R621 Register (Offset = 0x26D) [Reset = 0x00]

Return to the Summary Table.

Table 1-415. R621 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_23:16	R/W	0x0	See Register 623

1.414 R622 Register (Offset = 0x26E) [Reset = 0x00]

Return to the Summary Table.

Table 1-416. R622 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_15:8	R/W	0x0	See Register 623

1.415 R623 Register (Offset = 0x26F) [Reset = 0x00]

Return to the Summary Table.

Table 1-417. R623 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM	R/W	0x0	DPLL Feedback Divider Numerator Value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.416 R624 Register (Offset = 0x270) [Reset = 0x00]

Return to the Summary Table.

Table 1-418. R624 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_39:32	R/W	0x0	See Register 628

1.417 R625 Register (Offset = 0x271) [Reset = 0x00]

Return to the Summary Table.

Table 1-419. R625 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_31:24	R/W	0x0	See Register 628

1.418 R626 Register (Offset = 0x272) [Reset = 0x00]

Return to the Summary Table.

Table 1-420. R626 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_23:16	R/W	0x0	See Register 628

1.419 R627 Register (Offset = 0x273) [Reset = 0x00]

Return to the Summary Table.

Table 1-421. R627 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN_15:8	R/W	0x0	See Register 628

1.420 R628 Register (Offset = 0x274) [Reset = 0x00]

Return to the Summary Table.

Table 1-422. R628 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_DEN	R/W	0x0	DPLL Feedback Divider Denominator Value used with DPLL3 feedback configuration 1 ROM=Y, EEPROM=N

1.421 R629 Register (Offset = 0x275) [Reset = 0x00]

Return to the Summary Table.

Table 1-423. R629 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved

Table 1-423. R629 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DPLL3_FB2_DIV_32:32	R/W	0x0	See Register 633

1.422 R630 Register (Offset = 0x276) [Reset = 0x00]

Return to the Summary Table.

Table 1-424. R630 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV_31:24	R/W	0x0	See Register 633

1.423 R631 Register (Offset = 0x277) [Reset = 0x00]

Return to the Summary Table.

Table 1-425. R631 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV_23:16	R/W	0x0	See Register 633

1.424 R632 Register (Offset = 0x278) [Reset = 0x07]

Return to the Summary Table.

Table 1-426. R632 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV_15:8	R/W	0x7	See Register 633

1.425 R633 Register (Offset = 0x279) [Reset = 0xAE]

Return to the Summary Table.

Table 1-427. R633 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DIV	R/W	0xAE	DPLL Feedback Divider N Value used with DPLL3 feedback configuration 2 ROM=Y, EEPROM=N

1.426 R634 Register (Offset = 0x27A) [Reset = 0x14]

Return to the Summary Table.

Table 1-428. R634 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_39:32	R/W	0x14	See Register 638

1.427 R635 Register (Offset = 0x27B) [Reset = 0x7A]

Return to the Summary Table.

Table 1-429. R635 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_31:24	R/W	0x7A	See Register 638

1.428 R636 Register (Offset = 0x27C) [Reset = 0xE1]

Return to the Summary Table.

Table 1-430. R636 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_23:16	R/W	0xE1	See Register 638

1.429 R637 Register (Offset = 0x27D) [Reset = 0x47]

Return to the Summary Table.

Table 1-431. R637 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM_15:8	R/W	0x47	See Register 638

1.430 R638 Register (Offset = 0x27E) [Reset = 0xAE]

Return to the Summary Table.

Table 1-432. R638 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_NUM	R/W	0xAE	DPLL Feedback Divider Numerator Value used with DPLL3 feedback configuration 2 ROM=Y, EEPROM=N

1.431 R639 Register (Offset = 0x27F) [Reset = 0xFF]

Return to the Summary Table.

Table 1-433. R639 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_39:32	R/W	0xFF	See Register 643

1.432 R640 Register (Offset = 0x280) [Reset = 0xFF]

Return to the Summary Table.

Table 1-434. R640 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_31:24	R/W	0xFF	See Register 643

1.433 R641 Register (Offset = 0x281) [Reset = 0xFF]

Return to the Summary Table.

Table 1-435. R641 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_23:16	R/W	0xFF	See Register 643

1.434 R642 Register (Offset = 0x282) [Reset = 0xFF]

Return to the Summary Table.

Table 1-436. R642 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN_15:8	R/W	0xFF	See Register 643

1.435 R643 Register (Offset = 0x283) [Reset = 0xFF]

Return to the Summary Table.

Table 1-437. R643 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB2_DEN	R/W	0xFF	DPLL Feedback Divider Denominator Value used with DPLL3 feedback configuration 2 ROM=Y, EEPROM=N

1.436 R644 Register (Offset = 0x284) [Reset = 0x00]

Return to the Summary Table.

Table 1-438. R644 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	DPLL3_REF5_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF5. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
4	DPLL3_REF4_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF4. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
3	DPLL3_REF3_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF3. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
2	DPLL3_REF2_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF2. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
1	DPLL3_REF1_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF1. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2
0	DPLL3_REF0_FB_SEL	R/W	0x0	DPLL Feedback N, NUM, DEN select for REF0. When this bit is a 0, Value 1 is chosen for each of the three parameters. When it is set to a 1, Value 2 is used. ROM=Y, EEPROM=N 0x0 = FB Config 1 0x1 = FB Config 2

1.437 R645 Register (Offset = 0x285) [Reset = 0x02]

Return to the Summary Table.

Table 1-439. R645 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:3	RESERVED	R/W	0x0	Reserved
2:0	DPLL3_FB_MASH_ORDER	R/W	0x2	DPLL Feedback Divider MASH Order. ROM=Y, EEPROM=N 0x0 = Integer 0x1 = 1st order 0x2 = 2nd order 0x3 = 3rd order 0x4 = 4th order

1.438 R646 Register (Offset = 0x286) [Reset = 0x00]

Return to the Summary Table.

Table 1-440. R646 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL3_FB_FDEV_37:32	R/W	0x0	See Register 650

1.439 R647 Register (Offset = 0x287) [Reset = 0x00]

Return to the Summary Table.

Table 1-441. R647 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV_31:24	R/W	0x0	See Register 650

1.440 R648 Register (Offset = 0x288) [Reset = 0x00]

Return to the Summary Table.

Table 1-442. R648 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV_23:16	R/W	0x0	See Register 650

1.441 R649 Register (Offset = 0x289) [Reset = 0x00]

Return to the Summary Table.

Table 1-443. R649 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV_15:8	R/W	0x0	See Register 650

1.442 R650 Register (Offset = 0x28A) [Reset = 0x00]

Return to the Summary Table.

Table 1-444. R650 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_FDEV	R/W	0x0	DPLL Feedback Divider DCO Frequency Deviation Value ROM=Y, EEPROM=N

1.443 R651 Register (Offset = 0x28B) [Reset = 0x00]

Return to the Summary Table.

Table 1-445. R651 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB_FDEV_UPDATE	R/W	0x0	Increment/Decrement DPLL Feedback Numerator value with DPLL_FB_FDEV value ROM=Y, EEPROM=N

1.444 R652 Register (Offset = 0x28C) [Reset = 0x00]

Return to the Summary Table.

Table 1-446. R652 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL3_FB_FDEV_EN	R/W	0x0	Enable DPLL DCO mode ROM=Y, EEPROM=N

1.445 R653 Register (Offset = 0x28D) [Reset = 0x00]

Return to the Summary Table.

Table 1-447. R653 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_39:32	R	0x0	See Register 657

1.446 R654 Register (Offset = 0x28E) [Reset = 0x00]

Return to the Summary Table.

Table 1-448. R654 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_31:24	R	0x0	See Register 657

1.447 R655 Register (Offset = 0x28F) [Reset = 0x00]

Return to the Summary Table.

Table 1-449. R655 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_23:16	R	0x0	See Register 657

1.448 R656 Register (Offset = 0x290) [Reset = 0x00]

Return to the Summary Table.

Table 1-450. R656 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT_15:8	R	0x0	See Register 657

1.449 R657 Register (Offset = 0x291) [Reset = 0x00]

Return to the Summary Table.

Table 1-451. R657 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_FB_NUM_STAT	R	0x0	Readback DPLL Feedback Divider Numerator value as a result of DCO mode ROM=N, EEPROM=N

1.450 R658 Register (Offset = 0x292) [Reset = 0x00]

Return to the Summary Table.

Table 1-452. R658 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL3_REF0_DBLR_EN	R/W	0x0	DPLL Reference 0 Doubler Enable ROM=Y, EEPROM=N
2	DPLL3_REF1_DBLR_EN	R/W	0x0	DPLL Reference 1 Doubler Enable ROM=Y, EEPROM=N
1	DPLL3_REF2_DBLR_EN	R/W	0x0	DPLL Reference 2 Doubler Enable ROM=Y, EEPROM=N
0	DPLL3_REF3_DBLR_EN	R/W	0x0	DPLL Reference 3 Doubler Enable ROM=Y, EEPROM=N

1.451 R659 Register (Offset = 0x293) [Reset = 0x00]

Return to the Summary Table.

Table 1-453. R659 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF0_RDIV_15:8	R/W	0x0	See Register 660

1.452 R660 Register (Offset = 0x294) [Reset = 0x01]

Return to the Summary Table.

Table 1-454. R660 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF0_RDIV	R/W	0x1	DPLL Reference 0 R divider value ROM=Y, EEPROM=N

1.453 R661 Register (Offset = 0x295) [Reset = 0x00]

Return to the Summary Table.

Table 1-455. R661 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF1_RDIV_15:8	R/W	0x0	See Register 662

1.454 R662 Register (Offset = 0x296) [Reset = 0x01]

Return to the Summary Table.

Table 1-456. R662 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF1_RDIV	R/W	0x1	DPLL Reference 1 R divider value ROM=Y, EEPROM=N

1.455 R663 Register (Offset = 0x297) [Reset = 0x00]

Return to the Summary Table.

Table 1-457. R663 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF2_RDIV_15:8	R/W	0x0	See Register 664

1.456 R664 Register (Offset = 0x298) [Reset = 0x00]

Return to the Summary Table.

Table 1-458. R664 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF2_RDIV	R/W	0x0	DPLL Reference 2 R divider value ROM=Y, EEPROM=N

1.457 R665 Register (Offset = 0x299) [Reset = 0x00]

Return to the Summary Table.

Table 1-459. R665 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF3_RDIV_15:8	R/W	0x0	See Register 666

1.458 R666 Register (Offset = 0x29A) [Reset = 0x00]

Return to the Summary Table.

Table 1-460. R666 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF3_RDIV	R/W	0x0	DPLL Reference 3 R divider value ROM=Y, EEPROM=N

1.459 R667 Register (Offset = 0x29B) [Reset = 0x00]

Return to the Summary Table.

Table 1-461. R667 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF4_RDIV_15:8	R/W	0x0	See Register 668

1.460 R668 Register (Offset = 0x29C) [Reset = 0x00]

Return to the Summary Table.

Table 1-462. R668 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF4_RDIV	R/W	0x0	DPLL Reference 4 R divider value ROM=Y, EEPROM=N

1.461 R669 Register (Offset = 0x29D) [Reset = 0x01]

Return to the Summary Table.

Table 1-463. R669 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF5_RDIV_15:8	R/W	0x1	See Register 670

1.462 R670 Register (Offset = 0x29E) [Reset = 0x01]

Return to the Summary Table.

Table 1-464. R670 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL3_REF5_RDIV	R/W	0x1	DPLL Reference 5 R divider value ROM=Y, EEPROM=N

1.463 R707 Register (Offset = 0x2C3) [Reset = 0x6D]

Return to the Summary Table.

Table 1-465. R707 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_CP_PU_R	R/W	0x6D	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ 0x2F = 1.65 kΩ 0x30 = 1.61 kΩ 0x31 = 1.58 kΩ 0x32 = 1.55 kΩ 0x33 = 1.52 kΩ 0x34 = 1.49 kΩ 0x35 = 1.46 kΩ 0x36 = 1.44 kΩ 0x37 = 1.41 kΩ 0x38 = 1.38 kΩ 0x39 = 1.36 kΩ 0x3A = 1.34 kΩ 0x3B = 1.31 kΩ 0x3C = 1.29 kΩ 0x3D = 1.27 kΩ 0x3E = 1.25 kΩ 0x3F = 1.23 kΩ 0x40 = 1.2 kΩ 0x41 = 1.18 kΩ

Table 1-465. R707 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = 1.16 kΩ 0x43 = 1.15 kΩ 0x44 = 1.13 kΩ 0x45 = 1.12 kΩ 0x46 = 1.1 kΩ 0x47 = 1.08 kΩ 0x48 = 1.07 kΩ 0x49 = 1.05 kΩ 0x4A = 1.04 kΩ 0x4B = 1.03 kΩ 0x4C = 1.01 kΩ 0x4D = 1 kΩ 0x4E = 0.989 kΩ 0x4F = 0.977 kΩ 0x50 = 0.964 kΩ 0x51 = 0.952 kΩ 0x52 = 0.941 kΩ 0x53 = 0.929 kΩ 0x54 = 0.92 kΩ 0x55 = 0.909 kΩ 0x56 = 0.898 kΩ 0x57 = 0.888 kΩ 0x58 = 0.878 kΩ 0x59 = 0.868 kΩ 0x5A = 0.858 kΩ 0x5B = 0.849 kΩ 0x5C = 0.841 kΩ 0x5D = 0.832 kΩ 0x5E = 0.823 kΩ 0x5F = 0.814 kΩ 0x60 = 0.8 kΩ 0x61 = 0.792 kΩ 0x62 = 0.784 kΩ 0x63 = 0.776 kΩ 0x64 = 0.769 kΩ 0x65 = 0.762 kΩ 0x66 = 0.754 kΩ 0x67 = 0.747 kΩ 0x68 = 0.74 kΩ 0x69 = 0.733 kΩ 0x6A = 0.726 kΩ 0x6B = 0.719 kΩ 0x6C = 0.713 kΩ 0x6D = 0.707 kΩ 0x6E = 0.7 kΩ 0x6F = 0.694 kΩ 0x70 = 0.688 kΩ 0x71 = 0.682 kΩ 0x72 = 0.676 kΩ 0x73 = 0.67 kΩ 0x74 = 0.665 kΩ 0x75 = 0.659 kΩ 0x76 = 0.654 kΩ 0x77 = 0.648 kΩ 0x78 = 0.643 kΩ 0x79 = 0.637 kΩ 0x7A = 0.632 kΩ 0x7B = 0.627 kΩ 0x7C = 0.623 kΩ 0x7D = 0.618 kΩ 0x7E = 0.613 kΩ 0x7F = 0.608 kΩ 0x80 = 0.6 kΩ 0x81 = 0.595 kΩ 0x82 = 0.591 kΩ 0x83 = 0.586 kΩ 0x84 = 0.583 kΩ 0x85 = 0.578 kΩ

Table 1-465. R707 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x86 = 0.574 kΩ 0x87 = 0.57 kΩ 0x88 = 0.565 kΩ 0x89 = 0.561 kΩ 0x8A = 0.557 kΩ 0x8B = 0.553 kΩ 0x8C = 0.55 kΩ 0x8D = 0.546 kΩ 0x8E = 0.542 kΩ 0x8F = 0.538 kΩ 0x90 = 0.535 kΩ 0x91 = 0.531 kΩ 0x92 = 0.527 kΩ 0x93 = 0.524 kΩ 0x94 = 0.521 kΩ 0x95 = 0.517 kΩ 0x96 = 0.514 kΩ 0x97 = 0.51 kΩ 0x98 = 0.507 kΩ 0x99 = 0.504 kΩ 0x9A = 0.5 kΩ 0x9B = 0.497 kΩ 0x9C = 0.494 kΩ 0x9D = 0.491 kΩ 0x9E = 0.488 kΩ 0x9F = 0.485 kΩ 0xA0 = 0.48 kΩ 0xA1 = 0.477 kΩ 0xA2 = 0.474 kΩ 0xA3 = 0.471 kΩ 0xA4 = 0.469 kΩ 0xA5 = 0.466 kΩ 0xA6 = 0.463 kΩ 0xA7 = 0.46 kΩ 0xA8 = 0.458 kΩ 0xA9 = 0.455 kΩ 0xAA = 0.452 kΩ 0xAB = 0.45 kΩ 0xAC = 0.447 kΩ 0xAD = 0.445 kΩ 0xAE = 0.442 kΩ 0xAF = 0.44 kΩ 0xB0 = 0.437 kΩ 0xB1 = 0.435 kΩ 0xB2 = 0.432 kΩ 0xB3 = 0.43 kΩ 0xB4 = 0.428 kΩ 0xB5 = 0.425 kΩ 0xB6 = 0.423 kΩ 0xB7 = 0.421 kΩ 0xB8 = 0.419 kΩ 0xB9 = 0.416 kΩ 0xBA = 0.414 kΩ 0xBB = 0.412 kΩ 0xBC = 0.41 kΩ 0xBD = 0.408 kΩ 0xBE = 0.406 kΩ 0xBF = 0.404 kΩ 0xC0 = 0.4 kΩ 0xC1 = 0.398 kΩ 0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ

Table 1-465. R707 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ 0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.464 R708 Register (Offset = 0x2C4) [Reset = 0x03]

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Table 1-466. R708 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved

Table 1-466. R708 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL1_CPG	R/W	0x3	PLL charge pump gain Pump up/down. ROM=Y, EEPROM=Y 0x0 = 1.6 mA 0x1 = 3.2 mA 0x2 = 4.8 mA 0x3 = 6.4 mA

1.465 R709 Register (Offset = 0x2C5) [Reset = 0x09]

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Table 1-467. R709 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-467. R709 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R2	R/W	0x9	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.262 kΩ 0x2 = 0.357 kΩ 0x3 = 0.166 kΩ 0x4 = 0.642 kΩ 0x5 = 0.199 kΩ 0x6 = 0.244 kΩ 0x7 = 0.142 kΩ 0x8 = 1.14 kΩ 0x9 = 0.222 kΩ 0xA = 0.283 kΩ 0xB = 0.152 kΩ 0xC = 0.425 kΩ 0xD = 0.177 kΩ 0xE = 0.21 kΩ 0xF = 0.132 kΩ 0x10 = 0.847 kΩ 0x11 = 1.06 kΩ 0x12 = 1.16 kΩ 0x13 = 0.966 kΩ 0x14 = 1.44 kΩ 0x15 = 0.998 kΩ 0x16 = 1.04 kΩ 0x17 = 0.941 kΩ 0x18 = 1.94 kΩ 0x19 = 1.02 kΩ 0x1A = 1.08 kΩ 0x1B = 0.951 kΩ 0x1C = 1.22 kΩ 0x1D = 0.976 kΩ 0x1E = 1.01 kΩ 0x1F = 0.931 kΩ 0x20 = 1.66 kΩ 0x21 = 1.88 kΩ 0x22 = 1.97 kΩ 0x23 = 1.78 kΩ 0x24 = 2.26 kΩ 0x25 = 1.81 kΩ 0x26 = 1.86 kΩ 0x27 = 1.76 kΩ 0x28 = 2.75 kΩ 0x29 = 1.84 kΩ 0x2A = 1.9 kΩ 0x2B = 1.77 kΩ 0x2C = 2.04 kΩ 0x2D = 1.79 kΩ 0x2E = 1.82 kΩ 0x2F = 1.75 kΩ 0x30 = 2.46 kΩ 0x31 = 2.68 kΩ 0x32 = 2.77 kΩ 0x33 = 2.58 kΩ 0x34 = 3.06 kΩ 0x35 = 2.61 kΩ 0x36 = 2.66 kΩ 0x37 = 2.56 kΩ 0x38 = 3.55 kΩ 0x39 = 2.64 kΩ 0x3A = 2.7 kΩ 0x3B = 2.57 kΩ 0x3C = 2.84 kΩ 0x3D = 2.59 kΩ 0x3E = 2.62 kΩ 0x3F = 2.55 kΩ

1.466 R710 Register (Offset = 0x2C6) [Reset = 0x02]

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Table 1-468. R710 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-468. R710 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R3	R/W	0x2	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ 0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.467 R711 Register (Offset = 0x2C7) [Reset = 0x02]

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Table 1-469. R711 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-469. R711 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R4	R/W	0x2	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ 0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.468 R712 Register (Offset = 0x2C8) [Reset = 0xFF]

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Table 1-470. R712 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL1_DISABLE_3RD4TH	R/W	0x3	PLL Loop Filter Disconnects C3 and C4 ROM=Y, EEPROM=N 0x0 = C3/C4 Disconnected 0x1 = C3=Enabled, C4=Disconnected 0x2 = C3=Disconnected, C4=Enabled 0x3 = C3=Enabled, C4=Enabled
5:3	PLL1_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF
2:0	PLL1_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.469 R713 Register (Offset = 0x2C9) [Reset = 0x00]

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Table 1-471. R713 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_RDIV_8:8	R/W	0x0	See Register 714

1.470 R714 Register (Offset = 0x2CA) [Reset = 0x0A]

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Table 1-472. R714 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_RDIV	R/W	0xA	PLL R Divider ROM=Y, EEPROM=Y

1.471 R715 Register (Offset = 0x2CB) [Reset = 0x02]

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Table 1-473. R715 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL1_RDIV_XO_EN	R/W	0x0	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[1] = 1 ROM=Y, EEPROM=Y

Table 1-473. R715 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PLL1_RDIV_XO_DBLR_EN	R/W	0x0	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL1_RDIV_BYPASS_EN	R/W	0x0	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL1_RDIV_MUX_SEL	R/W	0x2	Select R Divider input. When enabling reference from feedback divider, the APLL PLLx_VCO_BUF_2REF_EN bit must also be set appropriately. ROM=Y, EEPROM=Y 0x0 = XO 0x1 = VCO2 feedback divider 0x2 = VCO3 feedback divider

1.472 R716 Register (Offset = 0x2CC) [Reset = 0x00]

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Table 1-474. R716 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_NDIV_8:8	R/W	0x0	See Register 717

1.473 R717 Register (Offset = 0x2CD) [Reset = 0x32]

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Table 1-475. R717 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NDIV	R/W	0x32	PLL N Divider ROM=Y, EEPROM=Y

1.474 R718 Register (Offset = 0x2CE) [Reset = 0x61]

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Table 1-476. R718 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_MSB	R/W	0x61	When PLL1_MODE is set for 24 bit fractional. PLL1_NUM_MSB is effective PLL1_NUM[23:16]. Other PLL1_NUM and PLL1_DEN bits in programmable mode are in PLL1_NUM field. When in 40-bit fixed denominator PLL mode, then PLL1_NUM_MSB is unused. ROM=Y, EEPROM=Y

1.475 R719 Register (Offset = 0x2CF) [Reset = 0x86]

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Table 1-477. R719 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_39:32	R/W	0x86	See Register 723

1.476 R720 Register (Offset = 0x2D0) [Reset = 0x4E]

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Table 1-478. R720 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_31:24	R/W	0x4E	See Register 723

1.477 R721 Register (Offset = 0x2D1) [Reset = 0x80]

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Table 1-479. R721 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_23:16	R/W	0x80	See Register 723

1.478 R722 Register (Offset = 0x2D2) [Reset = 0x07]

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Table 1-480. R722 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_15:8	R/W	0x7	See Register 723

1.479 R723 Register (Offset = 0x2D3) [Reset = 0xE1]

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Table 1-481. R723 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM	R/W	0xE1	When PLL1_MODE = 1 (40-bit fixed denominator) mode then PLL1_NUM contains the APLL1 numerator. When PLL1_MODE = 0 (24-bit programmable denominator) then PLL1_NUM[23:0] stores the programmable PLL1 denominator and PLL1_NUM[39:24] stores the 16 LSBs of the PLL1 numerator. Total PLL1 numerator is calculated with PLL1_NUM_MSB as the 8 MSBs. In 24-bit programmable denominator mode PLL1_NUM[23:0] = 0 is 2^{24}. ROM=Y, EEPROM=Y

1.480 R724 Register (Offset = 0x2D4) [Reset = 0x36]

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Table 1-482. R724 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5:4	PLL1_DTHRMODE	R/W	0x3	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL1_ORDER	R/W	0x3	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd

Table 1-482. R724 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL1_MODE	R/W	0x0	In APLL 24-bit num/den mode, APLL denominator is programmable. Recommended not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL1_NUM[23:0] The numerator is stored in (PLL1_NUM_MSB << 16) + PLL1_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.481 R725 Register (Offset = 0x2D5) [Reset = 0x00]

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Table 1-483. R725 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_39:32	R	0x0	See Register 729

1.482 R726 Register (Offset = 0x2D6) [Reset = 0x00]

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Table 1-484. R726 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_31:24	R	0x0	See Register 729

1.483 R727 Register (Offset = 0x2D7) [Reset = 0x00]

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Table 1-485. R727 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_23:16	R	0x0	See Register 729

1.484 R728 Register (Offset = 0x2D8) [Reset = 0x00]

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Table 1-486. R728 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT_15:8	R	0x0	See Register 729

1.485 R729 Register (Offset = 0x2D9) [Reset = 0x00]

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Table 1-487. R729 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL1_NUM_STAT	R	0x0	Readback current effective APLL1 Numerator after FDEV and/or DPLL correction ROM=N, EEPROM=N

1.486 R731 Register (Offset = 0x2DB) [Reset = 0xCA]

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Table 1-488. R731 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_PRI_DIV_SYNC_EN	R/W	0x1	PLL1 P1 Divider Sync Enable. Enables synchronization of PLL1 P1 post-divider. ROM=Y, EEPROM=N
6	PLL1_PRI_DIV_EN	R/W	0x1	Enables the VCO1 P1 divider ROM=Y, EEPROM=Y
5:3	PLL1_PRI_DIV	R/W	0x1	Sets the VCO post-divider VCO1 P1 from 2 to 7. ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7
2:0	PLL1_PRI_DIV_DRVR_EN	R/W	0x2	Enables VCO1 P1 divider output driver to channel output banks: [Bit 0] -> OUT0_1 [Bit 1] -> OUT2_3 [Bit 2] -> OUT14_15 ROM=Y, EEPROM=Y

1.487 R732 Register (Offset = 0x2DC) [Reset = 0xA0]

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Table 1-489. R732 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_SEC_DIV_SYNC_EN	R/W	0x1	PLL1 P2 Divider Sync Enable. Enables synchronization of PLL1 P2 post-divider. ROM=Y, EEPROM=N
6	PLL1_SEC_DIV_EN	R/W	0x0	Enables the VCO1 P2 divider ROM=Y, EEPROM=Y
5:3	PLL1_SEC_DIV	R/W	0x4	Sets the VCO post-divider VCO1 P2 from 2 to 7. ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7
2:0	PLL1_SEC_DIV_DRVR_EN	R/W	0x0	Enables the VCO1 P2 divider output driver to channel output banks: [Bit 0] -> OUT0_1 [Bit 1] -> Reserved [Bit 2] -> Reserved ROM=Y, EEPROM=Y

1.488 R733 Register (Offset = 0x2DD) [Reset = 0x08]

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Table 1-490. R733 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_VCO_BUF_EN	R/W	0x0	Enables the VCO1 Buffer which drives the DPLL feedback, reference window detector, DPLL reference for cascade mode, and test mode ROM=Y, EEPROM=N
6:5	PLL1_VCO_BUF_2REF_EN	R/W	0x0	Enables the APLL1 Div-by-4 cascade divider to APLL2/3 reference input for cascade mode. [0] - > APLL2, [1] -> APLL3 ROM=Y, EEPROM=Y

Table 1-490. R733 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLL1_VCO_BUF_2DPLL_EN	R/W	0x0	Enables the VCO1 Buffer output driver to DPLL feedback divider ROM=Y, EEPROM=N
3	RESERVED	R/W	0x1	Reserved
2	PLL1_VCO_BUF_PPM_CHECK_EN	R/W	0x0	Enables the APLL1 Div-by-4/8 cascade divider to DPLL/PPM frequency detector ROM=Y, EEPROM=N
1:0	PLL1_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables APLL1 Div-by-8 cacade divider to TDC2 and TDC3 for cascade mode [0] = TDC2 driver enable [1] = TDC3 driver enable ROM=Y, EEPROM=N

1.489 R736 Register (Offset = 0x2E0) [Reset = 0x00]

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Table 1-491. R736 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	Reserved
3	PLL1_RDIV_TEST_EN	R/W	0x0	If GPIOx_SEL selects PLL1 R/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
2:0	RESERVED	R/W	0x0	Reserved

1.490 R741 Register (Offset = 0x2E5) [Reset = 0x00]

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Table 1-492. R741 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL1_VM_INSIDE	R	0x0	Denotes if the VCO tuning voltage is within operational range. ROM=N, EEPROM=N
4	PLL1_VM_HI	R	0x0	Denotes if the charge pump voltage is too high and outside range. If PLL1_VM_INSIDE = 0 and VM_HI = 0, then charge pump voltage is too low. ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.491 R745 Register (Offset = 0x2E9) [Reset = 0x00]

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Table 1-493. R745 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	PLL1_NDIV_TEST_EN	R/W	0x0	If GPIOx_SEL selects PLL1 N/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
4:0	RESERVED	R/W	0x0	Reserved

1.492 R746 Register (Offset = 0x2EA) [Reset = 0x01]

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Table 1-494. R746 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	PLL1_VCO_PREBUF_EN	R/W	0x1	Set to same value as APLL1_EN. ROM=Y, EEPROM=Y

1.493 R773 Register (Offset = 0x305) [Reset = 0x06]

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Table 1-495. R773 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	RESERVED	R/W	0x6	Reserved

1.494 R777 Register (Offset = 0x309) [Reset = 0x22]

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Table 1-496. R777 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_CP_PU_R	R/W	0x22	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ 0x2F = 1.65 kΩ 0x30 = 1.61 kΩ 0x31 = 1.58 kΩ 0x32 = 1.55 kΩ 0x33 = 1.52 kΩ 0x34 = 1.49 kΩ 0x35 = 1.46 kΩ 0x36 = 1.44 kΩ 0x37 = 1.41 kΩ 0x38 = 1.38 kΩ 0x39 = 1.36 kΩ 0x3A = 1.34 kΩ 0x3B = 1.31 kΩ 0x3C = 1.29 kΩ 0x3D = 1.27 kΩ 0x3E = 1.25 kΩ 0x3F = 1.23 kΩ 0x40 = 1.2 kΩ 0x41 = 1.18 kΩ

Table 1-496. R777 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = 1.16 kΩ 0x43 = 1.15 kΩ 0x44 = 1.13 kΩ 0x45 = 1.12 kΩ 0x46 = 1.1 kΩ 0x47 = 1.08 kΩ 0x48 = 1.07 kΩ 0x49 = 1.05 kΩ 0x4A = 1.04 kΩ 0x4B = 1.03 kΩ 0x4C = 1.01 kΩ 0x4D = 1 kΩ 0x4E = 0.989 kΩ 0x4F = 0.977 kΩ 0x50 = 0.964 kΩ 0x51 = 0.952 kΩ 0x52 = 0.941 kΩ 0x53 = 0.929 kΩ 0x54 = 0.92 kΩ 0x55 = 0.909 kΩ 0x56 = 0.898 kΩ 0x57 = 0.888 kΩ 0x58 = 0.878 kΩ 0x59 = 0.868 kΩ 0x5A = 0.858 kΩ 0x5B = 0.849 kΩ 0x5C = 0.841 kΩ 0x5D = 0.832 kΩ 0x5E = 0.823 kΩ 0x5F = 0.814 kΩ 0x60 = 0.8 kΩ 0x61 = 0.792 kΩ 0x62 = 0.784 kΩ 0x63 = 0.776 kΩ 0x64 = 0.769 kΩ 0x65 = 0.762 kΩ 0x66 = 0.754 kΩ 0x67 = 0.747 kΩ 0x68 = 0.74 kΩ 0x69 = 0.733 kΩ 0x6A = 0.726 kΩ 0x6B = 0.719 kΩ 0x6C = 0.713 kΩ 0x6D = 0.707 kΩ 0x6E = 0.7 kΩ 0x6F = 0.694 kΩ 0x70 = 0.688 kΩ 0x71 = 0.682 kΩ 0x72 = 0.676 kΩ 0x73 = 0.67 kΩ 0x74 = 0.665 kΩ 0x75 = 0.659 kΩ 0x76 = 0.654 kΩ 0x77 = 0.648 kΩ 0x78 = 0.643 kΩ 0x79 = 0.637 kΩ 0x7A = 0.632 kΩ 0x7B = 0.627 kΩ 0x7C = 0.623 kΩ 0x7D = 0.618 kΩ 0x7E = 0.613 kΩ 0x7F = 0.608 kΩ 0x80 = 0.6 kΩ 0x81 = 0.595 kΩ 0x82 = 0.591 kΩ 0x83 = 0.586 kΩ 0x84 = 0.583 kΩ 0x85 = 0.578 kΩ

Table 1-496. R777 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x86 = 0.574 kΩ 0x87 = 0.57 kΩ 0x88 = 0.565 kΩ 0x89 = 0.561 kΩ 0x8A = 0.557 kΩ 0x8B = 0.553 kΩ 0x8C = 0.55 kΩ 0x8D = 0.546 kΩ 0x8E = 0.542 kΩ 0x8F = 0.538 kΩ 0x90 = 0.535 kΩ 0x91 = 0.531 kΩ 0x92 = 0.527 kΩ 0x93 = 0.524 kΩ 0x94 = 0.521 kΩ 0x95 = 0.517 kΩ 0x96 = 0.514 kΩ 0x97 = 0.51 kΩ 0x98 = 0.507 kΩ 0x99 = 0.504 kΩ 0x9A = 0.5 kΩ 0x9B = 0.497 kΩ 0x9C = 0.494 kΩ 0x9D = 0.491 kΩ 0x9E = 0.488 kΩ 0x9F = 0.485 kΩ 0xA0 = 0.48 kΩ 0xA1 = 0.477 kΩ 0xA2 = 0.474 kΩ 0xA3 = 0.471 kΩ 0xA4 = 0.469 kΩ 0xA5 = 0.466 kΩ 0xA6 = 0.463 kΩ 0xA7 = 0.46 kΩ 0xA8 = 0.458 kΩ 0xA9 = 0.455 kΩ 0xAA = 0.452 kΩ 0xAB = 0.45 kΩ 0xAC = 0.447 kΩ 0xAD = 0.445 kΩ 0xAE = 0.442 kΩ 0xAF = 0.44 kΩ 0xB0 = 0.437 kΩ 0xB1 = 0.435 kΩ 0xB2 = 0.432 kΩ 0xB3 = 0.43 kΩ 0xB4 = 0.428 kΩ 0xB5 = 0.425 kΩ 0xB6 = 0.423 kΩ 0xB7 = 0.421 kΩ 0xB8 = 0.419 kΩ 0xB9 = 0.416 kΩ 0xBA = 0.414 kΩ 0xBB = 0.412 kΩ 0xBC = 0.41 kΩ 0xBD = 0.408 kΩ 0xBE = 0.406 kΩ 0xBF = 0.404 kΩ 0xC0 = 0.4 kΩ 0xC1 = 0.398 kΩ 0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ

Table 1-496. R777 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ 0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.495 R778 Register (Offset = 0x30A) [Reset = 0x09]

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Table 1-497. R778 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL2_CP_PU_DIS	R/W	0x0	PLL charge pump - pump up disable ROM=Y, EEPROM=N

Table 1-497. R778 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PLL2_CPG	R/W	0x9	PLL charge pump gain ROM=Y, EEPROM=Y 0x0 = 0 mA 0x1 = 0.4 mA 0x2 = 0.8 mA 0x3 = 1.2 mA 0x4 = 1.6 mA 0x5 = 2.0 mA 0x6 = 2.4 mA 0x7 = 2.8 mA 0x8 = 3.0 mA 0x9 = 3.4 mA 0xA = 3.8 mA 0xB = 4.2 mA 0xC = 4.6 mA 0xD = 5.0 mA 0xE = 5.4 mA 0xF = 5.8 mA

1.496 R779 Register (Offset = 0x30B) [Reset = 0x07]

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Table 1-498. R779 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_LF_R2	R/W	0x7	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.301 kΩ 0x2 = 0.551 kΩ 0x3 = 0.209 kΩ 0x4 = 1.05 kΩ 0x5 = 0.244 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 2.05 kΩ 0x9 = 0.269 kΩ 0xA = 0.444 kΩ 0xB = 0.194 kΩ 0xC = 0.709 kΩ 0xD = 0.224 kΩ 0xE = 0.0446 kΩ 0xF = 0.0421 kΩ 0x10 = 0.932 kΩ 0x11 = 1.18 kΩ 0x12 = 1.43 kΩ 0x13 = 1.09 kΩ 0x14 = 1.93 kΩ 0x15 = 1.13 kΩ 0x16 = 1.26 kΩ 0x17 = 1.07 kΩ 0x18 = 2.93 kΩ 0x19 = 1.15 kΩ 0x1A = 1.33 kΩ 0x1B = 1.08 kΩ 0x1C = 1.59 kΩ 0x1D = 1.11 kΩ 0x1E = 0.929 kΩ 0x1F = 0.926 kΩ 0x20 = 1.83 kΩ 0x21 = 2.08 kΩ 0x22 = 2.33 kΩ 0x23 = 1.99 kΩ 0x24 = 2.83 kΩ 0x25 = 2.03 kΩ 0x26 = 2.16 kΩ 0x27 = 1.97 kΩ 0x28 = 3.83 kΩ 0x29 = 2.05 kΩ 0x2A = 2.23 kΩ 0x2B = 1.98 kΩ 0x2C = 2.49 kΩ 0x2D = 2.01 kΩ 0x2E = 1.83 kΩ 0x2F = 1.83 kΩ 0x30 = 2.72 kΩ 0x31 = 2.97 kΩ 0x32 = 3.22 kΩ 0x33 = 2.88 kΩ 0x34 = 3.72 kΩ 0x35 = 2.91 kΩ 0x36 = 3.04 kΩ 0x37 = 2.85 kΩ 0x38 = 4.72 kΩ 0x39 = 2.94 kΩ 0x3A = 3.11 kΩ 0x3B = 2.86 kΩ 0x3C = 3.38 kΩ 0x3D = 2.89 kΩ 0x3E = 2.71 kΩ 0x3F = 2.71 kΩ

1.497 R780 Register (Offset = 0x30C) [Reset = 0x02]

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Table 1-499. R780 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-499. R780 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R3	R/W	0x2	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ 0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.498 R781 Register (Offset = 0x30D) [Reset = 0x02]

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Table 1-500. R781 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-500. R781 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R4	R/W	0x2	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.016 kΩ 0x1 = 0.277 kΩ 0x2 = 0.657 kΩ 0x3 = 0.214 kΩ 0x4 = 0.754 kΩ 0x5 = 0.221 kΩ 0x6 = 0.375 kΩ 0x7 = 0.183 kΩ 0x8 = 0.863 kΩ 0x9 = 1.08 kΩ 0xA = 1.46 kΩ 0xB = 1.01 kΩ 0xC = 1.55 kΩ 0xD = 1.02 kΩ 0xE = 1.17 kΩ 0xF = 0.982 kΩ 0x10 = 1.68 kΩ 0x11 = 1.89 kΩ 0x12 = 2.27 kΩ 0x13 = 1.83 kΩ 0x14 = 2.37 kΩ 0x15 = 1.84 kΩ 0x16 = 1.99 kΩ 0x17 = 1.8 kΩ 0x18 = 2.48 kΩ 0x19 = 2.69 kΩ 0x1A = 3.07 kΩ 0x1B = 2.63 kΩ 0x1C = 3.17 kΩ 0x1D = 2.63 kΩ 0x1E = 2.79 kΩ 0x1F = 2.6 kΩ 0x20 = 3.31 kΩ 0x21 = 3.52 kΩ 0x22 = 3.9 kΩ 0x23 = 3.46 kΩ 0x24 = 4 kΩ 0x25 = 3.47 kΩ 0x26 = 3.62 kΩ 0x27 = 3.43 kΩ 0x28 = 4.11 kΩ 0x29 = 4.32 kΩ 0x2A = 4.7 kΩ 0x2B = 4.26 kΩ 0x2C = 4.8 kΩ 0x2D = 4.26 kΩ 0x2E = 4.42 kΩ 0x2F = 4.23 kΩ 0x30 = 4.92 kΩ 0x31 = 5.14 kΩ 0x32 = 5.52 kΩ 0x33 = 5.07 kΩ 0x34 = 5.61 kΩ 0x35 = 5.08 kΩ 0x36 = 5.23 kΩ 0x37 = 5.04 kΩ 0x38 = 5.72 kΩ 0x39 = 5.94 kΩ 0x3A = 6.32 kΩ 0x3B = 5.87 kΩ 0x3C = 6.41 kΩ 0x3D = 5.88 kΩ 0x3E = 6.03 kΩ 0x3F = 5.84 kΩ

1.499 R782 Register (Offset = 0x30E) [Reset = 0xFF]

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Table 1-501. R782 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL2_DISABLE_3RD4TH	R/W	0x3	PLL Loop Filter Disconnects C3 and C4 ROM=Y, EEPROM=N 0x0 = C3/C4 Disconnected 0x1 = C3=Enabled, C4=Disconnected 0x2 = C3=Disconnected, C4=Enabled 0x3 = C3=Enabled, C4=Enabled
5:3	PLL2_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF
2:0	PLL2_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.500 R783 Register (Offset = 0x30F) [Reset = 0x00]

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Table 1-502. R783 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_RDIV_8:8	R/W	0x0	See Register 784

1.501 R784 Register (Offset = 0x310) [Reset = 0x0A]

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Table 1-503. R784 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_RDIV	R/W	0xA	PLL R Divider ROM=Y, EEPROM=Y

1.502 R785 Register (Offset = 0x311) [Reset = 0x02]

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Table 1-504. R785 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL2_RDIV_XO_EN	R/W	0x0	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[2] = 1 ROM=Y, EEPROM=Y

Table 1-504. R785 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PLL2_RDIV_XO_DBLR_EN	R/W	0x0	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL2_RDIV_BYPASS_EN	R/W	0x0	Bypass R Divider ROM=Y, EEPROM=Y
1:0	PLL2_RDIV_MUX_SEL	R/W	0x2	Select R Divider input: 0=XO, 1=VCO1 feedback divider, 2=VCO3 feedback divider ROM=Y, EEPROM=Y 0x0 = XO 0x1 = VCO1 feedback divider 0x2 = VCO3 feedback divider

1.503 R786 Register (Offset = 0x312) [Reset = 0x00]

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Table 1-505. R786 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_NDIV_8:8	R/W	0x0	See Register 787

1.504 R787 Register (Offset = 0x313) [Reset = 0x37]

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Table 1-506. R787 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NDIV	R/W	0x37	PLL N Divider ROM=Y, EEPROM=Y

1.505 R788 Register (Offset = 0x314) [Reset = 0x29]

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Table 1-507. R788 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_MSB	R/W	0x29	When PLL2_MODE is set for 24 bit fractional. PLL2_NUM_MSB is effective PLL2_NUM[23:16]. Other PLL2_NUM and PLL2_DEN bits in programmable mode are in PLL2_NUM field. When in 40-bit fixed denominator PLL mode, then PLL2_NUM_MSB is unused. ROM=Y, EEPROM=Y

1.506 R789 Register (Offset = 0x315) [Reset = 0xB0]

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Table 1-508. R789 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_39:32	R/W	0xB0	See Register 793

1.507 R790 Register (Offset = 0x316) [Reset = 0x00]

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Table 1-509. R790 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_31:24	R/W	0x0	See Register 793

1.508 R791 Register (Offset = 0x317) [Reset = 0x00]

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Table 1-510. R791 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_23:16	R/W	0x0	See Register 793

1.509 R792 Register (Offset = 0x318) [Reset = 0x00]

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Table 1-511. R792 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_15:8	R/W	0x0	See Register 793

1.510 R793 Register (Offset = 0x319) [Reset = 0x00]

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Table 1-512. R793 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM	R/W	0x0	When PLL2_MODE = 1 (40-bit fixed denominator) mode then PLL2_NUM contains the APLL2 numerator. When PLL2_MODE = 0 (24-bit programmable denominator) then PLL2_NUM[23:0] stores the programmable PLL2 denominator and PLL2_NUM[39:24] stores the 16 LSBs of the PLL2 numerator. Total PLL2 numerator is calculated with PLL2_NUM_MSB as the 8 MSBs. In 24-bit programmable denominator mode PLL2_NUM[23:0] = 0 is 2^{24}. ROM=Y, EEPROM=Y

1.511 R794 Register (Offset = 0x31A) [Reset = 0x07]

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Table 1-513. R794 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5:4	PLL2_DTHRMODE	R/W	0x0	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL2_ORDER	R/W	0x3	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd

Table 1-513. R794 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL2_MODE	R/W	0x1	In APLL 24-bit num/den mode, APLL denominator is programmable. Not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL2_NUM[23:0] The numerator is stored in (PLL2_NUM_MSB << 16) + PLL2_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.512 R795 Register (Offset = 0x31B) [Reset = 0x00]

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Table 1-514. R795 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_39:32	R	0x0	See Register 799

1.513 R796 Register (Offset = 0x31C) [Reset = 0x00]

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Table 1-515. R796 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_31:24	R	0x0	See Register 799

1.514 R797 Register (Offset = 0x31D) [Reset = 0x00]

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Table 1-516. R797 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_23:16	R	0x0	See Register 799

1.515 R798 Register (Offset = 0x31E) [Reset = 0x00]

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Table 1-517. R798 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT_15:8	R	0x0	See Register 799

1.516 R799 Register (Offset = 0x31F) [Reset = 0x00]

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Table 1-518. R799 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL2_NUM_STAT	R	0x0	Readback current effective APLL2 Numerator after FDEV and/or DPLL correction ROM=N, EEPROM=N

1.517 R803 Register (Offset = 0x323) [Reset = 0x40]

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Table 1-519. R803 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R/W	0x2	Reserved
4	PLL2_VCO_BUF_EN	R/W	0x0	Enables the VCO2 Buffer which drives the DPLL feedback, reference window detector, DPLL reference for cascade mode, and test mode ROM=Y, EEPROM=N
3:2	PLL2_VCO_BUF_2REF_EN	R/W	0x0	Enables the APLL2 Div-by-4 cascade divider to [0] -> APLL1 and [1] -> APLL3 reference input for cascade mode. ROM=Y, EEPROM=Y
1	PLL2_VCO_BUF_2DPLL_EN	R/W	0x0	Enables the VCO2 Buffer output driver to DPLL2 feedback divider ROM=Y, EEPROM=N
0	PLL2_VCO_BUF_2WNDDET_EN	R/W	0x0	Enables the APLL2 Div-by-5 cascade divider to reference window detectors input buffer and prepares pre-divided clock for DPLL2 loop filter and PPM/Frequency detector. ROM=Y, EEPROM=N

1.518 R804 Register (Offset = 0x324) [Reset = 0x3C]

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Table 1-520. R804 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VCO_DIV_SYNC_EN	R/W	0x1	PLL2 Divider Sync Enable. Enables synchronization of post-dividers and reference dividers for PLL2. ROM=Y, EEPROM=N
4	PLL2_VCO_DIV_EN	R/W	0x1	Enables the VCO2 Div By 2 to 13 divide block. ROM=Y, EEPROM=Y
3:0	PLL2_VCO_DIV	R/W	0xC	Sets the VCO2 divider divide value from 2 to 13 ROM=Y, EEPROM=Y 0x0 = 2 (Reserved) 0x1 = 2 (Reserved) 0x2 = 2 0x3 = 3 0x4 = 4 0x5 = 5 0x6 = 6 0x7 = 7 0x8 = 8 0x9 = 9 0xA = 10 0xB = 11 0xC = 12 0xD = 13

1.519 R805 Register (Offset = 0x325) [Reset = 0x04]

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Table 1-521. R805 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	PLL2_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables APLL2 Div-by-10 cascade divider to TDC1 and TDC3 for cascade mode [0] = TDC1 driver enable [1] = TDC3 driver enable ROM=Y, EEPROM=N

Table 1-521. R805 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	PLL2_VCO_DIV_DRVR_EN	R/W	0x4	Enables VCO2 to Outputs. Output buffer outputs: [0] -> OUT0_1, [1] -> OUT2_3, [2] -> OUT4_5 and OUT6_7, [3] -> OUT8_9, OUT10_11, and OUT12_13, and [4] -> OUT14_15. ROM=Y, EEPROM=Y

1.520 R808 Register (Offset = 0x328) [Reset = 0x00]

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Table 1-522. R808 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	Reserved
3	PLL2_RDIV_TEST_EN	R/W	0x0	If GPIOx_SEL selects PLL2 R/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
2:0	RESERVED	R/W	0x0	Reserved

1.521 R813 Register (Offset = 0x32D) [Reset = 0x00]

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Table 1-523. R813 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VM_INSIDE	R	0x0	Denotes if the VCO tuning voltage is within operational range. ROM=N, EEPROM=N
4	PLL2_VM_HI	R	0x0	Denotes if the charge pump voltage is too high and outside range. If PLL2_VM_INSIDE = 0 and VM_HI = 0, then charge pump voltage is too low. ROM=N, EEPROM=N
3:0	RESERVED	R	0x0	Reserved

1.522 R818 Register (Offset = 0x332) [Reset = 0x00]

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Table 1-524. R818 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	PLL2_NDIV_TEST_EN	R/W	0x0	If GPIOx_SEL selects PLL2 N/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
4:0	RESERVED	R/W	0x0	Reserved

1.523 R819 Register (Offset = 0x333) [Reset = 0x01]

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Table 1-525. R819 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:1	RESERVED	R/W	0x0	Reserved

Table 1-525. R819 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL2_VCO_PREBUF_EN	R/W	0x1	Set to same value as APLL2_EN. ROM=Y, EEPROM=Y

1.524 R840 Register (Offset = 0x348) [Reset = 0x22]

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Table 1-526. R840 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_CPBAW_BLEED	R/W	0x22	PLL charge pump pull-up resistor selection ROM=Y, EEPROM=N 0x0 = Disabled 0x1 = 78 kΩ 0x2 = 39 kΩ 0x3 = 26 kΩ 0x4 = 20 kΩ 0x5 = 15.9 kΩ 0x6 = 13.2 kΩ 0x7 = 11.3 kΩ 0x8 = 9.8 kΩ 0x9 = 8.71 kΩ 0xA = 7.83 kΩ 0xB = 7.12 kΩ 0xC = 6.58 kΩ 0xD = 6.07 kΩ 0xE = 5.63 kΩ 0xF = 5.25 kΩ 0x10 = 4.9 kΩ 0x11 = 4.61 kΩ 0x12 = 4.35 kΩ 0x13 = 4.12 kΩ 0x14 = 3.94 kΩ 0x15 = 3.75 kΩ 0x16 = 3.57 kΩ 0x17 = 3.42 kΩ 0x18 = 3.27 kΩ 0x19 = 3.14 kΩ 0x1A = 3.01 kΩ 0x1B = 2.9 kΩ 0x1C = 2.81 kΩ 0x1D = 2.71 kΩ 0x1E = 2.62 kΩ 0x1F = 2.53 kΩ 0x20 = 2.4 kΩ 0x21 = 2.33 kΩ 0x22 = 2.26 kΩ 0x23 = 2.2 kΩ 0x24 = 2.14 kΩ 0x25 = 2.09 kΩ 0x26 = 2.03 kΩ 0x27 = 1.98 kΩ 0x28 = 1.93 kΩ 0x29 = 1.88 kΩ 0x2A = 1.84 kΩ 0x2B = 1.79 kΩ 0x2C = 1.76 kΩ 0x2D = 1.72 kΩ 0x2E = 1.68 kΩ 0x2F = 1.65 kΩ 0x30 = 1.61 kΩ 0x31 = 1.58 kΩ 0x32 = 1.55 kΩ 0x33 = 1.52 kΩ 0x34 = 1.49 kΩ 0x35 = 1.46 kΩ 0x36 = 1.44 kΩ 0x37 = 1.41 kΩ 0x38 = 1.38 kΩ 0x39 = 1.36 kΩ 0x3A = 1.34 kΩ 0x3B = 1.31 kΩ 0x3C = 1.29 kΩ 0x3D = 1.27 kΩ 0x3E = 1.25 kΩ 0x3F = 1.23 kΩ 0x40 = 1.2 kΩ 0x41 = 1.18 kΩ

Table 1-526. R840 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = 1.16 kΩ 0x43 = 1.15 kΩ 0x44 = 1.13 kΩ 0x45 = 1.12 kΩ 0x46 = 1.1 kΩ 0x47 = 1.08 kΩ 0x48 = 1.07 kΩ 0x49 = 1.05 kΩ 0x4A = 1.04 kΩ 0x4B = 1.03 kΩ 0x4C = 1.01 kΩ 0x4D = 1 kΩ 0x4E = 0.989 kΩ 0x4F = 0.977 kΩ 0x50 = 0.964 kΩ 0x51 = 0.952 kΩ 0x52 = 0.941 kΩ 0x53 = 0.929 kΩ 0x54 = 0.92 kΩ 0x55 = 0.909 kΩ 0x56 = 0.898 kΩ 0x57 = 0.888 kΩ 0x58 = 0.878 kΩ 0x59 = 0.868 kΩ 0x5A = 0.858 kΩ 0x5B = 0.849 kΩ 0x5C = 0.841 kΩ 0x5D = 0.832 kΩ 0x5E = 0.823 kΩ 0x5F = 0.814 kΩ 0x60 = 0.8 kΩ 0x61 = 0.792 kΩ 0x62 = 0.784 kΩ 0x63 = 0.776 kΩ 0x64 = 0.769 kΩ 0x65 = 0.762 kΩ 0x66 = 0.754 kΩ 0x67 = 0.747 kΩ 0x68 = 0.74 kΩ 0x69 = 0.733 kΩ 0x6A = 0.726 kΩ 0x6B = 0.719 kΩ 0x6C = 0.713 kΩ 0x6D = 0.707 kΩ 0x6E = 0.7 kΩ 0x6F = 0.694 kΩ 0x70 = 0.688 kΩ 0x71 = 0.682 kΩ 0x72 = 0.676 kΩ 0x73 = 0.67 kΩ 0x74 = 0.665 kΩ 0x75 = 0.659 kΩ 0x76 = 0.654 kΩ 0x77 = 0.648 kΩ 0x78 = 0.643 kΩ 0x79 = 0.637 kΩ 0x7A = 0.632 kΩ 0x7B = 0.627 kΩ 0x7C = 0.623 kΩ 0x7D = 0.618 kΩ 0x7E = 0.613 kΩ 0x7F = 0.608 kΩ 0x80 = 0.6 kΩ 0x81 = 0.595 kΩ 0x82 = 0.591 kΩ 0x83 = 0.586 kΩ 0x84 = 0.583 kΩ 0x85 = 0.578 kΩ

Table 1-526. R840 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x86 = 0.574 kΩ 0x87 = 0.57 kΩ 0x88 = 0.565 kΩ 0x89 = 0.561 kΩ 0x8A = 0.557 kΩ 0x8B = 0.553 kΩ 0x8C = 0.55 kΩ 0x8D = 0.546 kΩ 0x8E = 0.542 kΩ 0x8F = 0.538 kΩ 0x90 = 0.535 kΩ 0x91 = 0.531 kΩ 0x92 = 0.527 kΩ 0x93 = 0.524 kΩ 0x94 = 0.521 kΩ 0x95 = 0.517 kΩ 0x96 = 0.514 kΩ 0x97 = 0.51 kΩ 0x98 = 0.507 kΩ 0x99 = 0.504 kΩ 0x9A = 0.5 kΩ 0x9B = 0.497 kΩ 0x9C = 0.494 kΩ 0x9D = 0.491 kΩ 0x9E = 0.488 kΩ 0x9F = 0.485 kΩ 0xA0 = 0.48 kΩ 0xA1 = 0.477 kΩ 0xA2 = 0.474 kΩ 0xA3 = 0.471 kΩ 0xA4 = 0.469 kΩ 0xA5 = 0.466 kΩ 0xA6 = 0.463 kΩ 0xA7 = 0.46 kΩ 0xA8 = 0.458 kΩ 0xA9 = 0.455 kΩ 0xAA = 0.452 kΩ 0xAB = 0.45 kΩ 0xAC = 0.447 kΩ 0xAD = 0.445 kΩ 0xAE = 0.442 kΩ 0xAF = 0.44 kΩ 0xB0 = 0.437 kΩ 0xB1 = 0.435 kΩ 0xB2 = 0.432 kΩ 0xB3 = 0.43 kΩ 0xB4 = 0.428 kΩ 0xB5 = 0.425 kΩ 0xB6 = 0.423 kΩ 0xB7 = 0.421 kΩ 0xB8 = 0.419 kΩ 0xB9 = 0.416 kΩ 0xBA = 0.414 kΩ 0xBB = 0.412 kΩ 0xBC = 0.41 kΩ 0xBD = 0.408 kΩ 0xBE = 0.406 kΩ 0xBF = 0.404 kΩ 0xC0 = 0.4 kΩ 0xC1 = 0.398 kΩ 0xC2 = 0.396 kΩ 0xC3 = 0.394 kΩ 0xC4 = 0.392 kΩ 0xC5 = 0.39 kΩ 0xC6 = 0.388 kΩ 0xC7 = 0.386 kΩ 0xC8 = 0.384 kΩ 0xC9 = 0.382 kΩ

Table 1-526. R840 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0xCA = 0.381 kΩ 0xCB = 0.379 kΩ 0xCC = 0.377 kΩ 0xCD = 0.375 kΩ 0xCE = 0.373 kΩ 0xCF = 0.372 kΩ 0xD0 = 0.37 kΩ 0xD1 = 0.368 kΩ 0xD2 = 0.366 kΩ 0xD3 = 0.365 kΩ 0xD4 = 0.363 kΩ 0xD5 = 0.361 kΩ 0xD6 = 0.36 kΩ 0xD7 = 0.358 kΩ 0xD8 = 0.356 kΩ 0xD9 = 0.355 kΩ 0xDA = 0.353 kΩ 0xDB = 0.352 kΩ 0xDC = 0.35 kΩ 0xDD = 0.349 kΩ 0xDE = 0.347 kΩ 0xDF = 0.345 kΩ 0xE0 = 0.343 kΩ 0xE1 = 0.341 kΩ 0xE2 = 0.34 kΩ 0xE3 = 0.338 kΩ 0xE4 = 0.337 kΩ 0xE5 = 0.336 kΩ 0xE6 = 0.334 kΩ 0xE7 = 0.333 kΩ 0xE8 = 0.331 kΩ 0xE9 = 0.33 kΩ 0xEA = 0.328 kΩ 0xEB = 0.327 kΩ 0xEC = 0.326 kΩ 0xED = 0.325 kΩ 0xEE = 0.323 kΩ 0xEF = 0.322 kΩ 0xF0 = 0.32 kΩ 0xF1 = 0.319 kΩ 0xF2 = 0.318 kΩ 0xF3 = 0.317 kΩ 0xF4 = 0.315 kΩ 0xF5 = 0.314 kΩ 0xF6 = 0.313 kΩ 0xF7 = 0.312 kΩ 0xF8 = 0.31 kΩ 0xF9 = 0.309 kΩ 0xFA = 0.308 kΩ 0xFB = 0.307 kΩ 0xFC = 0.306 kΩ 0xFD = 0.304 kΩ 0xFE = 0.303 kΩ 0xFF = 0.302 kΩ

1.525 R841 Register (Offset = 0x349) [Reset = 0x15]

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Table 1-527. R841 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL3_CP_PU_DIS	R/W	0x1	PLL charge pump pump-up disable ROM=Y, EEPROM=N

Table 1-527. R841 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PLL3_CPG	R/W	0x5	PLL charge pump gain ROM=Y, EEPROM=N 0x0 = 0 mA 0x1 = 0.4 mA 0x2 = 0.8 mA 0x3 = 1.2 mA 0x4 = 1.6 mA 0x5 = 2.0 mA 0x6 = 2.4 mA 0x7 = 2.8 mA 0x8 = 3.0 mA 0x9 = 3.4 mA 0xA = 3.8 mA 0xB = 4.2 mA 0xC = 4.6 mA 0xD = 5.0 mA 0xE = 5.4 mA 0xF = 5.8 mA

1.526 R842 Register (Offset = 0x34A) [Reset = 0x01]

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Table 1-528. R842 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-528. R842 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL3_LF_R2	R/W	0x1	PLL Loop Filter R2 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.985 kΩ 0x3 = 1.39 kΩ 0x4 = 1.72 kΩ 0x5 = 2.12 kΩ 0x6 = 2.6 kΩ 0x7 = 3 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.23 kΩ 0xB = 4.63 kΩ 0xC = 4.96 kΩ 0xD = 5.36 kΩ 0xE = 5.84 kΩ 0xF = 6.24 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.49 kΩ 0x13 = 7.89 kΩ 0x14 = 8.22 kΩ 0x15 = 8.63 kΩ 0x16 = 9.1 kΩ 0x17 = 9.5 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.7 kΩ 0x1B = 11.1 kΩ 0x1C = 11.5 kΩ 0x1D = 11.9 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 14 kΩ 0x23 = 14.4 kΩ 0x24 = 14.7 kΩ 0x25 = 15.1 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.2 kΩ 0x2B = 17.6 kΩ 0x2C = 17.9 kΩ 0x2D = 18.3 kΩ 0x2E = 18.8 kΩ 0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.5 kΩ 0x33 = 20.9 kΩ 0x34 = 21.2 kΩ 0x35 = 21.6 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.7 kΩ 0x3B = 24.1 kΩ 0x3C = 24.4 kΩ 0x3D = 24.9 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.527 R843 Register (Offset = 0x34B) [Reset = 0x0D]

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Table 1-529. R843 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-529. R843 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL3_LF_R3	R/W	0xD	PLL Loop Filter R3 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.826 kΩ 0x3 = 1.23 kΩ 0x4 = 1.85 kΩ 0x5 = 2.26 kΩ 0x6 = 2.57 kΩ 0x7 = 2.97 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.07 kΩ 0xB = 4.47 kΩ 0xC = 5.09 kΩ 0xD = 5.5 kΩ 0xE = 5.81 kΩ 0xF = 6.22 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.33 kΩ 0x13 = 7.73 kΩ 0x14 = 8.36 kΩ 0x15 = 8.76 kΩ 0x16 = 9.08 kΩ 0x17 = 9.48 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.6 kΩ 0x1B = 11 kΩ 0x1C = 11.6 kΩ 0x1D = 12 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 13.8 kΩ 0x23 = 14.2 kΩ 0x24 = 14.8 kΩ 0x25 = 15.2 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.1 kΩ 0x2B = 17.5 kΩ 0x2C = 18.1 kΩ 0x2D = 18.5 kΩ 0x2E = 18.8 kΩ 0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.3 kΩ 0x33 = 20.7 kΩ 0x34 = 21.3 kΩ 0x35 = 21.7 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.6 kΩ 0x3B = 24 kΩ 0x3C = 24.6 kΩ 0x3D = 25 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.528 R844 Register (Offset = 0x34C) [Reset = 0x0D]

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Table 1-530. R844 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-530. R844 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL3_LF_R4	R/W	0xD	PLL Loop Filter R4 setting ROM=Y, EEPROM=N 0x0 = 0.0139 kΩ 0x1 = 0.51 kΩ 0x2 = 0.826 kΩ 0x3 = 1.23 kΩ 0x4 = 1.85 kΩ 0x5 = 2.26 kΩ 0x6 = 2.57 kΩ 0x7 = 2.97 kΩ 0x8 = 3.3 kΩ 0x9 = 3.75 kΩ 0xA = 4.07 kΩ 0xB = 4.47 kΩ 0xC = 5.09 kΩ 0xD = 5.5 kΩ 0xE = 5.81 kΩ 0xF = 6.22 kΩ 0x10 = 6.57 kΩ 0x11 = 7.01 kΩ 0x12 = 7.33 kΩ 0x13 = 7.73 kΩ 0x14 = 8.36 kΩ 0x15 = 8.76 kΩ 0x16 = 9.08 kΩ 0x17 = 9.48 kΩ 0x18 = 9.81 kΩ 0x19 = 10.3 kΩ 0x1A = 10.6 kΩ 0x1B = 11 kΩ 0x1C = 11.6 kΩ 0x1D = 12 kΩ 0x1E = 12.3 kΩ 0x1F = 12.7 kΩ 0x20 = 13 kΩ 0x21 = 13.5 kΩ 0x22 = 13.8 kΩ 0x23 = 14.2 kΩ 0x24 = 14.8 kΩ 0x25 = 15.2 kΩ 0x26 = 15.6 kΩ 0x27 = 16 kΩ 0x28 = 16.3 kΩ 0x29 = 16.7 kΩ 0x2A = 17.1 kΩ 0x2B = 17.5 kΩ 0x2C = 18.1 kΩ 0x2D = 18.5 kΩ 0x2E = 18.8 kΩ 0x2F = 19.2 kΩ 0x30 = 19.6 kΩ 0x31 = 20 kΩ 0x32 = 20.3 kΩ 0x33 = 20.7 kΩ 0x34 = 21.3 kΩ 0x35 = 21.7 kΩ 0x36 = 22.1 kΩ 0x37 = 22.5 kΩ 0x38 = 22.8 kΩ 0x39 = 23.2 kΩ 0x3A = 23.6 kΩ 0x3B = 24 kΩ 0x3C = 24.6 kΩ 0x3D = 25 kΩ 0x3E = 25.3 kΩ 0x3F = 25.7 kΩ

1.529 R845 Register (Offset = 0x34D) [Reset = 0xFF]

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Table 1-531. R845 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x3	Reserved
5:3	PLL3_LF_C3	R/W	0x7	PLL Loop Filter C3 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF
2:0	PLL3_LF_C4	R/W	0x7	PLL Loop Filter C4 setting ROM=Y, EEPROM=N 0x0 = 0 pF 0x1 = 10 pF 0x2 = 20 pF 0x3 = 30 pF 0x4 = 40 pF 0x5 = 50 pF 0x6 = 60 pF 0x7 = 70 pF

1.530 R846 Register (Offset = 0x34E) [Reset = 0x00]

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Table 1-532. R846 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL3_RDIV_8:8	R/W	0x0	See Register 847

1.531 R847 Register (Offset = 0x34F) [Reset = 0x0A]

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Table 1-533. R847 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_RDIV	R/W	0xA	PLL R Divider ROM=Y, EEPROM=Y

1.532 R848 Register (Offset = 0x350) [Reset = 0x1C]

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Table 1-534. R848 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	PLL3_RDIV_XO_EN	R/W	0x1	APLL reference source is from XO. Must also enable XO to drive this APLL with XO_OUT_BUF_EN[3] = 1 ROM=Y, EEPROM=Y
3	PLL3_RDIV_XO_DBLR_EN	R/W	0x1	Enables XO Doubler ROM=Y, EEPROM=Y
2	PLL3_RDIV_BYPASS_EN	R/W	0x1	Bypass R Divider ROM=Y, EEPROM=Y

Table 1-534. R848 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PLL3_RDIV_MUX_SEL	R/W	0x0	Select R Divider input: 0=XO, 1=VCO1 feedback divider, 2=VCO2 feedback divider ROM=Y, EEPROM=Y 0x0 = XO 0x1 = VCO1 feedback divider 0x2 = VCO2 feedback divider

1.533 R849 Register (Offset = 0x351) [Reset = 0x00]

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Table 1-535. R849 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL3_NDIV_8:8	R/W	0x0	See Register 850

1.534 R850 Register (Offset = 0x352) [Reset = 0x1A]

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Table 1-536. R850 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NDIV	R/W	0x1A	PLL N Divider ROM=Y, EEPROM=Y

1.535 R851 Register (Offset = 0x353) [Reset = 0x4C]

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Table 1-537. R851 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_MSB	R/W	0x4C	When PLL3_MODE is set for 24 bit fractional. PLL3_NUM_MSB is effective PLL3_NUM[23:16]. Other PLL3_NUM and PLL3_DEN bits in programmable mode are in PLL3_NUM field. When in 40-bit fixed denominator PLL mode, then PLL3_NUM_MSB is unused. ROM=Y, EEPROM=Y

1.536 R852 Register (Offset = 0x354) [Reset = 0x0A]

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Table 1-538. R852 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_39:32	R/W	0xA	See Register 856

1.537 R853 Register (Offset = 0x355) [Reset = 0xAA]

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Table 1-539. R853 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_31:24	R/W	0xAA	See Register 856

1.538 R854 Register (Offset = 0x356) [Reset = 0xAA]

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Table 1-540. R854 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_23:16	R/W	0xAA	See Register 856

1.539 R855 Register (Offset = 0x357) [Reset = 0xAA]

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Table 1-541. R855 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM_15:8	R/W	0xAA	See Register 856

1.540 R856 Register (Offset = 0x358) [Reset = 0xAB]

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Table 1-542. R856 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL3_NUM	R/W	0xAB	When PLL3_MODE = 1 (40-bit fixed denominator) mode then PLL3_NUM contains the APLL3 numerator. When PLL3_MODE = 0 (24-bit programmable denominator) then PLL3_NUM[23:0] stores the programmable PLL3 denominator and PLL3_NUM[39:24] stores the 16 LSBs of the PLL3 numerator. Total PLL3 numerator is calculated with PLL3_NUM_MSB as the 8 MSBs. In 24-bit programmable denominator mode PLL3_NUM[23:0] = 0 is 2^{24}. ROM=Y, EEPROM=Y

1.541 R857 Register (Offset = 0x359) [Reset = 0x05]

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Table 1-543. R857 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5:4	PLL3_DTHRMODE	R/W	0x0	PLL MASH Dither Mode ROM=Y, EEPROM=N 0x0 = Constant Dither MACC2 0x1 = Constant Dither MACC2 and MACC3 0x2 = LFSR Dither MACC2 0x3 = Dither Disabled
3:1	PLL3_ORDER	R/W	0x2	PLL MASH Order ROM=Y, EEPROM=N 0x0 = Integer Mode Divider 0x1 = 1st 0x2 = 2nd 0x3 = 3rd
0	PLL3_MODE	R/W	0x1	In APLL 24-bit num/den mode, APLL denominator is programmable. Recommended not for use with DPLL mode. In 24-bit mode, the denominator is stored in PLL3_NUM[23:0] The numerator is stored in (PLL3_NUM_MSB << 16) + PLL3_NUM[39:24]. In APLL 40-bit mode, APLL denominator is fixed. For use with DPLL. ROM=Y, EEPROM=Y 0x0 = APLL 24-bit num/den 0x1 = APLL 40-bit num (Req for DPLL)

1.542 R858 Register (Offset = 0x35A) [Reset = 0x00]

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Table 1-544. R858 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT_39:32	R	0x0	See Register 862

1.543 R859 Register (Offset = 0x35B) [Reset = 0x00]

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Table 1-545. R859 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT_31:24	R	0x0	See Register 862

1.544 R860 Register (Offset = 0x35C) [Reset = 0x00]

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Table 1-546. R860 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT_23:16	R	0x0	See Register 862

1.545 R861 Register (Offset = 0x35D) [Reset = 0x00]

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Table 1-547. R861 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT_15:8	R	0x0	See Register 862

1.546 R862 Register (Offset = 0x35E) [Reset = 0x00]

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Table 1-548. R862 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	APLL3_NUM_STAT	R	0x0	Readback current effective APLL3 Numerator after FDEV and/or DPLL correction ROM=N, EEPROM=N

1.547 R864 Register (Offset = 0x360) [Reset = 0xF8]

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Table 1-549. R864 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	PLL3_VCO_BUF_OUT_EN	R/W	0xF	Enables VCO3 to: [0] -> VCO3 Post-divider, [1] -> VCO3 Auxiliary Buffer (TDC1 Reference Clock Buffer, TDC2 Reference Clock Buffer, APLL1 Reference Clock Buffer, APLL2 Reference Clock Buffer, Window Monitor), [2] -> APLL3 N-Divider, [3] -> DPLL3 N-Divider ROM=Y, EEPROM=Y
3	PLL3_VCO_DIV_SYNC_EN	R/W	0x1	PLL3 Divider Sync Enable. Enables synchronization of post-dividers and reference dividers for PLL3. ROM=Y, EEPROM=N

Table 1-549. R864 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL3_PRI_DIV	R/W	0x0	Sets the VCO3 primary divider divide value from 1 to 8 (div = field value + 1) ROM=Y, EEPROM=Y 0x0 = 1 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = 8

1.548 R865 Register (Offset = 0x361) [Reset = 0xB9]

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Table 1-550. R865 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	PLL3_VCO_DIV_SEL	R/W	0x2	Selects APLL3 P1 post-divider block or APLL3 P1 followed by additional divide-by 2 block. ROM=Y, EEPROM=Y 0x0 = PLL3 drive off 0x1 = Reserved 0x2 = Divide-by-1-to-8 direct 0x3 = Divide-by-1-to-8 and /2
7:6	RESERVED	R/W	0x2	Reserved
5	PLL3_VCO_CHAN_DRVR_IN_EN	R/W	0x1	Enables the selected clock (div1to8 or div2) to the VCO3 to Outputs Output Buffer. See PLL3_VCO_DIV1TO8_EN and PLL3_VCO_DIV2_EN. Optimization to prevent unused domain from interacting with active domains. Always on if using PLL3. Might be on to help reduce crosstalk from APLL3. ROM=Y, EEPROM=Y
4:0	PLL3_CHAN_EN	R/W	0x19	Enables the VCO3 to Outputs output buffer outputs: [0] -> OUT0_1, [1] -> OUT2 and OUT3, [2] -> OUT4_5 and OUT6_7, [3] -> OUT8_9, OUT10_11, and OUT12_13, [4] -> OUT14 and OUT15 ROM=Y, EEPROM=Y

1.549 R866 Register (Offset = 0x362) [Reset = 0x1C]

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Table 1-551. R866 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	PLL3_VCO_BUF_2REF_EN	R/W	0x3	Enables the APLL3 Div-by-2 cascade divider to [0] -> APLL1 and [1] -> APLL2 reference input for cascade mode. ROM=Y, EEPROM=Y
2	PLL3_WIN_DET_DRVR_EN	R/W	0x1	Enables the APLL3 Div-by-2 cascade divider to reference window detectors input buffer, ROM=Y, EEPROM=N
1:0	PLL3_VCO_BUF_FB_TDC_EN	R/W	0x0	Enables APLL3 Div-by-4 cascade divider to TDC1 and TDC2 for cascade mode [0] = TDC1 driver enable [1] = TDC2 driver enable ROM=Y, EEPROM=N

1.550 R872 Register (Offset = 0x368) [Reset = 0x00]

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Table 1-552. R872 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	PLL3_NCLK_TEST_EN	R/W	0x0	If GPIOx_SEL selects PLL3 N/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
3	PLL3_RDIV_TEST_EN	R/W	0x0	If GPIOx_SEL selects PLL3 R/2 as an output. Then this bit must be set along with STATUS_MUX_DIV2_EN=1. ROM=N, EEPROM=N
2:0	RESERVED	R/W	0x0	Reserved

1.551 R961 Register (Offset = 0x3C1) [Reset = 0x40]

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Table 1-553. R961 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	OUT_0_EN	R/W	0x1	OUT0 Enable. If CMOS on OUT0 is used, this enable must also be set. ROM=Y, EEPROM=Y
5:3	OUT_0_VCM	R/W	0x0	Controls the differential output common mode voltage for OUT0 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_0_VOD	R/W	0x0	Controls the differential output voltage swing for OUT0 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.552 R962 Register (Offset = 0x3C2) [Reset = 0x30]

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Table 1-554. R962 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_0_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
6	OUT_0_STATIC_LOW	R/W	0x0	When OUT0 is forced to a static output, this bit determines if the output voltage will be 0: Static Low 1: Static High ROM=Y, EEPROM=N 0x0 = L 0x1 = H

Table 1-554. R962 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	OUT_0_P_CMOS_EN	R/W	0x1	OUT0P CMOS Enable. Overrides the OUT_0_VOD setting and makes OUT_0 CMOS. Setting this bit enables of the positive terminal of OUT0 for CMOS outputs. OUT_0_ENABLE must also be set. ROM=Y, EEPROM=Y
4	OUT_0_N_CMOS_EN	R/W	0x1	OUT0N CMOS Enable. Setting this bit enables of the negative terminal of OUT0 for CMOS outputs. OUT_0_ENABLE must also be set. ROM=Y, EEPROM=Y
3	OUT_0_P_INVERT_POLARITY	R/W	0x0	OUT0P CMOS Invert Polarity. Setting this bit inverts the polarity of the positive terminal of OUT0 for CMOS outputs. ROM=Y, EEPROM=N
2	OUT_0_N_INVERT_POLARITY	R/W	0x0	OUT0N CMOS Invert Polarity. Setting this bit inverts the polarity of the negative terminal of OUT0 for CMOS outputs. ROM=Y, EEPROM=N
1	OUT_0_P_FORCELOW	R/W	0x0	OUT0P CMOS Force Low. Setting this bit forces the positive terminal of OUT0 low. ROM=Y, EEPROM=N
0	OUT_0_N_FORCELOW	R/W	0x0	OUT0N CMOS Force Low. Setting this bit forces the negative terminal of OUT0 low. ROM=Y, EEPROM=N

1.553 R963 Register (Offset = 0x3C3) [Reset = 0x00]

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Table 1-555. R963 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_CONFIGURATION	R/W	0x0	OUT0 configuration. Selects from CH0 Bypass, CH1 Bypass, CHDIV0, CHDIV1, CH0/2 low-noise divide by two path, SYSREF, SYSREF + Analog Delay, or static DC H/L. ROM=Y, EEPROM=Y and N 0x0 = CH0/2 0x14 = CHDIV1 0x20 = SYSREF+ADLY 0x21 = SYSREF 0x22 = Static DC 0x28 = CHDIV0 0x40 = CH1 Bypass 0x80 = CH0 Bypass

1.554 R964 Register (Offset = 0x3C4) [Reset = 0x4F]

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Table 1-556. R964 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	OUT_1_EN	R/W	0x1	OUT1 Enable. If CMOS on OUT1 is used, this enable must also be set. ROM=Y, EEPROM=Y

Table 1-556. R964 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	OUT_1_VCM	R/W	0x1	Controls the differential output common mode voltage for OUT1 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_1_VOD	R/W	0x7	Controls the differential output voltage swing for OUT1 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.555 R965 Register (Offset = 0x3C5) [Reset = 0x00]

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Table 1-557. R965 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_1_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
6	OUT_1_STATIC_LOW	R/W	0x0	When OUT1 is forced to a static output, this bit determines if the output voltage will be 0=Static Low or 1=Static High ROM=Y, EEPROM=N 0x0 = L 0x1 = H
5	OUT_1_P_CMOS_EN	R/W	0x0	OUT1P CMOS Enable. Setting this bit enables the positive terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=Y
4	OUT_1_N_CMOS_EN	R/W	0x0	OUT1N CMOS Enable. Setting this bit enables the negative terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=Y
3	OUT_1_P_INVERT_POLARITY	R/W	0x0	OUT1P CMOS Invert Polarity. Setting this bit inverts the polarity of the positive terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=N
2	OUT_1_N_INVERT_POLARITY	R/W	0x0	OUT1N CMOS Invert Polarity. Setting this bit inverts the polarity of the negative terminal of OUT1 for CMOS outputs. ROM=Y, EEPROM=N
1	OUT_1_P_FORCELOW	R/W	0x0	OUT1P CMOS Force Low. Setting this bit forces the positive terminal of OUT1 low. ROM=Y, EEPROM=N
0	OUT_1_N_FORCELOW	R/W	0x0	OUT1N CMOS Force Low. Setting this bit forces the negative terminal of OUT1 low. ROM=Y, EEPROM=N

1.556 R966 Register (Offset = 0x3C6) [Reset = 0x00]

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Table 1-558. R966 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_1_CONFIGURATION	R/W	0x0	OUT1 configuration. Selects from CH0 Bypass, CH1 Bypass, CHDIV0, CHDIV1, CH0/2 low-noise divide by two path, SYSREF, SYSREF + Analog Delay, or static DC H/L. ROM=Y, EEPROM=Y and N 0x0 = CH0/2 0x14 = CHDIV1 0x20 = SYSREF+ADLY 0x21 = SYSREF 0x22 = Static DC 0x28 = CHDIV0 0x40 = CH1 Bypass 0x80 = CH0 Bypass

1.557 R967 Register (Offset = 0x3C7) [Reset = 0x01]

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Table 1-559. R967 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	OUT_0_1_CMOS_OUT_VOLTAGE_SEL	R/W	0x0	CMOS LDO Voltage. Selects CMOS LDO voltage. ROM=Y, EEPROM=Y 0x0 = 1.8V 0x1 = 2.65V
0	OUT_0_1_CMOS_OUT_LDO_EN	R/W	0x1	CMOS LDO Enable. Enables LDO used for CMOS outputs. Must be enabled for CMOS mode. ROM=Y, EEPROM=Y

1.558 R968 Register (Offset = 0x3C8) [Reset = 0x00]

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Table 1-560. R968 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:1	OUT_0_1_ZDM_TDC_SEL	R/W	0x0	Select zero delay output to TDC's ROM=Y, EEPROM=N 0x0 = None 0x1 = TDC1 0x2 = TDC2 0x4 = TDC3
0	OUT_0_1_ZDM_EN	R/W	0x0	Enable the output from CH_DIV0_1 to be used as DPLL feedback input for zero delay mode ROM=Y, EEPROM=N

1.559 R969 Register (Offset = 0x3C9) [Reset = 0x33]

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Table 1-561. R969 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_0_1_DIV_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
5	OUT_0_1_DIV_SYNC_EN	R/W	0x1	OUT0_1 Divider Sync Enable. Enables synchronization of chandiv and div2 dividers for OUT0_1. ROM=Y, EEPROM=N

Table 1-561. R969 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	OUT_0_1_SR_DIV_SYNC_EN	R/W	0x1	OUT0_1 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT0_1. ROM=Y, EEPROM=N
3	OUT_0_1_CH0_CHAN_POL_SEL	R/W	0x0	OUT0_1 Ch0 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the Ch0 channel divider. ROM=Y, EEPROM=N
2	OUT_0_1_CH1_CHAN_POL_SEL	R/W	0x0	OUT0_1 Ch1 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the Ch1 channel divider. ROM=Y, EEPROM=N
1	OUT_0_1_CH0_DIV_EN	R/W	0x1	OUT0_1 Ch0 ChanDiv Enable. Enables the Ch0 channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y
0	OUT_0_1_CH1_DIV_EN	R/W	0x1	OUT0_1 Ch1 ChanDiv Enable. Enables the Ch1 channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.560 R972 Register (Offset = 0x3CC) [Reset = 0x00]

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Table 1-562. R972 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	OUT_0_1_CH0_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT0_1 Ch0 ChanDiv to SYSREF Input Clock Select. When set, the Ch0 channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N 0x0 = POS POL to SR_DIV 0x1 = NEG POL to SR_DIV
0	RESERVED	R/W	0x0	Reserved

1.561 R973 Register (Offset = 0x3CD) [Reset = 0x00]

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Table 1-563. R973 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	OUT_0_1_CLK_IN_FANOUT	R/W	0x0	OUT0_1 input clock fanout. Distributes the input clock to the channel dividers and the standalone divide-by-2s. ROM=Y, EEPROM=Y 0x0 = DISABLED 0x3 = IN1 to CHDIV1 0x4 = IN0 to SYSREF 0x7 = IN0 to SYSREF, IN1 to CHDIV1 0xC = IN0 to CHDIV0 0xF = IN0 to CHDIV0, IN1 to CHDIV1 0x10 = IN0 to CH0/2 (OUT0) 0x13 = IN0 to CH0/2 (OUT0), IN1 to CHDIV1 (OUT1) 0x14 = IN0 to CH0/2 (OUT0) and SYSREF (OUT1) 0x1C = IN0 to CH0/2 (OUT0) and CHDIV0 (OUT1) 0x20 = IN0 to CH0/2 (OUT1) 0x23 = IN0 to CH0/2 (OUT1), IN1 to CHDIV1 (OUT0) 0x24 = IN0 to CH0/2 (OUT1) and SYSREF (OUT0) 0x2C = IN0 to CH0/2 (OUT1) and CHDIV0 (OUT0) 0x30 = IN0 to CH0/2 (OUT0 and OUT1)
1:0	RESERVED	R	0x0	Reserved

1.562 R974 Register (Offset = 0x3CE) [Reset = 0x00]

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Table 1-564. R974 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH0_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 975

1.563 R975 Register (Offset = 0x3CF) [Reset = 0x00]

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Table 1-565. R975 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH0_CH_STATIC_OFFSET	R/W	0x0	CH0_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.564 R976 Register (Offset = 0x3D0) [Reset = 0x00]

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Table 1-566. R976 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH1_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 977

1.565 R977 Register (Offset = 0x3D1) [Reset = 0x00]

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Table 1-567. R977 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH1_CH_STATIC_OFFSET	R/W	0x0	CH1_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.566 R978 Register (Offset = 0x3D2) [Reset = 0x00]

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Table 1-568. R978 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH0_CH_DIV_11:8	R/W	0x0	See Register 979

1.567 R979 Register (Offset = 0x3D3) [Reset = 0x19]

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Table 1-569. R979 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH0_CH_DIV	R/W	0x19	OUT0_1 Ch0 Channel Divider (ChanDiv) Divide Value. ROM=Y, EEPROM=Y

1.568 R980 Register (Offset = 0x3D4) [Reset = 0x00]

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Table 1-570. R980 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_CH1_CH_DIV_11:8	R/W	0x0	See Register 981

1.569 R981 Register (Offset = 0x3D5) [Reset = 0x64]

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Table 1-571. R981 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_CH1_CH_DIV	R/W	0x64	OUT0_1 Ch1 Channel Divider (ChanDiv) Divide Value. ROM=Y, EEPROM=Y

1.570 R982 Register (Offset = 0x3D6) [Reset = 0x00]

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Table 1-572. R982 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_0_1_SR_ANA_DELAY	R/W	0x0	OUT0_1 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.571 R983 Register (Offset = 0x3D7) [Reset = 0x05]

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Table 1-573. R983 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_0_1_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT0_1 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_0_1_SR_ANA_DELAY_EN	R/W	0x0	OUT0_1 SYSREF Analog Delay Enable. ROM=Y, EEPROM=N
3	OUT_0_1_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT0_1 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N

Table 1-573. R983 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_0_1_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.572 R984 Register (Offset = 0x3D8) [Reset = 0x00]

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Table 1-574. R984 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_0_1_SR_DDLY	R/W	0x0	OUT0_1 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.573 R985 Register (Offset = 0x3D9) [Reset = 0x00]

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Table 1-575. R985 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_0_1_SR_DIV_19:16	R/W	0x0	See Register 987

1.574 R986 Register (Offset = 0x3DA) [Reset = 0x00]

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Table 1-576. R986 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV_15:8	R/W	0x0	See Register 987

1.575 R987 Register (Offset = 0x3DB) [Reset = 0xFA]

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Table 1-577. R987 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV	R/W	0xFA	OUT0_1 SYSREF Divide Value. ROM=Y, EEPROM=N

1.576 R988 Register (Offset = 0x3DC) [Reset = 0x00]

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Table 1-578. R988 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_0_1_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 989

1.577 R989 Register (Offset = 0x3DD) [Reset = 0x00]

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Table 1-579. R989 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_0_1_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_0_1_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.578 R990 Register (Offset = 0x3DE) [Reset = 0x00]

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Table 1-580. R990 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_0_1_SR_REQ_MODE	R/W	0x0	ROM=Y, EEPROM=N
6	OUT_0_1_SR_GPIO_EN	R/W	0x0	Enable SYSREF to digital for SYSREF request resampling, continuous SYSREF, 1-PPS GPIO output, 1-PPS phase validation. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
5	RESERVED	R/W	0x0	Reserved
4:2	OUT_0_1_PULSE_COUNT	R/W	0x0	OUT0_1 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
1:0	OUT_0_1_SR_MODE	R/W	0x0	OUT0_1 SYSREF Mode. Selects Pulser mode, Continuous mode, or None. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.579 R991 Register (Offset = 0x3DF) [Reset = 0x00]

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Table 1-581. R991 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5	OUT_0_1_SR_CH0_DIV_BYPASS	R/W	0x0	OUT0_1 cascaded SYSREF bypass mux. If set, bypasses CHDIV0 for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N 0x0 = ChanDiv input to SysRef 0x1 = Bypass ChanDiv
4:0	RESERVED	R/W	0x0	Reserved

1.580 R1024 Register (Offset = 0x400) [Reset = 0x4C]

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Table 1-582. R1024 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_2_EN	R/W	0x1	OUT2 Enable. ROM=Y, EEPROM=Y
5:3	OUT_2_VCM	R/W	0x1	Controls the differential output common mode voltage for OUT2 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_2_VOD	R/W	0x4	Controls the differential output voltage swing for OUT2 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.581 R1025 Register (Offset = 0x401) [Reset = 0x00]

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Table 1-583. R1025 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_2_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
2:0	OUT_2_CONFIGURATION	R/W	0x0	OUT2 configuration. ROM=Y, EEPROM=Y and N 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS

1.582 R1026 Register (Offset = 0x402) [Reset = 0x0F]

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Table 1-584. R1026 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_2_CHAN_POL_SEL	R/W	0x0	OUT2 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
6:5	OUT_2_CLK_MUX	R/W	0x0	OUT2 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=Y, EEPROM=Y 0x0 = PLL3 0x1 = PLL2 0x2 = PLL1_PRI
4	RESERVED	R/W	0x0	Reserved
3	OUT_2_DIV_EN	R/W	0x1	OUT2 ChanDiv Enable. Enables the channel divider. Note: SYSREF/ chandiv mode must be configured separately. ROM=Y, EEPROM=Y

Table 1-584. R1026 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_2_CH_MUX_SEL	R/W	0x7	OUT2 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1->BYPASS 0x7 = PLL1->CHDIV

1.583 R1027 Register (Offset = 0x403) [Reset = 0x08]

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Table 1-585. R1027 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_2_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_2_SYNC_EN	R/W	0x1	OUT2 ChanDiv Sync Enable. Enables synchronization of chandiv dividers for OUT2. ROM=Y, EEPROM=N
2:0	RESERVED	R/W	0x0	Reserved

1.584 R1028 Register (Offset = 0x404) [Reset = 0x00]

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Table 1-586. R1028 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_2_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1029

1.585 R1029 Register (Offset = 0x405) [Reset = 0x00]

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Table 1-587. R1029 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_2_CH_STATIC_OFFSET	R/W	0x0	OUT_2_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.586 R1030 Register (Offset = 0x406) [Reset = 0x00]

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Table 1-588. R1030 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_2_CH_DIV_11:8	R/W	0x0	See Register 1031

1.587 R1031 Register (Offset = 0x407) [Reset = 0x11]

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Table 1-589. R1031 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_2_CH_DIV	R/W	0x11	OUT2 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.588 R1056 Register (Offset = 0x420) [Reset = 0x4C]

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Table 1-590. R1056 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_3_EN	R/W	0x1	OUT3 Enable. ROM=Y, EEPROM=Y
5:3	OUT_3_VCM	R/W	0x1	Controls the differential output common mode voltage for OUT3 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_3_VOD	R/W	0x4	Controls the differential output voltage swing for OUT3 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.589 R1057 Register (Offset = 0x421) [Reset = 0x00]

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Table 1-591. R1057 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	OUT_3_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
2:0	OUT_3_CONFIGURATION	R/W	0x0	OUT3 configuration. ROM=Y, EEPROM=Y and N 0x2 = Static DC 0x3 = CHDIV 0x4 = BYPASS

1.590 R1058 Register (Offset = 0x422) [Reset = 0x0F]

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Table 1-592. R1058 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_3_CHAN_POL_SEL	R/W	0x0	OUT3 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
6:5	OUT_3_CLK_MUX	R/W	0x0	OUT3 Input Clock Select. Selects the input clock which will be used to drive the output. ROM=Y, EEPROM=Y 0x0 = PLL3 0x1 = PLL2 0x2 = PLL1_PRI
4	RESERVED	R/W	0x0	Reserved
3	OUT_3_DIV_EN	R/W	0x1	OUT3 ChanDiv Enable. Enables the channel divider. Note: SYSREF/ chandiv mode must be configured separately. ROM=Y, EEPROM=Y
2:0	OUT_3_CH_MUX_SEL	R/W	0x7	OUT3 Clock Enable. Bit 2, if set, passes the selected VCO1 clock (VCO1P or VCO1S), to the second stage of clock selection. Bit 1 and Bit0 enable the selected clock to drive the channel divider and the channel divider retimer respectively. ROM=Y, EEPROM=Y 0x0 = PLL2->BYPASS 0x3 = PLL2->CHDIV 0x4 = PLL1->BYPASS 0x7 = PLL1->CHDIV

1.591 R1059 Register (Offset = 0x423) [Reset = 0x08]

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Table 1-593. R1059 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OUT_3_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
3	OUT_3_SYNC_EN	R/W	0x1	OUT3 ChanDiv Sync Enable. Enables synchronization of chandiv dividers for OUT3. ROM=Y, EEPROM=N
2:0	RESERVED	R/W	0x0	Reserved

1.592 R1060 Register (Offset = 0x424) [Reset = 0x00]

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Table 1-594. R1060 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_3_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1061

1.593 R1061 Register (Offset = 0x425) [Reset = 0x00]

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Table 1-595. R1061 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_3_CH_STATIC_OFFSET	R/W	0x0	OUT_3_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.594 R1062 Register (Offset = 0x426) [Reset = 0x00]

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Table 1-596. R1062 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_3_CH_DIV_11:8	R/W	0x0	See Register 1063

1.595 R1063 Register (Offset = 0x427) [Reset = 0x11]

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Table 1-597. R1063 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_3_CH_DIV	R/W	0x11	OUT3 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.596 R1088 Register (Offset = 0x440) [Reset = 0x04]

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Table 1-598. R1088 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	OUT_4_5_SR_ANA_DLY_BIASTRIM	R/W	0x4	Channel Analog Delay Bias Trim ROM=N, EEPROM=Y

1.597 R1089 Register (Offset = 0x441) [Reset = 0x49]

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Table 1-599. R1089 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_4_EN	R/W	0x1	OUT4 Enable. ROM=Y, EEPROM=Y
5:3	OUT_4_VCM	R/W	0x1	Controls the differential output common mode voltage for OUT4 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved

Table 1-599. R1089 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OUT_4_VOD	R/W	0x1	Controls the differential output voltage swing for OUT4 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.598 R1090 Register (Offset = 0x442) [Reset = 0x00]

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Table 1-600. R1090 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_4_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_4_CONFIGURATION	R/W	0x0	OUT4 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.599 R1091 Register (Offset = 0x443) [Reset = 0x49]

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Table 1-601. R1091 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_5_EN	R/W	0x1	OUT5 Enable. ROM=Y, EEPROM=Y
5:3	OUT_5_VCM	R/W	0x1	Controls the differential output common mode voltage for OUT5 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_5_VOD	R/W	0x1	Controls the differential output voltage swing for OUT5 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.600 R1092 Register (Offset = 0x444) [Reset = 0x00]

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Table 1-602. R1092 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_5_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_5_CONFIGURATION	R/W	0x0	OUT5 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.601 R1093 Register (Offset = 0x445) [Reset = 0x31]

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Table 1-603. R1093 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5	OUT_4_5_DIV_SYNC_EN	R/W	0x1	OUT4_5 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT4_5. ROM=Y, EEPROM=N
4	OUT_4_5_SR_DIV_SYNC_EN	R/W	0x1	OUT4_5 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT4_5. ROM=Y, EEPROM=N
3:2	RESERVED	R/W	0x0	Reserved
1	OUT_4_5_CHAN_POL_SEL	R/W	0x0	OUT4_5 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_4_5_DIV_EN	R/W	0x1	OUT4_5 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.602 R1094 Register (Offset = 0x446) [Reset = 0x03]

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Table 1-604. R1094 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_4_5_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	OUT_4_5_ZDM_EN	R/W	0x0	OUT4_5 zero delay output enable ROM=Y, EEPROM=N
5	OUT_4_5_CLK_IN_SEL	R/W	0x0	OUT4_5 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_4_5_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT4_5 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-604. R1094 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_4_5_CH_MUX_SEL	R/W	0x3	OUT4_5 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT4, [3] -> Div2 to OUT5 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT4 0x5 = DIV2->OUT4, SYSREF->OUT5 0x7 = DIV2->OUT4, CHDIV->OUT5 0x8 = DIV2->OUT5 0x9 = SYSREF->OUT4, DIV2->OUT5 0xB = CHDIV->OUT4, DIV2->OUT5 0xC = DIV2->OUT4, DIV2->OUT5

1.603 R1095 Register (Offset = 0x447) [Reset = 0x00]

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Table 1-605. R1095 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1096

1.604 R1096 Register (Offset = 0x448) [Reset = 0x00]

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Table 1-606. R1096 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_CH_STATIC_OFFSET	R/W	0x0	OUT_4_5_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.605 R1097 Register (Offset = 0x449) [Reset = 0x00]

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Table 1-607. R1097 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_CH_DIV_11:8	R/W	0x0	See Register 1098

1.606 R1098 Register (Offset = 0x44A) [Reset = 0x03]

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Table 1-608. R1098 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_CH_DIV	R/W	0x3	OUT4_5 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.607 R1099 Register (Offset = 0x44B) [Reset = 0x00]

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Table 1-609. R1099 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_4_5_SR_ANA_DELAY	R/W	0x0	OUT4_5 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.608 R1100 Register (Offset = 0x44C) [Reset = 0x05]

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Table 1-610. R1100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_4_5_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT4_5 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_4_5_SR_ANA_DELAY_EN	R/W	0x0	OUT4_5 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_4_5_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT4_5 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_4_5_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.609 R1101 Register (Offset = 0x44D) [Reset = 0x00]

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Table 1-611. R1101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_4_5_SR_DDLY	R/W	0x0	OUT4_5 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.610 R1102 Register (Offset = 0x44E) [Reset = 0x00]

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Table 1-612. R1102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_4_5_SR_DIV_19:16	R/W	0x0	See Register 1104

1.611 R1103 Register (Offset = 0x44F) [Reset = 0x00]

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Table 1-613. R1103 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV_15:8	R/W	0x0	See Register 1104

1.612 R1104 Register (Offset = 0x450) [Reset = 0xFA]

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Table 1-614. R1104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV	R/W	0xFA	OUT4_5 SYSREF Divide Value. ROM=Y, EEPROM=N

1.613 R1105 Register (Offset = 0x451) [Reset = 0x00]

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Table 1-615. R1105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_4_5_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1106

1.614 R1106 Register (Offset = 0x452) [Reset = 0x00]

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Table 1-616. R1106 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_4_5_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_4_5_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.615 R1107 Register (Offset = 0x453) [Reset = 0x00]

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Table 1-617. R1107 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_4_5_SR_REQ_MODE	R/W	0x0	OUT4_5 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_4_5_PULSE_COUNT	R/W	0x0	OUT4_5 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N

Table 1-617. R1107 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OUT_4_5_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_4_5_SR_MODE	R/W	0x0	OUT4_5 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in Pulse Mode. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.616 R1108 Register (Offset = 0x454) [Reset = 0x00]

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Table 1-618. R1108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R/W	0x0	Reserved
4	OUT_4_5_SR_CH_DIV_BYPASS	R/W	0x0	OUT4_5 cascaded SYSREF bypass mux. If set, bypasses OUT4_5 channel divider for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N
3:0	RESERVED	R/W	0x0	Reserved

1.617 R1121 Register (Offset = 0x461) [Reset = 0x4E]

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Table 1-619. R1121 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_6_EN	R/W	0x1	OUT6 Enable. ROM=Y, EEPROM=Y
5:3	OUT_6_VCM	R/W	0x1	Controls the differential output common mode voltage for OUT6 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_6_VOD	R/W	0x6	Controls the differential output voltage swing for OUT6 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.618 R1122 Register (Offset = 0x462) [Reset = 0x00]

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Table 1-620. R1122 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_6_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_6_CONFIGURATION	R/W	0x0	OUT6 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.619 R1123 Register (Offset = 0x463) [Reset = 0x4E]

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Table 1-621. R1123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_7_EN	R/W	0x1	OUT7 Enable. ROM=Y, EEPROM=Y
5:3	OUT_7_VCM	R/W	0x1	Controls the differential output common mode voltage for OUT7 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_7_VOD	R/W	0x6	Controls the differential output voltage swing for OUT7 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.620 R1124 Register (Offset = 0x464) [Reset = 0x00]

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Table 1-622. R1124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_7_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved

Table 1-622. R1124 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	OUT_7_CONFIGURATION	R/W	0x0	OUT7 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.621 R1125 Register (Offset = 0x465) [Reset = 0x31]

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Table 1-623. R1125 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5	OUT_6_7_DIV_SYNC_EN	R/W	0x1	OUT6_7 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT6_7. ROM=Y, EEPROM=N
4	OUT_6_7_SR_DIV_SYNC_EN	R/W	0x1	OUT6_7 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT6_7. ROM=Y, EEPROM=N
3:2	RESERVED	R/W	0x0	Reserved
1	OUT_6_7_CHAN_POL_SEL	R/W	0x0	OUT6_7 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_6_7_DIV_EN	R/W	0x1	OUT6_7 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.622 R1126 Register (Offset = 0x466) [Reset = 0x03]

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Table 1-624. R1126 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_6_7_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R/W	0x0	Reserved
5	OUT_6_7_CLK_IN_SEL	R/W	0x0	OUT6_7 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_6_7_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT6_7 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-624. R1126 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_6_7_CH_MUX_SEL	R/W	0x3	OUT6_7 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT6, [3] -> Div2 to OUT7 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT6 0x5 = DIV2->OUT6, SYSREF->OUT7 0x7 = DIV2->OUT6, CHDIV->OUT7 0x8 = DIV2->OUT7 0x9 = SYSREF->OUT6, DIV2->OUT7 0xB = CHDIV->OUT6, DIV2->OUT7 0xC = DIV2->OUT6, DIV2->OUT7

1.623 R1127 Register (Offset = 0x467) [Reset = 0x00]

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Table 1-625. R1127 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1128

1.624 R1128 Register (Offset = 0x468) [Reset = 0x00]

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Table 1-626. R1128 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_CH_STATIC_OFFSET	R/W	0x0	OUT_6_7_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.625 R1129 Register (Offset = 0x469) [Reset = 0x00]

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Table 1-627. R1129 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_CH_DIV_11:8	R/W	0x0	See Register 1130

1.626 R1130 Register (Offset = 0x46A) [Reset = 0x03]

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Table 1-628. R1130 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_CH_DIV	R/W	0x3	OUT6_7 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.627 R1131 Register (Offset = 0x46B) [Reset = 0x00]

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Table 1-629. R1131 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_6_7_SR_ANA_DELAY	R/W	0x0	OUT6_7 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.628 R1132 Register (Offset = 0x46C) [Reset = 0x05]

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Table 1-630. R1132 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_6_7_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT6_7 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_6_7_SR_ANA_DELAY_EN	R/W	0x0	OUT6_7 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_6_7_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT6_7 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_6_7_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.629 R1133 Register (Offset = 0x46D) [Reset = 0x00]

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Table 1-631. R1133 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_6_7_SR_DDLY	R/W	0x0	OUT6_7 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.630 R1134 Register (Offset = 0x46E) [Reset = 0x00]

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Table 1-632. R1134 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_6_7_SR_DIV_19:16	R/W	0x0	See Register 1136

1.631 R1135 Register (Offset = 0x46F) [Reset = 0x00]

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Table 1-633. R1135 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV_15:8	R/W	0x0	See Register 1136

1.632 R1136 Register (Offset = 0x470) [Reset = 0xFA]

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Table 1-634. R1136 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV	R/W	0xFA	OUT6_7 SYSREF Divide Value. ROM=Y, EEPROM=N

1.633 R1137 Register (Offset = 0x471) [Reset = 0x00]

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Table 1-635. R1137 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_6_7_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1138

1.634 R1138 Register (Offset = 0x472) [Reset = 0x00]

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Table 1-636. R1138 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_6_7_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_6_7_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.635 R1139 Register (Offset = 0x473) [Reset = 0x00]

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Table 1-637. R1139 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_6_7_SR_REQ_MODE	R/W	0x0	OUT6_7 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_6_7_PULSE_COUNT	R/W	0x0	OUT6_7 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N

Table 1-637. R1139 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OUT_6_7_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_6_7_SR_MODE	R/W	0x0	OUT6_7 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.636 R1140 Register (Offset = 0x474) [Reset = 0x00]

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Table 1-638. R1140 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R/W	0x0	Reserved
4	OUT_6_7_SR_CH_DIV_BYPASS	R/W	0x0	OUT6_7 cascaded SYSREF bypass mux. If set, bypasses OUT6_7 channel divider for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N
3:0	RESERVED	R/W	0x0	Reserved

1.637 R1153 Register (Offset = 0x481) [Reset = 0x73]

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Table 1-639. R1153 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_8_EN	R/W	0x1	OUT8 Enable. ROM=Y, EEPROM=Y
5:3	OUT_8_VCM	R/W	0x6	Controls the differential output common mode voltage for OUT8 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_8_VOD	R/W	0x3	Controls the differential output voltage swing for OUT8 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.638 R1154 Register (Offset = 0x482) [Reset = 0x00]

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Table 1-640. R1154 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_8_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_8_CONFIGURATION	R/W	0x0	OUT8 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.639 R1155 Register (Offset = 0x483) [Reset = 0x73]

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Table 1-641. R1155 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_9_EN	R/W	0x1	OUT9 Enable. ROM=Y, EEPROM=Y
5:3	OUT_9_VCM	R/W	0x6	Controls the differential output common mode voltage for OUT9 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_9_VOD	R/W	0x3	Controls the differential output voltage swing for OUT9 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.640 R1156 Register (Offset = 0x484) [Reset = 0x00]

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Table 1-642. R1156 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_9_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved

Table 1-642. R1156 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	OUT_9_CONFIGURATION	R/W	0x0	OUT9 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.641 R1157 Register (Offset = 0x485) [Reset = 0x31]

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Table 1-643. R1157 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5	OUT_8_9_DIV_SYNC_EN	R/W	0x1	OUT8_9 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT8_9. ROM=Y, EEPROM=N
4	OUT_8_9_SR_DIV_SYNC_EN	R/W	0x1	OUT8_9 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT8_9. ROM=Y, EEPROM=N
3:2	RESERVED	R/W	0x0	Reserved
1	OUT_8_9_CHAN_POL_SEL	R/W	0x0	OUT8_9 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_8_9_DIV_EN	R/W	0x1	OUT8_9 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.642 R1158 Register (Offset = 0x486) [Reset = 0x23]

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Table 1-644. R1158 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_8_9_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R/W	0x0	Reserved
5	OUT_8_9_CLK_IN_SEL	R/W	0x1	OUT8_9 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_8_9_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT8_9 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N

Table 1-644. R1158 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	OUT_8_9_CH_MUX_SEL	R/W	0x3	OUT8_9 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT8, [3] -> Div2 to OUT9 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT8 0x5 = DIV2->OUT8, SYSREF->OUT9 0x7 = DIV2->OUT8, CHDIV->OUT9 0x8 = DIV2->OUT9 0x9 = SYSREF->OUT8, DIV2->OUT9 0xB = CHDIV->OUT8, DIV2->OUT9 0xC = DIV2->OUT8, DIV2->OUT9

1.643 R1159 Register (Offset = 0x487) [Reset = 0x00]

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Table 1-645. R1159 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1160

1.644 R1160 Register (Offset = 0x488) [Reset = 0x00]

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Table 1-646. R1160 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_CH_STATIC_OFFSET	R/W	0x0	OUT_8_9_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.645 R1161 Register (Offset = 0x489) [Reset = 0x00]

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Table 1-647. R1161 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_CH_DIV_11:8	R/W	0x0	See Register 1162

1.646 R1162 Register (Offset = 0x48A) [Reset = 0x10]

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Table 1-648. R1162 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_CH_DIV	R/W	0x10	OUT8_9 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.647 R1163 Register (Offset = 0x48B) [Reset = 0x00]

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Table 1-649. R1163 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_8_9_SR_ANA_DELAY	R/W	0x0	OUT8_9 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.648 R1164 Register (Offset = 0x48C) [Reset = 0x05]

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Table 1-650. R1164 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_8_9_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT8_9 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_8_9_SR_ANA_DELAY_EN	R/W	0x0	OUT8_9 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N
3	OUT_8_9_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT8_9 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_8_9_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.649 R1165 Register (Offset = 0x48D) [Reset = 0x00]

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Table 1-651. R1165 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_8_9_SR_DDLY	R/W	0x0	OUT8_9 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.650 R1166 Register (Offset = 0x48E) [Reset = 0x00]

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Table 1-652. R1166 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_8_9_SR_DIV_19:16	R/W	0x0	See Register 1168

1.651 R1167 Register (Offset = 0x48F) [Reset = 0x00]

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Table 1-653. R1167 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV_15:8	R/W	0x0	See Register 1168

1.652 R1168 Register (Offset = 0x490) [Reset = 0xFA]

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Table 1-654. R1168 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV	R/W	0xFA	OUT8_9 SYSREF Divide Value. ROM=Y, EEPROM=N

1.653 R1169 Register (Offset = 0x491) [Reset = 0x00]

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Table 1-655. R1169 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_8_9_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1170

1.654 R1170 Register (Offset = 0x492) [Reset = 0x00]

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Table 1-656. R1170 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_8_9_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_8_9_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.655 R1171 Register (Offset = 0x493) [Reset = 0x00]

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Table 1-657. R1171 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_8_9_SR_REQ_MODE	R/W	0x0	OUT8_9 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_8_9_PULSE_COUNT	R/W	0x0	OUT8_9 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N

Table 1-657. R1171 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OUT_8_9_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_8_9_SR_MODE	R/W	0x0	OUT8_9 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.656 R1185 Register (Offset = 0x4A1) [Reset = 0x73]

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Table 1-658. R1185 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_10_EN	R/W	0x1	OUT10 Enable. ROM=Y, EEPROM=Y
5:3	OUT_10_VCM	R/W	0x6	Controls the differential output common mode voltage for OUT10 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_10_VOD	R/W	0x3	Controls the differential output voltage swing for OUT10 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.657 R1186 Register (Offset = 0x4A2) [Reset = 0x00]

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Table 1-659. R1186 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_10_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_10_CONFIGURATION	R/W	0x0	OUT10 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.658 R1187 Register (Offset = 0x4A3) [Reset = 0x73]

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Table 1-660. R1187 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_11_EN	R/W	0x1	OUT11 Enable. ROM=Y, EEPROM=Y
5:3	OUT_11_VCM	R/W	0x6	Controls the differential output common mode voltage for OUT11 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_11_VOD	R/W	0x3	Controls the differential output voltage swing for OUT11 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.659 R1188 Register (Offset = 0x4A4) [Reset = 0x00]

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Table 1-661. R1188 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_11_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_11_CONFIGURATION	R/W	0x0	OUT11 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.660 R1189 Register (Offset = 0x4A5) [Reset = 0x31]

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Table 1-662. R1189 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5	OUT_10_11_DIV_SYNC_EN	R/W	0x1	OUT10_11 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT10_11. ROM=Y, EEPROM=N
4	OUT_10_11_SR_DIV_SYNC_EN	R/W	0x1	OUT10_11 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT10_11. ROM=Y, EEPROM=N

Table 1-662. R1189 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	RESERVED	R/W	0x0	Reserved
1	OUT_10_11_CHAN_POL_SEL	R/W	0x0	OUT10_11 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_10_11_DIV_EN	R/W	0x1	OUT10_11 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.661 R1190 Register (Offset = 0x4A6) [Reset = 0x23]

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Table 1-663. R1190 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_10_11_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	OUT_10_11_ZDM_EN	R/W	0x0	OUT10_11 zero delay output enable. ROM=Y, EEPROM=N
5	OUT_10_11_CLK_IN_SEL	R/W	0x1	OUT10_11 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_10_11_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT10_11 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N
3:0	OUT_10_11_CH_MUX_SEL	R/W	0x3	OUT10_11 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT10, [3] -> Div2 to OUT11 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT10 0x5 = DIV2->OUT10, SYSREF->OUT11 0x7 = DIV2->OUT10, CHDIV->OUT11 0x8 = DIV2->OUT11 0x9 = SYSREF->OUT10, DIV2->OUT11 0xB = CHDIV->OUT10, DIV2->OUT11 0xC = DIV2->OUT10, DIV2->OUT11

1.662 R1191 Register (Offset = 0x4A7) [Reset = 0x00]

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Table 1-664. R1191 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1192

1.663 R1192 Register (Offset = 0x4A8) [Reset = 0x00]

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Table 1-665. R1192 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_CH_STATIC_OFFSET	R/W	0x0	OUT_10_11_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.664 R1193 Register (Offset = 0x4A9) [Reset = 0x00]

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Table 1-666. R1193 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_CH_DIV_11:8	R/W	0x0	See Register 1194

1.665 R1194 Register (Offset = 0x4AA) [Reset = 0x10]

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Table 1-667. R1194 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_CH_DIV	R/W	0x10	OUT10_11 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.666 R1195 Register (Offset = 0x4AB) [Reset = 0x00]

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Table 1-668. R1195 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_10_11_SR_ANA_DELAY	R/W	0x0	OUT10_11 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.667 R1196 Register (Offset = 0x4AC) [Reset = 0x05]

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Table 1-669. R1196 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_10_11_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT10_11 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_10_11_SR_ANA_DELAY_EN	R/W	0x0	OUT10_11 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N

Table 1-669. R1196 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_10_11_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT10_11 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_10_11_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.668 R1197 Register (Offset = 0x4AD) [Reset = 0x00]

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Table 1-670. R1197 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_10_11_SR_DDLY	R/W	0x0	OUT10_11 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.669 R1198 Register (Offset = 0x4AE) [Reset = 0x00]

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Table 1-671. R1198 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_10_11_SR_DIV_19:16	R/W	0x0	See Register 1200

1.670 R1199 Register (Offset = 0x4AF) [Reset = 0x00]

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Table 1-672. R1199 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV_15:8	R/W	0x0	See Register 1200

1.671 R1200 Register (Offset = 0x4B0) [Reset = 0xFA]

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Table 1-673. R1200 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV	R/W	0xFA	OUT10_11 SYSREF Divide Value. ROM=Y, EEPROM=N

1.672 R1201 Register (Offset = 0x4B1) [Reset = 0x00]

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Table 1-674. R1201 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_10_11_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1202

1.673 R1202 Register (Offset = 0x4B2) [Reset = 0x00]

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Table 1-675. R1202 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_10_11_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_10_11_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.674 R1203 Register (Offset = 0x4B3) [Reset = 0x00]

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Table 1-676. R1203 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_10_11_SR_REQ_MODE	R/W	0x0	OUT10_11 SYSREF Mute Enable ROM=Y, EEPROM=N
5:3	OUT_10_11_PULSE_COUNT	R/W	0x0	OUT10_11 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_10_11_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_10_11_SR_MODE	R/W	0x0	OUT10_11 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.675 R1204 Register (Offset = 0x4B4) [Reset = 0x00]

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Table 1-677. R1204 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-677. R1204 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	RESERVED	R/W	0x0	Reserved
4	OUT_10_11_SR_CH_DIV_BYPASS	R/W	0x0	OUT10_11 cascaded SYSREF bypass mux. If set, bypasses OUT10_11 channel divider for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N
3:0	RESERVED	R/W	0x0	Reserved

1.676 R1217 Register (Offset = 0x4C1) [Reset = 0x49]

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Table 1-678. R1217 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_12_EN	R/W	0x1	OUT12 Enable. ROM=Y, EEPROM=Y
5:3	OUT_12_VCM	R/W	0x1	Controls the differential output common mode voltage for OUT12 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_12_VOD	R/W	0x1	Controls the differential output voltage swing for OUT12 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.677 R1218 Register (Offset = 0x4C2) [Reset = 0x00]

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Table 1-679. R1218 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_12_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_12_CONFIGURATION	R/W	0x0	OUT12 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.678 R1219 Register (Offset = 0x4C3) [Reset = 0x4E]

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Table 1-680. R1219 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_13_EN	R/W	0x1	OUT13 Enable. ROM=Y, EEPROM=Y
5:3	OUT_13_VCM	R/W	0x1	Controls the differential output common mode voltage for OUT13 ROM=Y, EEPROM=Y 0x0 = Reserved 0x1 = Setting 1 0x2 = Setting 2 0x3 = Reserved 0x4 = Setting 3 0x5 = Reserved 0x6 = Setting 2+3 0x7 = Reserved
2:0	OUT_13_VOD	R/W	0x6	Controls the differential output voltage swing for OUT13 ROM=Y, EEPROM=Y 0x0 = 400 mV 0x1 = 500 mV 0x2 = 600 mV 0x3 = 700 mV 0x4 = 800 mV 0x5 = 900 mV 0x6 = 1000 mV 0x7 = HCSL (750 mV)

1.679 R1220 Register (Offset = 0x4C4) [Reset = 0x00]

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Table 1-681. R1220 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_13_CAP_EN	R/W	0x0	ROM=Y, EEPROM=N
5	RESERVED	R	0x0	Reserved
4:0	OUT_13_CONFIGURATION	R/W	0x0	OUT13 configuration. ROM=Y, EEPROM=Y and N 0x0 = CH/2 0x8 = SYSREF+ADLY 0x9 = SYSREF 0xA = Static DC 0xC = CHDIV 0x10 = BYPASS

1.680 R1221 Register (Offset = 0x4C5) [Reset = 0x31]

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Table 1-682. R1221 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5	OUT_12_13_DIV_SYNC_EN	R/W	0x1	OUT12_13 Divider Sync Enable. Enables synchronization of chandiv dividers for OUT12_13. ROM=Y, EEPROM=N
4	OUT_12_13_SR_DIV_SYNC_EN	R/W	0x1	OUT12_13 SYSREF Divider Sync Enable. Enables synchronization of SYSREF dividers for OUT12_13. ROM=Y, EEPROM=N

Table 1-682. R1221 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	RESERVED	R/W	0x0	Reserved
1	OUT_12_13_CHAN_POL_SEL	R/W	0x0	OUT12_13 ChanDiv Polarity Select. When cleared, this bit inverts the polarity of the input to the channel divider. ROM=Y, EEPROM=N
0	OUT_12_13_DIV_EN	R/W	0x1	OUT12_13 ChanDiv Enable. Enables the channel divider. Note: SYSREF/chandiv mode must be configured separately. ROM=Y, EEPROM=Y

1.681 R1222 Register (Offset = 0x4C6) [Reset = 0x23]

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Table 1-683. R1222 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_12_13_MUTE_EN	R/W	0x0	Mute enable. ROM=Y, EEPROM=N
6	RESERVED	R/W	0x0	Reserved
5	OUT_12_13_CLK_IN_SEL	R/W	0x1	OUT12_13 Input Clock Select. Selects the input clock which will be used to drive the output: 0 = VCO2, 1 = VCO3 ROM=Y, EEPROM=Y 0x0 = PLL2 0x1 = PLL3
4	OUT_12_13_CH_DIV_SR_MUX_CLK_SEL	R/W	0x0	OUT12_13 ChanDiv to SYSREF Clock Select. When set, the channel divider output is inverted before being fed to the SYSREF. ROM=Y, EEPROM=N
3:0	OUT_12_13_CH_MUX_SEL	R/W	0x3	OUT12_13 Input Clock Enable. Enables the selected clock to various inputs: [0] -> ChanDiv, [1] -> ChanDiv Retimer, [2] -> Div2 to OUT12, [3] -> Div2 to OUT13 ROM=Y, EEPROM=Y 0x0 = OFF 0x1 = SYSREF 0x3 = CHDIV 0x4 = DIV2->OUT12 0x5 = DIV2->OUT12, SYSREF->OUT13 0x7 = DIV2->OUT12, CHDIV->OUT13 0x8 = DIV2->OUT13 0x9 = SYSREF->OUT12, DIV2->OUT13 0xB = CHDIV->OUT12, DIV2->OUT13 0xC = DIV2->OUT12, DIV2->OUT13

1.682 R1223 Register (Offset = 0x4C7) [Reset = 0x00]

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Table 1-684. R1223 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_CH_STATIC_OFFSET_11:8	R/W	0x0	See Register 1224

1.683 R1224 Register (Offset = 0x4C8) [Reset = 0x00]

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Table 1-685. R1224 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_CH_STATIC_OFFSET	R/W	0x0	OUT_12_13_CH_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization. Lower 8 bits are stored in EEPROM. ROM=Y, EEPROM=Y

1.684 R1225 Register (Offset = 0x4C9) [Reset = 0x00]

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Table 1-686. R1225 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_CH_DIV_11:8	R/W	0x0	See Register 1226

1.685 R1226 Register (Offset = 0x4CA) [Reset = 0x08]

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Table 1-687. R1226 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_CH_DIV	R/W	0x8	OUT12_13 ChanDiv Divide Value. ROM=Y, EEPROM=Y

1.686 R1227 Register (Offset = 0x4CB) [Reset = 0x00]

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Table 1-688. R1227 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_12_13_SR_ANA_DELAY	R/W	0x0	OUT12_13 SYSREF Analog Delay. Specified here in multiples of one delay step duration. ROM=Y, EEPROM=N

1.687 R1228 Register (Offset = 0x4CC) [Reset = 0x05]

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Table 1-689. R1228 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	OUT_12_13_SR_ANA_DELAY_DIV2_SEL	R/W	0x0	OUT12_13 SYSREF Analog Delay Div By 2 Select. Divides the incoming clock by 2 to double the delay step size. Useful for increasing analog delay range, given high incoming clock frequencies. ROM=Y, EEPROM=N
4	OUT_12_13_SR_ANA_DELAY_EN	R/W	0x0	OUT12_13 SYSREF Analog Delay Enable. Enables the analog delay generator. Set to a 0 to save power if analog delay generator is not needed. ROM=Y, EEPROM=N

Table 1-689. R1228 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT_12_13_SR_ANA_DELAY_SMALL_STEP_EN	R/W	0x0	OUT12_13 SYSREF Analog Delay Small Step Enable. If set to 1, the analog delay generator will use both rising and falling edges of the incoming clock to halve delay step size. Useful for when large pre-divider values have been used. ROM=Y, EEPROM=N
2:0	OUT_12_13_SR_ANA_DELAY_RANGE	R/W	0x5	Analog delay range is set according to the period entering the SYSREF analog delay block. The period can be calculated as (OUT_x_y_SR_ANA_DELAY_DIV2_SEL + 1) / (OUT_x_y_SR_ANA_DELAY_SMALL_STEP_EN + 1) / VCO post divider frequency. Calculated range must fall between 333 ps and 1050 ps. ROM=Y, EEPROM=N 0x0 = Reserved 0x1 = Reserved 0x2 = 333 ps to 450 ps 0x3 = > 450 ps to 600 ps 0x4 = > 600 ps to 750 ps 0x5 = > 750 ps to 1050 ps 0x6 = Reserved 0x7 = Reserved

1.688 R1229 Register (Offset = 0x4CD) [Reset = 0x00]

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Table 1-690. R1229 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	OUT_12_13_SR_DDLY	R/W	0x0	OUT12_13 SYSREF Digital Delay Value. Measured in VCO half-cycles. ROM=Y, EEPROM=N

1.689 R1230 Register (Offset = 0x4CE) [Reset = 0x00]

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Table 1-691. R1230 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	OUT_12_13_SR_DIV_19:16	R/W	0x0	See Register 1232

1.690 R1231 Register (Offset = 0x4CF) [Reset = 0x00]

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Table 1-692. R1231 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV_15:8	R/W	0x0	See Register 1232

1.691 R1232 Register (Offset = 0x4D0) [Reset = 0xFA]

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Table 1-693. R1232 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV	R/W	0xFA	OUT12_13 SYSREF Divide Value. ROM=Y, EEPROM=N

1.692 R1233 Register (Offset = 0x4D1) [Reset = 0x00]

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Table 1-694. R1233 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	OUT_12_13_SR_DIV_STATIC_OFFSET_14:8	R/W	0x0	See Register 1234

1.693 R1234 Register (Offset = 0x4D2) [Reset = 0x00]

Return to the Summary Table.

Table 1-695. R1234 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT_12_13_SR_DIV_STATIC_OFFSET	R/W	0x0	OUT_12_13_SR_DIV static digital delay value. Delays divider start by specified number of full clock cycles of divider input. This results in specified digital delay upon divider synchronization ROM=Y, EEPROM=N

1.694 R1235 Register (Offset = 0x4D3) [Reset = 0x00]

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Table 1-696. R1235 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	OUT_12_13_SR_REQ_MODE	R/W	0x0	OUT12_13 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
5:3	OUT_12_13_PULSE_COUNT	R/W	0x0	OUT12_13 SYSREF Pulse Count. The number of SYSREF pulses which will be generated by a SYSREF request. ROM=Y, EEPROM=N
2	OUT_12_13_SR_GPIO_EN	R/W	0x0	Enables SYSREF to digital for SYSREF request resampling, continuous SYSREF, or 1-PPS GPIO output. Only one OUT_x_y_SR_GPIO_EN should be enabled at a time. ROM=Y, EEPROM=N
1:0	OUT_12_13_SR_MODE	R/W	0x0	OUT12_13 SYSREF Mode. When this bit is set, the SYSREF operates in Continuous Mode. When cleared, the SYSREF operates in PULSE MODE. ROM=Y, EEPROM=N 0x0 = None 0x1 = Continuous 0x2 = Pulser

1.695 R1236 Register (Offset = 0x4D4) [Reset = 0x00]

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Table 1-697. R1236 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-697. R1236 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	RESERVED	R/W	0x0	Reserved
4	OUT_12_13_SR_CH_DIV_BYPASS	R/W	0x0	OUT12_13 cascaded SYSREF bypass mux. If set, bypasses OUT12_13 channel divider for the SYSREF input clock. This is useful for minimizing the step size of the digital delay adjustments on the SYSREF clock. ROM=Y, EEPROM=N
3:0	RESERVED	R/W	0x0	Reserved

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2022) to Revision A (September 2022)	Page
• Updated device registers for production-data release	1

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265