LMX2581EVM

User's Guide

Literature Number: SNAU136C
November 2012–Revised November 2013

LMX2581EVM User's Guide

The Texas Instruments LMX2581EVM evaluation module (EVM) helps designers evaluate the operation and performance of the LMX2581 Wideband Frequency Synthesizer. The EVM contains one Frequency Synthesizer.

Converter: U1

IC: LMX2581

Package: LQA32A

Topic **Page**

1 Setup

1.1 Input and Output Connector Description

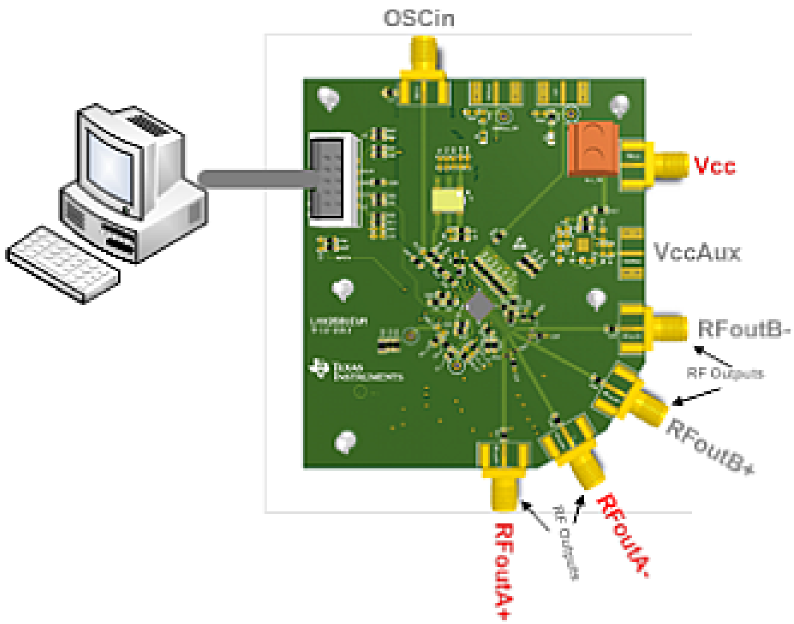


Figure 1. Evaluation Board Setup

Table 1. Inputs and Outputs

Output Name(s)	Input/Output	Required?	Function
RFoutA+/RFoutA-RFoutB+/RFoutB	Output	Required	These are two differential outputs. Connect any of the four outputs to a spectrum analyzer or phase noise analyzer. It is recommended to put a 50 ohm terminator for the unused side of the differential output. Failure to do so will degrade performance, especially output power and harmonics. The Agilent E5052A was used for these instructions.
V CC	Input	Required	Connect to a 3.3 V Power Supply. Ensure the current limit is set above 300 mA.
V CC Aux	Input	Optional	This gives the option to supply power to an external VCO.
Programming Interface	Input	Required	Connect the board to a PC using the provided cable.
OSCin	Input	Optional	The on-board 100 MHz XO has been enabled. To disable the XO and utilize the OSCin port move R13 to R12 and disconnect R4 (removing power from the XO).

1.2 Installing the EVM Software

Go to http://www.ti.com/tool/codeloader and download and run the most current software.

1.3 Loop Filter Values and Configuration Information

Table 2. Loop Filter values and Configuration

Category	Parameter	Value
Configuration	OSCin Frequency (MHz)	100 MHz
	Phase Detector Frequency (MHz)	20 MHz
	VCO Frequency	1850 to 3760 MHz
	Charge Pump Gain	2400 µA
VCO Gain	VCO Core 1	15 to 25 MHz/V
	VCO Core 2	18 to 32 MHz/V
	VCO Core 3	23 to 40 MHz/V
	VCO Core 4	26 to 46 MHz/V
Loop Filter Components	C1_LF	1.8 nF
	C2_LF	56 nF
	C3_LF	Open
	C4_LF	3.3 nF
	R2_LF	390 Ω
	R3_LF	270 Ω
	R4_LF	0
Loop Filter Characteristics	Loop Bandwidth	28.7 kHz
	Phase Margin	49.7°

Note that C4_LF is placed and C3_LF is left off because C4_LF is closer to the Vtune input. It is recommended that the capacitor next to the VCO be at least 3.3 nF for optimal VCO phase noise. If this constraint is violated, then there can be some degradation in the VCO phase noise in the 200kHz to 1 MHz region, depending on how much smaller than 3.3 nF this capacitor is.

1.4 Burning in the Crystal Oscillator

To get the best stability and phase noise from this XO, it is recommended to let the board run for several in order burn in the crystal oscillator.

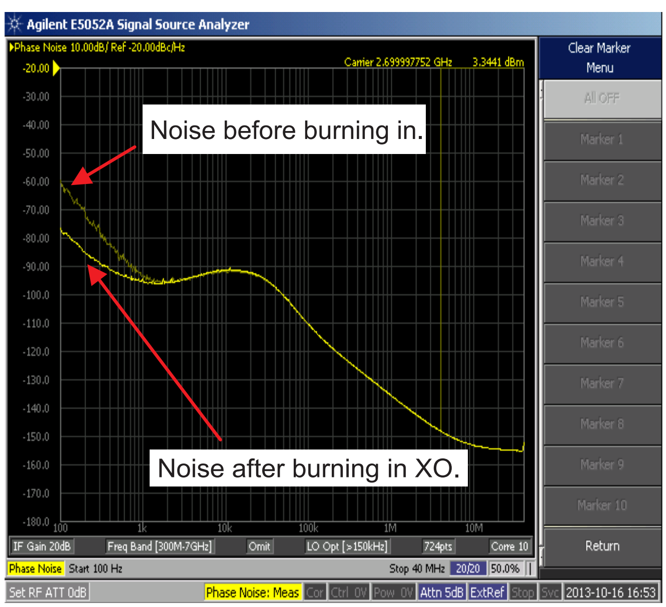


Figure 2. Impact of Burning in the XO

2 Using the EVM Software

2.1 Main Setup and Default Mode

NOTE: To restore the device to its default settings at any time, load the default mode from the “Modes” menu.

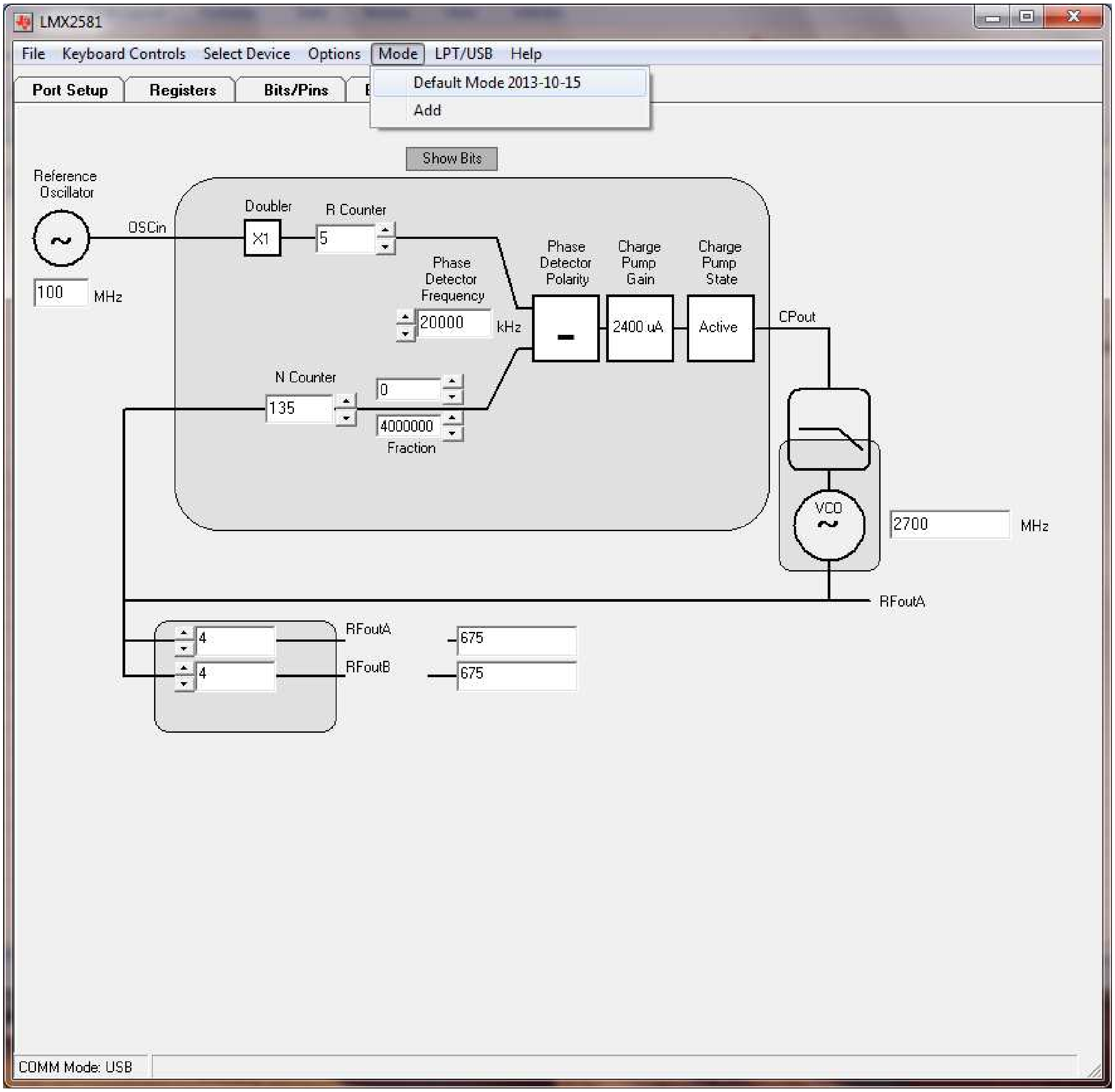


Figure 3. Loading Default Mode for the Main Configuration Screen

2.2 Loading the Device

To load the settings for the first time, you can either load this from the main menu as shown above or press <CTRL>+L. When the frequency or programmable bit settings are changed, CodeLoader will change the register associated with that programmable bit or change, but not all the registers.

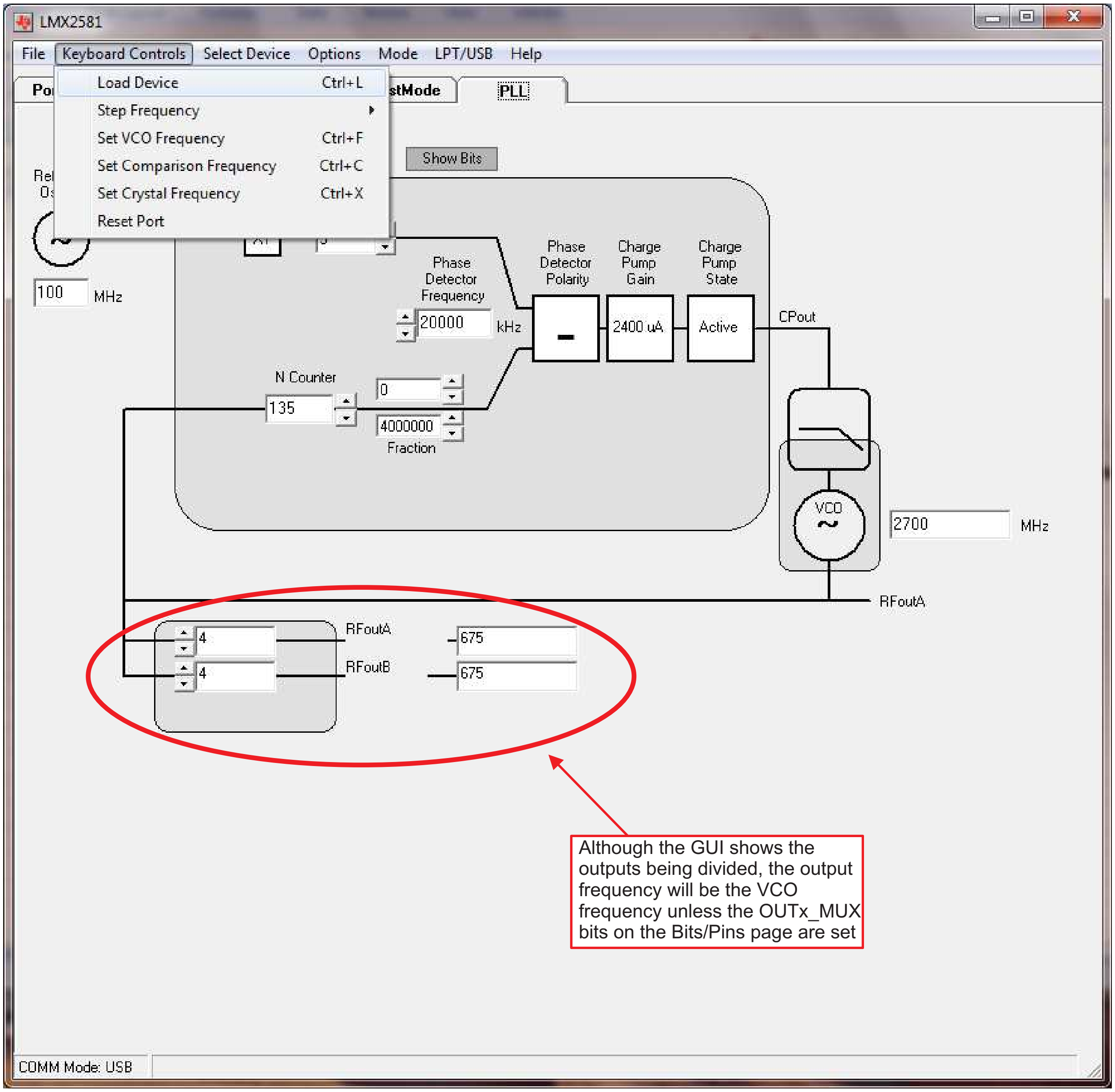


Figure 4. Loading the device

2.3 Port Setup

On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered. CodeLoader does NOT auto detect the correct settings for this. Also note that the BUFEN pin does not work with the USB2ANY board because pin location 5 is reserved for other purposes. Be aware that the board has been revised and the port setup has changed.

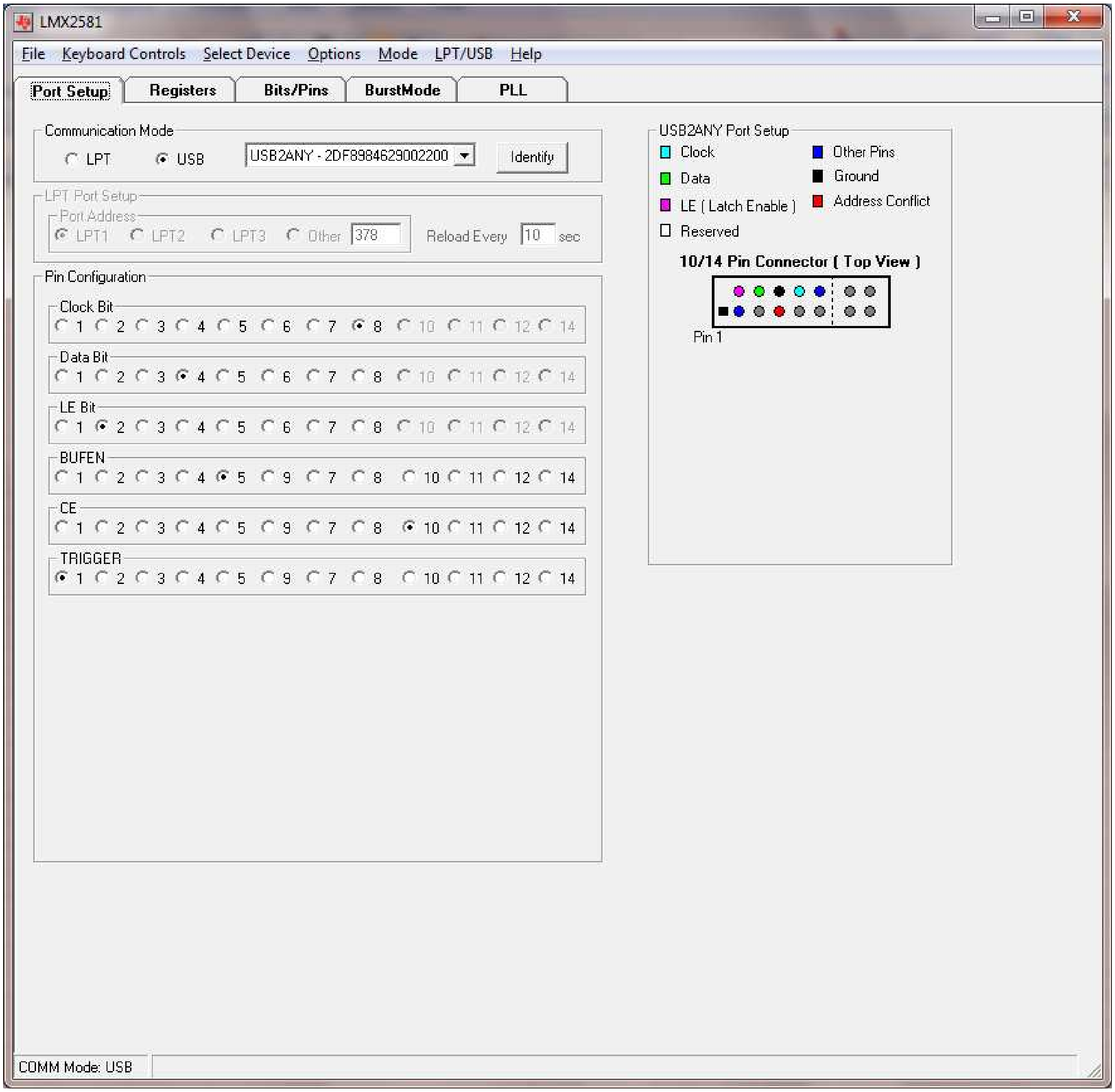


Figure 5.

2.4 Bits/Pins Settings

To view the function of any bit on the CodeLoader configuration tabs, place the cursor over the desired bit register label and click the right mouse button on it for a description.

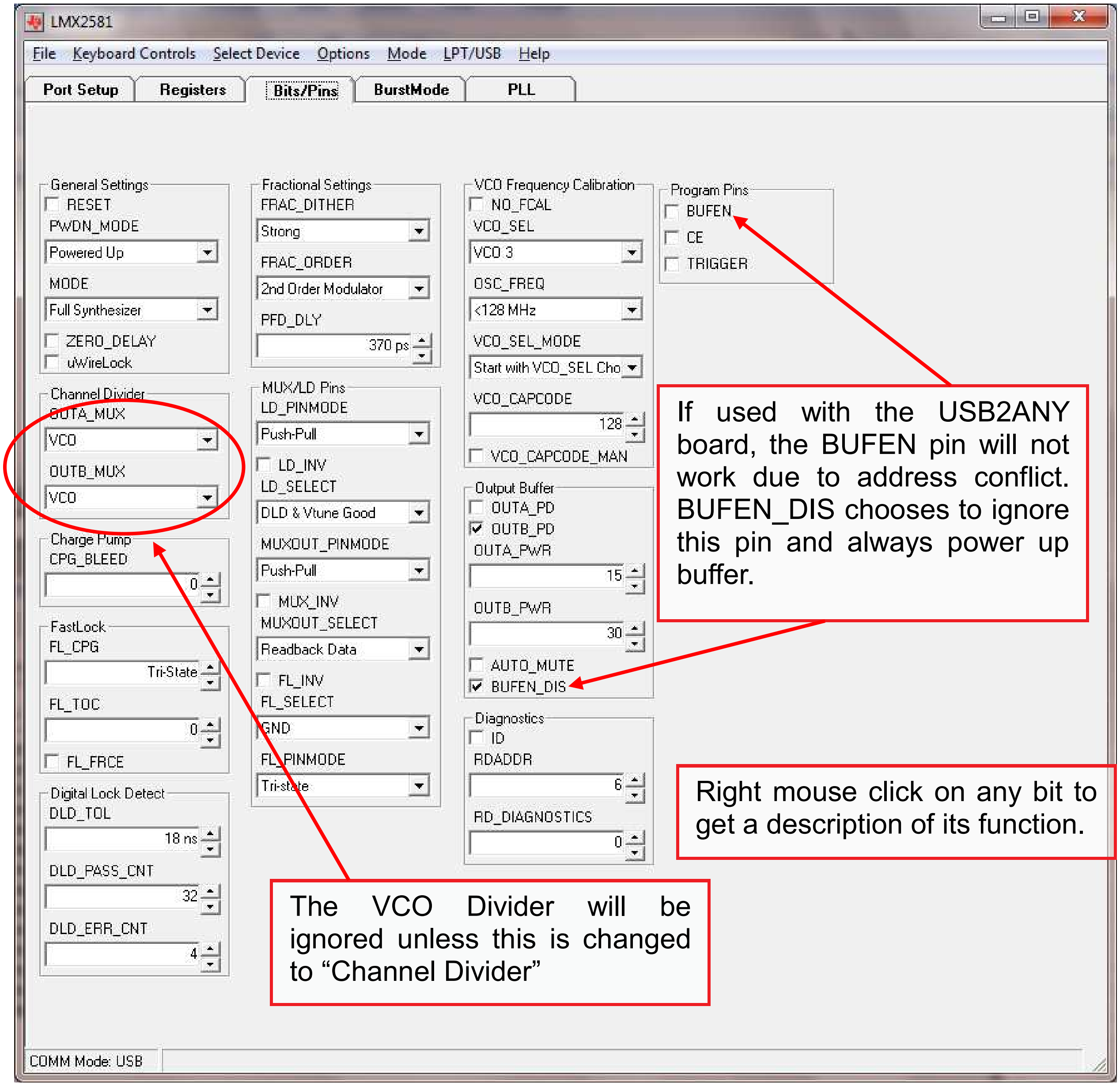


Figure 6. Bits/Pins Settings

3 Board Construction

3.1 Board Layer Stack Up

The board is made on FR4 for the Prepreg and Core Layers. The top layer is 1 oz copper.

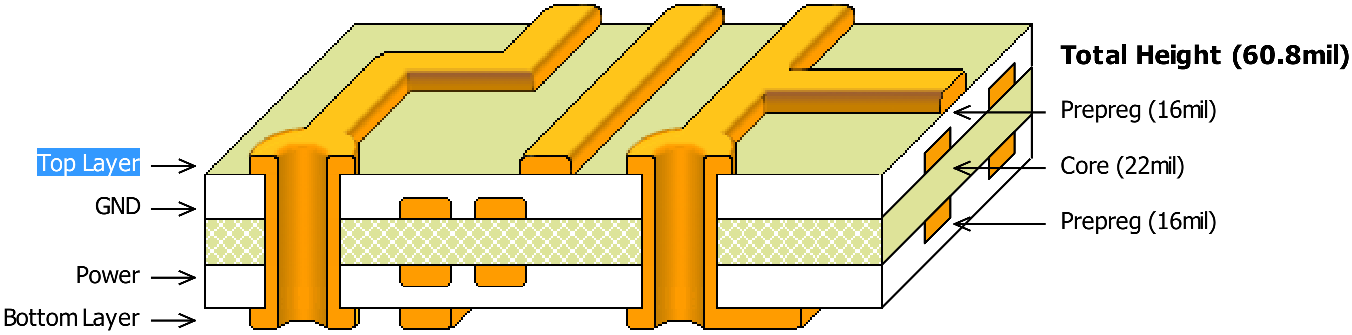


Figure 7. Board Layer Stack Up

FR4 material was chosen because of convenience, availability, and cost. If one was to use Rogers 4003 on the top Prepreg layer, the output power improves about 1 dB. Otherwise, the performance is very similar.

3.2 Schematic

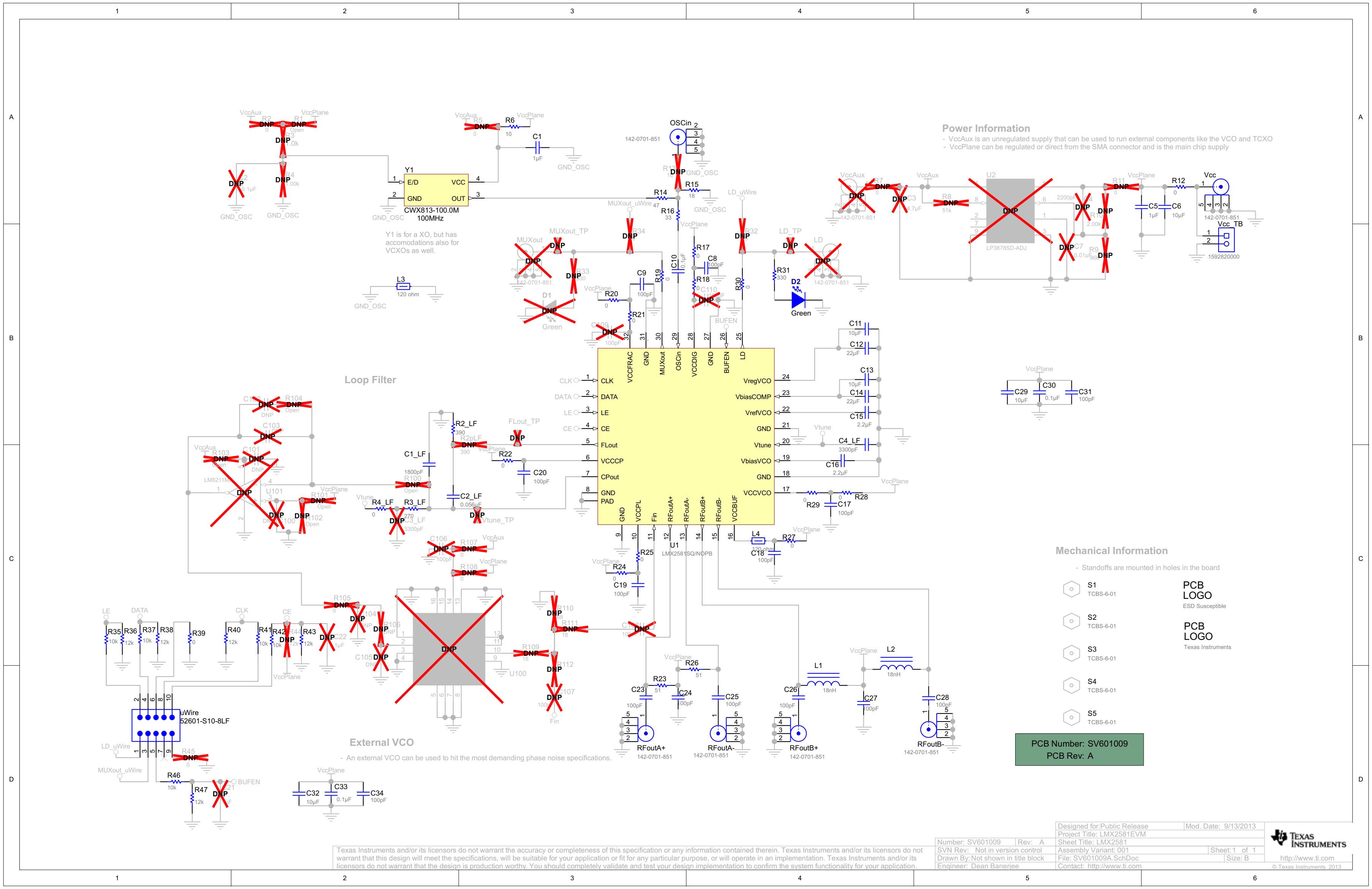


Figure 8. LMX2581 Schematic

3.3 Comments and Recommendations for Evaluation Board Schematic

OSCin Input

The OSCin input has components of a series 47 Ω, shunt 18 Ω, and series 33 Ω, followed by a DC blocker capacitor. This divides down the CMOS output level of the XO and also makes the impedance as seen from the OSCin pin looking out to be about 50 Ω.

The OSCin input can also be driven by the OSCin SMA. To do this, remove R6 and R14; change R13, R15, and L3 to 0 Ω; and make R15 51 Ω. Note that if L3 is not changed and left as a ferrite bead, this can create degraded performance when used with an external signal generator.

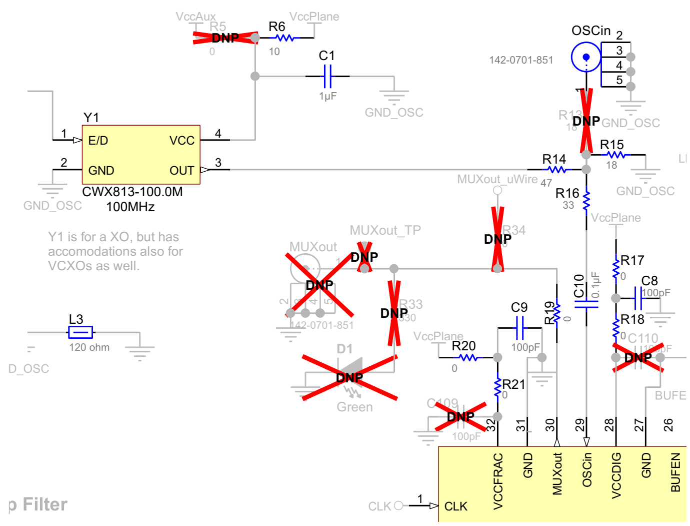


Figure 9. OSCin Input Diagram

Complementary OSCin Input Recommendation

When the OSCin trace is differential, the approach shown in Figure 10 can also be used to convert it for the single-ended input of the LMX2581. This circuit makes impedance seen from the LMX2581 OSCin pin looking out to be 50 Ω as well as the termination for the differential trace to be 100 Ω. Note that only one side of the 100 Ω differential trace can be grounded or it will change the desired 100 Ω termination for the differential trace.

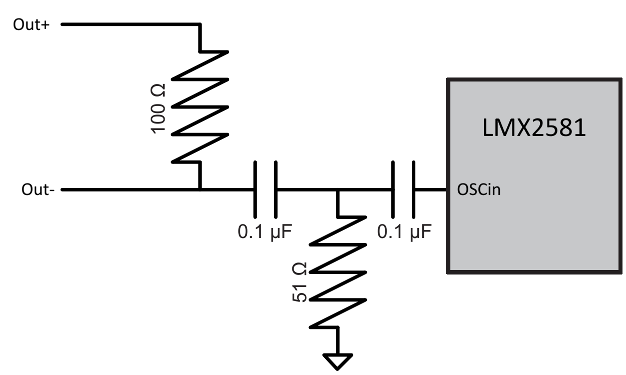


Figure 10. Complementary OSCin Input Recommendation Diagram

External VCO and Fin Input

An external VCO can be placed on the back side of the board and be driven by either a passive or active loop filter. The output of this can be observed on the RFout pins, or the RFoutA- connector can be flipped and used to see the VCO output directly.

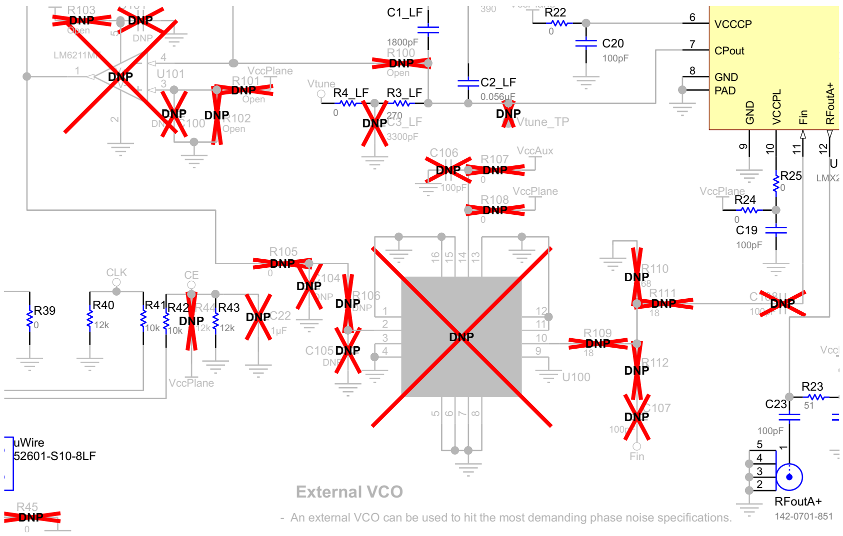


Figure 11. External VCO and Fin Input Diagram

Vtune Input

The highest order loop filter should be placed capacitor next to the Vtune input pin without vias for optimal spurs and VCO phase noise. A value of at least 3.3 nF will ensure that this will not impact the VCO phase noise. If it is smaller, the phase noise of the VCO in the 200k-1MHz range may be degraded based on how small this capacitor is. Smaller values for this capacitor, such as 1.5 nF, are possible, depending on the circumstances.

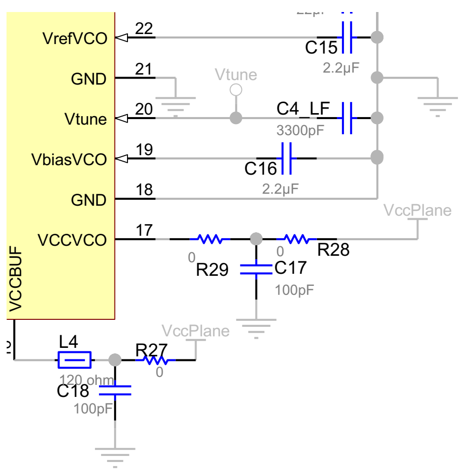


Figure 12. Vtune Input Diagram

Power Supply Bypassing

The bypassing of the power supply pins does not have a large impact on fractional spurs, although placing the ferrite bead L4 on the VccBUF pin improves the spurs at the phase detector frequency offset. This board accommodates the possibility to change this bypassing to either filter noise coming to the pin, or by preventing noise going out from the pin to the ground plane, as in the case of the VccBUF pin.

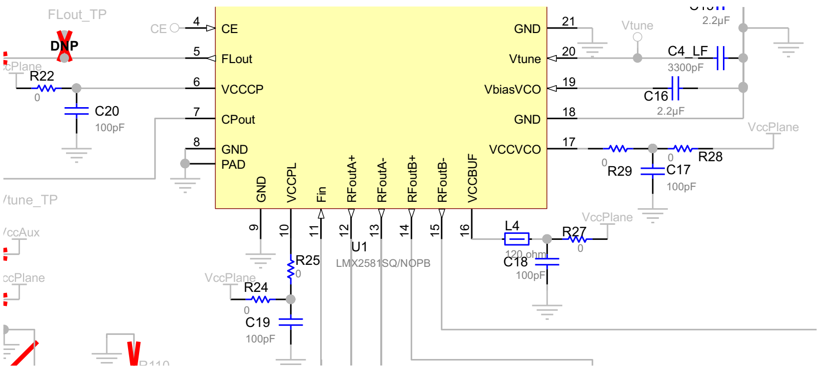


Figure 13. Power Supply Bypassing Diagram

Pins 18,19,22,23, and 24

For the best performance, it is best to have a solid ground connection between the grounds of these pins. Larger value, higher quality capacitors are good for pins 23 and 24

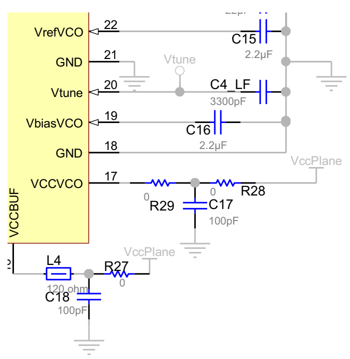


Figure 14. Pins 18,19,22,23, and 24 Diagram

Outputs

The outputs can have either an inductor or resistor pull-up. The board has both values. The placement of this pull-up component close to the chip is critical for output power. For this board, the routing of both outputs compromised the output power a little because it forced this component a little farther away and also it was done on FR4. If a single output was routed on a dielectric like Rogers4003, the output power could have been slightly higher.

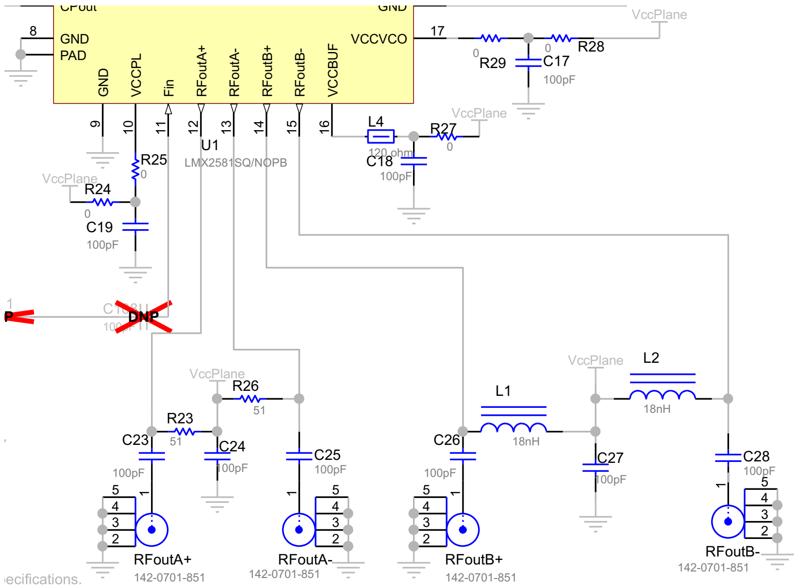


Figure 15. Outputs Diagram

4 PCB Layers

Figure 16 shows the assembly diagram that indicates where the components are placed.

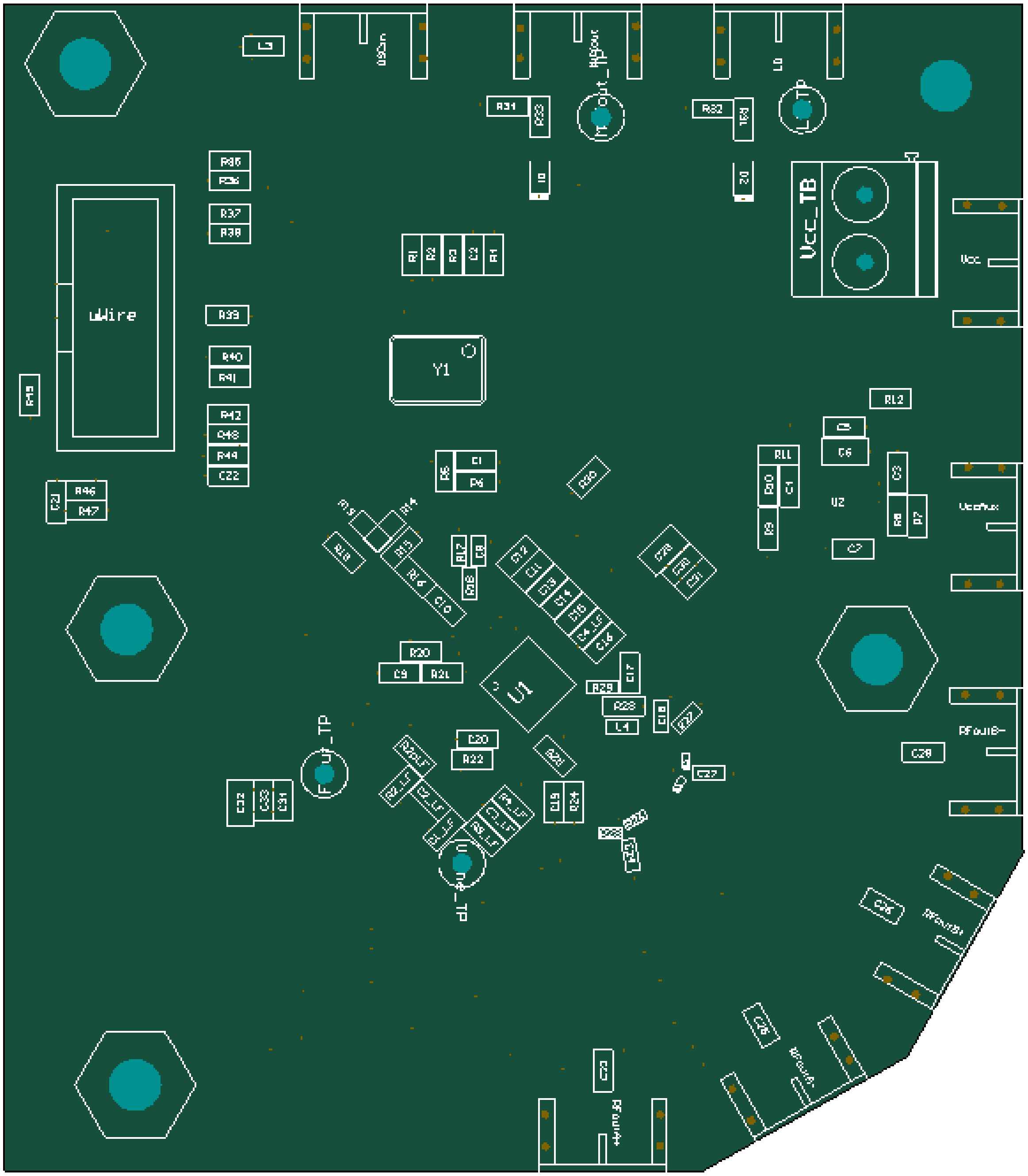


Figure 16. Top Assembly Layer

In the Top Layer, Figure 17, note the solid polygon on the northeast side of the chip, which gives solid grounding to the VregVCO, VbiasVCO, as well as the closed capacitor on the loop filter. This is recommended for optimal performance. On the output traces, the placement of the pull-up component also needs to be as close to the device as possible for optimal output power. For this layout, about 1 dB of power was sacrificed in order to route both outputs, thereby forcing this pull-up component farther away.

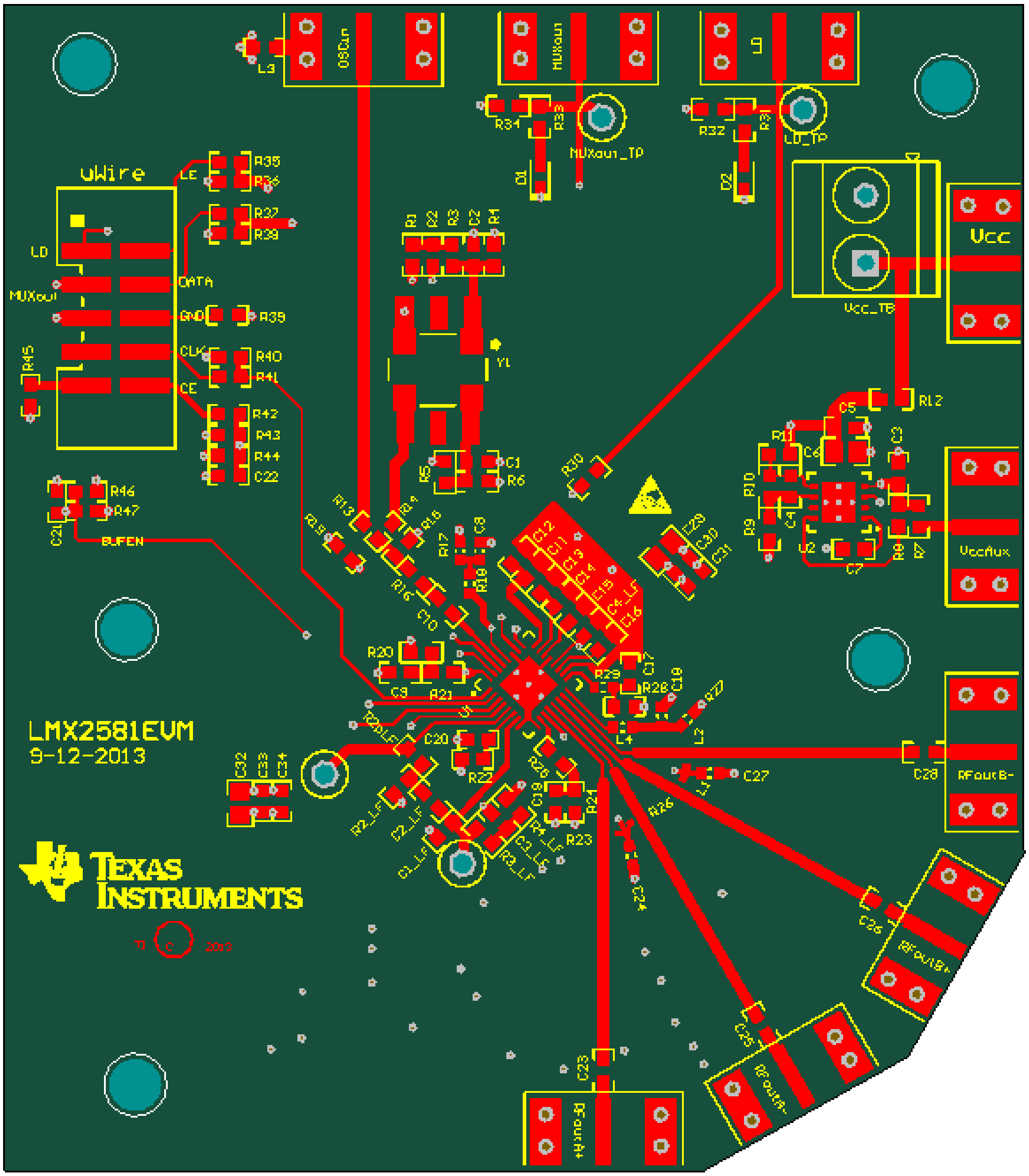


Figure 17. Top Layer

On the Ground Layer, Figure 18, notice there is a main region and a second region that is cut out below the OSCin source. There is a connection through component L3 on the top layer. This reduces coupling from the OSCin signal to the outputs that can potentially spurs at +/- Foscin offset.

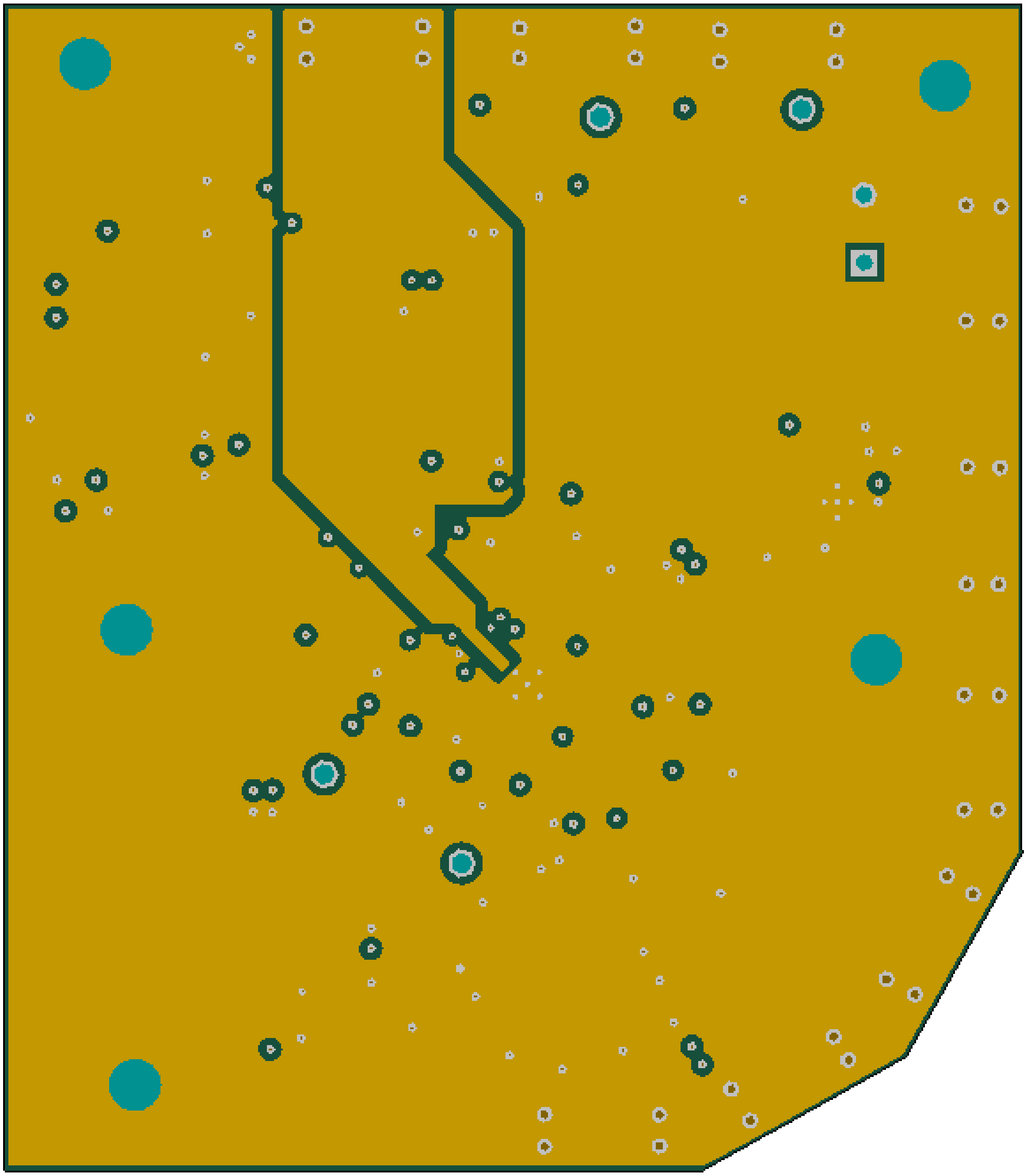


Figure 18. Ground Layer

The power layer, Figure 19, is used to route the power signals. There is a cutout below the OSCin signal to reduce any coupling the OSCin frequency from nearby vias to the power plane.

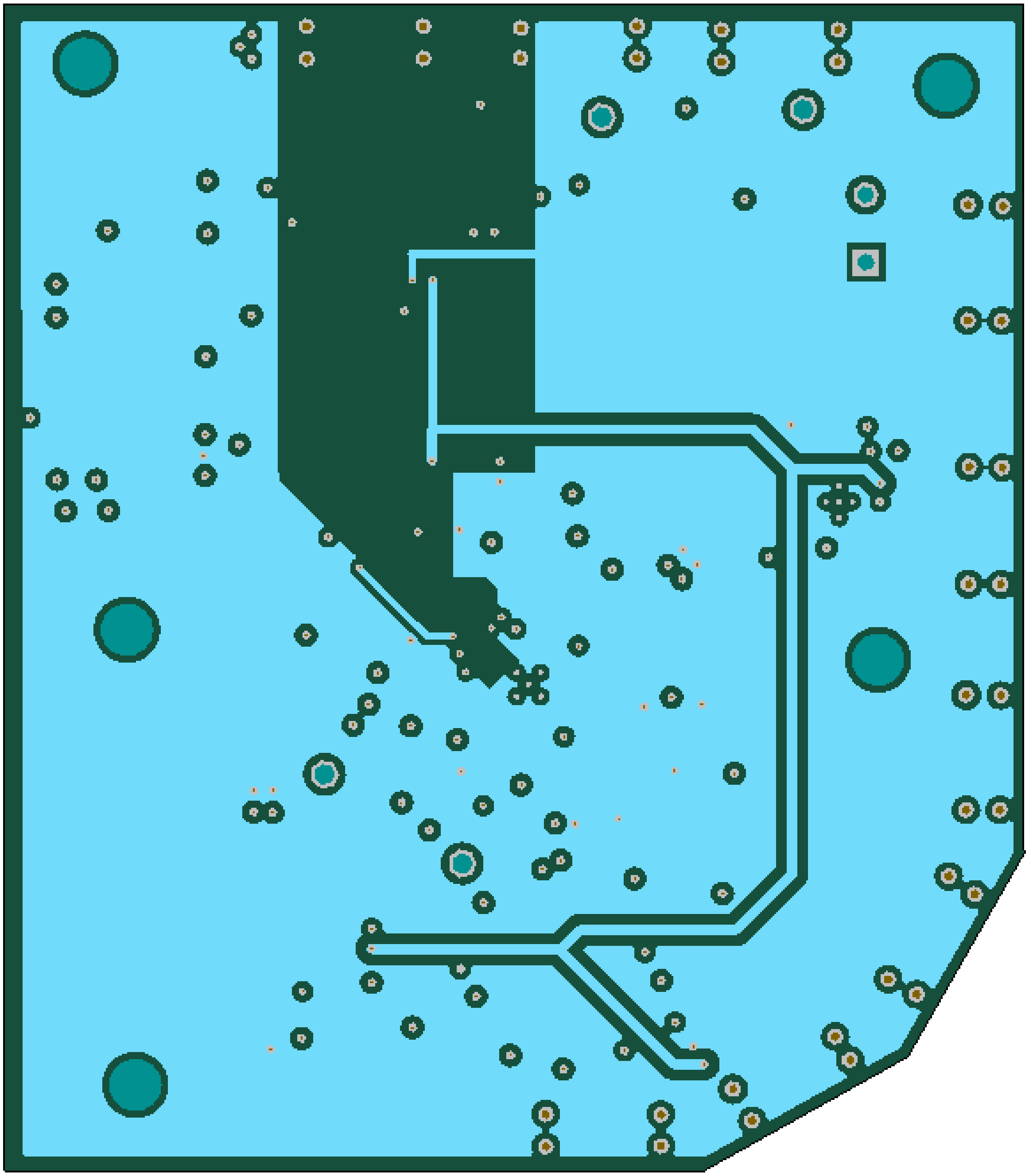


Figure 19. Power Layer

The Bottom Layer, Figure 20, is used to route less critical functions. There are several optional components on the bottom layer, including the option to use an external VCO.

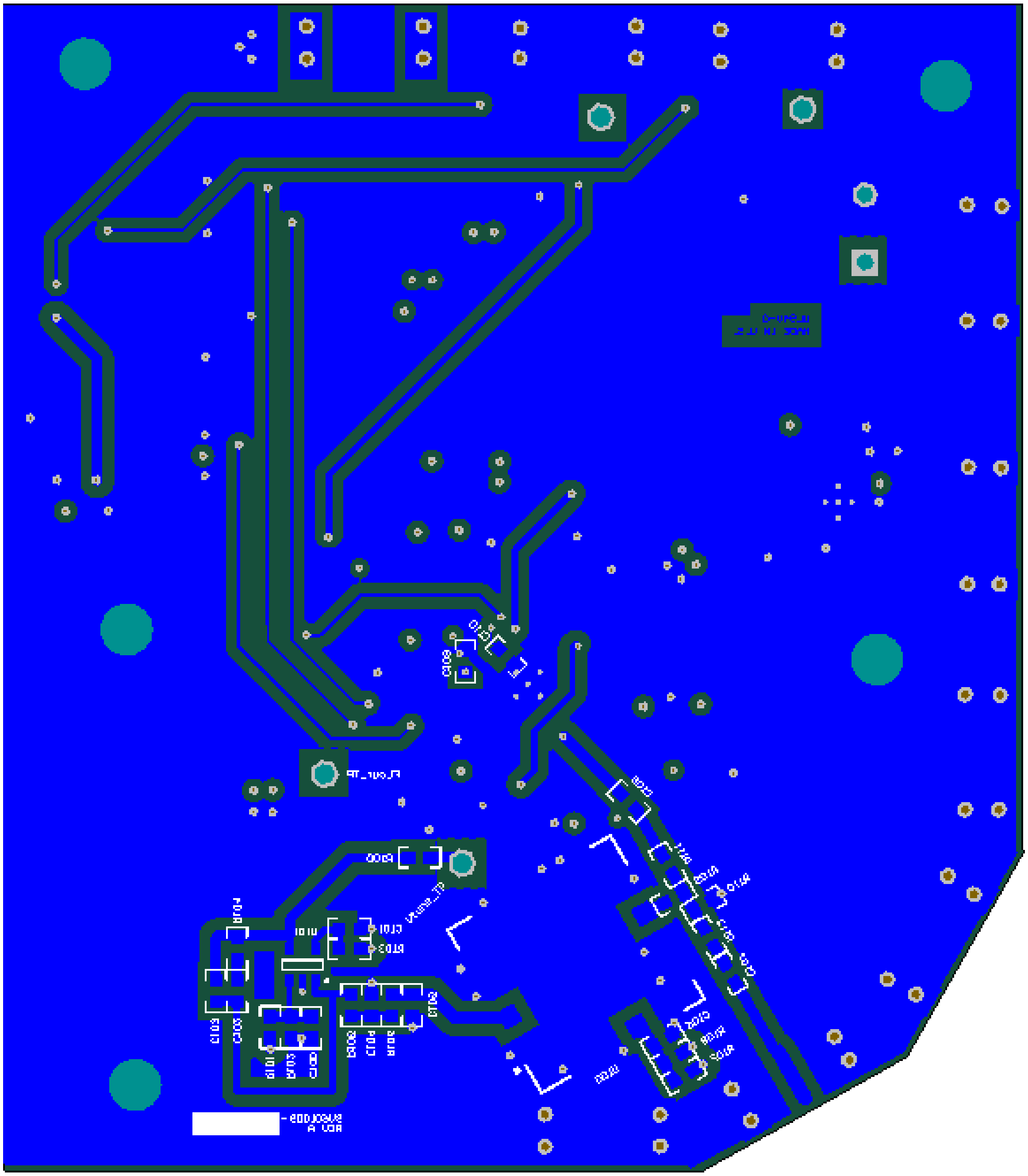


Figure 20. Bottom Layer

5 Measured Performance Data

5.1 Phase Noise in Default Mode

Figure 21 shows the phase noise in default mode. This was taken with a clean input (Wenzel 100 MHz Oscillator), which shows that the device can achieve -99 dBc/Hz for a 2.7 GHz carrier at 1 KHz offset.

The 10 kHz number could be improved for a wider bandwidth. See section Section 5.7 for some examples with a wider bandwidth filter.

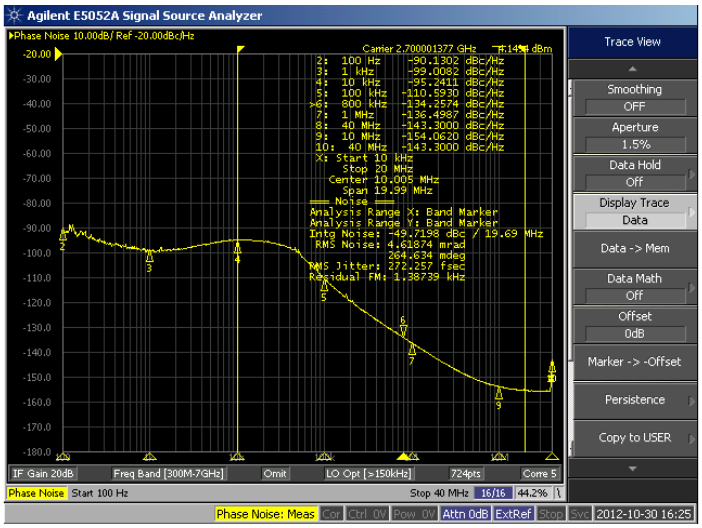


Figure 21. Phase Noise (Default Mode)
Plot 1 of 3

Figure 22 shows the phase noise in default mode. The difference for this one is that it uses the on-board XO. Comparing to the plot above, we see that the XO , not the LMX2581, is the dominant source of phase noise at 100 Hz and 1 kHz.

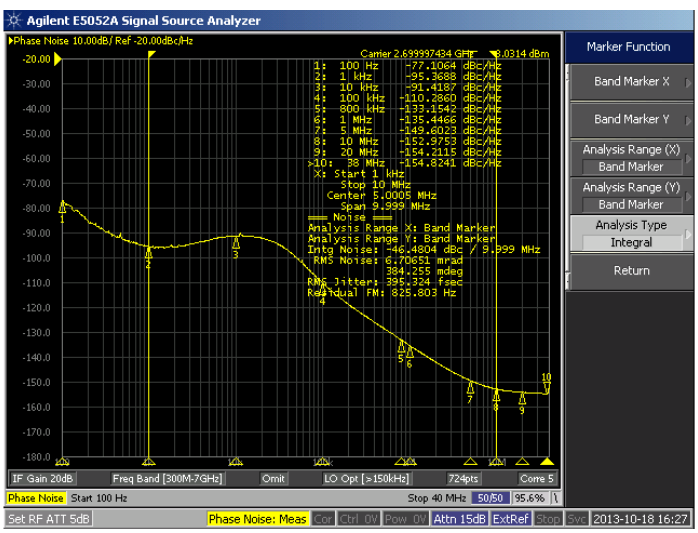


Figure 22. Phase Noise (Default Mode)
Plot 2 of 3

Figure 23 shows a 2700 MHz output signal with various divides. For offsets of 1 MHz and below the phase noise follows a 20*log(divide) relationship. However, past 10 MHz, the phase noise does not follow this and the larger divide values are showing the noise floor of the divider to be about -155 dBc/Hz.

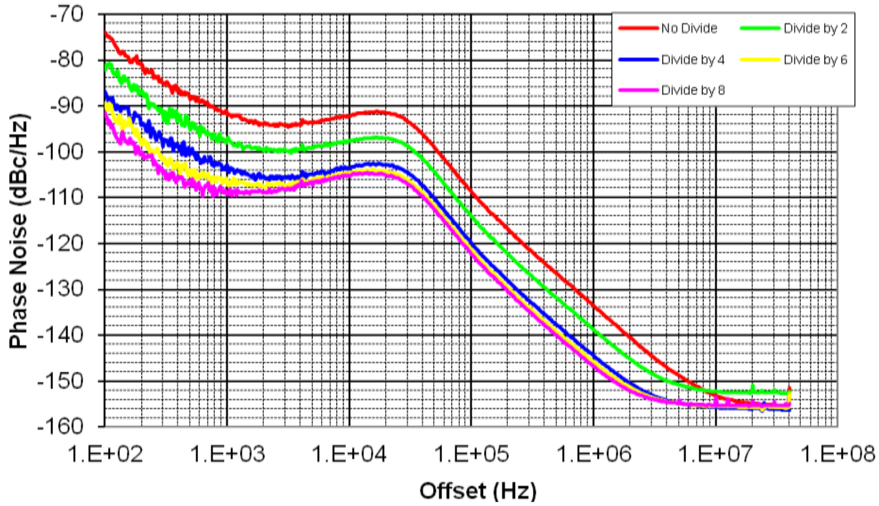


**Figure 23. Phase Noise (Default Mode)
Plot 3 of 3**

5.2 VCO Phase Noise

5.2.1 Fvco = 1900 MHz

Figure 24 and Figure 25 show the phase noise of just the VCO.

These are single-ended measurements and the unused side of the differential output was terminated with a 50 Ω terminator. For these measurements, the programmable output power settings were OUTA_PWR=15 and OUTB_PWR=30.

To get the most accurate measurement, the PLL was tuned 3 MHz away from any harmonic of the 100 MHz OSCin frequency and the charge pump was set to tri-state. Even though the charge pump was tri-stated, a narrow bandwidth filter was used to minimize any frequency drifting.

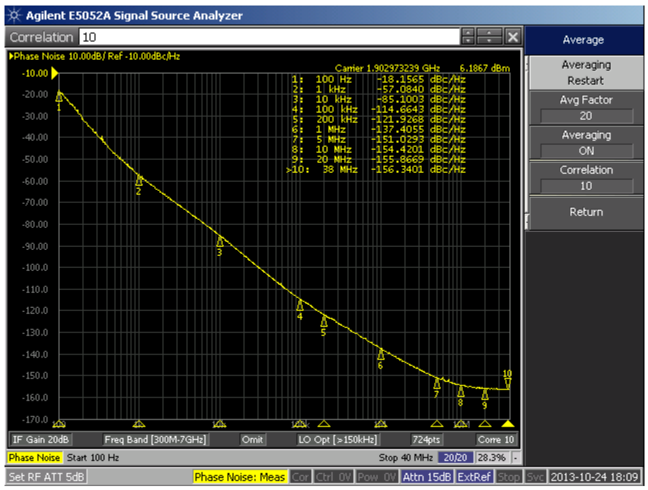


Figure 24. VCO Phase Noise Fvco = 1900 MHz RFOutA+

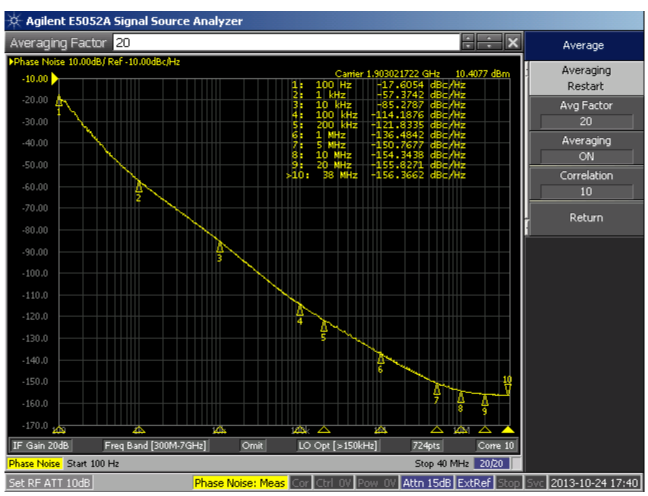


Figure 25. VCO Phase Noise Fvco = 1900 MHz RFOutB+

5.2.2 Fvco = 2200 MHz

Figure 26 and Figure 27 show the phase noise of just the VCO.

These are single-ended measurements and the unused side of the differential output was terminated with a 50 Ω terminator. For these measurements, the programmable output power settings were OUTA_PWR=15 and OUTB_PWR=30.

To get the most accurate easurement, the PLL was tuned 3 MHz away from any harmonic of the 100 MHz OSCin frequency and the charge pump was set to tri-state. Even though the charge pump was tri-stated, a narrow bandwidth filter was used to minimize any frequency drifting.

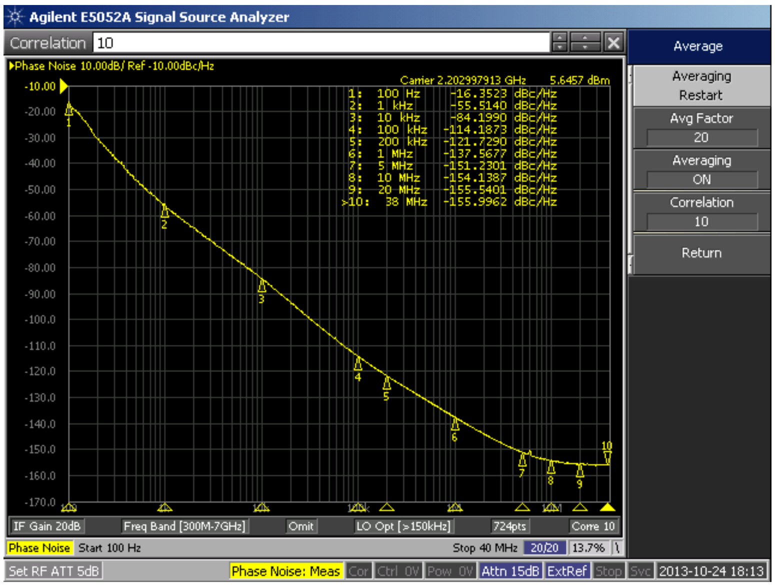


Figure 26. VCO Phase Noise
Fvco = 2200 MHz
RFOutA+

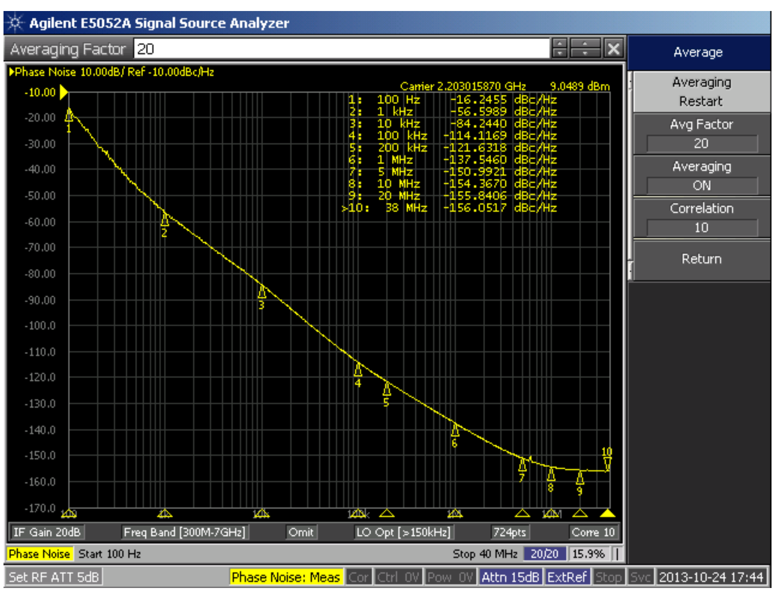


Figure 27. VCO Phase Noise
Fvco = 2200 MHz
RFOutB+

5.2.3 Fvco = 2700 MHz

Figure 28 and Figure 29 plots show the phase noise of just the VCO.

These are single-ended measurements and the unused side of the differential output was terminated with a 50 Ω terminator. For these measurements, the programmable output power settings were OUTA_PWR=15 and OUTB_PWR=30.

To get the most accurate easurement, the PLL was tuned 3 MHz away from any harmonic of the 100 MHz OSCin frequency and the charge pump was set to tri-state. Even though the charge pump was tri-stated, a narrow bandwidth filter was used to minimize any frequency drifting.

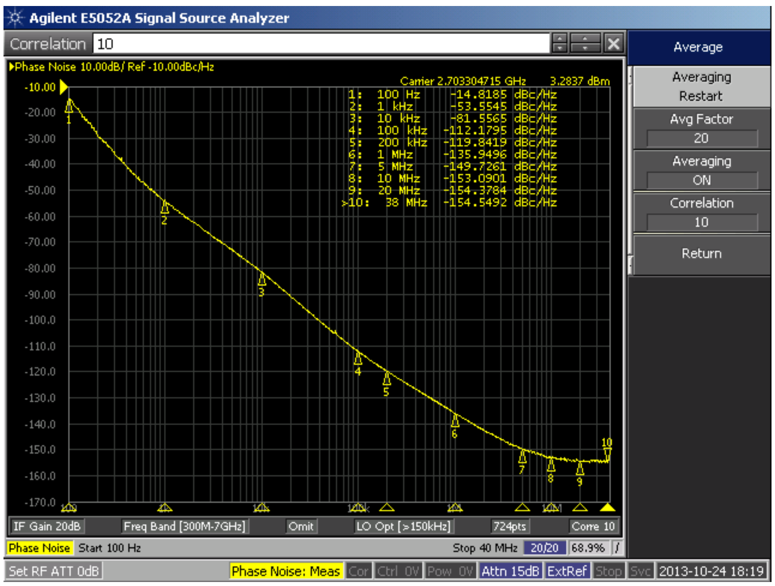


Figure 28. VCO Phase Noise Fvco = 2700 MHz RFOutA+

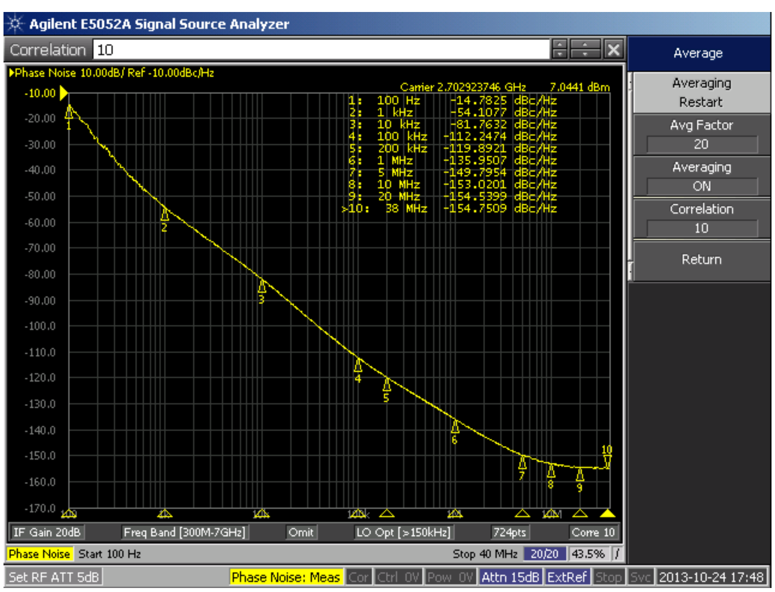


Figure 29. VCO Phase Noise Fvco = 2700 MHz RFOutB+

5.2.4 Fvco = 3300 MHz

Figure 30 and Figure 31 plots show the phase noise of just the VCO.

These are single-ended measurements and the unused side of the differential output was terminated with a 50 Ω terminator. For these measurements, the programmable output power settings were OUTA_PWR=15 and OUTB_PWR=30.

To get the most accurate measurement, the PLL was tuned 3 MHz away from any harmonic of the 100 MHz OSCin frequency. Unlike the plots at the other frequencies, the charge pump was NOT tri-stated and the PLL is locked. The marker at 100 Hz was removed because this is not pure VCO noise and is impacted by the loop filter.

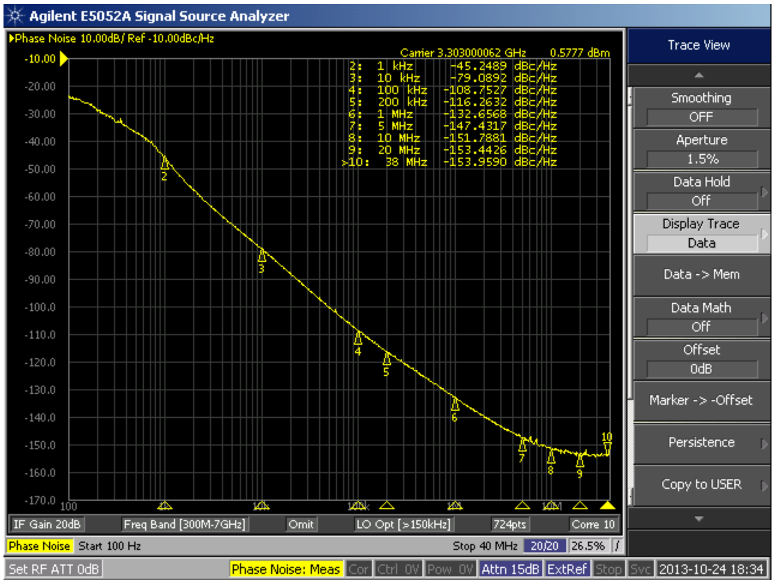


**Figure 30. VCO Phase Noise
Fvco = 3300 MHz
RFOutA+**

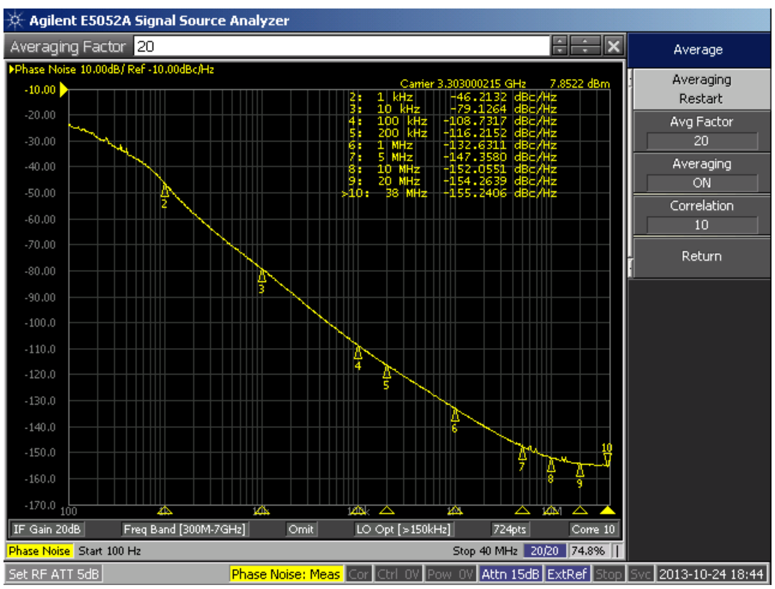


**Figure 31. VCO Phase Noise
Fvco = 3300 MHz
RFOutB+**

5.3 Fractional Spurs

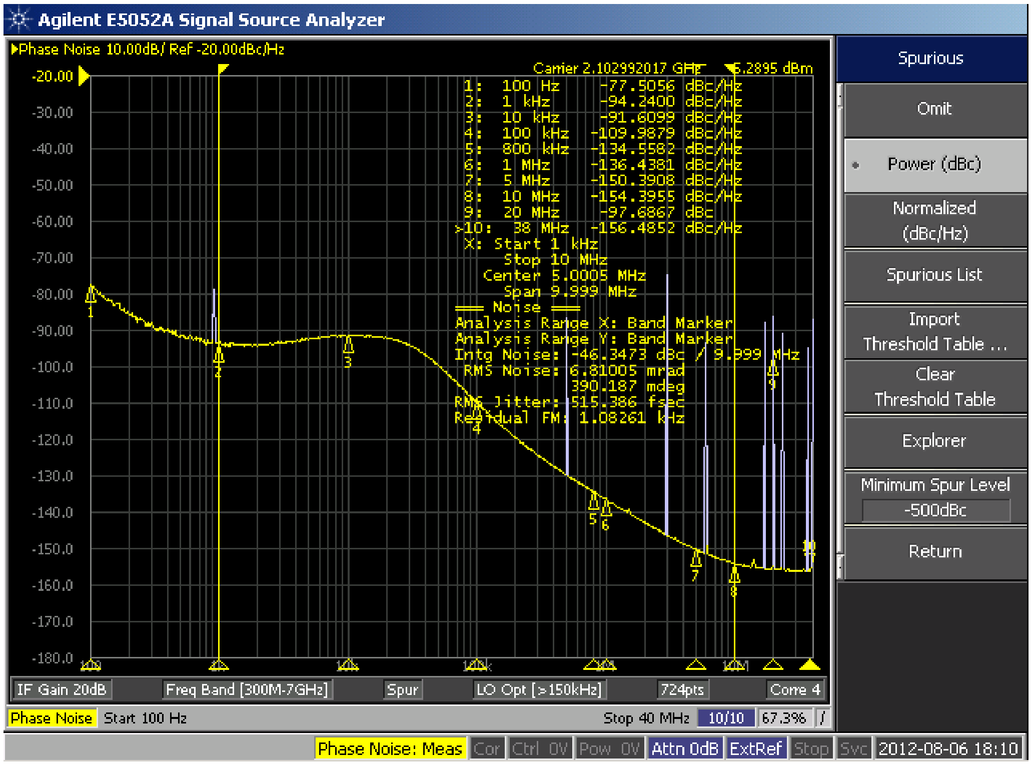


Figure 32. Fvco = 2103 MHz (No Divide)

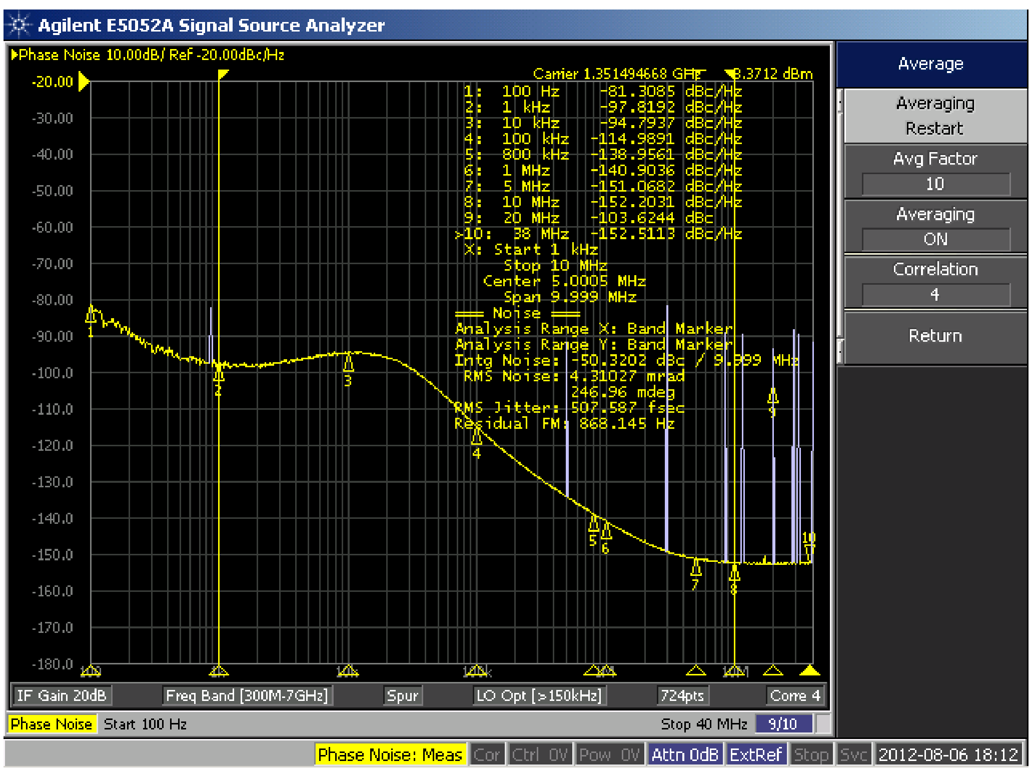


Figure 33. Fvco = 2103 MHz/2 = 1051.5 MHz (Divide by 2)

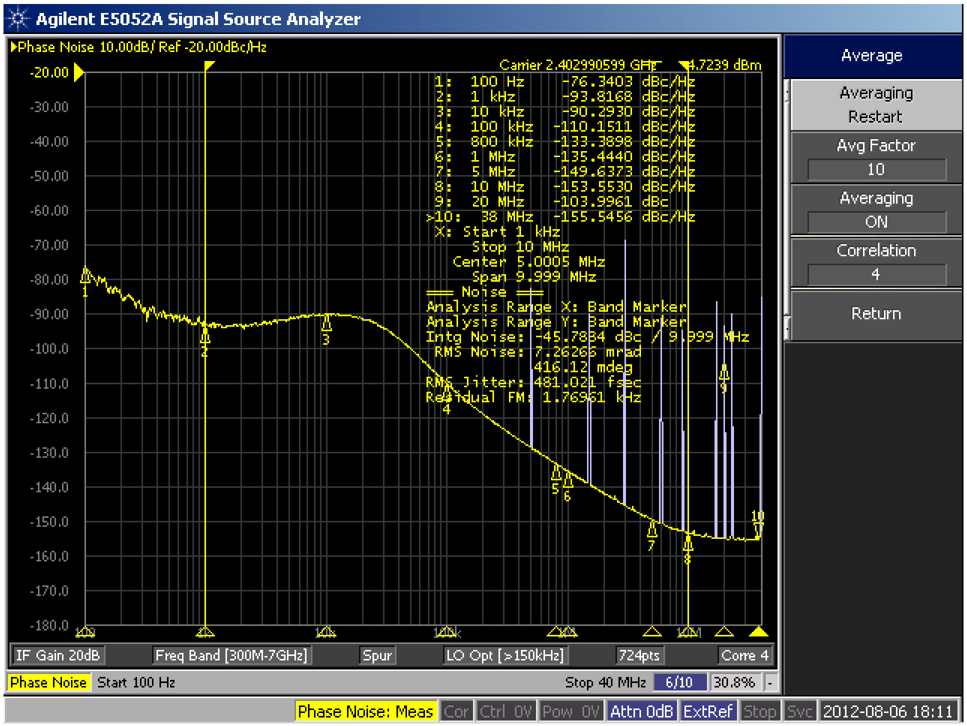


Figure 34. Fvco = 2403 MHz (No Divide)

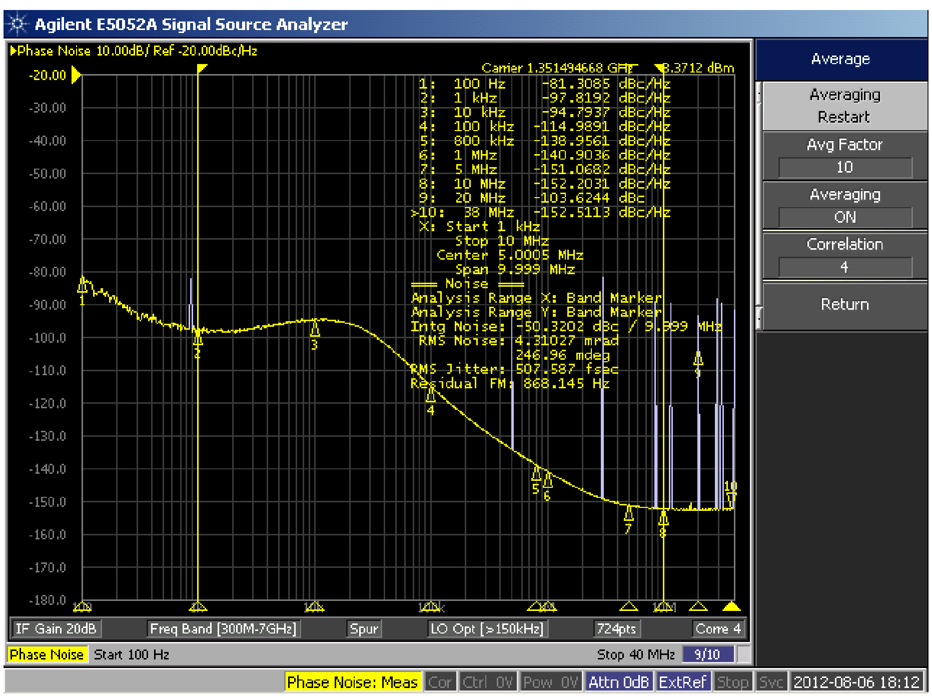


Figure 35. Frequency = 2403/2 = 1201.5 MHz (Divide by 2)

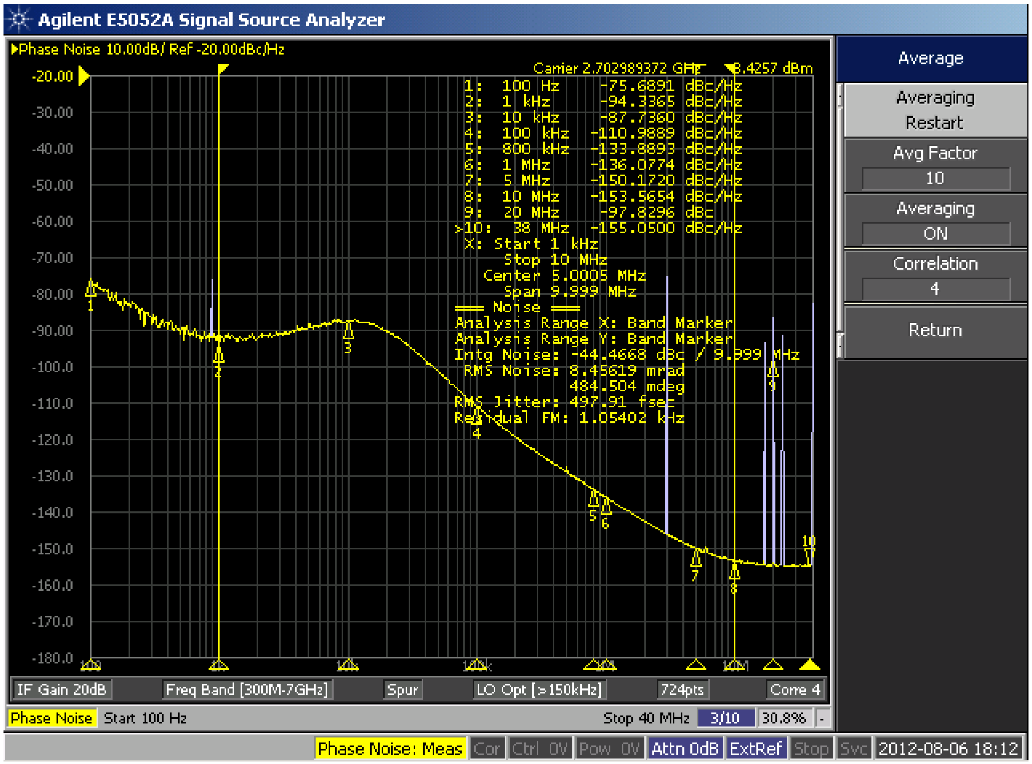


Figure 36. Fvco = 2703 MHz (No Divide)

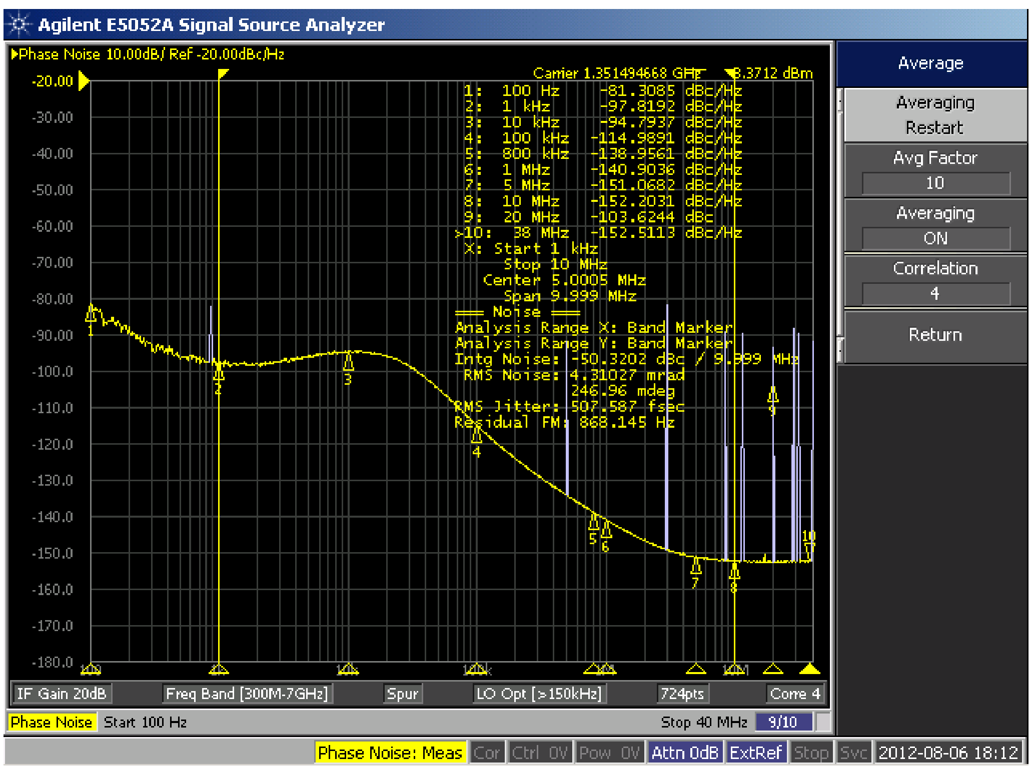


Figure 37. Frequency = 2703/2 = 1451.5 MHz (Divide by 2)

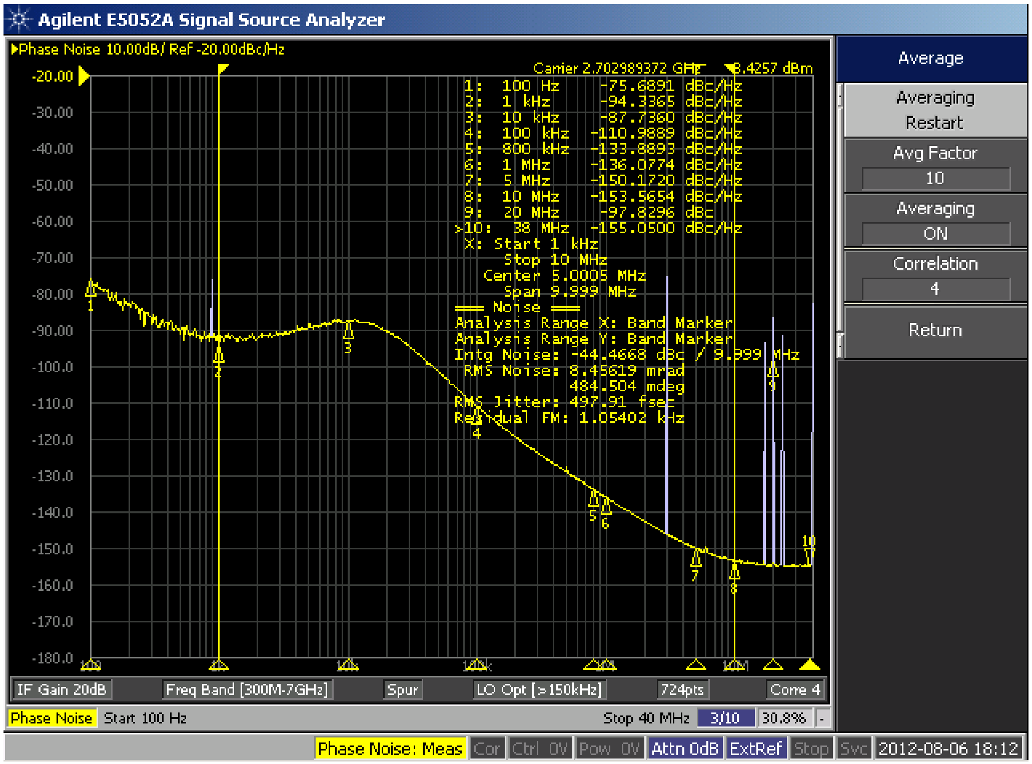


Figure 38. Fvco = 3403 MHz (No Divide)

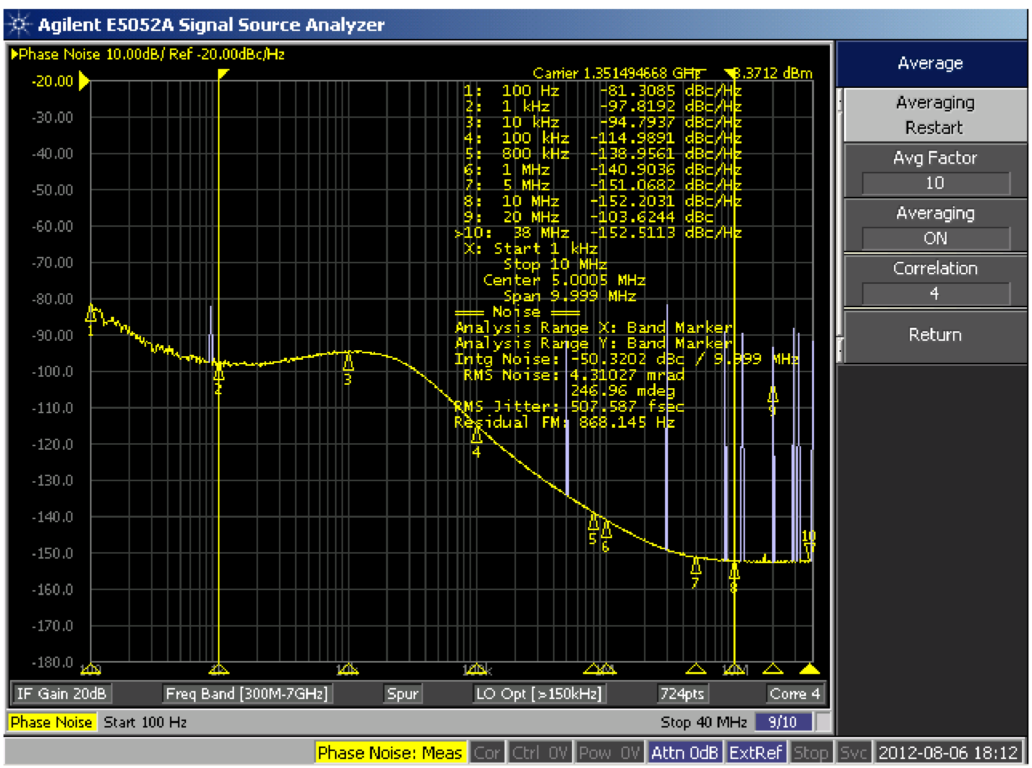


Figure 39. Frequency = 3403/2 = 1051.5 MHz (Divide by 2)

5.4 Lock Time (VCO Digital Calibration Time)

Figure 40 shows the VCO tuning from 1850 to 3800 MHz. The VCO divider has been set to 2 because the measurement equipment (HP53310A) could not handle the higher frequency. This is starting at Core 1 and we can see all the different cores switching in. This is the VCO calibration time and is independent of the loop filter. This can be dramatically improved by guiding the VCO to the correct frequency.

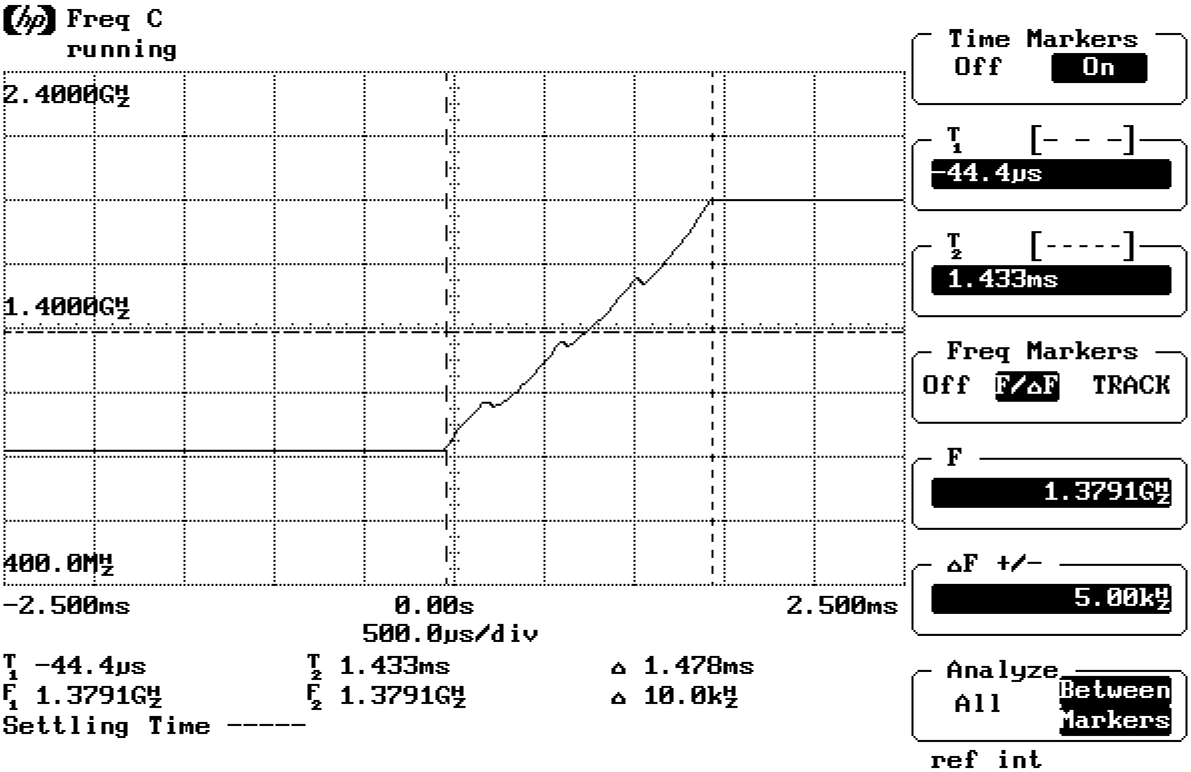


Figure 40.

Figure 41 shows that this lock time can be improved by telling the VCO where to start. For this, the VCO was selected to start at VCO core 4 with a capcode of 47. Although a different value could be used to improve the lock time more, a value of 47 represents might be a reasonable starting point that would account for process and temperature variations. Note that even if the wrong core is chosen, such as choosing the lower end of a higher frequency core vs. a higher end of a lower frequency core, this algorithm still dramatically improves lock time. This lock time can be decreased much further (<10 µs) if the OSCin and phase detector frequencies are raised.

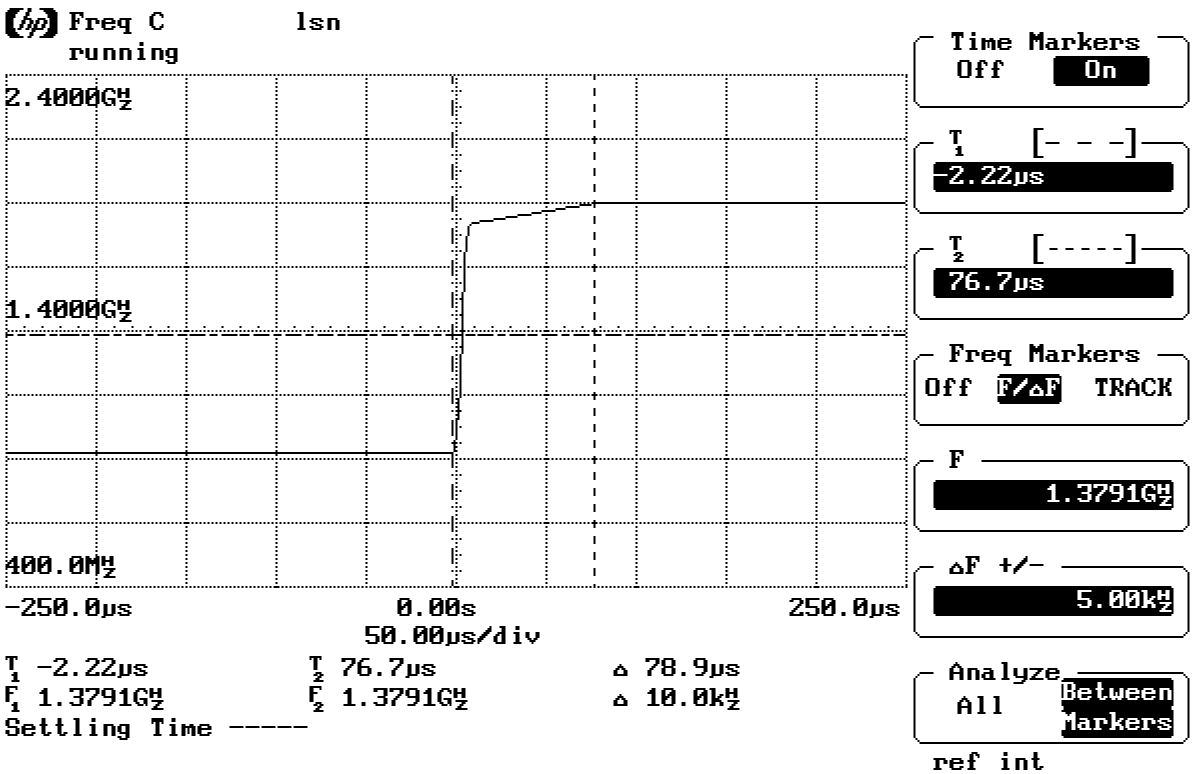


Figure 41.

5.5 Lock Time (Analog PLL Lock Time)

Figure 42 shows a glitch that may occur after the VCO calibration is finished. Because the LMX2581 has 4 cores with 256 different frequency bands, the PLL is fairly close on frequency the time that the VCO calibration is finished. This plot shows that this calibration is getting within about 200 kHz of the final frequency, so this is all the analog PLL has to settle out.

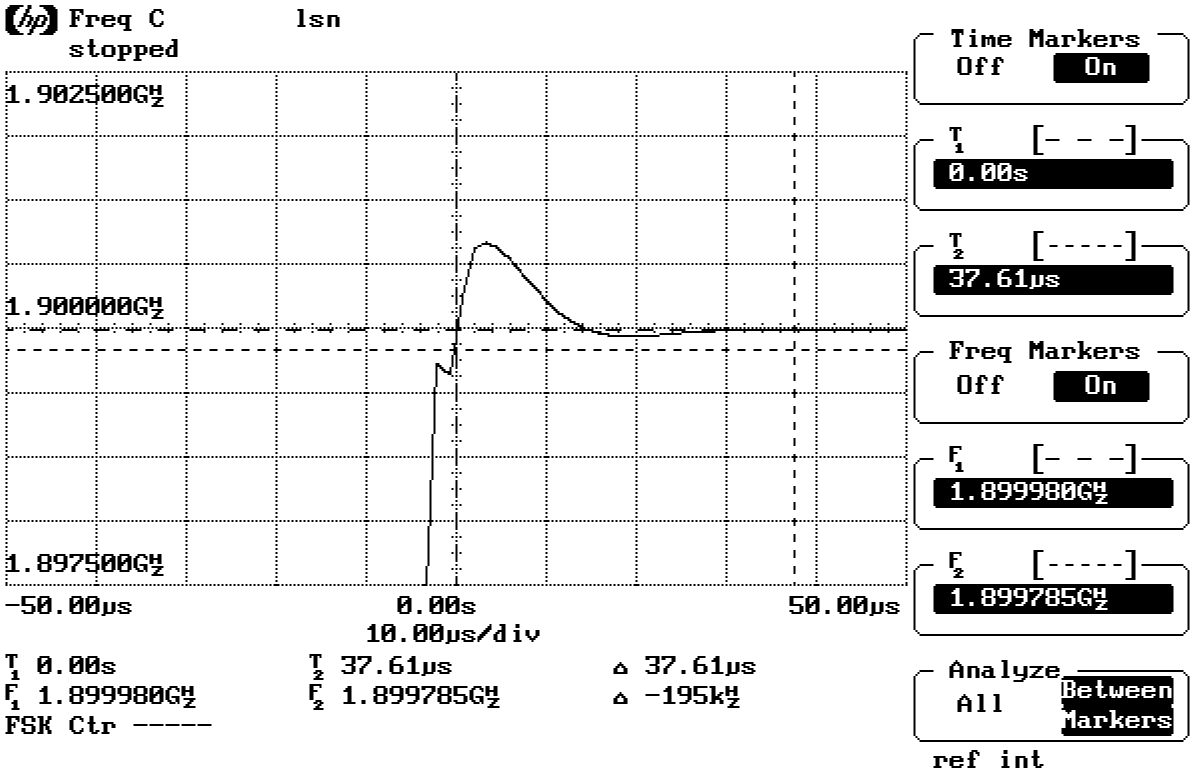


Figure 42.

Figure 43 shows the PLL settling to the final frequency.

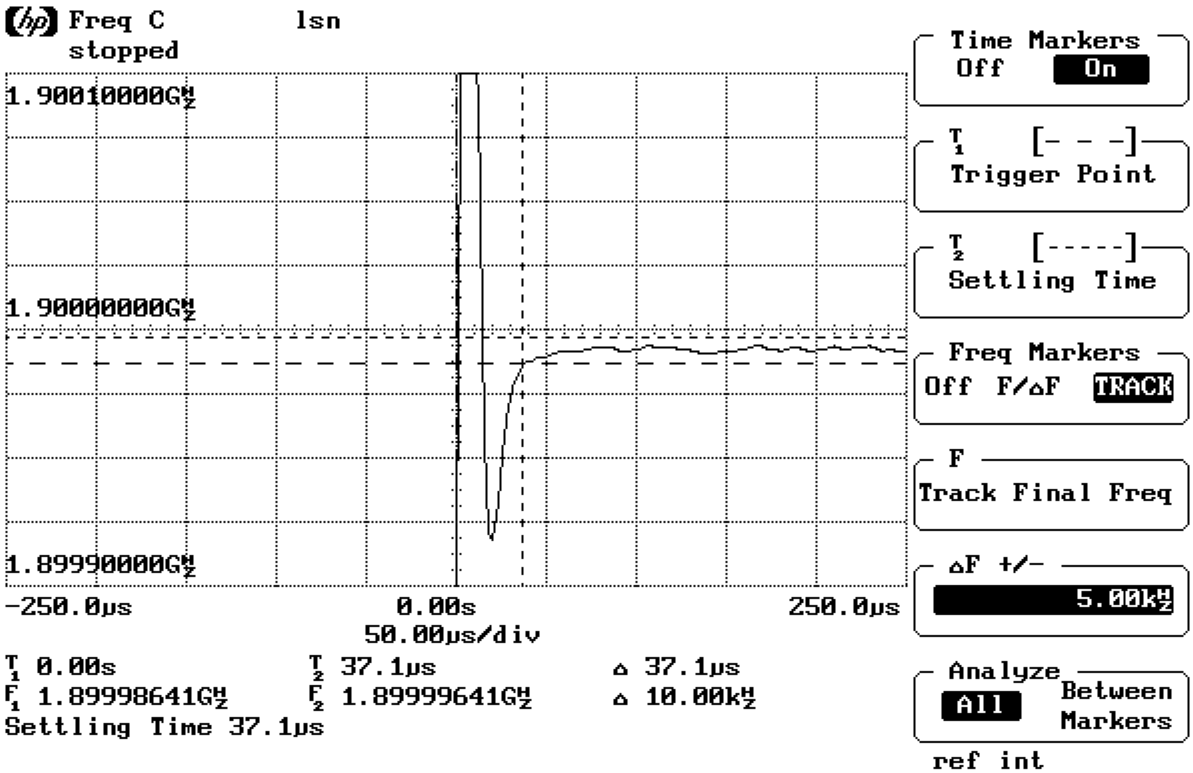


Figure 43.

5.6 Output Power

5.6.1 Impact of the Frequency and Board On Output Power for OUTx_PWR = 15

Figure 44 shows the impact of frequency on the output power for a setting of 15. The power from OUTA and OUTB are different because OUTA uses a 51 ohm pull-up and OUTB uses an 18 nH inductor. In general, the inductor gives higher output power for the same settings at higher frequencies, although the output impedance is not matched. The output impedance is equal to the impedance of the pull-up component. In general, the inductor gives more output power for the same setting, except at lower frequencies.

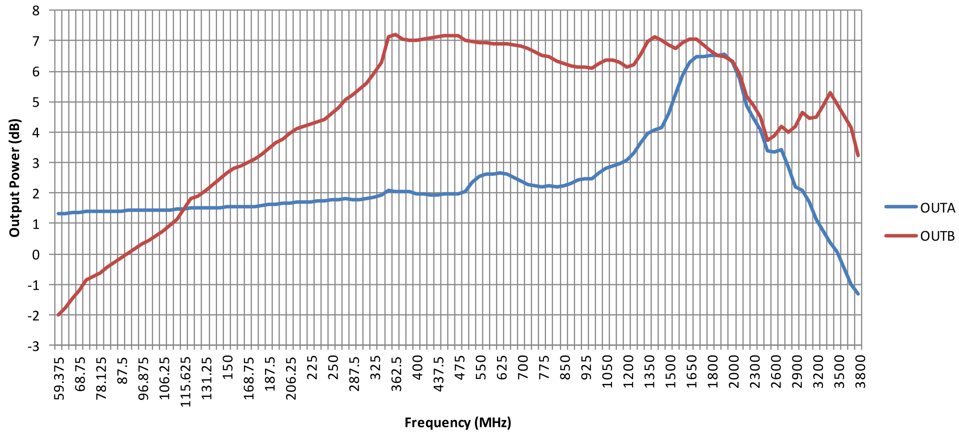


Figure 44.

Figure 45 shows the output power for two different versions of the evaluation board with identical layout for the output buffers, but different materials, for a setting of for OUTx_PWR=15. There is only a small difference in the output power between Rogers4003 and FR4.

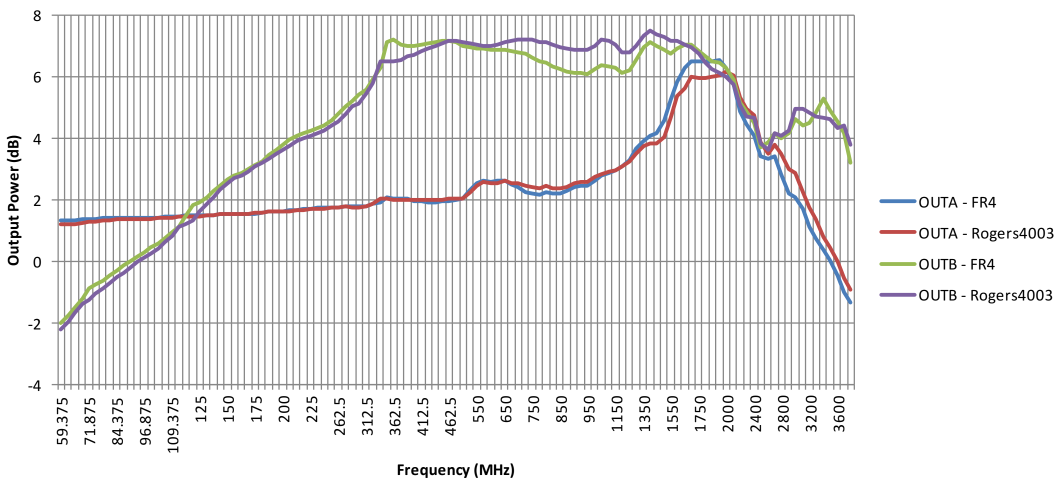
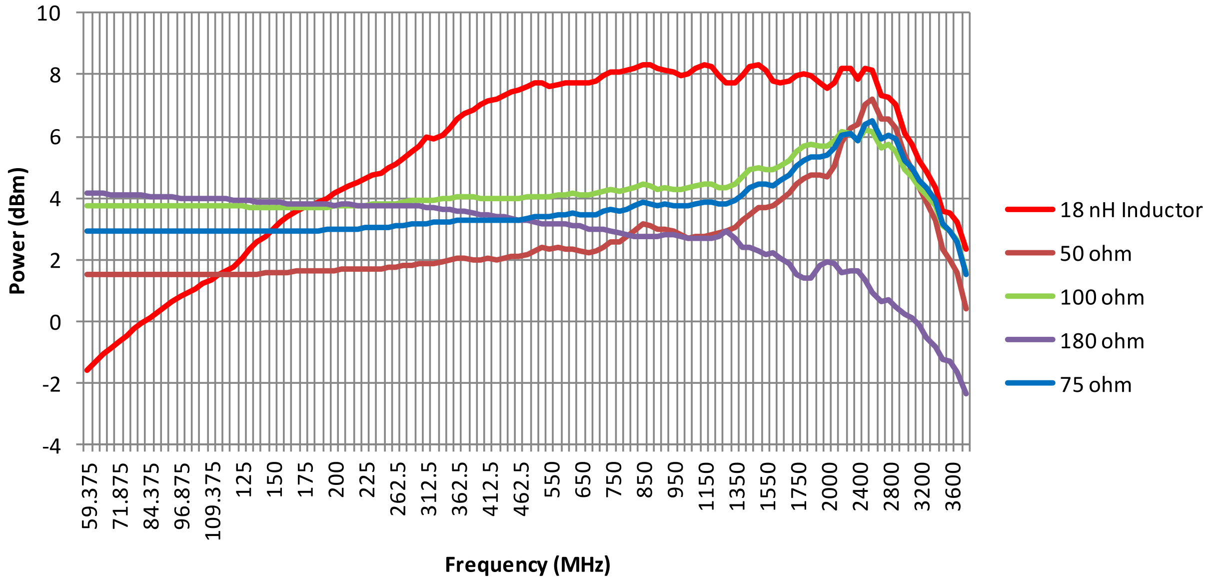


Figure 45.

Figure 46 is **from a different board** that had a single output routed with a very short trace and was on ROGERS4003 dielectric for a setting of OUTx_PWR = 15. Because only a single output was routed, the layout was more optimized and the result is a higher output power with a flatter frequency response. The legend shows different values of the pull-up component that were used.



10
8
6
4
2
0
-2
-4
Power (dBm)
59.375
71.875
84.375
96.875
109.375
125
150
175
200
225
262.5
312.5
362.5
412.5
462.5
550
650
750
850
950
1150
1350
1550
1750
2000
2400
2800
3200
3600
Frequency (MHz)
18 nH Inductor
50 ohm
100 ohm
180 ohm
75 ohm

Figure 46.

5.6.2 Impact of OUTx_PWR on Output Power and Noise Floor at 2.7 GHz

Figure 47 shows the impact of OUTx_PWR on the x axis and the output power. For the inductor pull-up on OUTB, higher settings give more power.

For the 51 Ω resistor pull-up (OUTA), it is not recommended to go above a setting of 30 Ω because it gives less output power, degrades the noise floor, and draws more current.

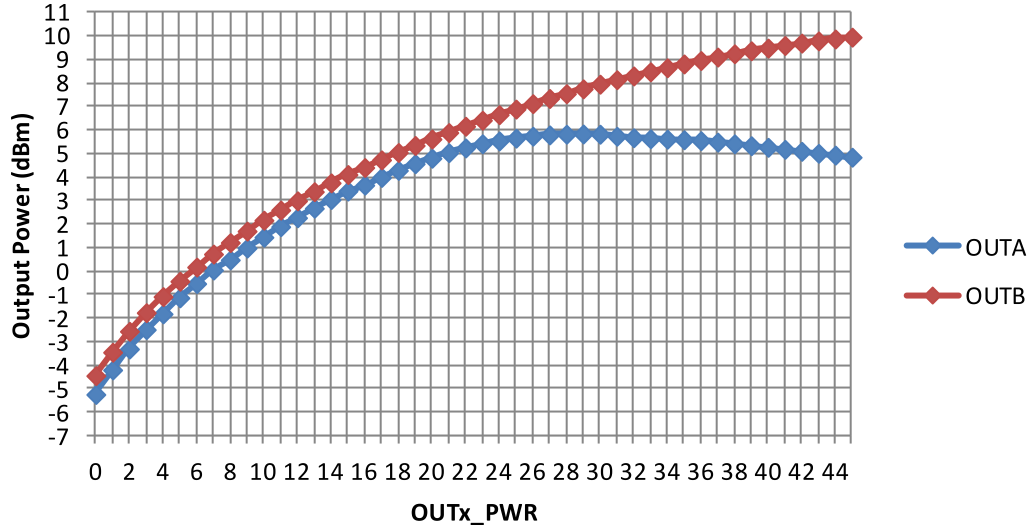


Figure 47.

Figure 48 shows the noise floor as a function of OUTx_PWR. This suggests that a setting of 15 is optimal for noise floor for the 51 ohm resistor pull-up (OUTA). For the inductor pull-up (OUTB), a setting closer to 30 is more optimal.

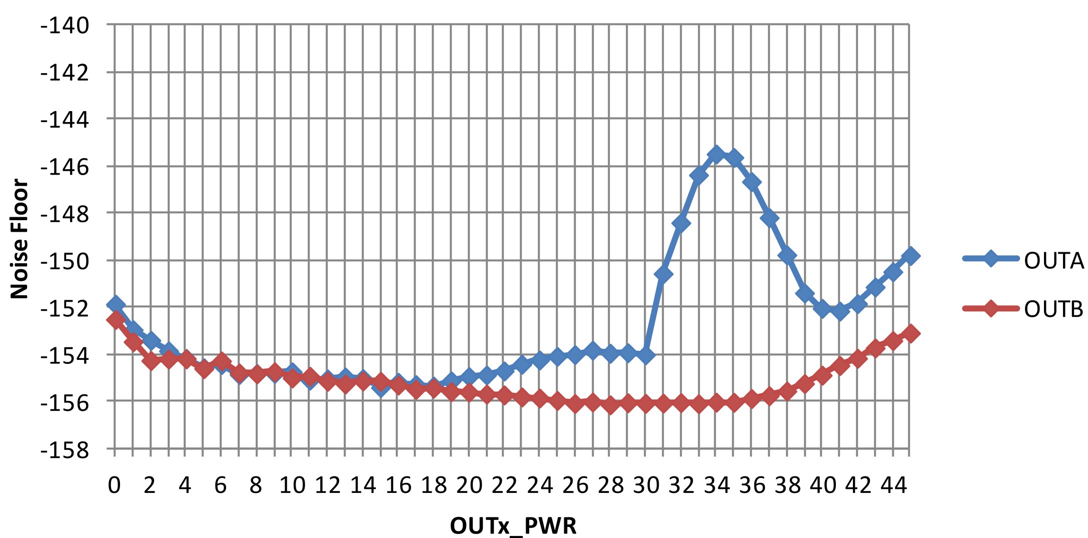


Figure 48.

5.7 LMX2581 and LMK04816 Measurements on a Different Board

5.7.1 Output Power and Phase Noise on Another Board

Figure 49 shows the output of the LMX2581 driven by the LMK04816 with a board routed with a single output. This used an inductor pull-up and was set to the maximum output power.

For the user that wants raw power, this is the part. When optimized for maximum output power, the SINGLE-ENDED output power is +14.4 dBm!

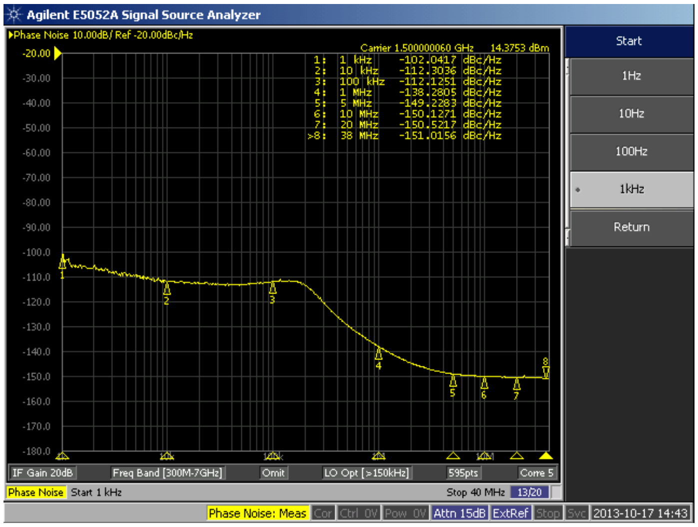


Figure 49.

Figure 50 is the same board output at 2.2 GHz output.

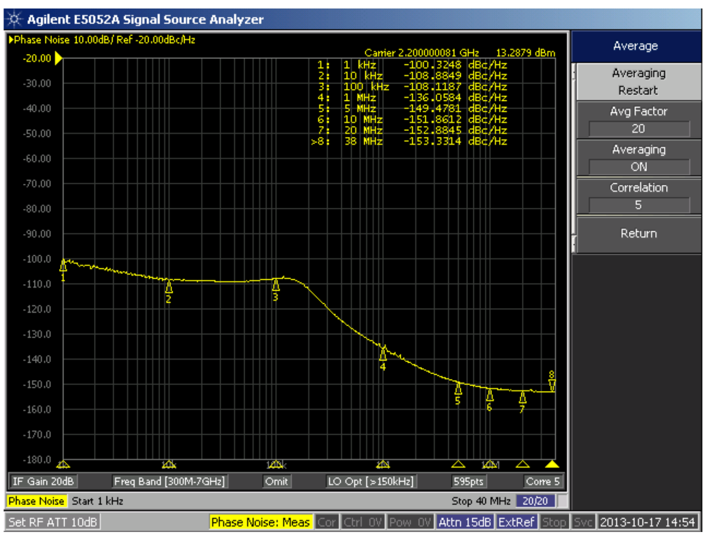


Figure 50.

Figure 51 is this same LMK04816 + LMX2581 board output at 2.7 GHz. This uses a 100 MHz phase detector and a wider loop bandwidth. Comparing to the plot in Section 5.1. Section 5.1, there is a significant improvement in close-in phase noise due mainly to the wider loop bandwidth

The noise floor is a little worse because it is slightly worse at the highest output power setting that was 45 in this case.

This is more typical of a loop bandwidth that one would use for a clocking application or something with wider channel spacing.

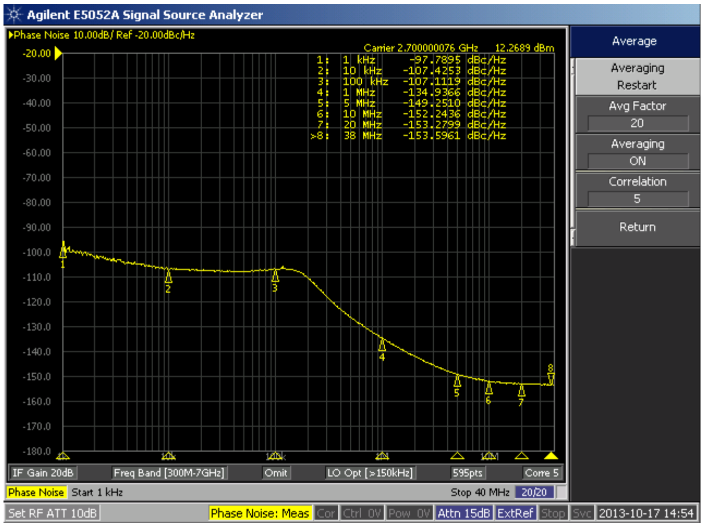


Figure 51.

6 Bill of Materials

Table 3. LMX2581 Bill of Materials

Schematic Rev A, Assembly Variant 001 Generated 9/13/2013					
Designator	**Description**	**RoHS**	**Manufacturer**	**Part Number**	**Qty**
!PCB	Printed Circuit Board	Y	Any	SV601009	1
C1, C5	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	Y	TDK	C1608X7R1C105K	2
C1_LF	CAP, CERM, 1800pF, 100V, +/-5%, X7R, 0603	Y	AVX	06031C182JAT2A	1
C2_LF	CAP, CERM, 0.056uF, 16V, +/-10%, X7R, 0603	Y	MuRata	GRM188R71H563KA93D	1
C4_LF	CAP, CERM, 3300pF, 100V, +/-10%, X7R, 0603	Y	AVX	06031C332KAT2A	1
C6, C29, C32	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	Y	Kemet	C0805C106K8PACTU	3
C8, C9, C17, C18, C19, C20, C23, C24, C25, C26, C27, C28, C31, C34	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	Y	Kemet	C0603C101J5GACTU	14
C10, C30, C33	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	Y	AVX	0603YC104JAT2A	3
C11, C13	CAP, CERM, 10uF, 10V, +/-10%, C0G/NP0, 0603	Y	TDK	C1608X5R1A106M	2
C12, C14	CAP, CERM, 22uF, 10V, +/-20%, X5R, 0603	Y	Samsung	CL10A226MP8NUNE	2
C15, C16	CAP, CERM, 2.2uF, 10V, +/-10%, X5R, 0603	Y	Kemet	C0603C225K8PACTU	2
D2	LED, Green, SMD	Y	Lite-On	LTST-C190GKT	1
L1, L2	Inductor, Multilayer, Air Core, 18nH, 0.3A, 0.36 Ω, SMD	Y	MuRata	LQG15HS18NJ02D	2
L3, L4	3A Ferrite Bead, 120 Ω @ 100MHz, SMD	Y	MuRata	BLM18SG121TN1D	2
OSCin, RFoutA+, RFoutA-, RFoutB+, RFoutB-, Vcc	Connector, SMT, End launch SMA 50 ohm	Y	Emerson	142-0701-851	6
R2_LF	RES, 390 Ω, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603390RJNEA	1
R3_LF	RES, 270 Ω, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603270RJNEA	1
R4_LF, R12, R17, R18, R19, R20, R21, R22, R24, R25, R27, R28, R29, R30, R39	RES, 0 Ω, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW06030000Z0EA	15
R6	RES, 10 Ω, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060310R0JNEA	1
R14	RES, 47 Ω, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060347R0JNEA	1
R15	RES, 18 Ω, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060318R0JNEA	1
R16	RES, 33 Ω, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060333R0JNEA	1
R23, R26	RES, 51 Ω, 5%, 0.063W, 0402	Y	Vishay-Dale	CRCW040251R0JNED	2

Table 3. LMX2581 Bill of Materials (continued)

Schematic Rev A, Assembly Variant 001 Generated 9/13/2013					
R31	RES, 330 Ω, 5%, 0.1W, 0603	Y	Yageo America	RC0603JR-07330RL	1
R35, R37, R41, R42, R46	RES, 10k Ω, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060310K0JNEA	5
R36, R38, R40, R43, R47	RES, 12k Ω, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060312K0JNEA	5
S1, S2, S3, S4, S5	HEX STANDOFF SPACER, 9.53 mm	Y	Richco Plastics	TCBS-6-01	5
U1	LMX2581 Wideband Frequency Synthesizer	Y	Texas Instruments	LMX2581SQ/NOPB	1
uWire	Header (shrouded), 100mil, 5x2, Gold-plated, SMD	Y	FCI	52601-S10-8LF	1
Vcc_TB	Terminal Block, 10.76x17x11 mm, 2POS, 26-12AWG, TH	Y	Weidmuller	1592820000	1
Y1	OSC 100.0000MHZ 3.3 V +-25PPM SMD	Y	Connor-Winfield	CWX813-100.0M	1

Revision History

This Revision History highlights the technical changes made to the **SNAU136A** document to make it the **SNAU136B** revision.

SNAU136 Revisions

SEE	ADDITIONS/MODIFICATIONS/DELETIONS
SNAU136C	**General Comments:** The evaluation board was updated to accommodate the USB2ANY header and was also conducted on FR4 instead of Rogers4003. Modifications to components and their placement, such as moving C4_LF next to the Vtune pin and pulling back the ground and power planes from the vias to minimize spurs were also implemented.
Section 2.3	Updated to show USB2ANY programming interface
Section 5.2	Updated VCO phase noise plots
Section 5.6	Added plots on output power
Section 5.7	Added plots for wider bandwidth
Section 3.2	Schematic Information Added
Section 4	Layout Information Added
Table 3	Bill of Material and Assembly Information Added
Section 3.3	Added comments about use with external signal.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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