National Semiconductor

ADC12D1X00RFRB
Reference Board Users' Guide
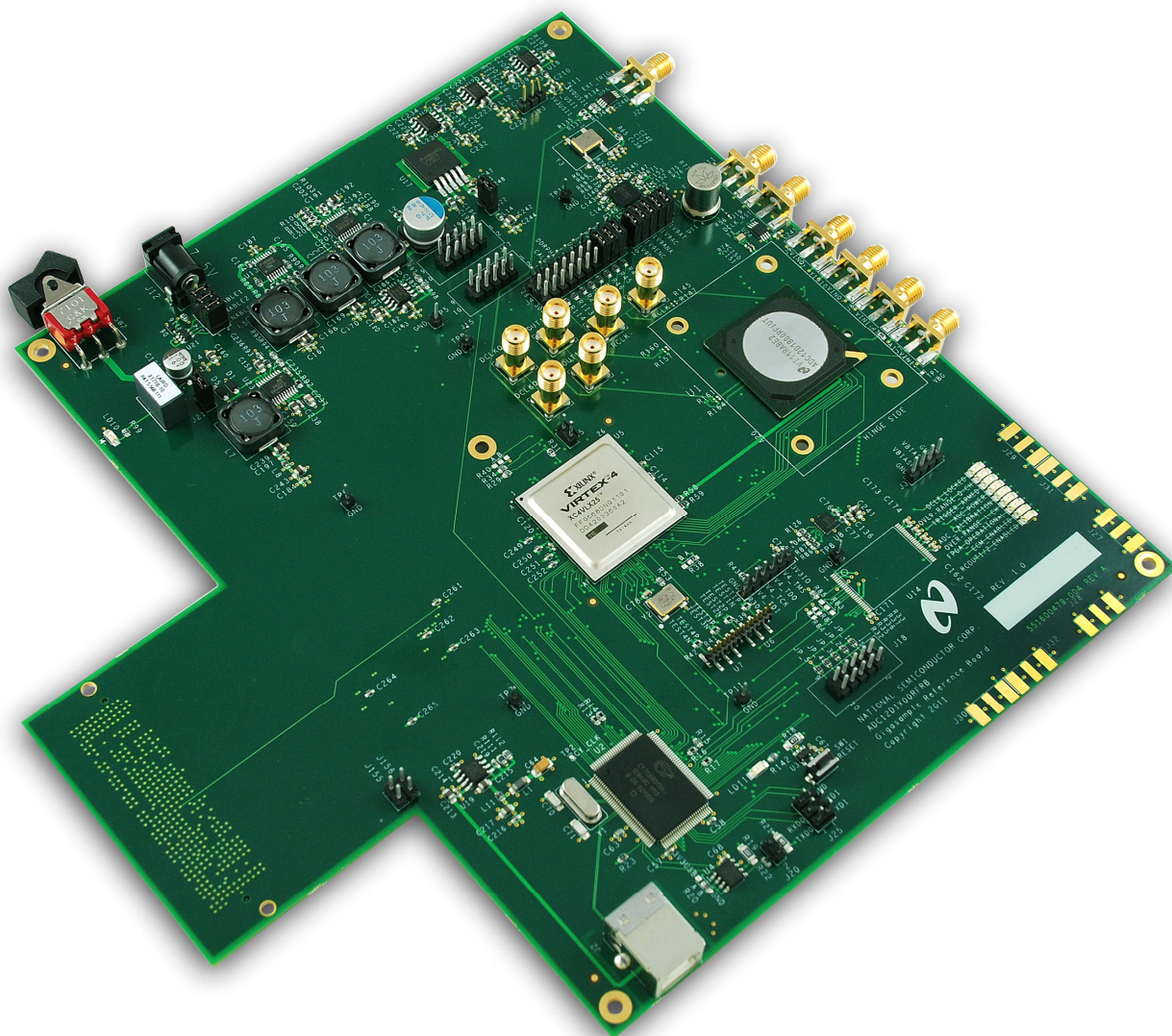
Table of Contents

1.0 Overview

The ADC12D1X00RFRB demonstrates a high-performance signal acquisition sub-system that achieves 12-bit resolution and corresponding SNR and dynamic range on two channels at signal frequencies in excess of 1.0 GHz and sampling rates of at least 1.6/1.8 GS/s or one channel at a sampling rate of 3.2/3.6 GHz. The board showcases the following National Semiconductor devices:

- **ADC12D1X00RF** analog-to-digital converter
- **LMX2531** clock synthesizer
- **LP3878** and **LP38513-ADJ** linear LDO regulators
- **LM20242**, **LM25576** and **LM26400** switching regulators
- **LM3880** power sequencing controller
- **LM95233** temperature sensor

In addition, the board also employs the **Xilinx XC4VLX25-11FFG668 Virtex-4** FPGA for the critical function of capturing the high-speed digital data sourced by the ADC.

1.1 Features

❑ Demonstrates the ADC12D1X00RF's typical dynamic performance – see the datasheet for full details.

❑ Dual channel sample rates of up to 1.6/1.8 GS/s (limited by the ADC specifications and the FPGA capture limitations)

❑ Single channel (Interleaved) sample rates of up to 3.2/3.6 GS/s (limited by the ADC specifications and the FPGA capture limitations)

❑ FMC Expansion Header for streaming data capture

❑ SMA I/O for easy AutoSync feature evaluation

❑ External Hardware Trigger

❑ Updated Status LEDs

❑ On-board LMX2531 based clock circuit with a connector for a selectable external clock

❑ A complete high-performance low-noise power management section for the ADC, clock circuit, FPGA and USB controller

❑ Single +7.5V power adapter input

❑ Simplicity and performance of USB 2.0 connection to the PC

❑ Functions with National's latest WaveVision 5 signal-path control and analysis software

1.2 Packing List

The ADC12D1X00RFRB kit consists of the following components:
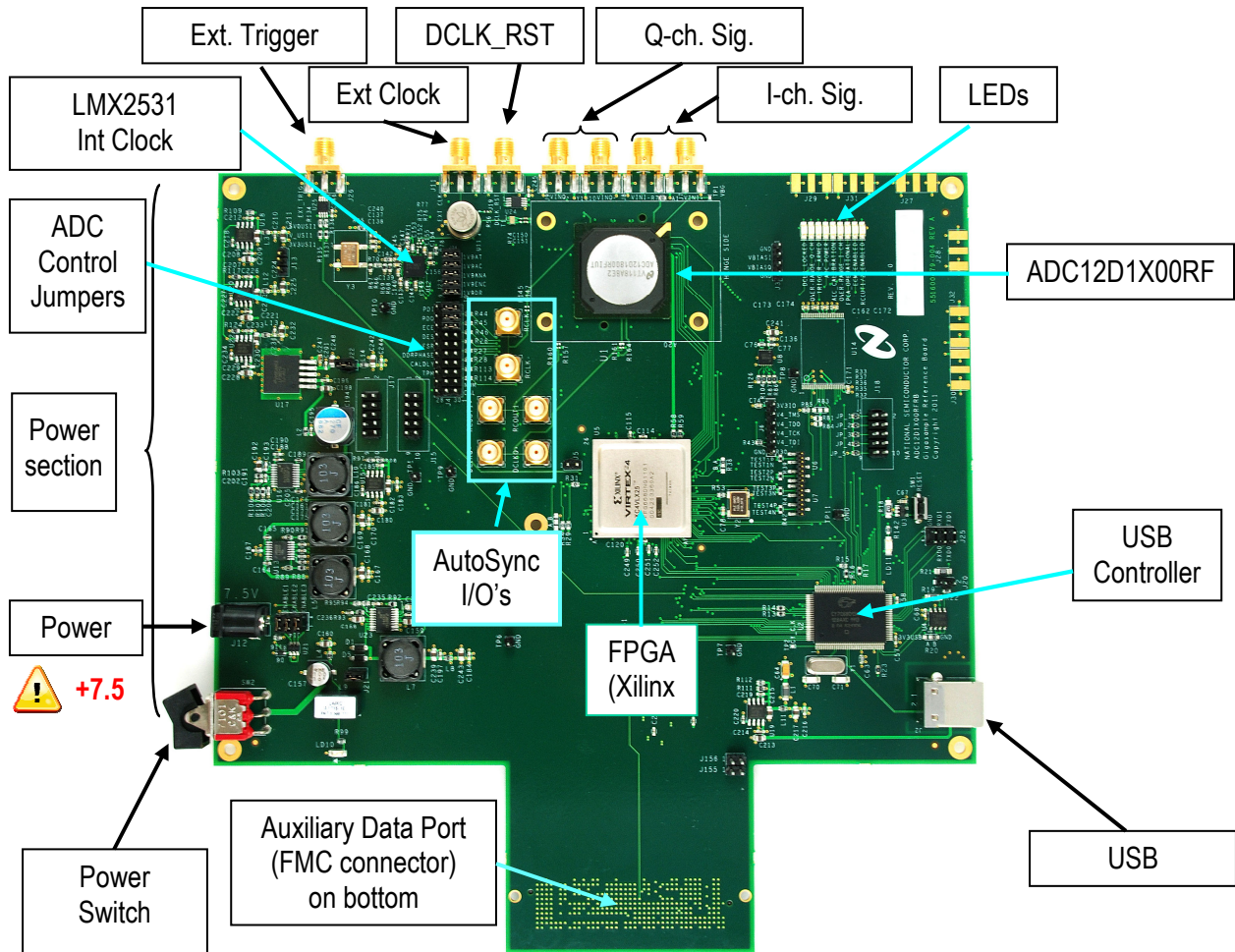- ADC12D1X00RFRB Board
- Documentation on CD Including
  - ADC12D1X00RFRB Users Guide (this document)
  - Wavevision 5 Software
  - ADC12D1X00RFRB schematic & layout
  - ADC12D1X00RFRB bill of materials
  - ADC12D1X00RFRB performance plots
  - FPGA source code
  - Balun datasheets
- Hardware Kit Including
  - 110V-240V AC to +7.5V DC Power Adapter
  - USB cable
  - 4 – DC blocks
  - 2 – 50Ω terminators
  - 1 – Anaren balun board (useful bandwidth of 400 MHz to 3 GHz)
  - 1 – Mini-Circuits balun board (useful bandwidth of 4.5 MHz to 3 GHz)
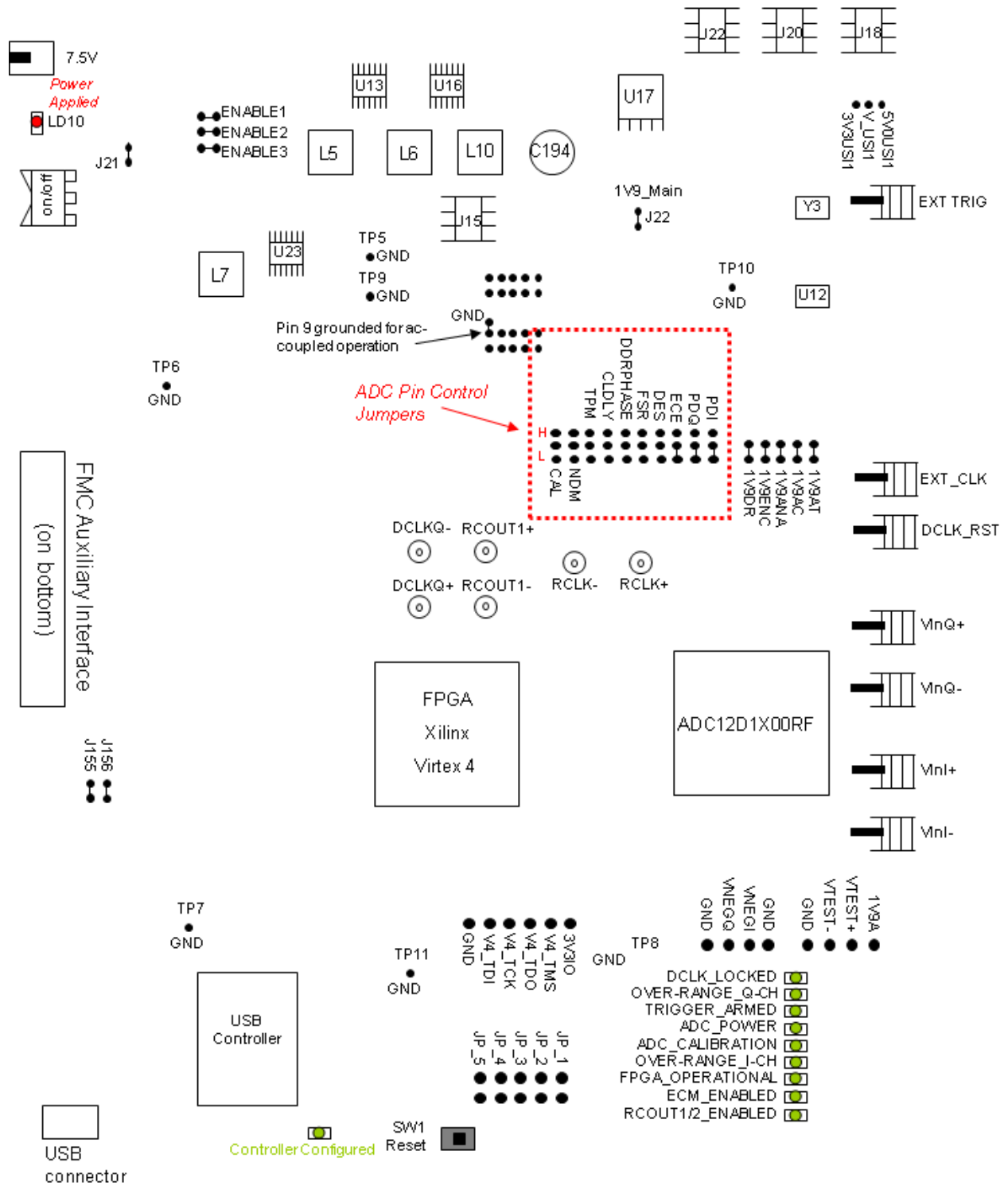 - 4 – 6" SMA cables

1.3 References

- *ADC12D1X00RF datasheet
- *LMX2531 datasheet
- *Application Note 2132: Synchronizing Multiple GSPS ADCs in a System: The AutoSync Feature

*Note: Please refer to www.national.com for the latest edition of all datasheets / application notes.

1.4 Board Orientation

Ext. Trigger

DCLK_RST

Q-ch. Sig.

LMX2531
Int Clock

Ext Clock

I-ch. Sig.

LEDs

ADC
Control
Jumpers

ADC12D1X00RF

Power
section

AutoSync
I/O's

USB
Controller

Power

FPGA
(Xilinx

⚠ **+7.5**

Power
Switch

Auxiliary Data Port
(FMC connector)
on bottom

USB

**Figure 1: ADC12D1X00RFRB Board Layout**

Figure 2: Jumpers and LEDs

2.0 Quick Start

This section will aid in bringing up the board for the first time as well as a brief tutorial on the WaveVision 5 (WV5) software. Further description of the Reference Board is in subsequent sections of this document. The software is further described in the WaveVision 5 Users' Guide or the HELP function within the software. The ADC12D1X00RF and LMX2531 datasheets should be consulted for detailed understanding of device functionality.

The user is advised to construct a lab setup as close to the one shown in Figure 3 as possible. This setup, along with the board and software configuration described below, is what was used to test the reference board at National's lab. This set of conditions produces the stated reference performance - which is normally included with each board shipped to customers. The objective is to assure that the user can achieve the same performance as that recorded at National's lab prior to board shipment.

Figure 3: Recommended lab setup. A filter may not be necessary on the clock if the generator is very clean (beyond -80dBm SFDR).
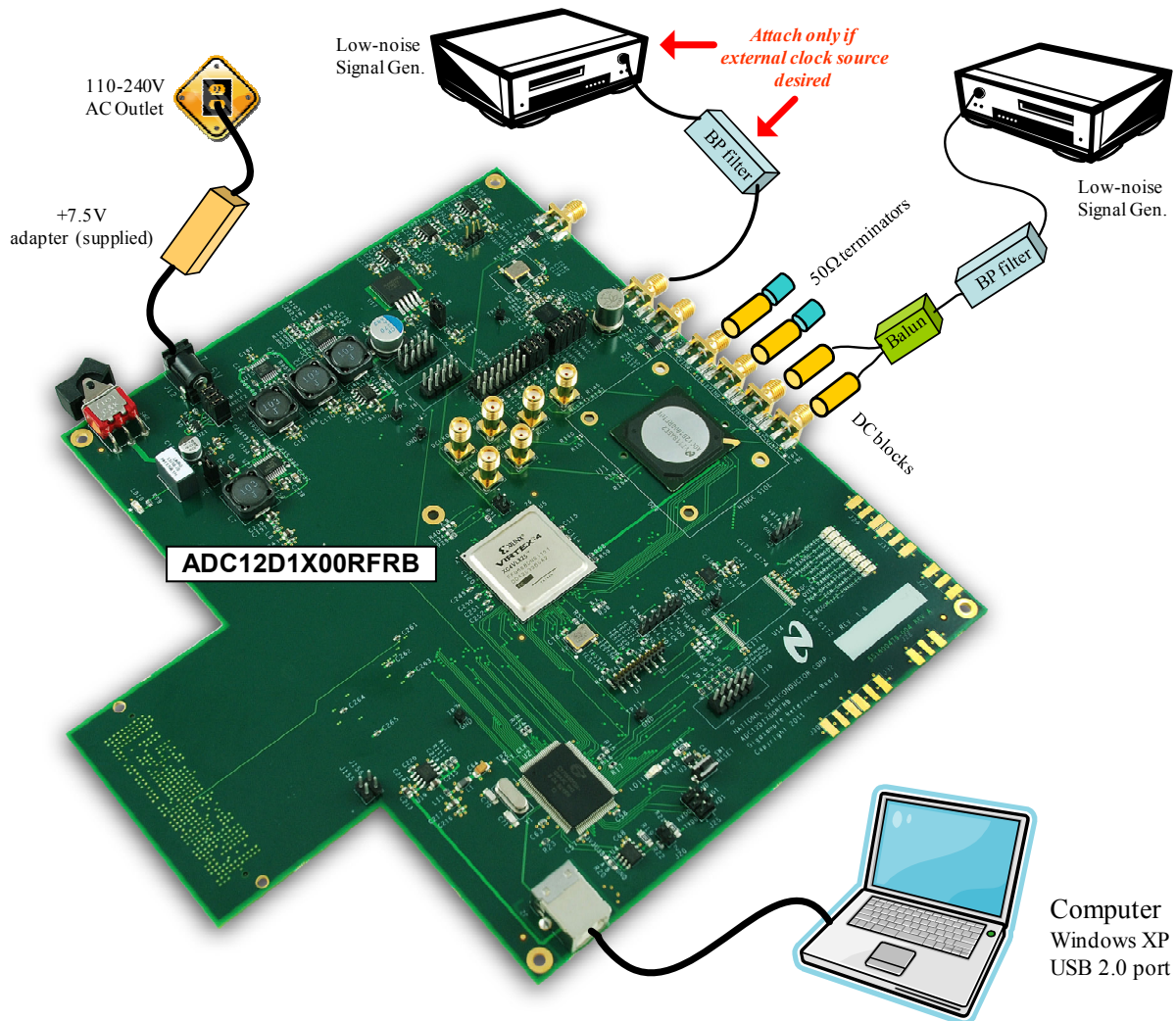
2.1 Installing the WaveVision 5 Software

(Note: The WaveVision 5 software requires Windows XP 32-bit operating system)
1. Insert the included WaveVision 5 CD-ROM into the computer CD drive.
2. Locate, unzip and run the install.bat program on the CD-ROM.
3. Follow the on-screen instructions to complete the installation.

2.2 Installing the ADC12D1X00RFRB Hardware

1. Place the ADC12D1X00RFRB Reference Board on a clean, static-free surface.
2. Make sure the board's jumpers are configured as follows as shown in Figure 2:
   a. For the ADC, the "ECE (Extended Control Enable, active low)" jumper should be installed in the LOW position. This enables SPI control of the ADC.
   b. Pin 9 on J15 must be connected to Ground for ac-coupled operation. The board ships with this jumper in place as it is configured for ac-coupled operation only. (The jumper is removed for dc-coupled operation. In that case the applied signal must be dc-coupled, and have the common mode DC voltage set to the required ADC12D1X00RF V_{CM} voltage.)
   c. The PDI and PDQ jumpers must be in place as shown to enable both channels of the ADC.
3. Connect the enclosed +7.5V DC power adapter to the power jack. Connect the other side of the power supply to an AC outlet (100-240 VAC, 50-60 Hz).
4. Connect the input signal generator, the band-pass filter, the balun and the DC blocks to the ADC12D1X00RFRB Reference Board's I-channel input connectors. Set the signal generator at one of the frequencies and signal levels stated in the reference performance report. Always use high-quality RF SMA cables for optimum performance.

> ⚠️ *Do not overdrive the signal and clock inputs as the ADC may be damaged. Refer to the Electrical Specification section of the datasheet for the voltage tolerance of these inputs. Including insertion loss from filters, baluns, cables, DC blocks, etc. input power should not exceed operating limits as found in the datasheet.*

5. In the National lab, the following (or equivalent performance) equipment are used to test the board. It is essential that the customer use signal generators, filters, DC blocks and a balun of equivalent or better performance.
   o Rohde & Schwarz SME-03 or SMA-100 signal generator
   o Filters - Trilithic 5VF 5% tunable bandpass filter or other fixed frequency bandpass filter of equivalent performance
   o Balun – Anaren Balun Board
   o DC blocks – Mini Circuits BLK-89 S+
   o 50 Ω terminators – Mini Circuits ANNE 50+

   Note: The board comes equipped with DC-blocks applied to the I-channel signal input connectors and DC blocks and terminators applied to the unused Q-channel input connectors. These must be used at all times - that is, the channel being used must be connected through dc-blocks if the ADC is configured for ac-coupled operation (as shipped). The unused channel must also be DC blocked then terminated to ac ground. This is graphically illustrated in Figure 3.
6. Turn on the SW2 rocker power switch. Verify that the red LED (labeled LD10, near the J12 power jack) is lit.
7. Connect the supplied USB 2.0 cable from the PC USB port to the ADC12D1X00RFRB USB jack.

2.3 Launch the WaveVision 5 Software.

Start the WaveVision 5 software on your computer by selecting the desktop icon "WaveVision 5" or by clicking on the Start button, and selecting

```
Programs -> WaveVision 5 -> WaveVision 5
```

The software will automatically detect the board and load the appropriate software profile and will proceed to download the controller firmware and FPGA code onto the reference board. As an alternative, the icon on the desktop can be used to launch WaveVision 5. The WaveVision 5 user interface will appear on the computer screen.

The status LED's should take on the following states when the system is initially powered up, Wavevision 5 has loaded the FPGA image and the system is ready for an acquisition:
(Where green is *on,* black is *off*)

DCLK_LOCKED 🟢
OVER-RANGE_Q-CH ⚫
TRIGGER_ARMED ⚫
ADC_POWER 🟢
ADC_CALIBRATION ⚫
OVER-RANGE_I-CH ⚫
FPGA_OPERATIONAL 🟢
ECM_ENABLED 🟢
RCOUT1/2_ENABLED ⚫

NOTE: The status of LED's are valid, only if the **FPGA_OPERATIONAL** LED is lit

Meaning of the status LED's:
- **DCLK_LOCKED**: If FPGA detects DCLKI and DCLKQ toggling, this LED lights.
  NOTE: If the board has been modified for AutoSync to route DCLKQ to the SMA's, this LED will not be lit.
- **OVER-RANGE_Q-CH**: ADC's overrange Q-ch pin pulse stretched to around a half second when overranged.
- **TRIGGER_ARMED**: Lights when "H/W Trigger" is checked inside the Wavevision 5 GUI. Does not clear upon data capture.
- **ADC_POWER**: Lights when ADC supply voltage of 1.9V is detected.
- **ADC_CALIBRATION**: Will light temporarily when calibration is run. ADC's CalRun pin is pulse stretched to about a half second.
- **OVER-RANGE_I-CH**: ADC's overrange I-ch pin pulse stretched to around a half second when overranged.
- **FPGA_OPERATIONAL**: Lights when FPGA's 100MHz reference is locked and FPGA is out of reset.
- **ECM_ENABLED**: Lights when ADC is in Extended Control Mode.
- **RCOUT1/2_ENABLED**: Lights when AutoSync RCOUT1/2 clocks are detected. Enabled when AutoSync-> DOC (disable output clocks) bit is unchecked in Wavevision 5 GUI.

2.4 WaveVision 5 - User Interface Overview
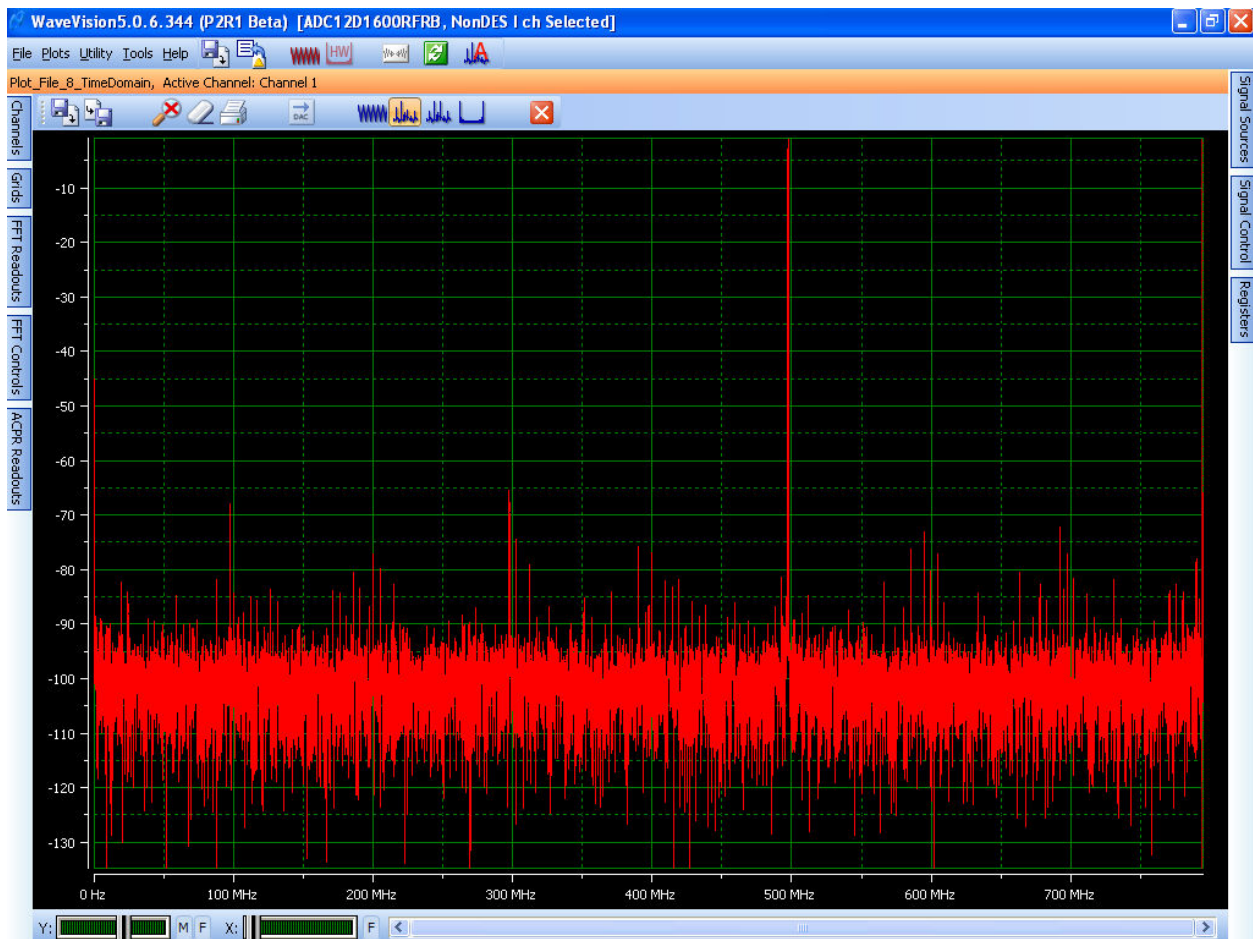
Figure 4: WaveVision 5 Example Window

Figure 4 above shows the WV5 user interface panel (GUI). This is the top level interface panel. It is arranged in such a way that the plot is always in the middle. There are tabs arranged on each side of the window to give the user additional information or control of features.

The tabs available on the **left side** access panels that are pertinent to the current plot window - such as *channel selection*, *grid selection*, *FFT Readouts*, and *FFT controls*.

The **right side** panels allow the user to take control of the hardware. These include the *Signal Source*, *Signal Control* and *Registers* panels (the most relevant for this board).

In addition, a small FFT parameter summary box can be displayed by pressing CTL-R.

For more details on the general operation and use of WaveVision 5, please refer to the **WaveVision 5 Users Guide**.

2.5 System / Device Configuration

Prior to capturing data, confirm that the board is in the "ECE (Extended Control Enable)" mode, The ECE jumper is located in the ADC pin control jumper area as shown in Figure 2. The board should be sent with this jumper in place. This means that the ADC will be controlled through the SPI interface and not with jumpers driving the control pins. This allows the user to control the ADC's behavior through the WaveVision 5 Registers panel.

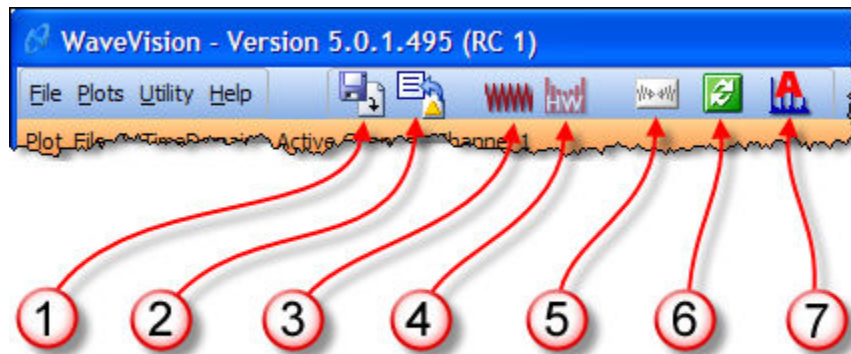**Figure 5: WaveVision 5 overview of control buttons**

Figure 6: WaveVision 5 main window command buttons

2.5.1 Main Panel

The main menu bar of the WaveVision 5 software has several control buttons as shown in Figures 5 and 6, which may be used to perform most tasks with a button click.

1 - Load Plot
A new plot window is created and the Plot Load dialog is displayed. The selected plot file is loaded into the new window.

2 - Import Data
Clicking this button creates a new time-domain plot and opens the Import Data dialog. Data may be imported from WaveVision 4 data files as well as from ASCII data files created by other programs.

3 - Create a New Time Domain Plot
Clicking this button creates a new time-domain plot. The plot will contain no data, but is available as a data destination.

4 - Create a New Hardware Histogram Plot
Clicking this button creates a new hardware histogram plot. Hardware histograms are available only in conjunction with evaluation boards which can gather histogram data internally. This button is enabled only when an evaluation board which supports hardware histograms is attached.

5 - Acquire Data
Click this button to acquire data to the active plot. If you have created more than one plot, the Active plot has a highlighted title bar.

6 - Continuous Acquisition
This button is a toggle - when it is pressed, data is acquired continuously, one buffer after another as fast as the hardware can go; when pressed again data acquisition stops. When in continuous acquisition mode, acquisition may be started and stopped using the Acquire button without leaving the continuous acquisition mode.

7 - FFT Averaging
This button is also a toggle - when it is pressed, FFT's are averaged. The number of buffers to be averaged is specified in the hardware section of the Signal Sources tab.

Please refer to the **WaveVision 5 Users Guide** for more information.
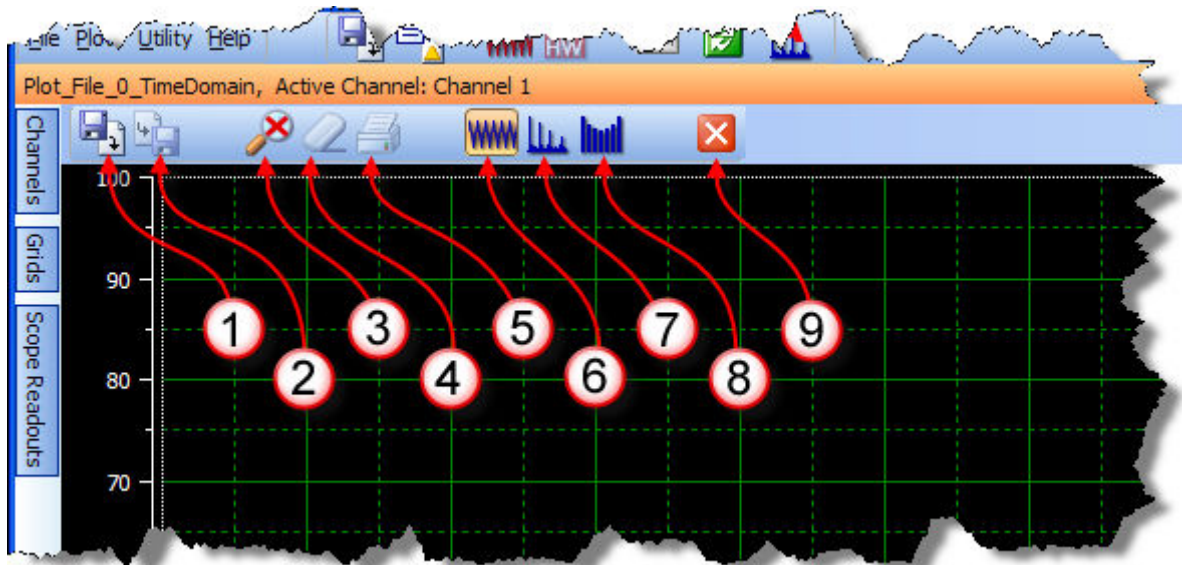
2.5.2 Plot Window Controls

Figure 7: WaveVision 5 plot window controls

1 - Load Plot
The Plot Load dialog is displayed, and the selected plot file is loaded into the new window.

2 - Save Plot
Displays the Plot Save dialog (this button is only active when the plot contains one or more channels with data).

3 - Reset Zoom
Reset X and Y axis zoom to 100%.

4 - Clear
Clear data from all channels.

5 - Print
Print the plot.

6 - Time Domain
Display the plot as time domain data.

7 - FFT
Display the plot as an FFT

8 – Histogram
Display a histogram of the data.

9 - Close
Close this plot.

## 2.5.3 Right Panels – Signal Source
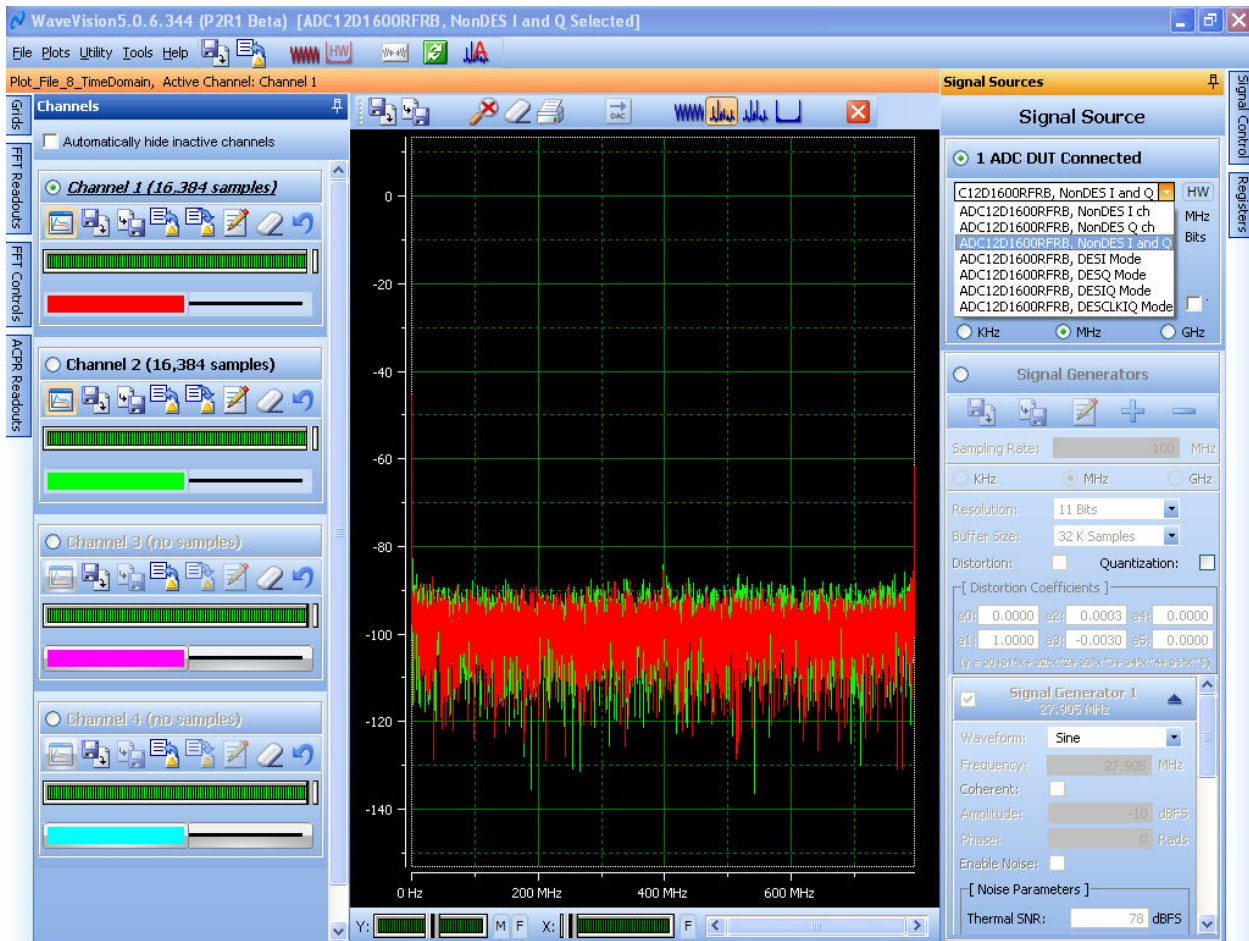
Figure 8a: WaveVision 5 main window command buttons

Open the *Signal Source* panel on the right side of the window and confirm that the ADC12D1X00RFRB is available and confirm that it is selected. There are seven possible modes of operation selectable here:

- NonDES I ch – Dual channel mode capturing and viewing the I-channel data
- NonDES Q ch – Dual channel mode capturing and viewing the Q-channel data
- NonDES I and Q – Dual channel mode capturing and viewing both the I- and Q-channel data
- DESI Mode – Double Edge Sample (interleaved) mode with I input
- DESQ Mode – Double Edge Sample (interleaved) mode with Q input
- DESIQ Mode – Double Edge Sample (interleaved) mode with I and Q as input – shorts both I and Q inputs together and must be externally driven by the same signal
- DESCLKIQ Mode – Sampling Clock samples the I- and Q-channels 180º out of phase with respect to one another – I and Q are not shorted together and must be externally driven by the same signal

Double Edge Sampling (DES) – Double edge sampling works much in the same way as single edge sampling except that the signals is sampled both on the rising and falling edge of the sample clock. This effectively doubles the sample rate. In this mode, both converters inside the ADC12D1X00RF work on a common input signal. The various DES modes are selected from the *Signal Source* tab on the right side and have requirements for how the inputs must be driven. See the datasheet for more details.

Note – When using "I and Q" mode, it is also necessary to select the *Channels* tab and deselect the "Automatically hide inactive channels" option box in order to allow both channels to appear on the plot. Alternatively, one channel may be displayed per plot:
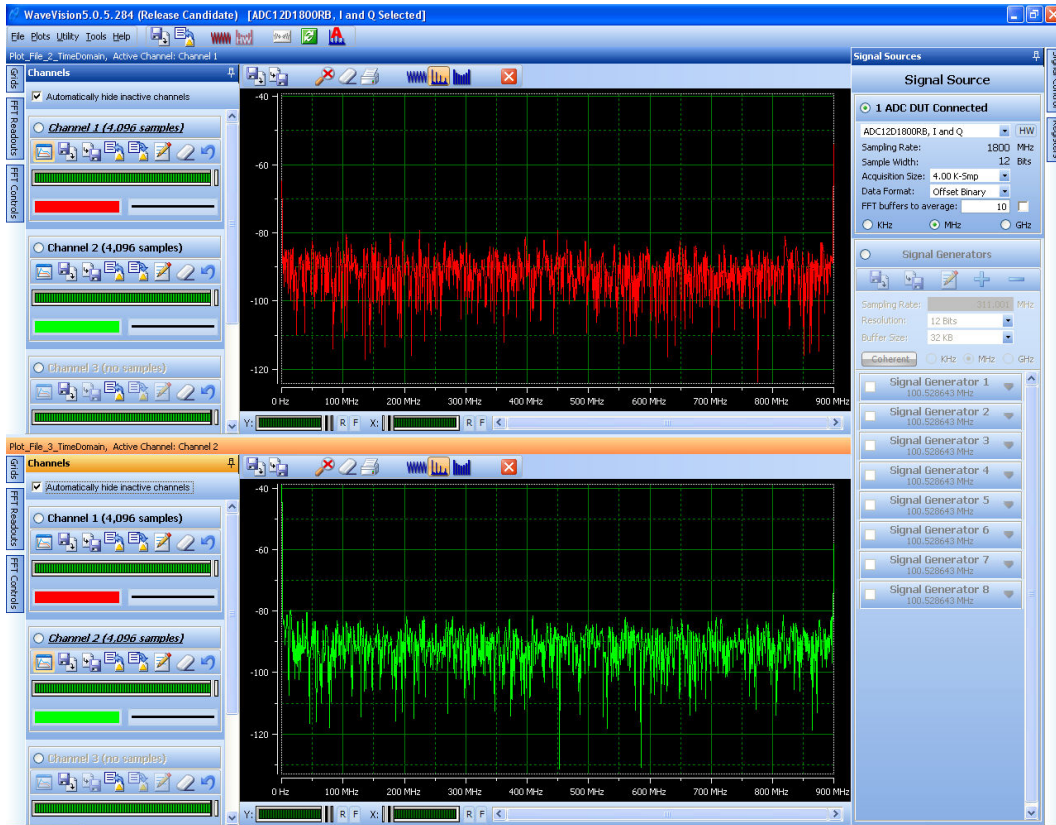
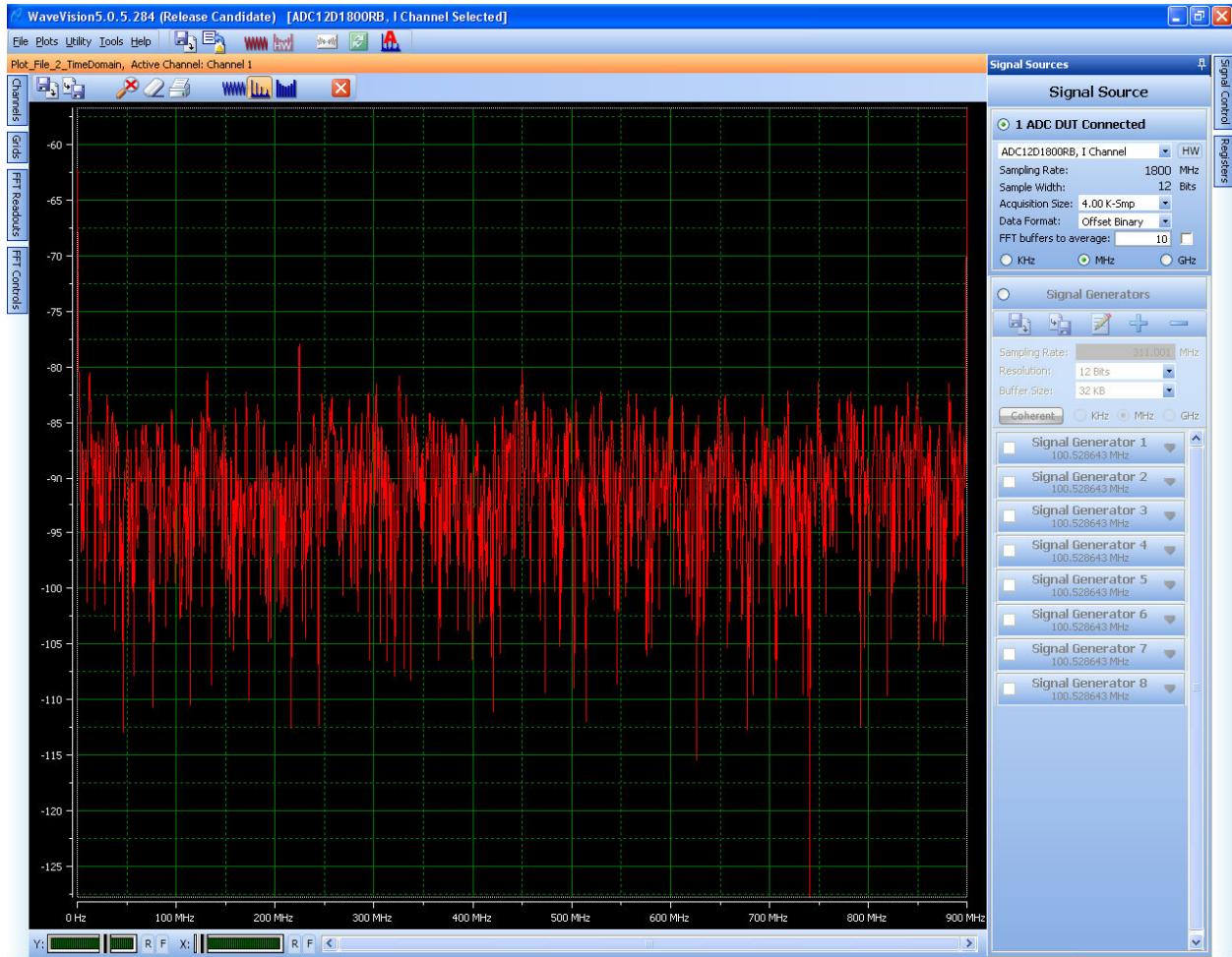**Figure 8b: I and Q mode – one channel displayed per plot**

**Figure 9: WaveVision 5 main window command buttons**

- **Sampling Rate** - When the signal source panel is selected, the clock frequency is displayed. This is initially the internal clock. In this example, 1800 MHz is generated by the LMX2531 on the reference board. The sampling rate is determined by the FPGA when the board is powered up. The calculation is accurate to better than 1%. If an external source is in use, confirm that this number corresponds to the clock reference that is applied. If it is not correct, subsequent data captures and display will not be correct.
- **Resolution** – This will always be set to the ADC12D1X00RF resolution which is 12 bits.
- **Acquisition Size** - This setting displays and selects the number of samples captured in each acquisition. 4K samples is the default, with settings up to 32K samples. A larger sample size increases the equivalent FFT bandwidth resolution, but at the expense of more memory and slower acquisition time.
- **Data Format** - The default data format is *offset binary* for the ADC12D1X00RF.
- **FFT buffers to average** - The last option is the FFT averaging function. Using this feature, subsequent samples can be averaged to obtain improved signal to noise. However, this is at the expense of time.

2.5.4 Right Panels - Registers

Next, configure the hardware (including the ADC) using the Registers control panel on the right side. This is the most important of all the panels for controlling the ADC12D1X00RFRB. This panel has twelve sub-tabs that control the settings of the board and registers inside the ADC12D1X00RF.   The twelve sub-tabs are shown below and include; *Settings, Config, Cal Adjust, I-channel, Q-channel, DES Adjust, t$_{AD}$ Adjust, AutoSync,* and *Temperature.* The last three tabs are register contents so that the user may verify register settings to be programmed in the system.
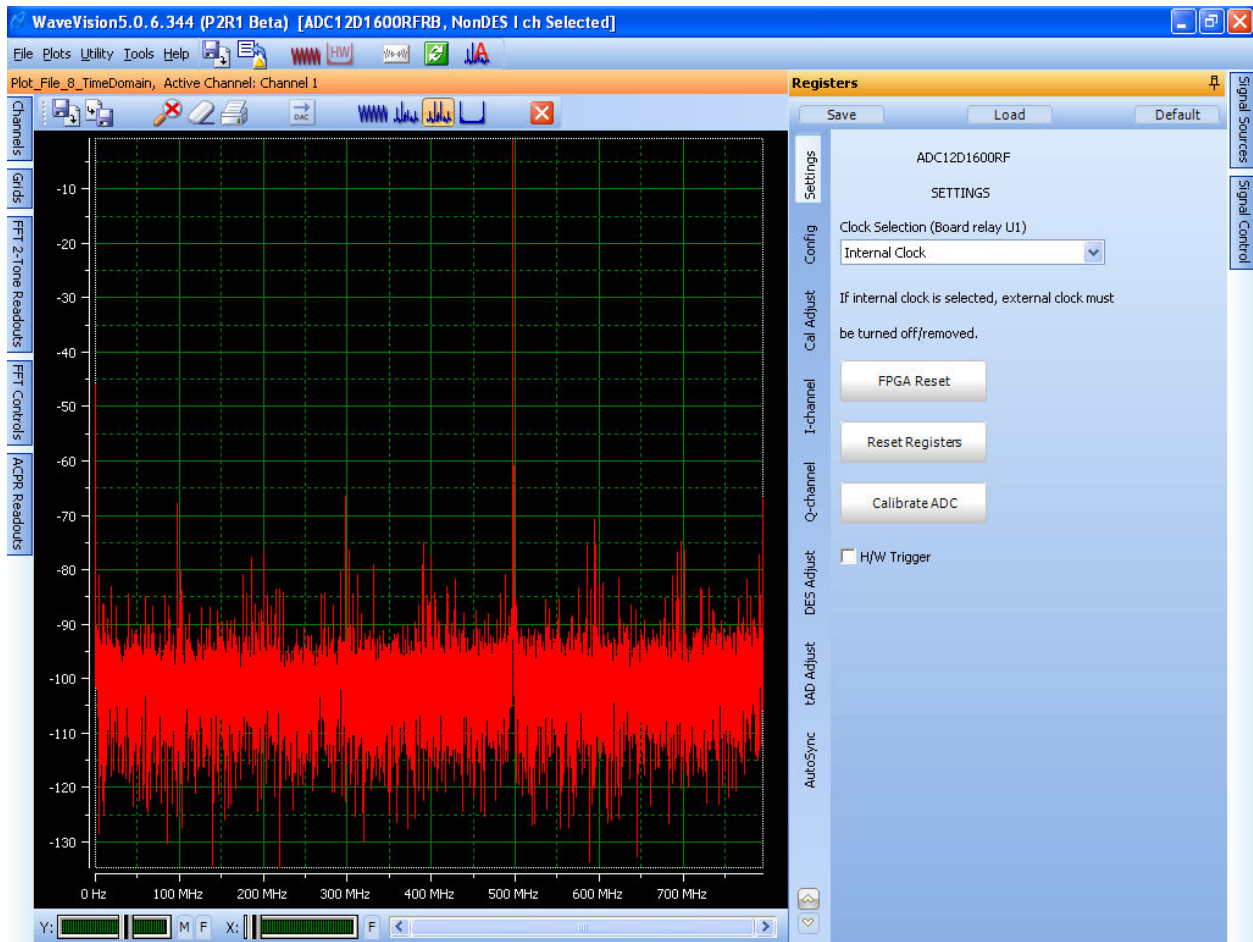
Figure 10: The top level of the Register panel showing the available tabs

The following is a short description of each tab under the ***Register*** panel.

Settings: This tab gives choice of either External Clock or Internal Clock, and buttons to initiate FPGA Reset, Reset Registers and Calibrate ADC. Calibration of the ADC should be performed if changes occur such as device temperature, mode changes (single channel to dual channel, single edge sampling (Non-DES) to double edge sampling (DES). For more information, refer to the Calibration section of the ADC12D1X00RF datasheet. The H/W Trigger function is also enabled using the check box on this tab.

Note: If the Internal Clock is selected, then the External Clock signal generator should be disconnected or switched off to prevent performance degradation.

Config: This tab configures various features and modes of the ADC12D1X00RF and is shown below. It accesses or changes the following functions, all of which are controlled through Configuration Register 1.
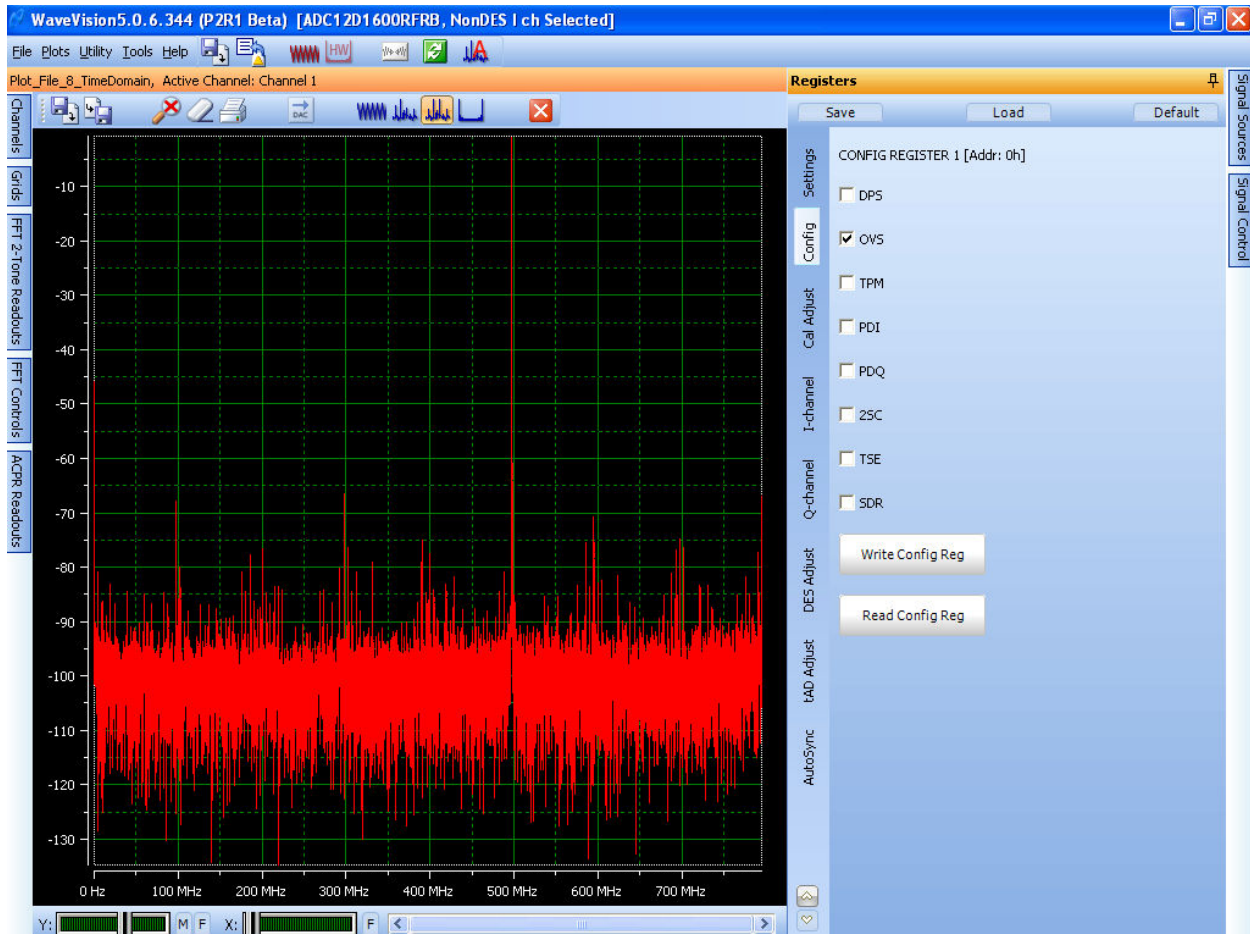

Figure 11: Config Panel

- **DPS** – DDR Phase Select –
  - In DDR, this determines the DDR Data-to-DCLK phase relationship. When unchecked, the 0° Mode is selected. When checked the 90° Mode is selected.
  - In SDR, when this box is unchecked data transitions on the Rising edge of DCLK and when checked data transitions on the Falling edge of DCLK.
- **OVS** – Output Voltage Select – Selects the LVDS differential output voltage. When this is unchecked, the reduced output amplitude is selected. When checked, the standard (higher) output amplitude is used.
- **TPM** – Test Pattern Mode – When checked the device will continually output a fixed pattern on the Data and OR outputs. When cleared, the normal ADC Data and OR information are output.
- **PDI** – Power down I Channel when checked.
- **PDQ** – Power down Q channel when checked.
- **2SC** – Two's Complement output mode is selected when checked. Default is offset binary.
- **TSE** – Check to enable Time Stamp feature.
- **SDR** – SDR mode when checked; DDR when unchecked. Default is DDR.
  Note: Will only work in DDR mode, unless FPGA is changed.

Note: No changes will take effect until the **Write Config Reg** button is clicked.

Cal Adjust: This tab controls the various adjustments which may be made to the Calibration feature.
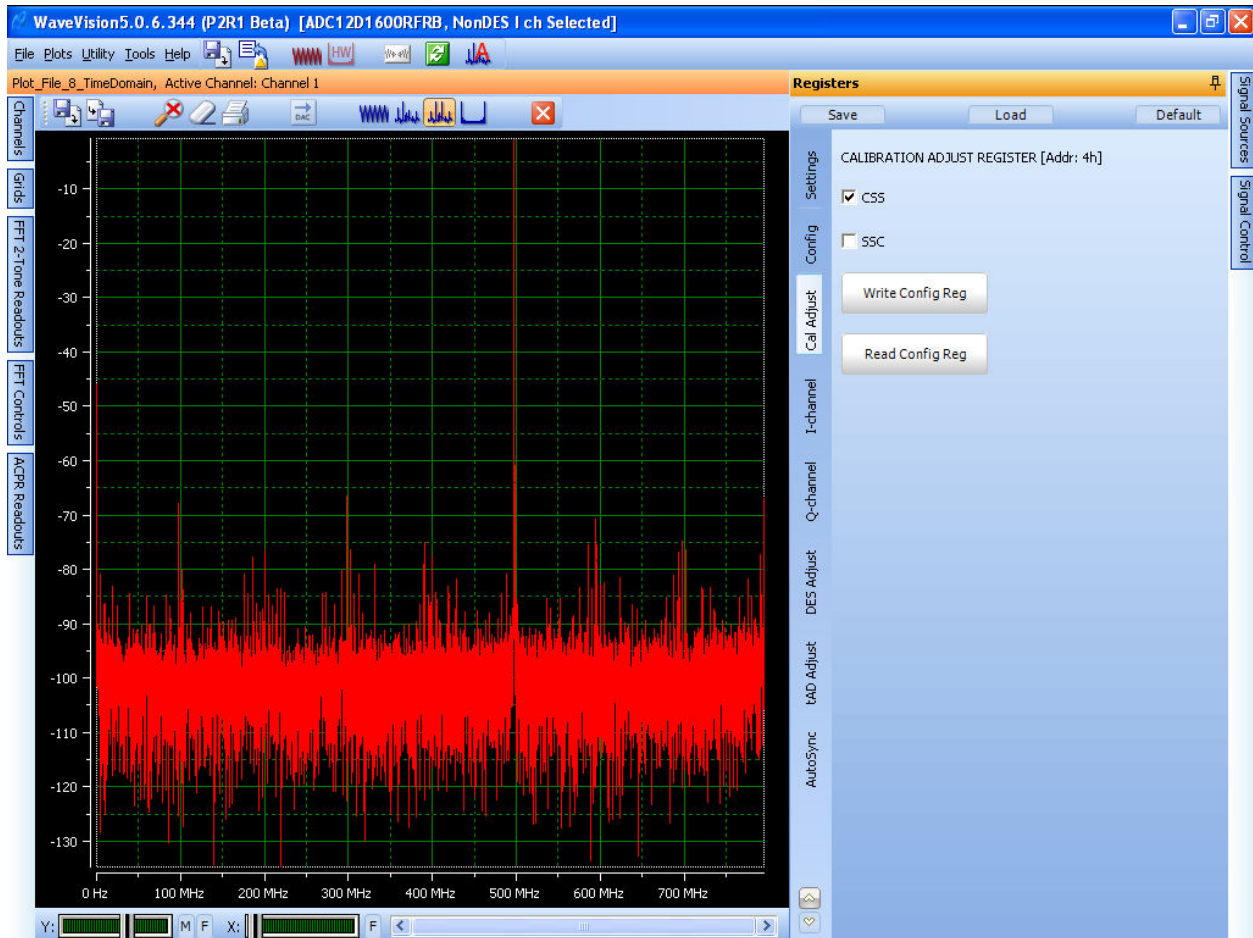

Figure 11a: Cal Adjust Panel

- **CSS** – Skip or include Rtrim calibration. When the Rtrim has been completed once, it is not necessary to do it again until the device is power cycled.
- **SSC** – Calibration control via the SPI, i.e. not the pin-controlled option for calibration.

Note: No changes will take effect until the **Write Config Reg** button is clicked.

I-channel: This tab changes the sign and the magnitude of the offset and the full scale range settings.
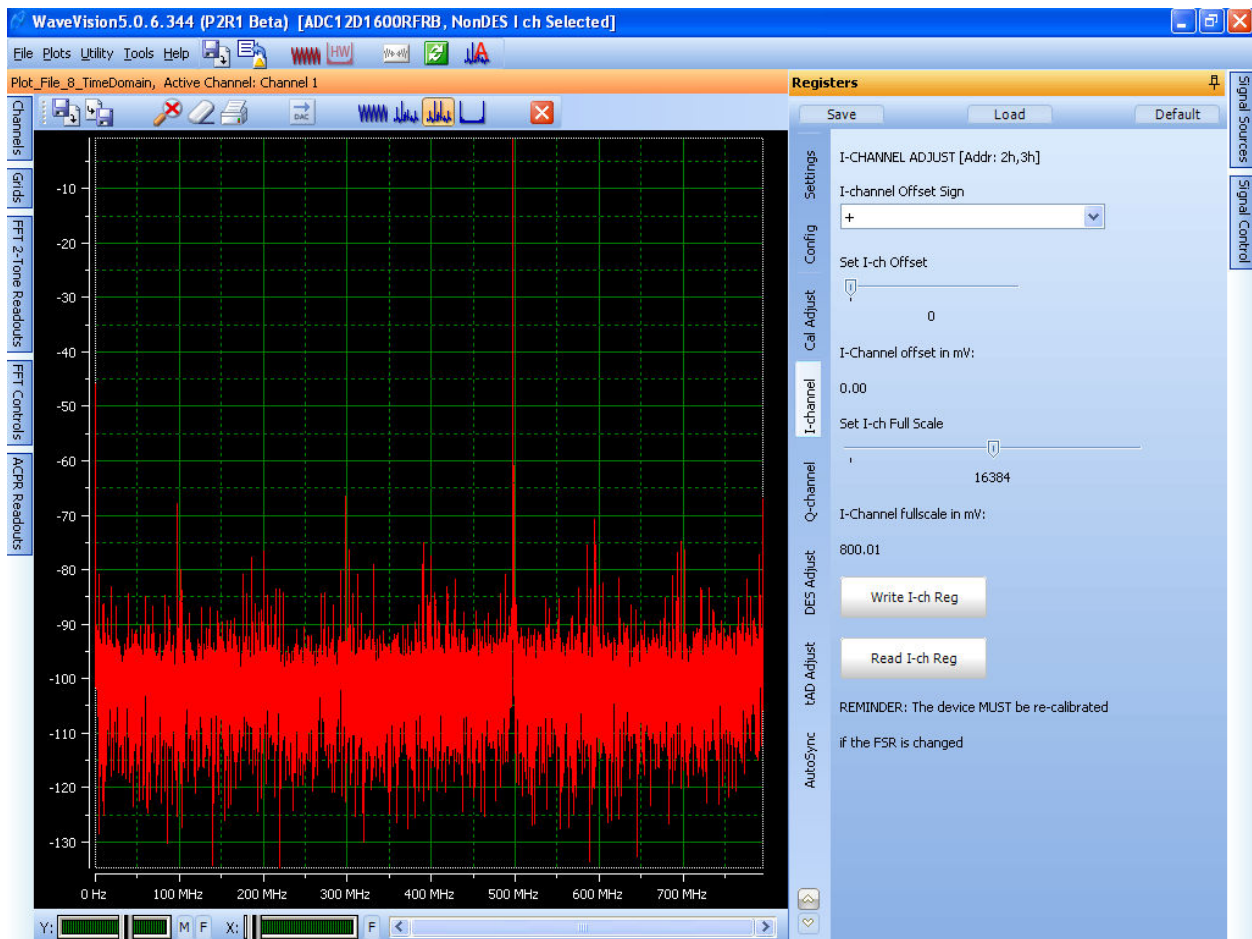
Figure 12: I-Channel Panel

- **I-channel Offset Sign** – This pull-down selects a positive or negative offset.
- **I-ch Offset** – This slider selects the magnitude of I-ch Offset applied. Adjustment can be done using the computer mouse/pointer, or using left/right arrow keys once the slider has been selected. Although the offset is entered in a 10 bit (0 to 4095) relative form, it is also displayed in approximate mV.
- **I-Channel Full Scale** - The approximate I-Channel input full scale range (mV peak-to-peak) is selected, ranging from a minimum of 600mV to a maximum of 1000mV. The default setting is 800mV.

Note: No changes will take effect until the **Write I-ch Reg** button is clicked. Also, the ADC must be re-calibrated if the full-scale is changed.

Q-channel: Similar to I-channel

DES Adjust: This tab controls the DES Mode time skew function.
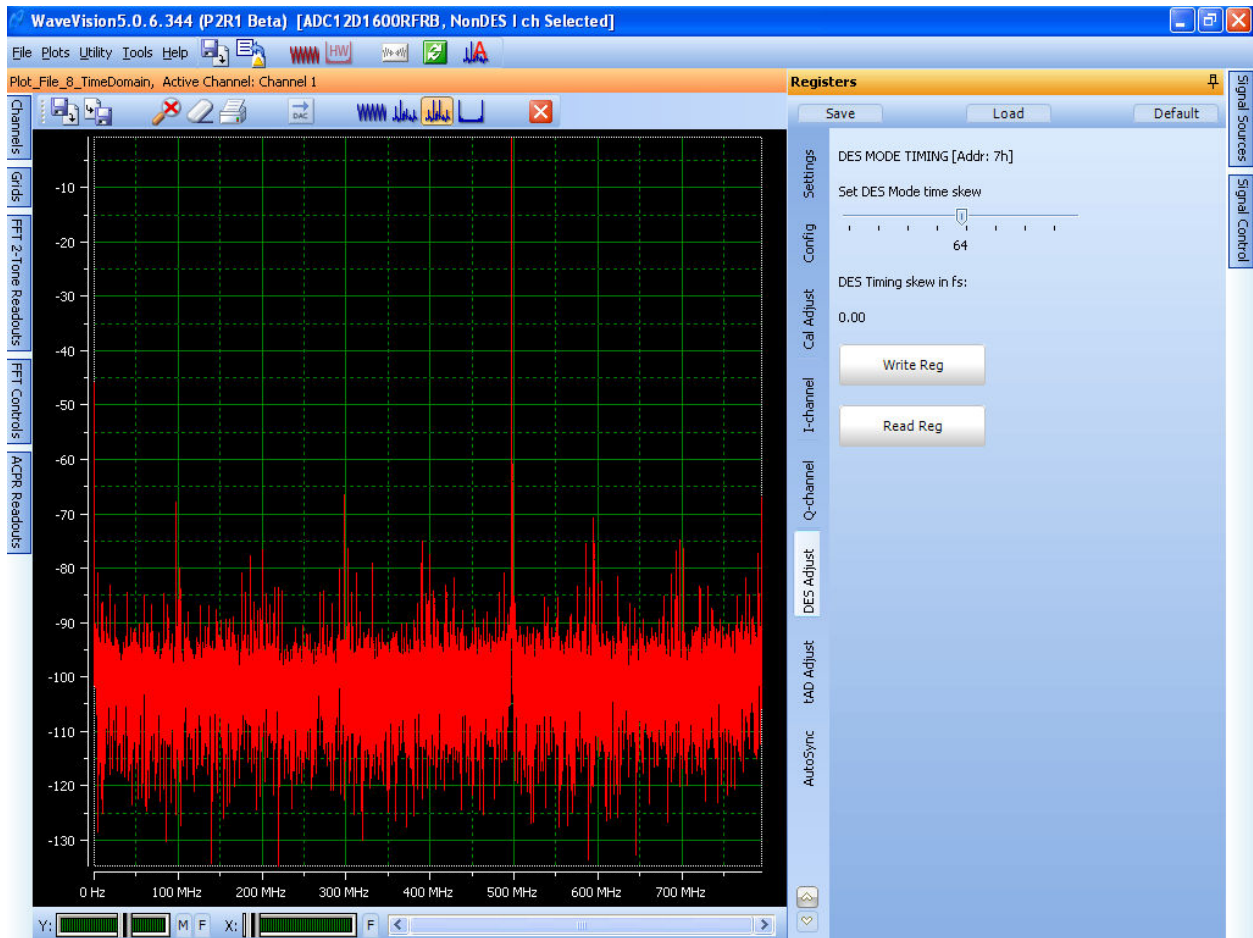
Figure 12a: DES Adjust Panel

Set DES Mode time skew – This slider adjusts the time skew between the falling edge sampling clock relative to the rising edge sampling clock in DES mode. Adjustment can be done using the computer mouse/pointer, or using left/right arrow keys once the slider has been selected. Although the time skew is entered in 8 bit (0 to 127) relative form, it is also displayed in approximate fs.

Note: No changes will take effect until the **Write Reg** button is clicked.

t$_{AD}$ Adjust: This tab controls the Aperture Delay function.
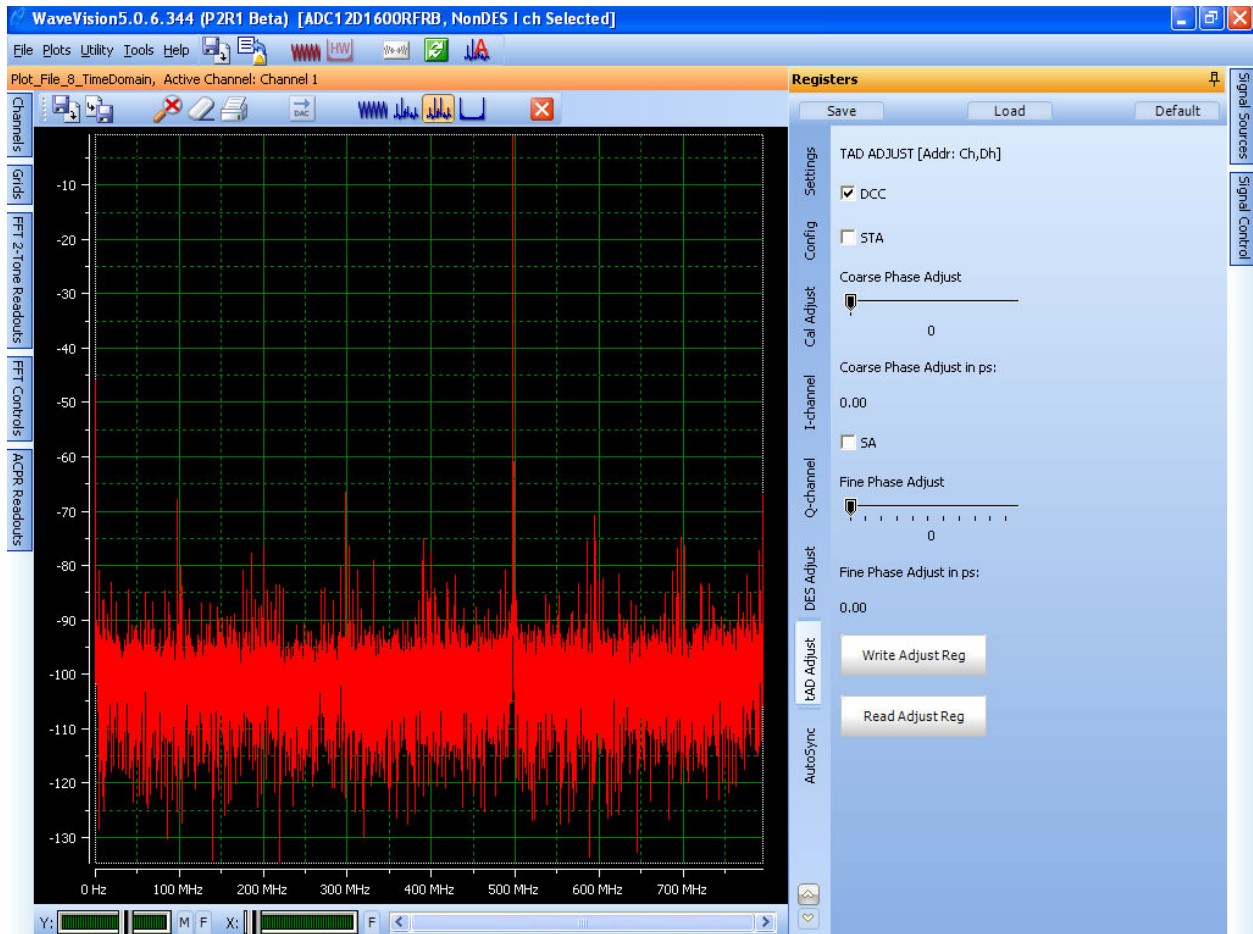
Figure 13: t$_{AD}$ Adjust Panel

- **DCC** – Duty Cycle Correction – When checked (default), the automatic Duty Cycle Correction circuit is enabled.
- **STA** - Select t$_{AD}$ Adjust – When checked, enables the Aperture Delay Time coarse adjust feature.
- **Coarse Phase Adjust** – Sets the approximate amount of coarse Aperture Delay applied.
- **Fine Phase Adjust** – Sets the approximate amount of fine Aperture Delay applied.
- **SA** – Select tAD Adjust – When checked, enables the Aperture Delay Time fine adjust feature. (Overrides the STA function)

Note: No changes will take effect until the **Write Adjust Reg** button is clicked.

AutoSync: This tab enables and controls the settings of the AutoSync feature.
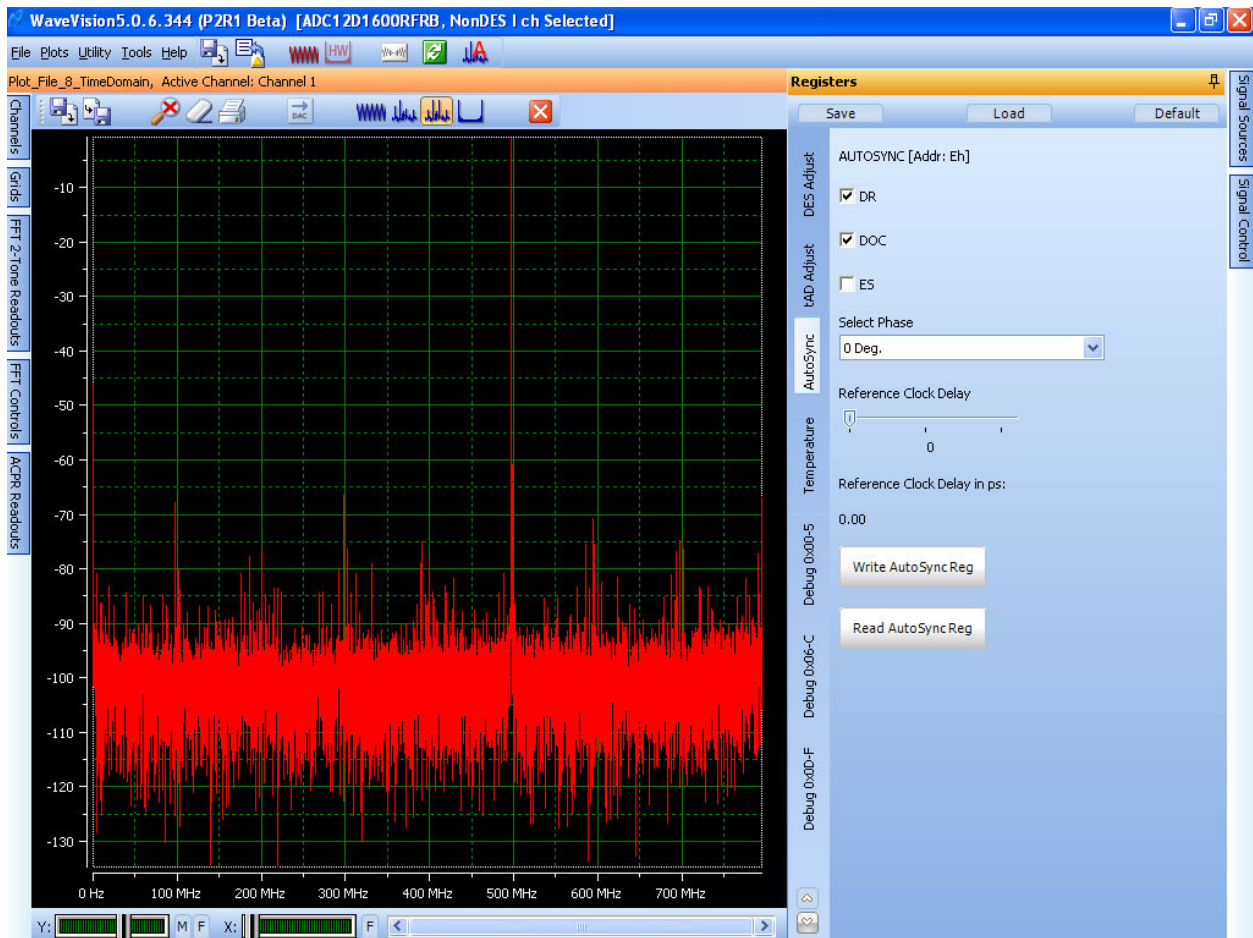
Figure 15: AutoSync Panel

- **DR** – Disable DCLK Reset – When checked (default) disables the DCLK Reset feature
- **DOC** – Disable Output reference Clocks – When checked (default) disables the AutoSync reference output clocks. When un-checked a CLK/4 signal is sent on the RCOut1 and RCOut2 outputs.
- **ES** – Enable Slave mode – When checked configures this ADC as an AutoSync slave device.
- **Select Phase** – Selects the Phase of the incoming reference clock used by the AutoSync feature.
- **Reference Clock Delay** – This selects the additional delay added to the input reference clock. Settings are 0d (0s) to 319d (1000ps). Settings higher than 319d will give 1000ps delay.

Note: No changes will take effect until the **Write AutoSync Reg** button is clicked.

Temperature: This panel provides a read-out of three different temperatures in the ADC12D1X00RFRB.
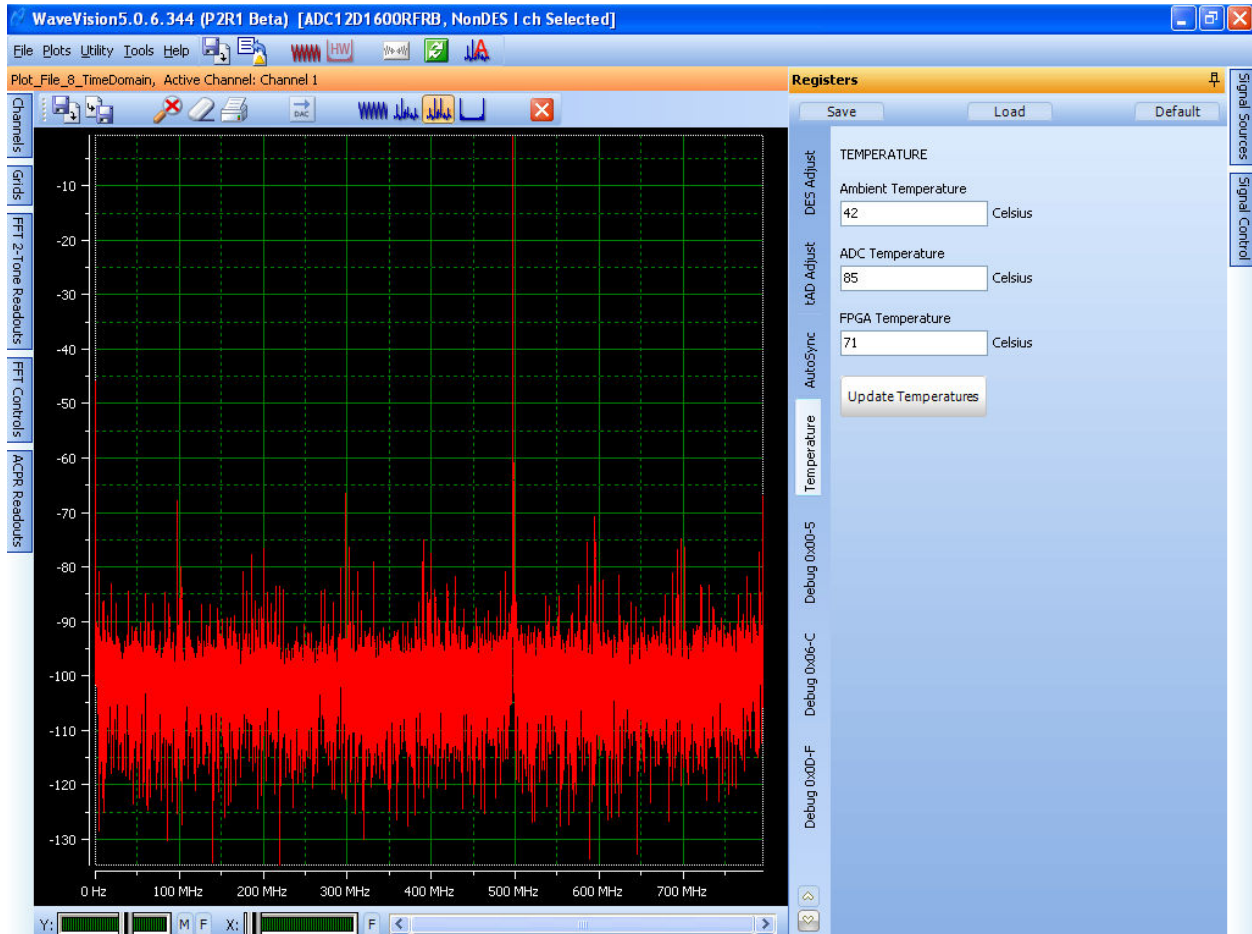
Figure 16: Temperature Panel

- **Ambient Temperature** – Provides the local/board temperature of the LM95233 IC.
- **ADC Temperature** – Provides the approximate die temperature of the ADC12D1X00RF.
- **FPGA Temperature** – Provides the approximate die temperature of the Xilinx Virtex-4 FPGA.

Note: No changes will appear until the **Update Temperatures** button is clicked.

Debug Tabs: These panels provide the actual register settings which are conveniently formatted in the other tabs above. They may also be read to and written from and these changes will be reflected in the corresponding tabs.
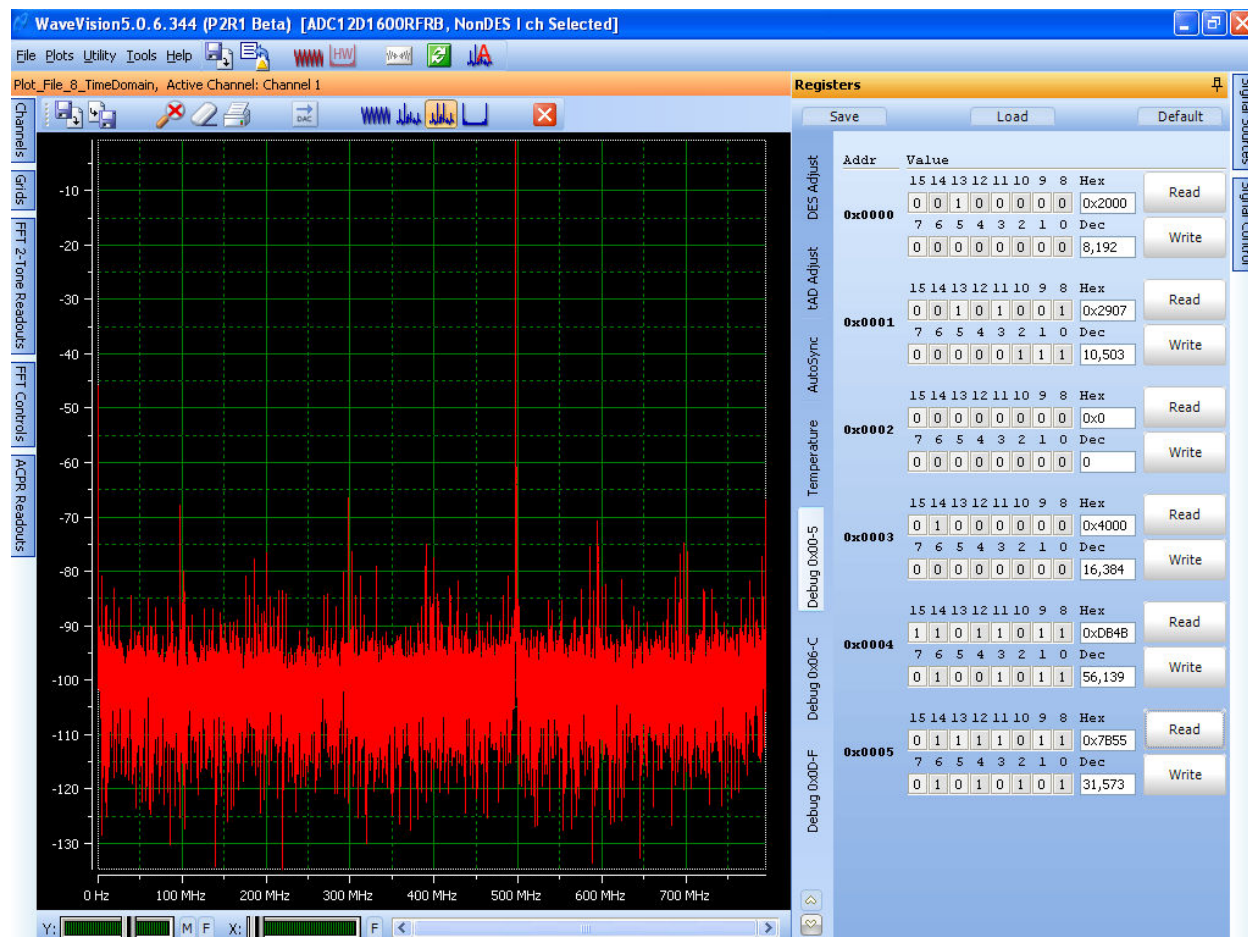
Figure 16: Debug Panel

Note: No changes will appear until the **Read/Write** button is clicked.

Special Note: Register 6**h** must be programmed to 1C0E**h** before calibrating for the ADC12D1800RF to function properly. This is accomplished automatically via the GUI programming for the ADC12D1800RF Reference Board, and in the customer's system, it must also be programmed.

2.6 Data Capturing

The board is now ready for a data capture. Before proceeding, perform a manual calibration of the ADC. Even though the ADC performs a self-calibration at the time of power-up, it is recommended that the user perform another calibration after sufficient time has passed for the system (primarily temperature) to stabilize. Manual calibration is performed by clicking the *Calibrate ADC* feature in the *Register* control panel, *Settings* sub-tab.

2.6.1 Configure Display Settings

Open the FFT Control left panel. Confirm that the *dBFS* unit is selected. Also confirm that the correct clock frequency is being measured by the software by checking in the *Signal Source* right panel. The default frequency of the on-board clock source is shown in the board performance data shipped with your board.

2.6.2 Check Input Amplitude

Confirm that the Over-range LEDs are not illuminated. Now increase the signal amplitude until the LED for the input in use is just barely lit. *DO NOT increase signal power much beyond this point as the ADC's inputs can be damaged if the Operating Maximums are exceeded (see Electrical Specification section).* Then reduce the signal amplitude until the Over-range LED is no longer illuminated. You should now have an input signal that is very close to the ADC's full-scale range (e.g., within 0.5 to 1.0 dB).

IMPORTANT: Since the ADC signal and clock inputs are not provided with additional protection circuitry on this board, the burden is on the user to not overdrive the inputs to the extent of damaging them. An "Over-range" LED is provided for each channel to indicate that the signal amplitude is beyond the ADC full-scale range. Keep the signal amplitude within the operating ratings as specified in the datasheet. Thus, the safe method of setting the signal amplitude to full-scale level is to utilize the LED as described in the previous paragraph to roughly obtain the full-scale amplitude and then inspect the captured data in the software's time-domain plot to fine tune the amplitude to the desired level.

2.6.3 Acquire and Display Data

Perform a data acquisition by clicking the Acquire Data button (Item #5 in Figure 6).
The acquired data will now appear in the (default) time domain plot window. Switch to the frequency-domain window (FFT) using the WaveVision 5 controls. Type Ctrl-r to obtain the summary of the acquisition. Place the software in continuous mode (Item #6 of Figure 6) and then acquire again. This is to confirm that the Over-range LED method used earlier indeed gave a signal to the ADC that is within -0.5 to -1.0 dB of the full-scale range. If not, adjust the input signal generator's signal power to approximately -0.5dB of full scale.

At this point, dynamic performance metrics similar to those shown on the reference data shipped with the board may be obtained. One of the basic variables that you may experiment with at this point is to change the input signal strength and frequency. Please note that to achieve the reference performance, band-pass filters similar to the items referenced in Section 2.2 should be used. The absence of these filters on the input signal or external clock will usually result in sub-standard performance.

The displayed units should be in dBFS as selected earlier. You may switch the units to dBc and back to dBFS as desired.

2.6.4 External Clock Source

It is also possible to apply a high-quality external signal source to the clock input rather than using the on-board LMX2531 clock synthesizer. This will help quantify the LMX2531's performance in an ultra-high-speed signal-path such as this one. When connecting an external clock source, the generator amplitude should be set to 0dBm. Experiment with the clock signal strength to determine what effect this has on the channel performance. Care should be taken to not exceed +4 dBm at the clock input, to avoid damage to the ADC.

The external clock source is enabled through the register control panel in the software after applying the signal generator to the Clock input SMA.

The external clock source should be disconnected or turned off when the on-board clock source is selected. Failure to do so will result in poor performance due to the mixing of the on-board clock and the small amount of external clock signal leaking through the clock selection relay.

It is important to keep in mind that if the ADC's operating conditions are changed in any significant way, especially temperature, the ADC should be calibrated again before proceeding.

Please refer to the WaveVision 5 Users' Guide and integral Help feature for more information concerning the software.

3.0   Secondary Panel Description

Please refer to the WaveVision 5 Users Guide for detailed descriptions of the remaining Left and Right panels, and additional Main Panel features.

4.0   Reference Board Functional Description

4.1 System Block Diagram
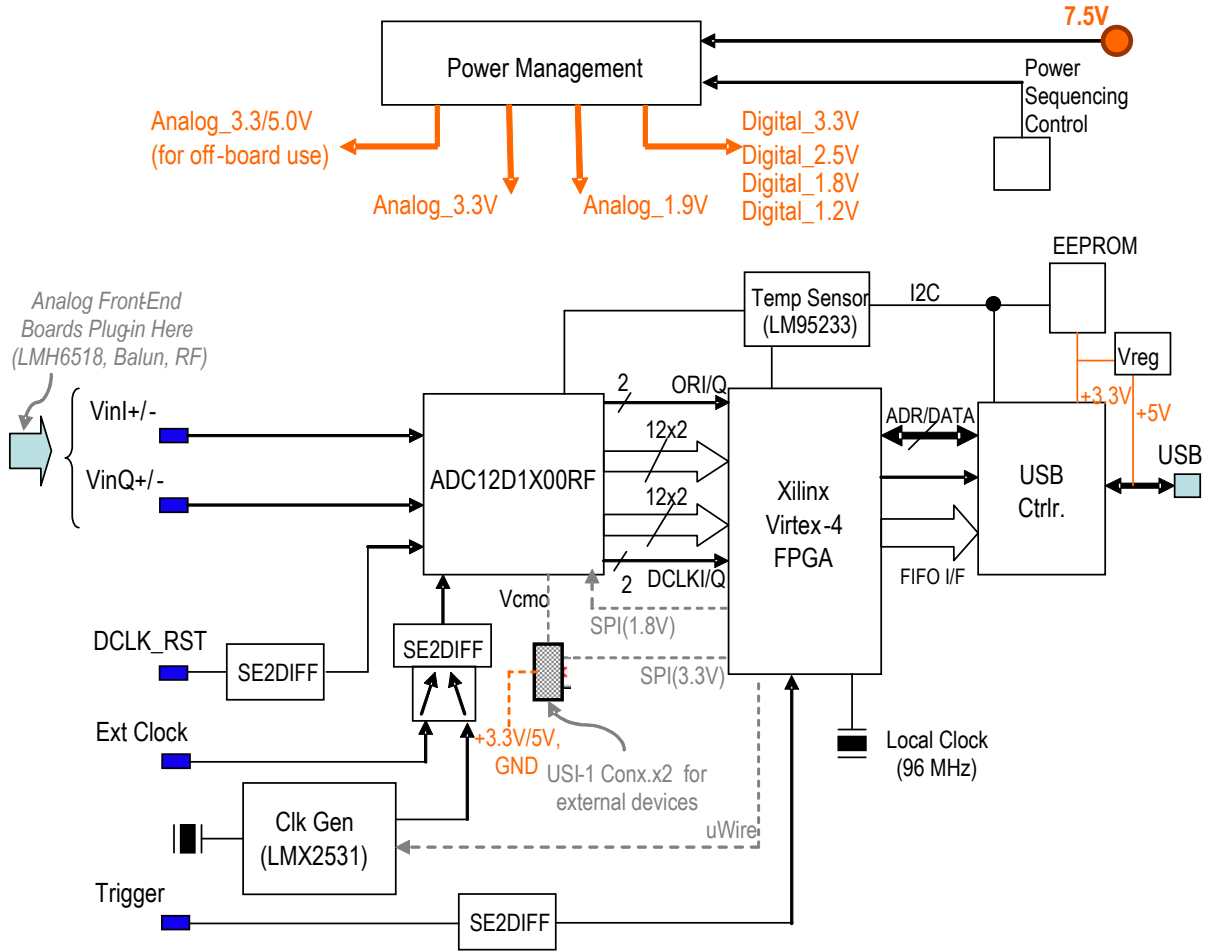
Figure 17: ADC12D1X00RFRB System Block Diagram

4.2 System Description

4.2.1 The ADC12D1X00RF

ADC12D1X00RF forms the heart of this reference board. This low-power, high-performance CMOS analog-to-digital converter digitizes signals at 12-bit resolution at guaranteed minimum sampling rates of 1.6/1.8 Gs/s in dual channel configuration and 3.2/3.6 Gs/s in single channel configuration. The ADC12D1X00RF is targeted at achieving very good accuracy and dynamic performance while consuming the lowest power available in the industry when both channels are powered-up. The product is packaged in a thermally enhanced BGA package that does not require a heat sink over the rated ambient temperature range of -40 degrees C to +70 degrees C. Refer to the latest version of the ADC12D1X00RF datasheet for more detailed information.

This reference board gives complete control over the ADC12D1X00RF and gives the user direct performance results of the chip without the need for an elaborate setup. Each of the device's control pins may be set high or low. Control is provided in two different manners - direct pin control with jumpers or through the serial interface (the device's extended control mode) using the WV 5 register control panel. *In order to use the extended control mode the ECE jumper must be set to LOW.* This is the recommended method and gives the user the most flexibility and ease of use.

Analog Front-End: The analog signal connection to the ADC is kept simple on this board in order to achieve the highest possible bandwidth. The board is designed to be coupled to front-end circuitry in a DC or AC coupled manner. AC-coupling requires the use of dc-blocks on the SMA connectors. By default, the board is shipped by National with dc-blocks. In addition, the board is also jumper-configured for DC-coupled operation (pin 9 on J15 is removed for DC operation).

Multi-channel ADC synchronization: A DCLK_RST signal input is provided to synchronize the ADCs on multiple boards or systems. In addition, the ADC12D1X00RF supports a new method of ADC synchronization, called AutoSync. Please refer to the ADC12D1X00RF datasheet for more details.

4.2.2 LMX2531 Clock Synthesis chip

The LMX2531xxxx family provides a single-chip, very low-jitter clock solution at frequencies up to 2.0 GHz. In this application, the LMX2531LQ1570E / LMX2531LQ1778E is used - which can be programmed to operate over a range of 1530-1636MHz / 1726-1840MHz. On the ADC12D1X00RFRB board, the device is configured for a frequency in this range through the serial interface which may be controlled through the WaveVision 5 register control panel. The particular frequency chosen is one that generates the least phase noise. It is not necessarily a round number but depends on the loop feedback of the PLL's in the clock synthesis chip.

The clock source for the ADC can be selected between the on-board LMX2531 or an external clock source connected through the J11 SMA connector. The selection is performed through the WV 5 register panel. It is recommended that the external clock source should be connected and enabled before it is selected. ***For optimum performance, the external clock signal generator and the LMX2531 should not be enabled at the same time.*** This is because the RF relay used to select between them does not provide adequate isolation to keep one from affecting the other. Having both clocks on simultaneously will result in excessive spurious signals. The default setting for this board is the on-board LMX2531 clock source.

4.2.3 FPGA

The design employs a Xilinx Virtex-4 FPGA for capturing the digital data. While the board is powered up and configured, the FPGA is continually receiving data from the ADC. In response to a user command through the WV-5 software, the ADC captures the desired amount of data in its on-chip buffer (up to a maximum of 32K samples per-channel). The user can then command the FPGA to upload the captured data to the PC through the USB interface for further processing.

This board can support the ability to program the FPGA for specific requirements. A standard JTAG connector is provided for downloading FPGA object code from the Xilinx development environment.

Please note that National Semiconductor does not provide support for any user-designed FPGA functionality beyond the standard functionality that is shipped with the board.

Hardware Trigger: The external trigger feature of the Reference Board is designed to enable applications which trigger a data capture. When the hardware trigger is enabled, an acquisition can be selected from the software, but the actual beginning of data capture will be postponed until the external trigger pulse is applied to the J26, the EXT_TRIG SMA.
Note: This only applies to the data which is captured and displayed in the WaveVision GUI; the streaming data to the FMC connector still runs continuously.

Apply the trigger signal at J26, the EXT_TRIG SMA. If the voltage applied, Vtrigger is less than the threshold, Vth, of the MC100EP16, then the system will not capture. If Vtrigger is greater than Vth, then a data capture will occur. Vth is approximately 2.1V, so it is recommended that high trigger voltage is in the range of {2.5V, 3.3V}. The low trigger voltage should be 0V. Note that this may be a single shot data capture or a continuous trigger. If the trigger is armed, but Vtrigger is not greater than Vth within approximately 3 minutes, then the software will time out and show the error message: "Board failed to collect samples."
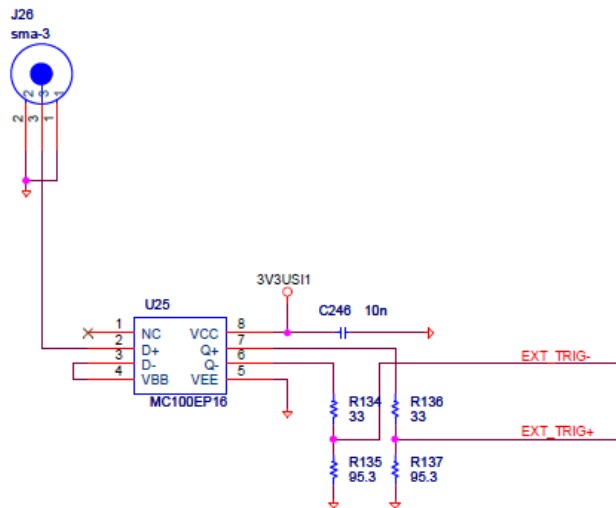
Figure 18: Trigger circuit on reference board

1. Connect a signal source to the EXT_TRIG SMA (J26).
2. In the WaveVision5 GUI, select Registers – Settings – check the H/W Trigger box.
3. Select single or continuous capture.
4. Apply Vtrigger above the threshold, Vth, when ready to capture.

Auxiliary Port: FMC connector forms an auxiliary data port. With it, the FPGA captures the ADC's high-speed continuous streaming data and retransmits the data out of the FMC port. See photo below of the FMC port on the bottom of the board.

- Install J155 to force FPGA to output data on FMC port (without a power good signal from Carrier to Mezzanine). This is useful when a non FMC compliant board is connected to Mezzanine (ADC12D1X00RFRB)
- Install J156 to force a power good signal from Mezzanine (ADC12D1X000RFRB) to Carrier. This is used to override for initial FPGA debug.
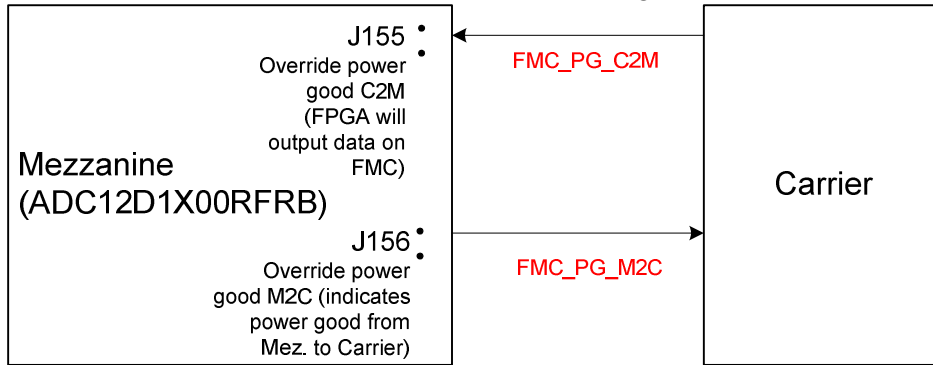
Figure 19: Explanation of Power Good override jumpers for FMC port
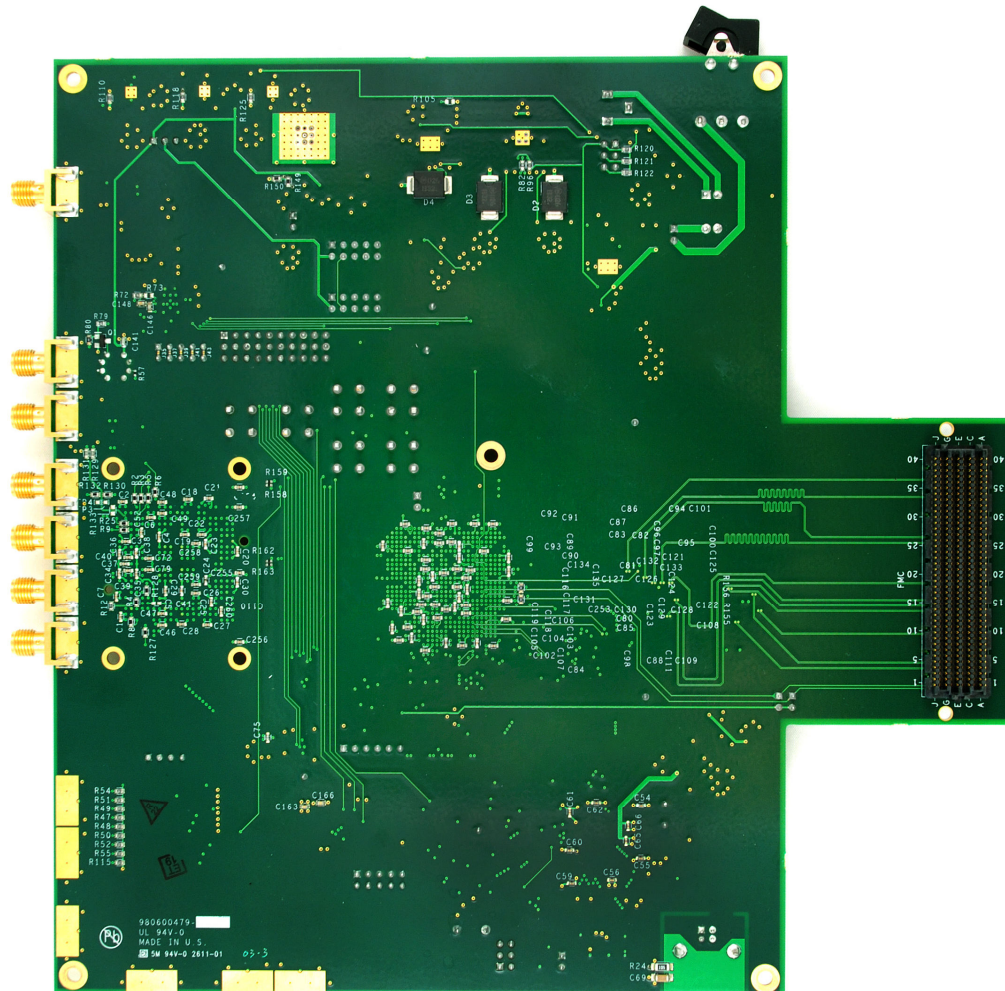
Figure 20: Bottom of ADC12D1X00RFRB showing FMC port

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AutoSync SMA connectors: Needs resistor jumper modification to evaluate AutoSync on the reference board. See schematic to find the resistor locations.

- Remove DCLKQ+/-, RCOUT1+/- to FPGA (Remove R162, R163, R158, R159)
- Route DCLKQ+/-, RCOUT1+/-, RCLK+/- to SMA connectors (Stuff 0ohm resistors to R161, R164, R157, R160, R145, R147)

Enable AutoSync output by going to Wavevision 5 Software GUI -> Registers tab -> AutoSync panel -> Uncheck DOC and click 'Write AutoSync Reg'. Notice that LED RCOUT1/2_ENABLED will light and DCLK_LOCKED will not light.

The board has SMA connectors for DCLKQ+, DCLKQ-, RCOUT1+, RCOUT1-, RCLK+, RCLK- on the board. See the ADC12D1X00RF datasheet and Application Note 2132 for details on how to use the AutoSync feature.

For example, one reference board can be configured in Slave Mode and its RCLK driven externally by a signal generator which is phase locked to the sampling clock. For this setup, the Reference Board must select the EXT CLK. The DCLK and RCOut1 may be conveniently monitored via the on-board SMA connectors for exploration of the AutoSync feature.
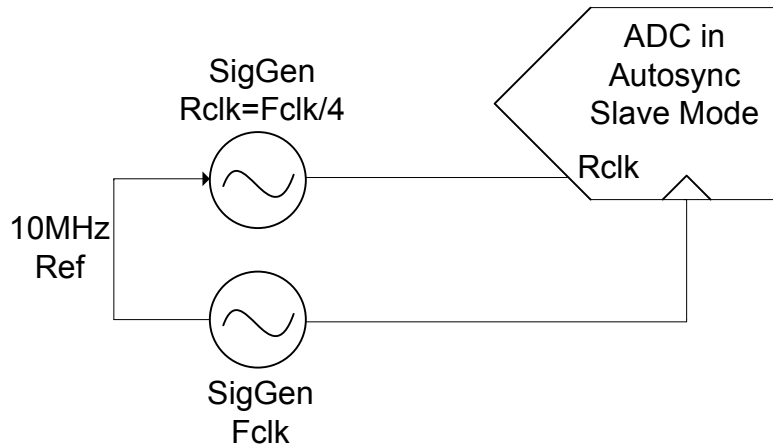
Figure 21: AutoSync example with one reference board in slave mode

4.2.4 LM95233 Temperature Sensor

Using the National LM95233 temp sensor chip; the ambient, ADC12D1X00RF and Xilinx FPGA temperatures can be monitored. The temperature readings are available through the WV-5 software.

5.0   Electrical Specification

Power Supply: Nominal = 7.5V
                       Minimum = 7.0V, Maximum = 8.0V
                       (Voltages outside these levels will cause damage!!)

Power Consumption: Nominal = 10 Watts
                       Maximum = 20 Watts

ADC Input Signals: Maximum Operating Voltage = see datasheet
                       Recommended/initial (full scale) generator setting = 0 dBm
                       (The maximum level at the signal generator is dependent upon the insertion loss from other hardware before the ADC inputs. Care should be taken not to exceed the Operating Ratings at the ADC input.)

Clock Input Signal: Maximum Operating Voltage = +2.0V
                       Recommended generator setting = +1 dBm
                       (The maximum level at the signal generator is dependent upon the insertion loss from other hardware before the clock inputs. Care should be taken not to exceed the maximum limits at the clock inputs.)

USB Port: USB 2.0 compliant

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