September 01, 2010
Revision 1.2

ADC10D1000/1500RB

Reference Board Users' Guide

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1.0 Overview

The ADC10D1000/1500RB demonstrates a high-performance signal acquisition sub-system that achieves 10-bit resolution and corresponding SNR and dynamic range on two channels at signal frequencies in excess of 1.0 GHz and sampling rates of at least 1.0/1.5 GS/s or one channel at a sampling rate of 2.0/3.0 GHz. The board showcases the following National Semiconductor devices:

- **ADC10D1000/1500** analog-to-digital converter
- **LMX2531** clock synthesizer
- **LP3878** and **LP38853** linear LDO regulators
- **LM20242**, **LM25576** and **LM26400** switching regulators
- **LM3880** power sequencing controller
- **LM95233** temperature sensor

In addition, the board also employs the **Xilinx XC4VLX25-11FFG668 Virtex-4** FPGA for the critical function of capturing the high-speed digital data sourced by the ADC.

1.1 Features

- Demonstrates the ADC10D1000/1500's typical dynamic performance – see the datasheet for full details.
- Sample rates of up to 1.0/1.5 GS/s (limited by the ADC specifications and the FPGA capture limitations)
- Input signal frequencies up to 2.8/3.1 GHz
- On-board LMX2531 based clock circuit with a connector for a selectable external clock
- A complete high-performance low-noise power management section for the ADC, clock circuit, FPGA and USB controller
- Single +7.5V power adapter input
- Simplicity and performance of USB 2.0 connection to the PC
- Functions with National's latest WaveVision 5 signal-path control and analysis software.

1.2 Packing List

The ADC10D1500RB kit consists of the following components:

- ADC10D1000/1500RB Board
- Documentation Including
  - Anaren balun datasheet
  - ADC10D1000/1500RB Users Guide (this document)
  - WaveVision 5 Users Guide
  - ADC10D1000/1500RB schematic
  - ADC10D1000/1500RB bill of materials
  - ADC10D1000/1500RB test results from National lab
  - End user license agreement
  - Letter to the user
- Hardware Kit Including
  - 110V-240V AC to +7.5V DC Power Adapter
  - USB cable
  - 4 – DC blocks
  - 2 – 50Ω terminators
  - 1 – Anaren balun board (useful bandwidth of 400 MHz to 3 GHz)
  - 1 – MiniCircuits balun board (useful bandwidth of 4.5 MHz to 3 GHz)
  - 4 – 6” SMA cables

1.3 References

- *ADC10D1000/1500 datasheet
- *LMX2531 datasheet

*Note: Please refer to www.national.com for the latest edition of all datasheets.

1.4 Board Orientation

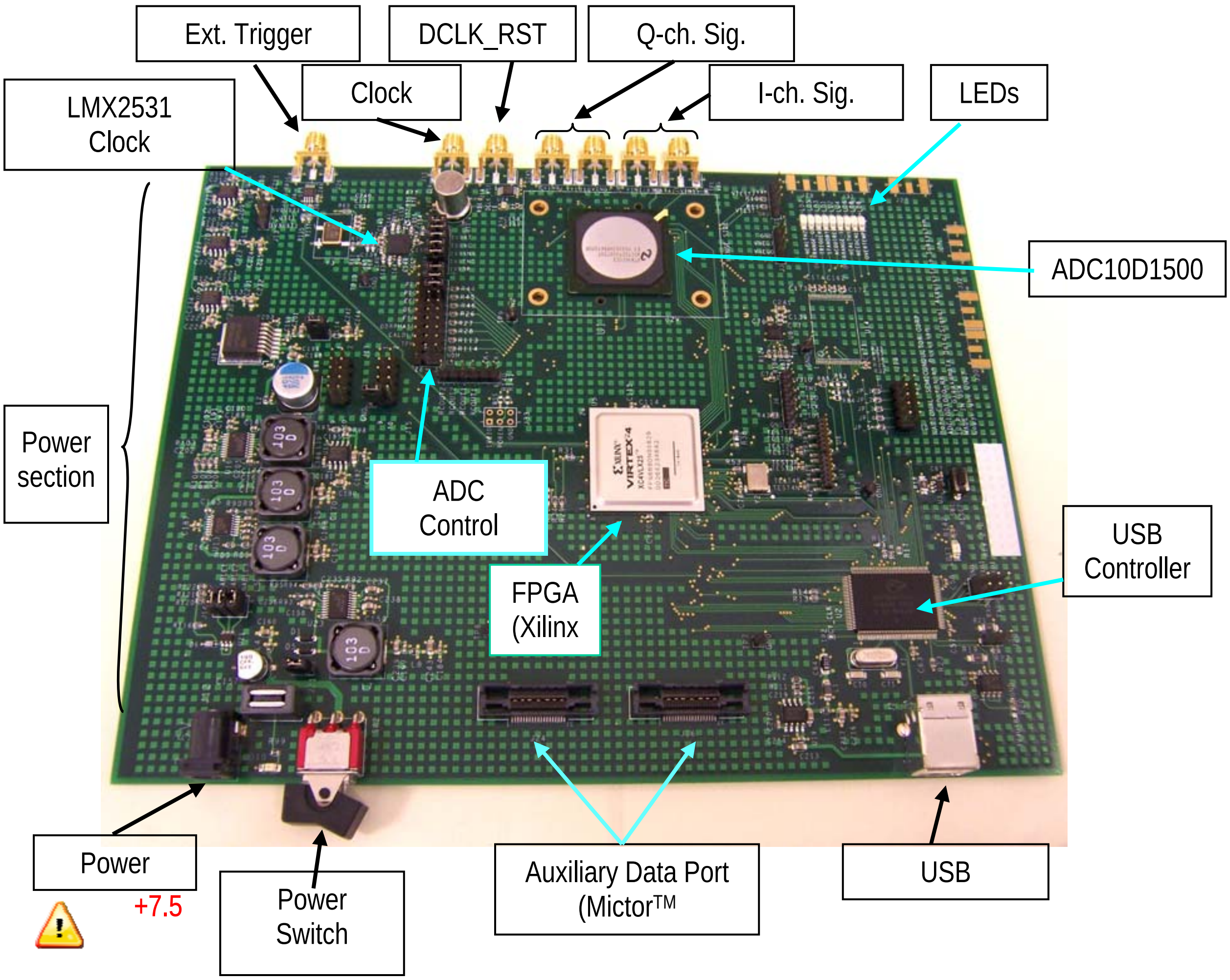
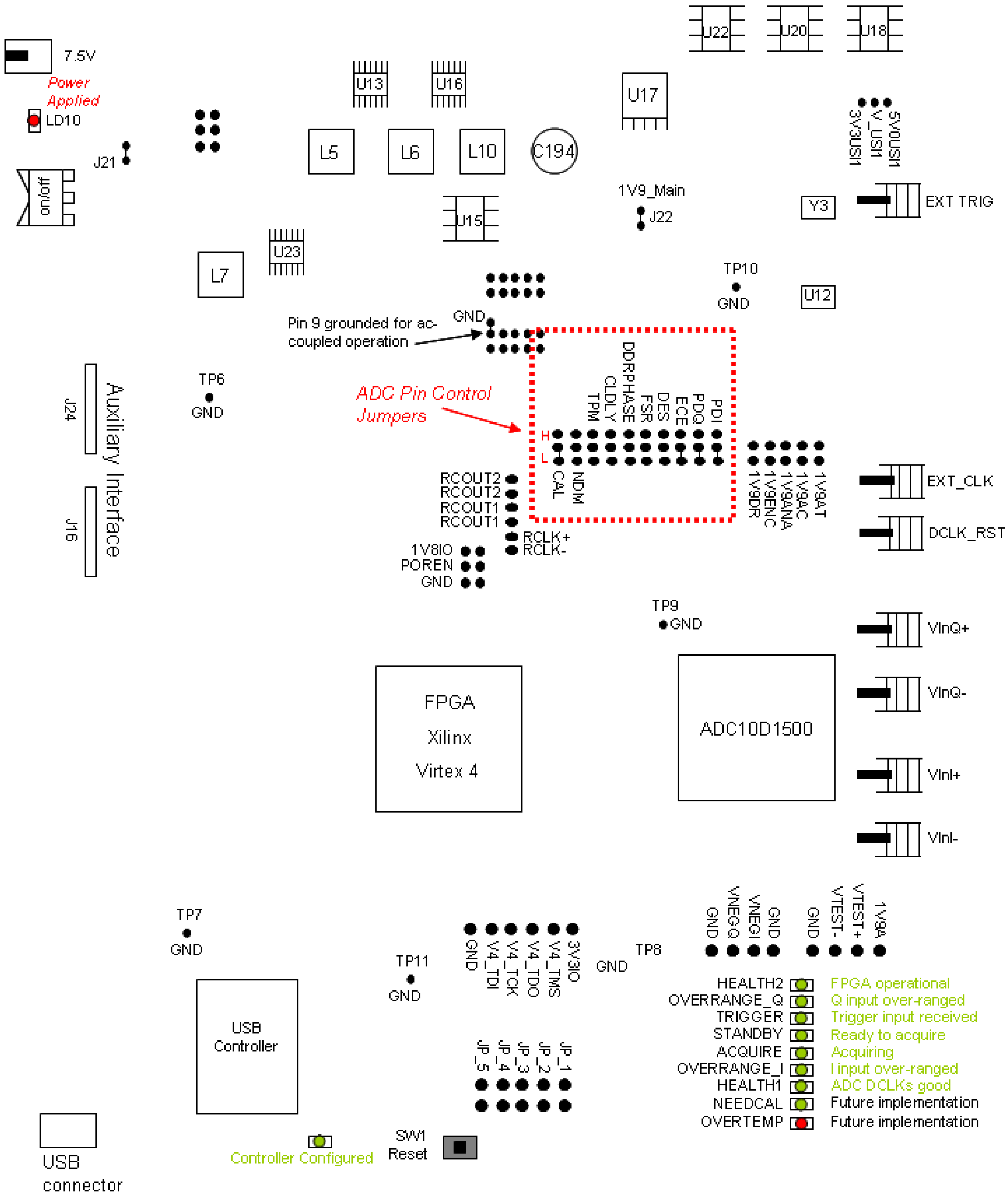


Figure 1: ADC10D1000/1500RB Board Layout


7.5V
Power Applied
LD10
on/off
J21
U13
U16
L5
L6
L10
C194
U17
U22
U20
U18
5V0USI1
V_USI1
3V3USI1
1V9_Main
J22
Y3
EXT TRIG
U15
U23
L7
TP10
GND
U12
Pin 9 grounded for ac-coupled operation
GND
J24
J16
Auxiliary Interface
TP6
GND
ADC Pin Control Jumpers
DDRPHASE
CLDLY
TPM
FSR
DES
ECE
PDQ
PDI
H
L
CAL
NDM
1V9DR
1V9ENC
1V9ANA
1V9AC
1V9AT
EXT_CLK
DCLK_RST
RCOUT2
RCOUT2
RCOUT1
RCOUT1
RCLK+
RCLK-
1V8IO
POREN
GND
TP9
GND
VInQ+
VInQ-
VInI+
VInI-
FPGA
Xilinx
Virtex 4
ADC10D1500
TP7
GND
TP11
GND
GND
V4_TDI
V4_TCK
V4_TDO
V4_TMS
3V3IO
TP8
GND
GND
VNEGQ
VNEGI
GND
GND
VTEST-
VTEST+
1V9A
JP_5
JP_4
JP_3
JP_2
JP_1
USB Controller
HEALTH2
OVERRANGE_Q
TRIGGER
STANDBY
ACQUIRE
OVERRANGE_I
HEALTH1
NEEDCAL
OVERTEMP
FPGA operational
Q input over-ranged
Trigger input received
Ready to acquire
Acquiring
I input over-ranged
ADC DCLKs good
Future implementation
Future implementation
USB connector
Controller Configured
SW1
Reset

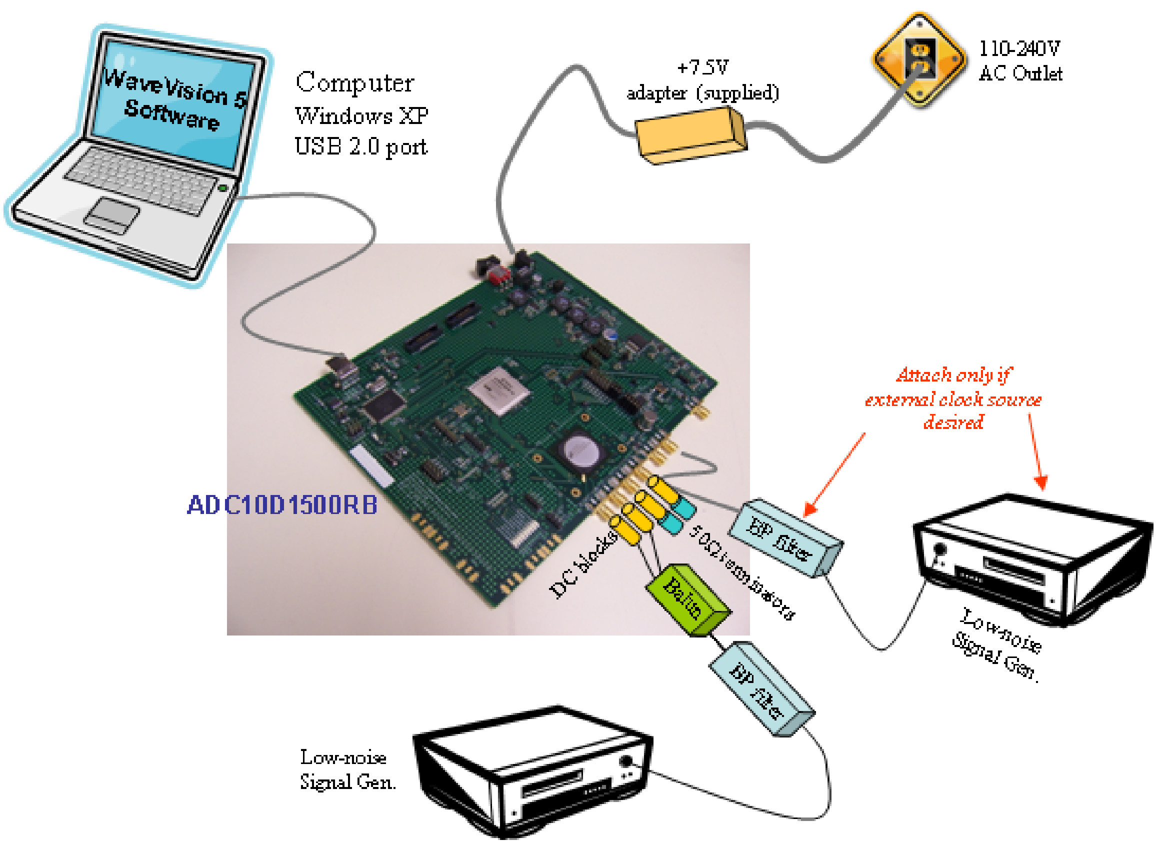
2.0 Quick Start

This section will aid in bringing up the board for the first time as well as a brief tutorial on the WaveVision 5 (WV5) software. Further description of the Reference Board is in subsequent sections of this document. The software is further described in the WaveVision 5 Users' Guide or the HELP function within the software. The ADC10D1000/1500 and LMX2531 datasheets should be consulted for detailed understanding of device functionality.

The user is advised to construct a lab setup as close to the one shown in Figure 3 as possible. This setup, along with the board and software configuration described below, is what was used to test the reference board at National's lab. This set of conditions produces the stated reference performance - which is normally included with each board shipped to customers. The objective is to assure that the user can achieve the same performance as that recorded at National's lab prior to board shipment.

Do not overdrive the signal and clock inputs or the ADC may be damaged. Refer to the Electrical Specification section for the voltage tolerance of these inputs. Be very cautious of signal generator power levels above +3 dBm. Input maximum is 4mW or about +5 dBm maximum.

Figure 3: Recommended lab setup. A filter may not be necessary on the clock if the generator is very clean (beyond -80dBm SFDR).



2.1 Installing the WaveVision 5 Software

(Note: The WaveVision 5 software requires Windows XP operating system)

1. Insert the included WaveVision 5 CD-ROM into the computer CD drive.
2. Locate, unzip and run the install.bat program on the CD-ROM.
3. Follow the on-screen instructions to complete the installation.

2.2 Installing the ADC10D1000/1500RB Hardware

1. Place the ADC10D1000/1500RB Reference Board on a clean, static-free surface.
2. Make sure the board's jumpers are configured as follows as shown in Figure 2:
    a. For the ADC, the "ECE (Extended Control Enable, active low)" jumper should be installed in the LOW position. This enables SPI control of the ADC.
    b. Pin 9 on J15 must be connected to Ground for ac-coupled operation. The board ships with this jumper in place as it is <u>configured for ac-coupled operation only</u>. (The jumper is removed for dc-coupled operation. In that case the applied signal must be dc-coupled, and have the common mode DC voltage set to the required ADC10D1500 V_{CM} voltage.)
    c. The PDI and PDQ jumpers must be in place as shown to enable both channels of the ADC.
3. Connect the enclosed +7.5V DC power adapter to the power jack. Connect the other side of the power supply to an AC outlet (100-240 VAC, 50-60 Hz).
4. Connect the input signal generator, the band-pass filter, the balun and the DC blocks to the ADC10D1000/1500RB Reference Board's I-channel input connectors. Set the signal generator at one of the frequencies and signal levels stated in the reference performance report. Always use high-quality RF SMA cables for optimum performance.

Do not overdrive the signal and clock inputs as the ADC may be damaged. Refer to the Electrical Specification section for the voltage tolerance of these inputs. Be very cautious of signal generator power levels above about +3 dBm (2mW). This is approximately 1 V-P-P which is also the full scale range of the ADC. Depending on other hardware that is casaded with the generator path (baluns, filters, etc), caution should be taken with signals above +3dBm

5. In the National lab, the following (or equivalent performance) equipment are used to test the board. It is essential that the customer use signal generators, filters, DC blocks and a balun of equivalent or better performance.
    - Rohde & Schwarz SME-03 or SMA-100 signal generator
    - Filters - Trilithic tunable bandpass filter or other fixed frequency bandpass filter of equivalent performance
    - Balun – Anaren Balun Board
    - DC blocks – Mini Circuits BLK-89 S+
    - 50 Ω terminators – Mini Circuits ANNE 50+

    Note: The board comes equipped with DC-blocks applied to the I-channel signal input connectors and DC blocks and terminators applied to the unused Q-channel input connectors. These must be used at all times - that is, the channel being used must be connected through dc-blocks if the ADC is configured for ac-coupled operation (as shipped). The unused channel must also be DC blocked then terminated to ac ground. This is graphically illustrated in Figure 3.
6. Turn on the SW1 rocker power switch. Verify that the red LED (labeled LD1, near the J2 power jack) is lit.

7. Connect the supplied USB 2.0 cable from the PC USB port to the ADC10D1000/1500RB USB jack.

2.3 Launch the WaveVision 5 Software.

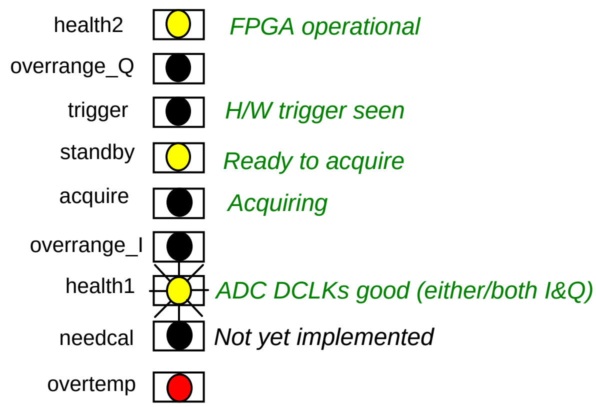
Start the WaveVision 5 software on your computer by selecting the desktop icon “WaveVision 5” or by clicking on the Start button, and selecting

`Programs -> WaveVision 5 -> WaveVision 5`

The software will automatically detect the board and load the appropriate software profile and will proceed to download the controller firmware and FPGA code onto the reference board. As an alternative, the icon on the desktop can be used to launch WaveVision 5.

The WaveVision 5 user interface will appear on the computer screen. The STANDBY LED should be green - meaning that the hardware is ready to capture data from the ADC upon the user's command. The software and the board are ready to acquire data at this point. The status LED’s should take on the following states when the system is ready for an acquisition:

(Where yellow or red is *on,* black is *off* and *yellow* with spokes indicates blinking)



2.4 WaveVision 5 - User Interface Overview

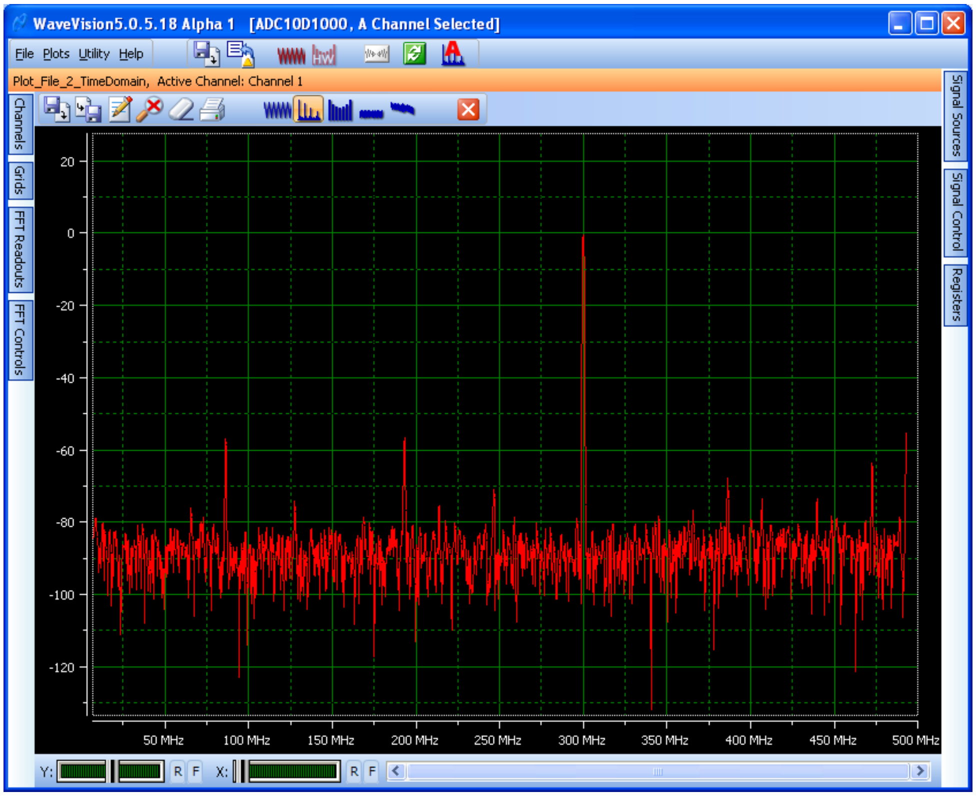


Figure 4: WaveVision 5 Example Window

Figure 4 above shows the WV5 user interface panel (GUI). This is the top level interface panel. It is arranged in such a way that the plot is always in the middle. There are tabs arranged on each side of the window to give the user additional information or control of features.

The tabs available on the **left side** access panels that are pertinent to the current plot window - such as *channel selection*, *grid selection*, *FFT Readouts*, and *FFT controls*.

The **right side** panels allow the user to take control of the hardware. These include the *Signal Source*, *Signal Control* and *Registers* panels (the most relevant for this board).

In addition, a small FFT parameter summary box can be displayed by pressing CTL-R.

For more details on the general operation and use of WaveVision 5, please refer to the **WaveVision 5 Users Guide**.

2.5 System / Device Configuration

Prior to capturing data, confirm that the board is in the "ECE (Extended Control Enable)" mode, The ECE jumper is located in the ADC pin control jumper area as shown in Figure 2. The board should be sent with this jumper in place. This means that the ADC will be controlled through the SPI interface and not with jumpers driving the control pins. This allows the user to control the ADC's behavior through the WaveVision 5 Registers panel.

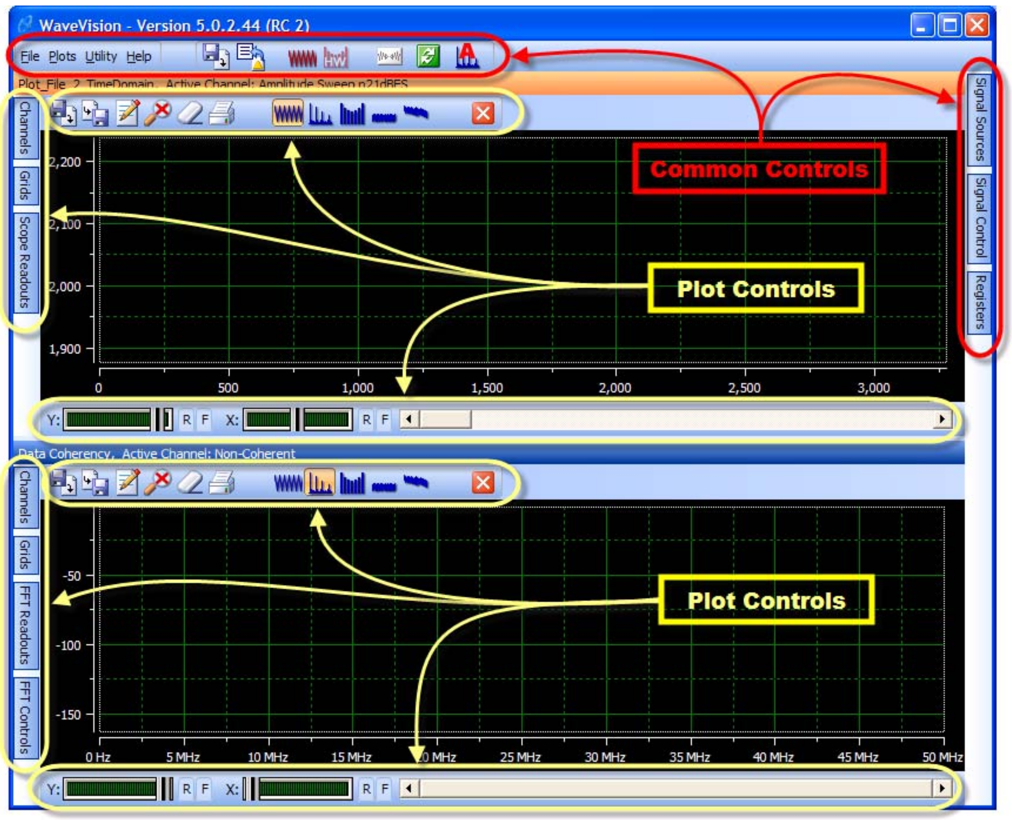


Figure 5: WaveVision 5 overview of control buttons

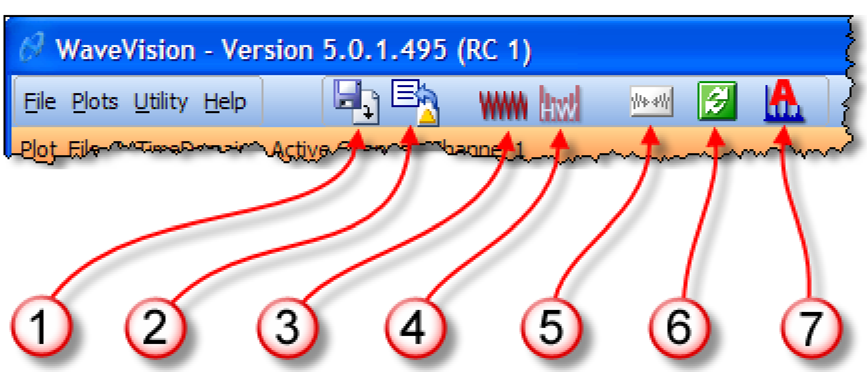


Figure 6: WaveVision 5 main window command buttons

2.5.1 Main Panel

The main menu bar of the WaveVision 5 software has several control buttons as shown in Figures 5 and 6, which may be used to perform most tasks with a button click.

1 - Load Plot
A new plot window is created and the Plot Load dialog is displayed. The selected plot file is loaded into the new window.

2 - Import Data
Clicking this button creates a new time-domain plot and opens the Import Data dialog. Data may be imported from WaveVision 4 data files as well as from ASCII data files created by other programs.

3 - Create a New Time Domain Plot
Clicking this button creates a new time-domain plot. The plot will contain no data, but is available as a data destination.

4 - Create a New Hardware Histogram Plot
Clicking this button creates a new hardware histogram plot. Hardware histograms are available only in conjunction with evaluation boards which can gather histogram data internally. This button is enabled only when an evaluation board which supports hardware histograms is attached.

5 - Acquire Data
Click this button to acquire data to the active plot. If you have created more than one plot, the Active plot has a highlighted title bar.

6 - Continuous Acquisition
This button is a toggle - when it is pressed, data is acquired continuously, one buffer after another as fast as the hardware can go; when pressed again data acquisition stops. When in continuous acquisition mode, acquisition may be started and stopped using the Acquire button without leaving the continuous acquisition mode.

7 - FFT Averaging
This button is also a toggle - when it is pressed, FFT's are averaged. The number of buffers to be averaged is specified in the hardware section of the Signal Sources tab.

Please refer to the **WaveVision 5 Users Guide** for more information.

2.5.2 Plot Window Controls

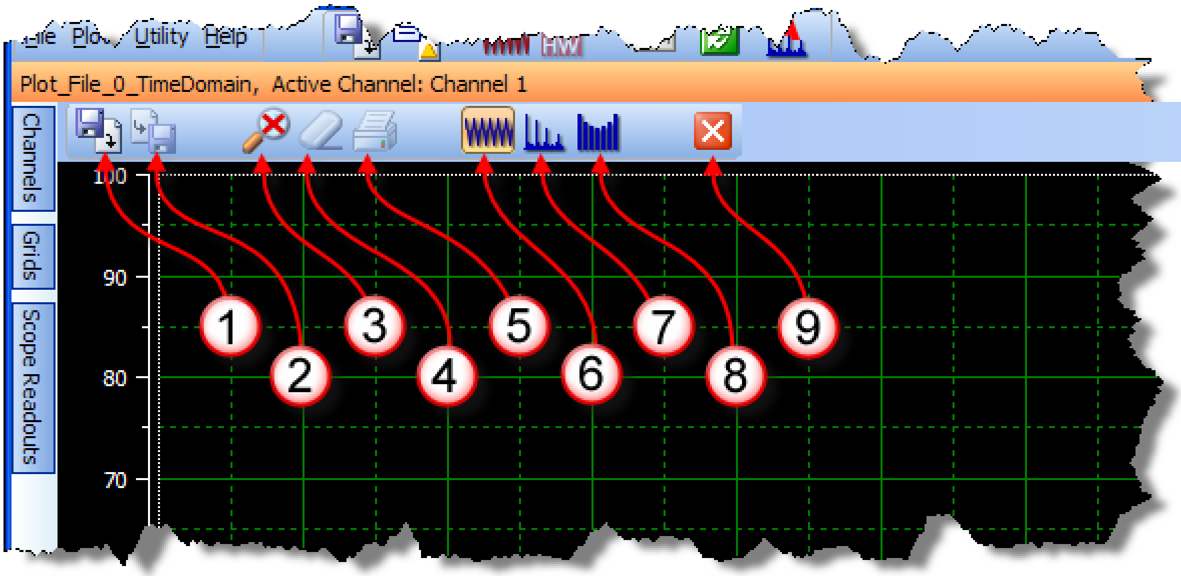


Figure 7: WaveVision 5 plot window controls

1 - Load Plot
The Plot Load dialog is displayed, and the selected plot file is loaded into the new window.

2 - Save Plot
Displays the Plot Save dialog (this button is only active when the plot contains one or more channels with data).

3 - Reset Zoom
Reset X and Y axis zoom to 100%.

4 - Clear
Clear data from all channels.

5 - Print
Print the plot.

6 - Time Domain
Display the plot as time domain data.

7 - FFT
Display the plot as an FFT

8 – Histogram
Display a histogram of the data.

9 - Close
Close this plot.

2.5.3 Right Panels – Signal Source

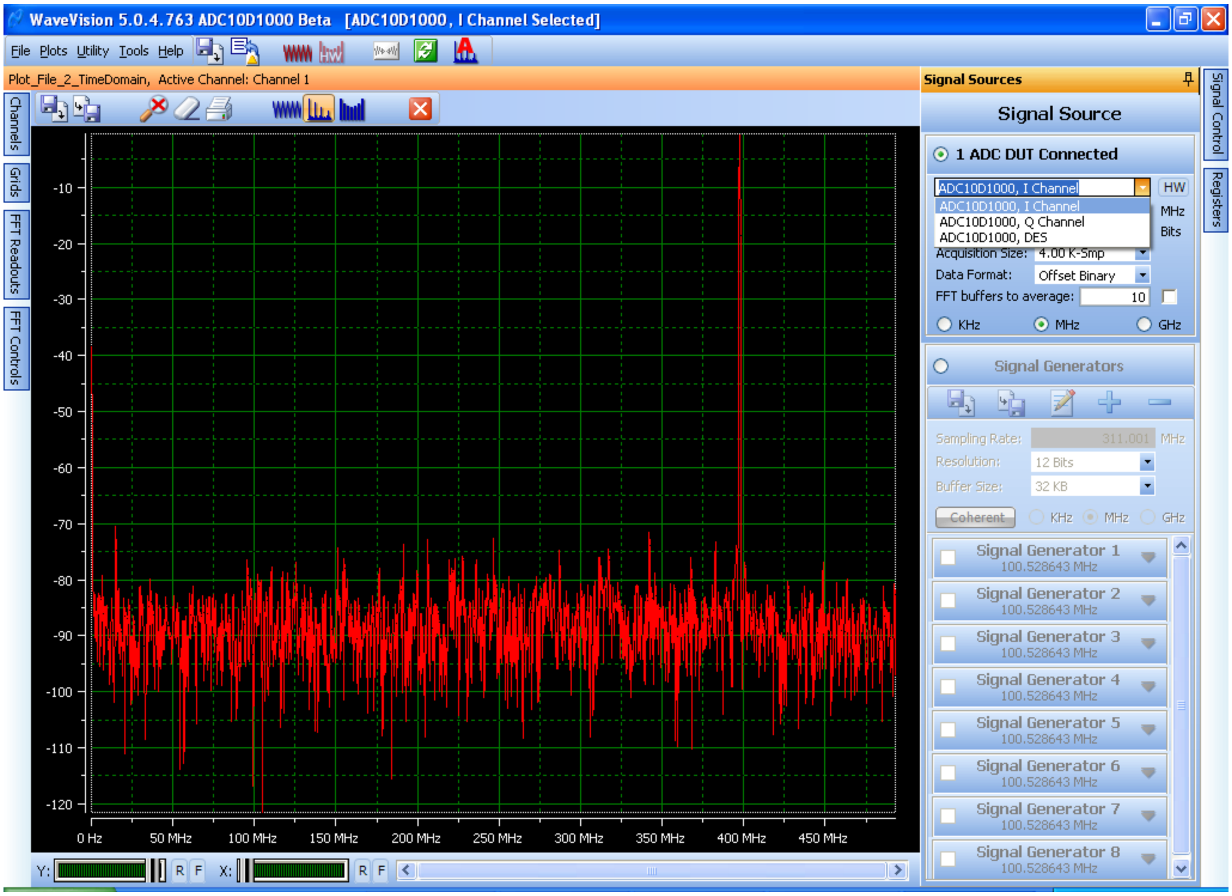


Figure 8: WaveVision 5 main window command buttons

Open the *Signal Source* panel on the right side of the window and confirm that the ADC10D1500RB is available and confirm that it is selected. There are three possible modes of operation selectable here:

- I-Channel – Two channel mode capturing and viewing the I-channel data
- Q-Channel – Two channel mode capturing and viewing the Q-channel data
- DES-mode –Dual Edge Sampling (interleaved) Mode

Double Edge Sampling (DES) – Double edge sampling works much in the same way as single edge sampling except that the signals is sampled both on the rising and falling edge of the sample clock. This effectively doubles the sample rate. In this mode, both converters inside the ADC10D1000/1500 work on a common input signal. The DES mode is selected from the *Signal Source* tab on the right side. Then, the Q-channel must also be selected as the input. To do this, go the *Register* panel select *Config* and *DESQ* and then perform a *Write Config Register*.

Q-channel operation will give the best DES mode performance. Also, selecting *DESIQ* in the *Config* register is not recommended since it parallels the I and Q channel inputs resulting in lower than normal input impedance.

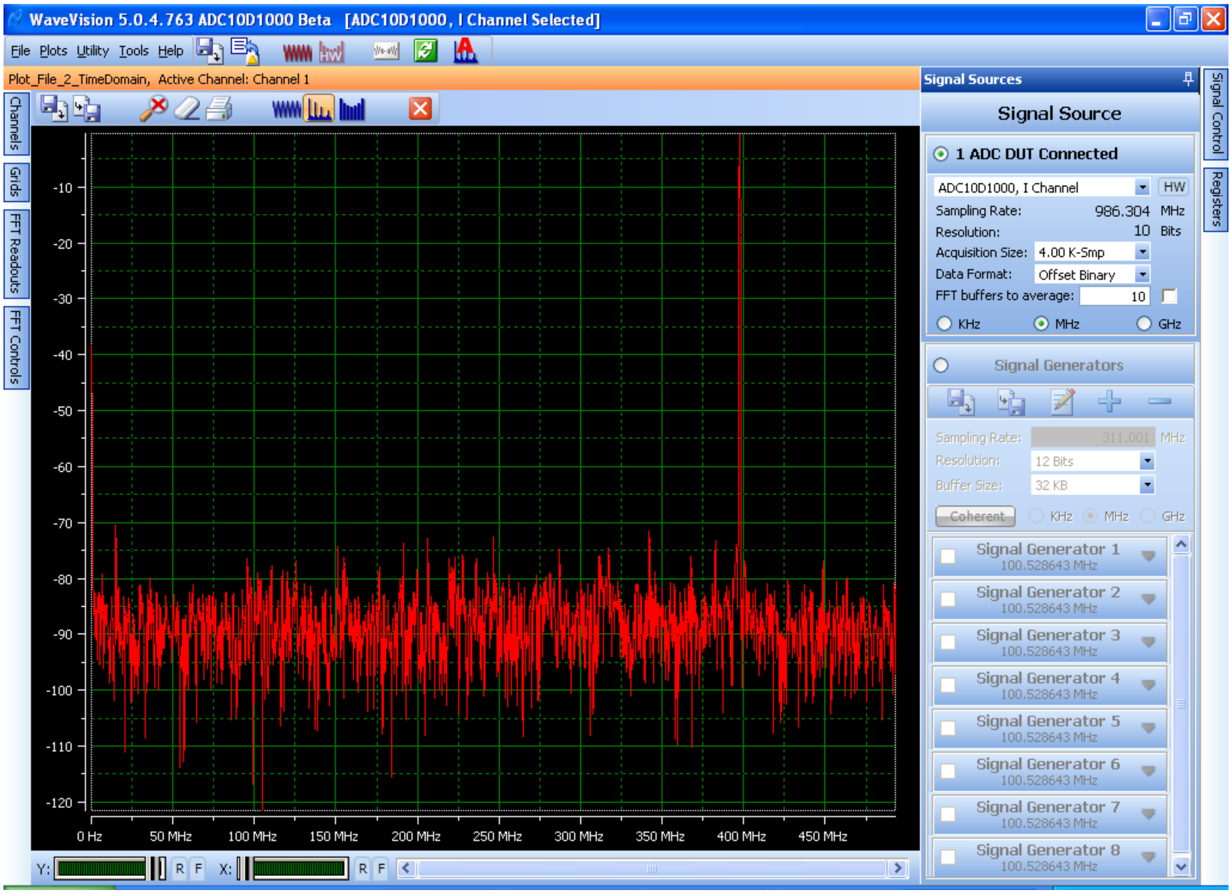


Figure 9: WaveVision 5 main window command buttons

- **Sampling Rate** - When the signal source panel is selected, the clock frequency is displayed. This is initially the internal clock. In this example, 986/1500 MHz is generated by the LMX2531 on the evaluation board. The sampling rate is determined by the FPGA when the board is powered up. The calculation is accurate to better than 1%. If an external source is in use, confirm that this number corresponds to the clock reference that is applied. If it is not correct, subsequent data captures and display will not be correct.
- **Resolution** – This will always be set to the ADC10D1000/1500 resolution which is 10 bits.
- **Acquisition Size** - This setting displays and selects the number of samples captured in each acquisition. 4K samples is the default, with settings up to 32K samples. A larger sample size increases the equivalent FFT bandwidth resolution, but at the expense of more memory and slower acquisition time.
- **Data Format** - The default data format is *offset binary* for the ADC10D1000/1500.
- **FFT buffers to average** - The last option is the FFT averaging function. Using this feature, subsequent samples can be averaged to obtain improved signal to noise. However, this is at the expense of time. For example, 10 averages will improve SNR by about 10dB but requires 10x more time.

2.5.4 Right Panels - Registers

Next, configure the hardware (including the ADC) using the Registers control panel on the right side. This is the most important of all the panels for controlling the ADC10D1000/1500RB. This panel has seven sub-tabs that control the settings of the board and registers inside the ADC10D1000/1500. The seven sub-tabs are shown below and include; *Settings, Config, I-channel, Q-channel, t_{AD} Adjust, LC Filter Adjust, AutoSync,* and *Temperature.*

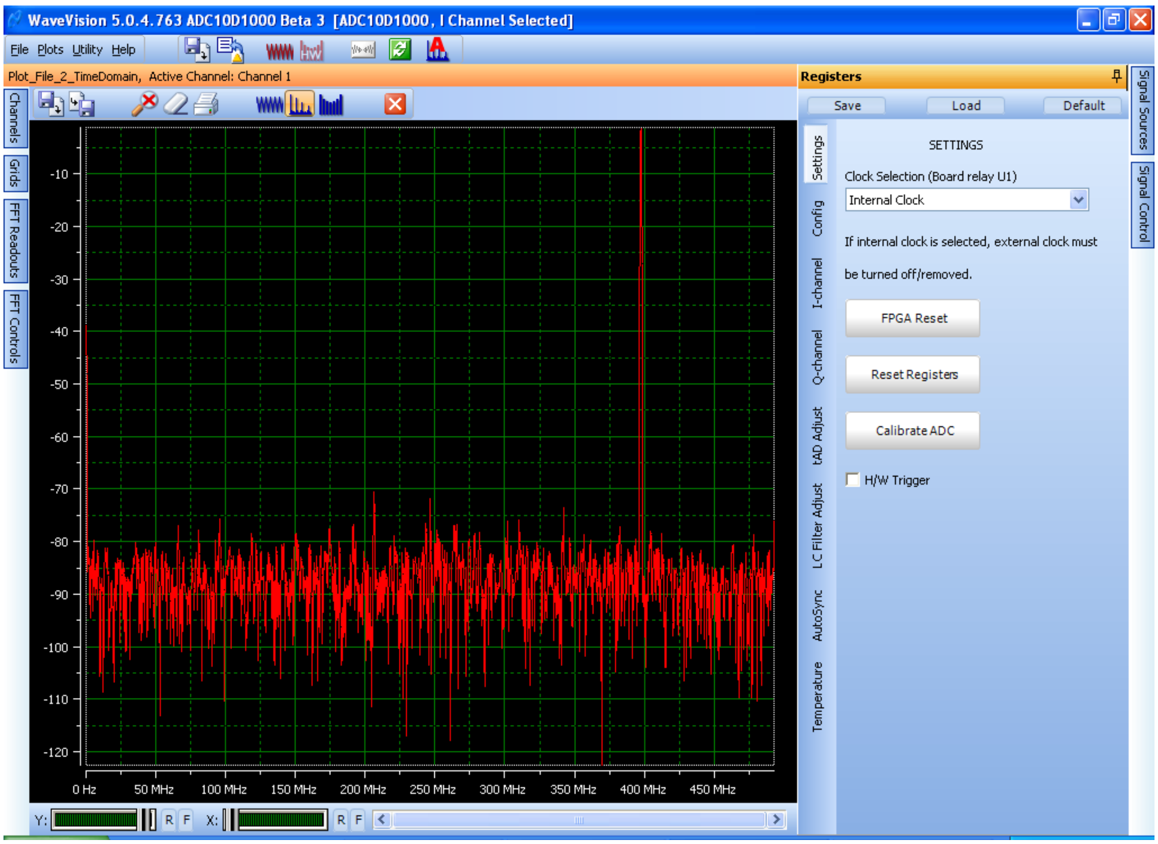


Figure 10: The top level of the Register panel showing the available tabs

The following is a short description of each tab under the ***Register*** panel.

Settings: This tab gives choice of either External Clock or Internal Clock, and buttons to initiate FPGA Reset, Reset Registers and Calibrate ADC. Calibration of the ADC should be performed if changes occur such as device temperature, mode changes (single channel to dual channel, single edge sampling (Non-DES) to double edge sampling (DES). For more information, refer to the Calibration section of the ADC10D1000/1500 datasheet. The H/W Trigger function is also enabled using the check box on this tab.

Note: If the Internal Clock is selected, then the External Clock signal generator should be disconnected or switched off to prevent performance degradation.

Config: This tab configures various features and modes of the ADC10D1000/1500 and is shown below. It accesses or changes the following functions, all of which are controlled through Configuration Register 1.

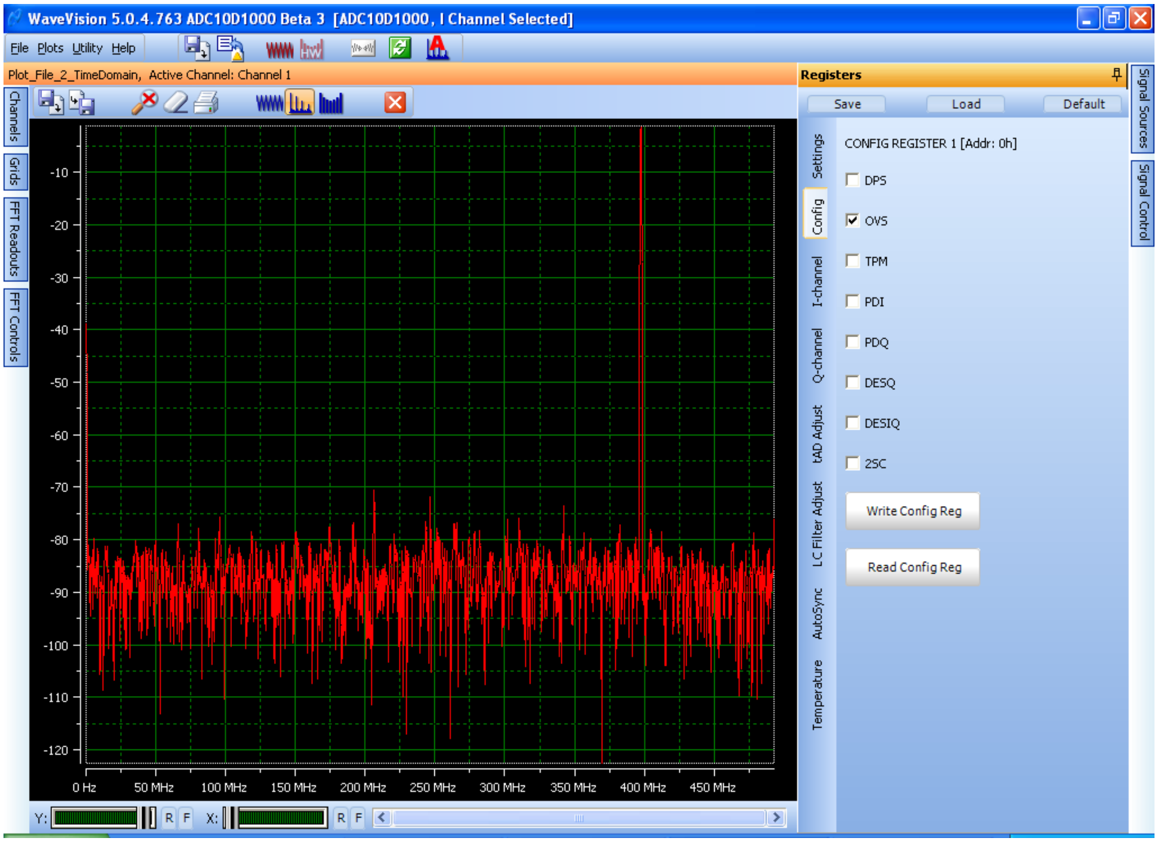


Figure 11: Config Panel

- **DPS** – DDR Phase Select – Determines the DDR Data-to-DCLK phase relationship. When unchecked, the 0° Mode is selected. When checked the 90° Mode is selected. This bit has no effect when the Non-Demux Mode is selected.
- **OVS** – Output Voltage Select – Selects the LVDS differential output voltage. When this is unchecked, the reduced output amplitude is selected. When checked, the standard (higher) output amplitude is used.
- **TPM** – Test Pattern Mode – When checked the device will continually output a fixed pattern on the Data and OR outputs. When cleared, the normal ADC Data and OR information are output.
- **PDI** – Power down I Channel when checked.
- **PDQ** – Power down Q channel when checked.
- **DES** – Double Edge Sample mode is selected when checked.
- **DESQ** – Double Edge Sample mode uses Q input (rather than I input) when checked.
- **DESIQ** – Double Edge Sample mode with I and Q as input – shorts both I and Q inputs together.
- **2SC** – Two's Complement output mode is selected when checked. Default is offset binary.

Note: No changes will take effect until the **Write Config Reg** button is clicked.

I-channel: This tab changes the sign and the magnitude of the offset and the full scale range settings.

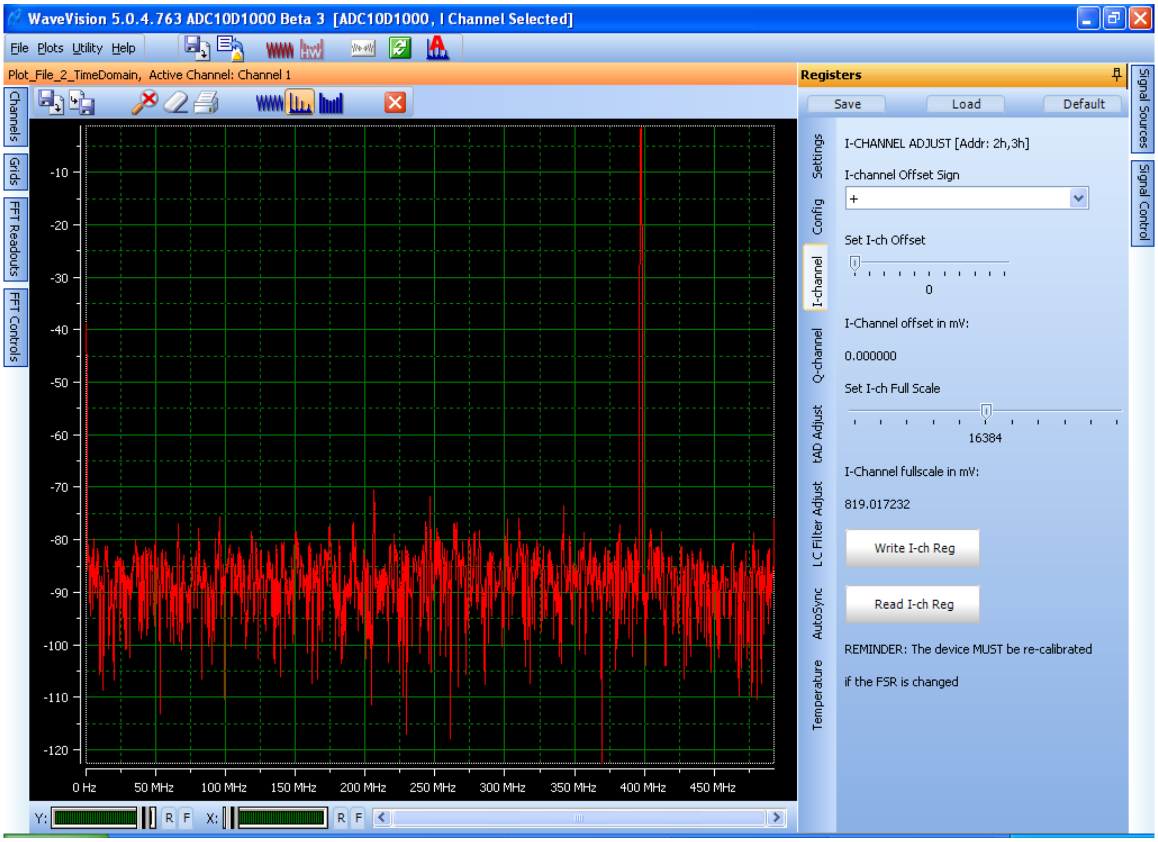


Figure 12: I-Channel Panel

- **I-channel Offset Sign** – This pull-down selects a positive or negative offset.
- **I-ch Offset** – This slider selects the magnitude of I-ch Offset applied. Adjustment can be done using the computer mouse/pointer, or using left/right arrow keys once the slider has been selected. Although the offset is entered in a 10 bit (0 to 4095) relative form, it is also displayed in approximate mV.
- **I-Channel Full Scale** - The approximate I-Channel input full scale range (mV peak-to-peak) is selected, ranging from a minimum of 600mV to a maximum of 980mV. The default setting is 790mV.

Note: No changes will take effect until the **Write I-ch Reg** button is clicked. Also, the ADC must be re-calibrated if the full-scale is changed.

Q-channel: Similar to I-channel

t_{AD} Adjust: This tab controls the Aperture Delay function.

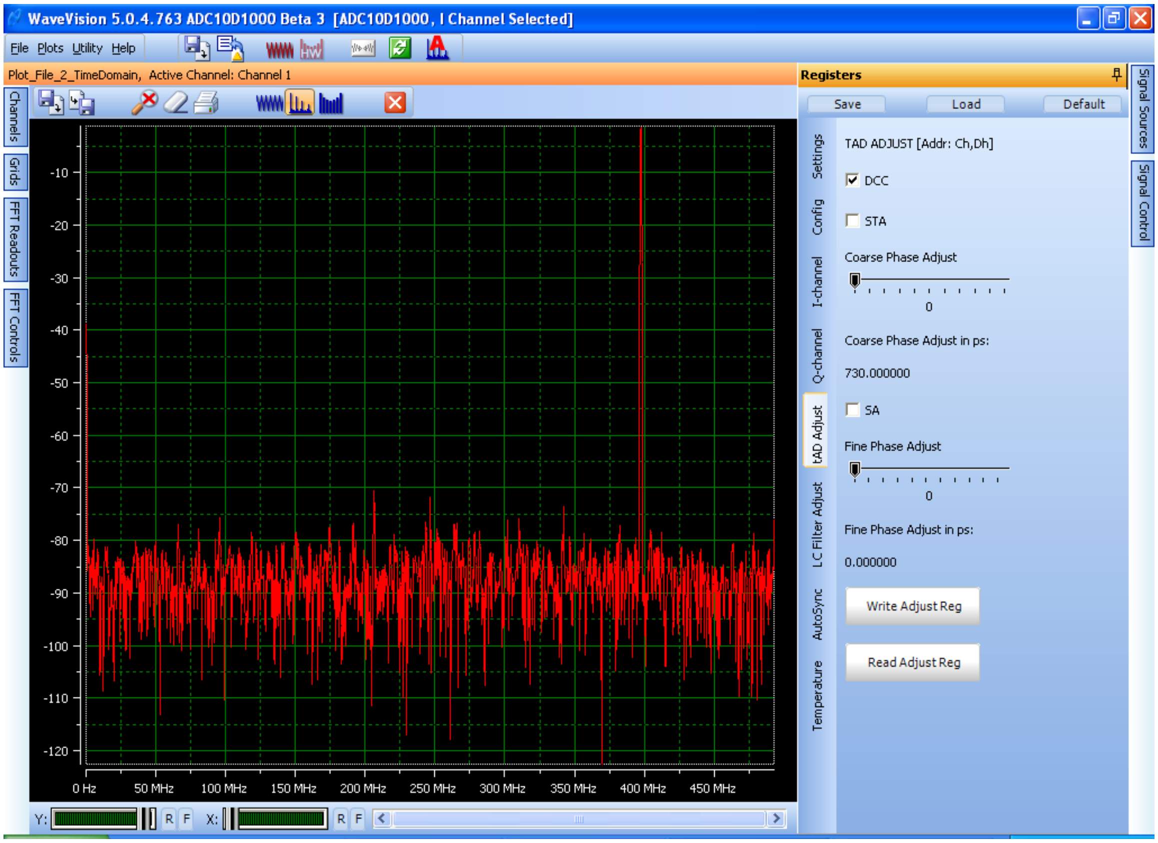


Figure 13: t_{AD} Filter Adjust Panel

- **DCC** – Duty Cycle Correction – When checked (default), the automatic Duty Cycle Correction circuit is enabled.
- **STA** - Select t_{AD} Adjust – When checked, enables the Aperture Delay Time adjust feature.
- **Coarse Phase Adjust** – Sets the approximate amount of coarse Aperture Delay applied.
- **Fine Phase Adjust** – Sets the approximate amount of fine Aperture Delay applied.
- **SA** – Select tAD Adjust with LC Filter Enabled – When checked, enables the Aperture Delay Time adjust feature, with the LC Filter enabled as well. (Overrides the STA function)

Note: No changes will take effect until the **Write Adjust Reg** button is clicked.

LC Filter Adjust: This tab enables and controls center frequency for clock LC filter.

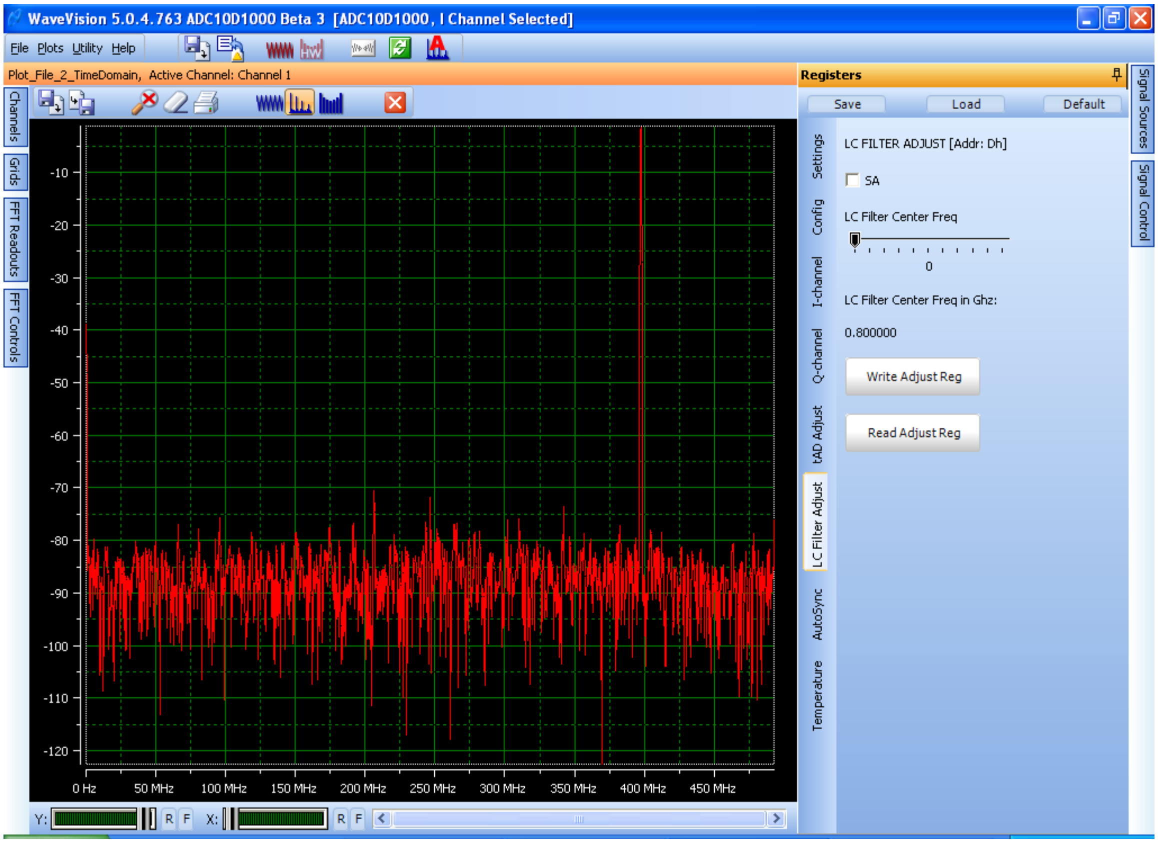


Figure 14: LC Filter Adjust Panel

- **SA** – Select tAD Adjust with LC Filter Enabled – When checked, enables the Aperture Delay Time adjust feature, with the LC Filter enabled as well. (Overrides the STA function)
- **LC Filter Adjust** – Selects the approximate LC Filter center frequency.

Note: No changes will take effect until the **Write Adjust Reg** button is clicked.

AutoSync: This tab enables and controls the settings of the AutoSync feature.

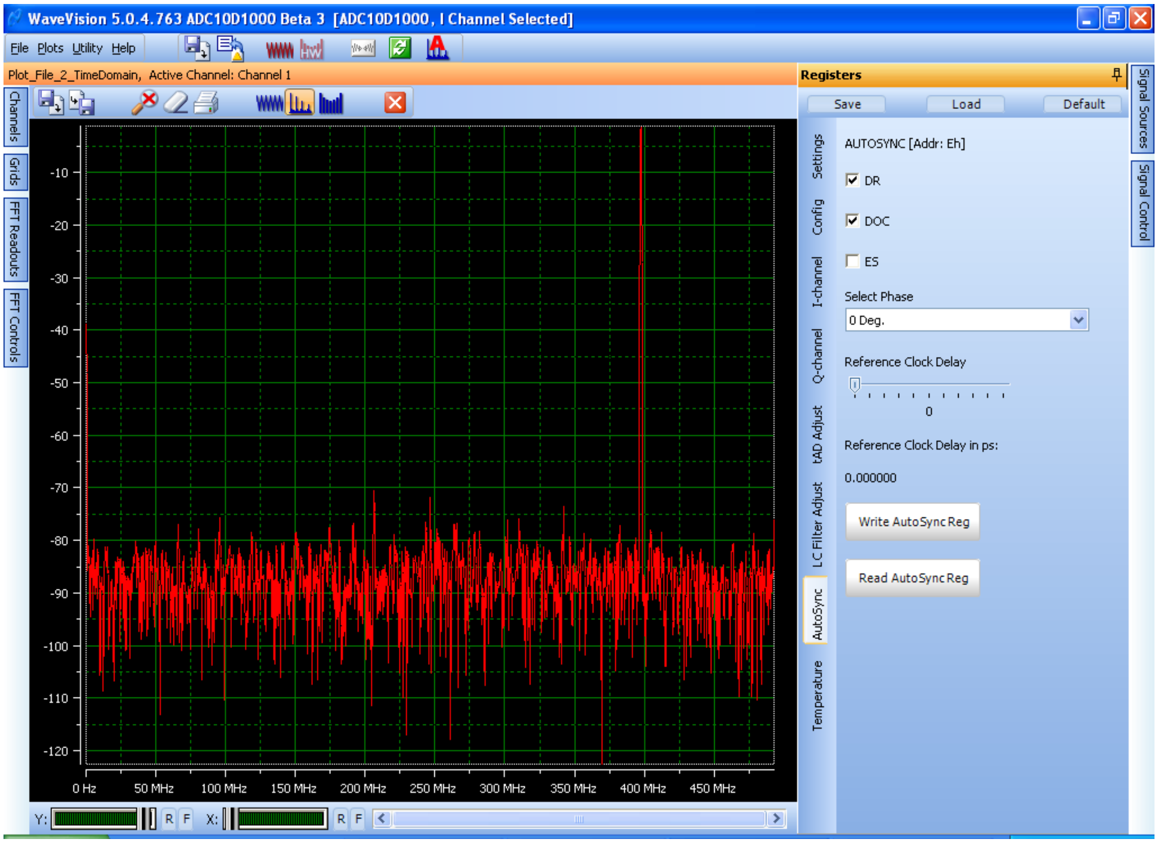


Figure 15: AutoSync Panel

- **DR** – Disable DCLK Reset – When checked (default) disables the DCLK Reset feature
- **DOC** – Disable Output reference Clocks – When checked (default) disables the AutoSync reference output clocks. When un-checked a CLK/4 signal is sent on the RCOut1 and RCOut2 outputs.
- **ES** – Enable Slave mode – When checked configures this ADC as an AutoSync slave device.
- **Select Phase** – Selects the Phase of the incoming reference clock used by the AutoSync feature.
- **Reference Clock Delay** – This selects the additional delay added to the input reference clock. Settings are 0d (0s) to 639d (1000ps). Settings higher than 639d will give 1000ps delay.

Note: No changes will take effect until the **Write AutoSync Reg** button is clicked.

Temperature: This panel provides a read-out of three different temperatures in the ADC10D1000/1500RB.

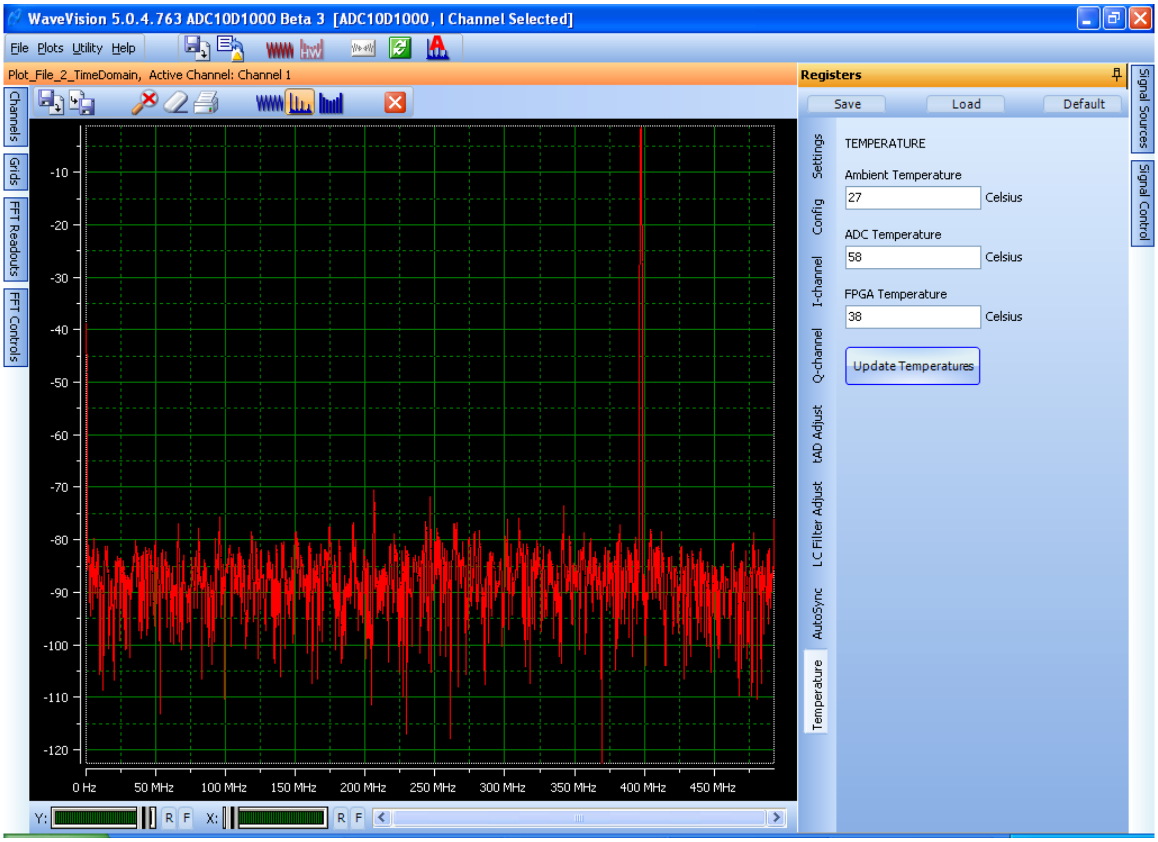


Figure 16: Temperature Panel

- **Ambient Temperature** – Provides the local/board temperature of the LM95233 IC.
- **ADC Temperature** – Provides the approximate die temperature of the ADC10D1000/1500.
- **FPGA Temperature** – Provides the approximate die temperature of the Xilinx Virtex-4 FPGA.

Note: No changes will appear until the **Update Temperatures** button is clicked.

2.6 Data Capturing

The board is now ready for a data capture. Before proceeding, perform a manual calibration of the ADC. Even though the ADC performs a self-calibration at the time of power-up, it is recommended that the user perform another calibration after sufficient time has passed for the system (primarily temperature) to stabilize. Manual calibration is performed by clicking the *Calibrate ADC* feature in the *Register* control panel, *Settings* sub-tab.

2.6.1 Configure Display Settings

Open the FFT Control left panel. Confirm that the *dBFS* unit is selected. Also confirm that the correct clock frequency is being measured by the software by checking in the *Signal Source* right panel. The default frequency of the on-board clock source is shown in the board performance data shipped with your board.

2.6.2 Check Input Amplitude

Confirm that the Over-range LEDs are not illuminated. Now increase the signal amplitude 'till the LED for the input in use is just barely lit. *DO NOT increase signal power much beyond this point as the ADC's inputs can be damaged if the Operating Maximums are exceeded (see Electrical Specification section).* Then reduce the signal amplitude until the Over-range LED is no longer illuminated. You should now have an input signal that is very close to the ADC's full-scale range (e.g., within 0.5 to 1.0 dB).

IMPORTANT: Since the ADC signal and clock inputs are not provided with additional protection circuitry on this board, the burden is on the user to not overdrive the inputs to the extent of damaging them. An "Over-range" LED is provided for each channel to indicate that the signal amplitude is beyond the ADC full-scale range. Increasing the signal amplitude much above this point will soon violate the Absolute Maximum ratings of the chip and irreparable damage to the device may be done. Thus, the safe method of setting the signal amplitude to full-scale level is to utilize the LED as described in the previous paragraph to roughly obtain the full-scale amplitude and then inspect the captured data in the software's time-domain plot to fine tune the amplitude to the desired level.

2.6.3 Acquire and Display Data

Perform a data acquisition by clicking the Acquire Data button (Item #5 in Figure 6).
The acquired data will now appear in the (default) time domain plot window. Switch to the frequency-domain window (FFT) using the WaveVision 5 controls. Type Ctrl-r to obtain the summary of the acquisition. Place the software in continuous mode (Item #6 of Figure 6) and then acquire again. This is to confirm that the Over-range LED method used earlier indeed gave a signal to the ADC that is within -0.5 to -1.0 dB of the full-scale range. If not, adjust the input signal generator's signal power to approximately -0.5dB of full scale.

At this point, dynamic performance metrics similar to those shown on the reference data shipped with the board may be obtained. One of the basic variables that you may experiment with at this point is to change the input signal strength and frequency. Please note that to achieve the reference performance, band-pass filters similar to the items referenced in Section 2.2 should be used. The absence of these filters on the input signal or external clock will usually result in sub-standard performance.

The displayed units should be in dBFS as selected earlier. You may switch the units to dBc and back to dBFS as desired.

2.6.4 External Clock Source

It is also possible to apply a high-quality external signal source to the clock input rather than using the on-board LMX2531 clock synthesizer. This will help quantify the LMX2531's performance in an ultra-high-speed signal-path such as this one. When connecting an external clock source, the generator amplitude should be set to 0dBm. Experiment with the clock signal strength to determine what effect this has on the channel performance. Care should be taken to not exceed +4 dBm at the clock input, to avoid damage to the ADC.

The external clock source is enabled through the register control panel in the software after applying the signal generator to the Clock input SMA.

The external clock source should be disconnected or turned off when the on-board clock source is selected. Failure to do so will result in poor performance due to the mixing of the on-board clock and the small amount of external clock signal leaking through the clock selection relay.

It is important to keep in mind that if the ADC's operating conditions are changed in any significant way, especially temperature, the ADC should be calibrated again before proceeding.

Please refer to the WaveVision 5 Users' Guide and integral Help feature for more information concerning the software.

3.0 Secondary Panel Description

Please refer to the WaveVision 5 Users Guide for detailed descriptions of the remaining Left and Right panels, and additional Main Panel features.

4.0 Reference Board Functional Description

4.1 System Block Diagram

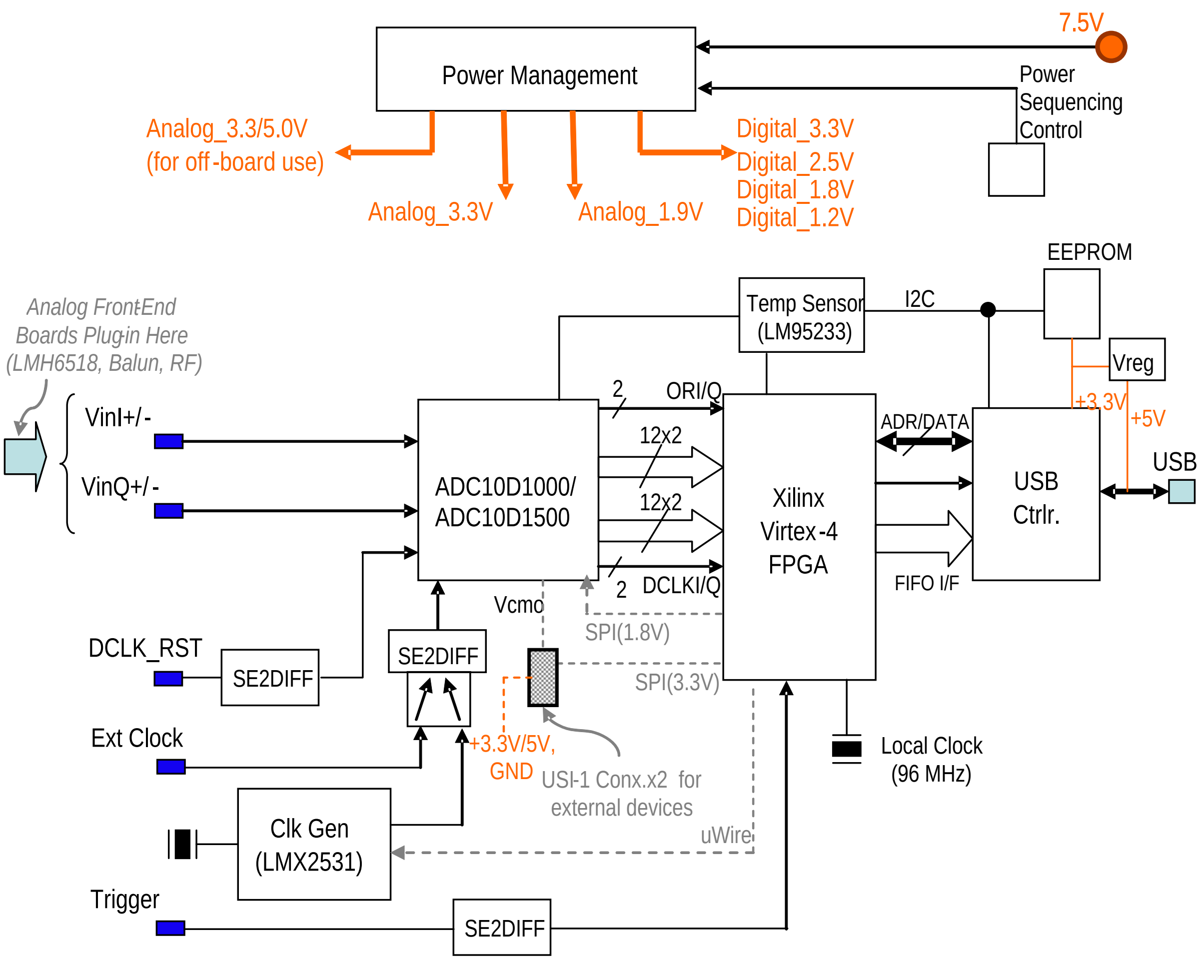


Figure 17: ADC10D1000/1500RB System Block Diagram

4.2 System Description

4.2.1 The ADC10D1000/1500

ADC10D1000/1500 forms the heart of this reference board. This low-power, high-performance CMOS analog-to-digital converter digitizes signals at 10-bit resolution at guaranteed minimum sampling rates of 1.0/1.5 Gs/s in dual channel configuration and 2.0/3.0 Gs/s in single channel configuration. The ADC10D1000/1500 is targeted at achieving very good accuracy and dynamic performance while consuming less than 4 Watts of power when both channels are powered-up. The product is packaged in a thermally enhanced BGA package that does not require a heat sink over the rated ambient temperature range of -40 degrees C to +70 degrees C. Refer to the latest version of the ADC10D1000/1500 datasheet for more detailed information.

This reference board gives complete control over the ADC10D1000/1500 and gives the user direct performance results of the chip without the need for an elaborate setup. Each of the device's control pins may be set high or low. Control is provided in two different manners - direct pin control with jumpers or through the serial interface (the device's extended control mode) using the WV 5 register control panel. *In order to use the extended control mode the ECE jumper must be set to LOW.* This is the recommended method and gives the user the most flexibility and ease of use.

Analog Front-End: The analog signal connection to the ADC is kept simple on this board in order to achieve the highest possible bandwidth. The board is designed to be coupled to front-end circuitry in a DC or AC coupled manner. AC-coupling requires the use of dc-blocks on the SMA connectors. By default, the board is shipped by National with dc-blocks. In addition, the board is also jumper-configured for DC-coupled operation (pin 9 on J15 is removed for DC operation).

IMPORTANT: Since the ADC signal and clock inputs are not provided with additional protection circuitry on this board, the burden is on the user to not overdrive the inputs to the extent of damaging them. An "Over-range" LED is provided for each channel to indicate that the signal amplitude is beyond the ADC full-scale range. Increasing the signal amplitude much above this point will soon violate the Absolute Maximum ratings of the chip and irreparable damage to the device may be done. The same caution applies to the clock input when an external signal generator is used. However, in this case, there is no Over-range LED to assist the user. In National's lab setups, a clock signal generator power level of 0dBm is used. Going beyond +4dBm at the IC pins could damage the device.

Multi-channel ADC synchronization: A DCLK_RST signal input is provided to synchronize the ADCs on multiple boards or systems. In addition, the ADC10D1000/1500 supports a new method of ADC synchronization, called AutoSync. Please refer to the ADC10D1000/1500 datasheet for more details.

4.2.2 LMX2531 Clock Synthesis chip

The LMX2531xxxx family provides a single-chip, very low-jitter clock solution at frequencies up to almost 3.0 GHz. In this application, the LMX2531LQ1500E is used - which can be programmed to operate over a range of 1499-1510 MHz. On the ADC10D1500RB board, the device is configured for a frequency in this range through the serial interface which may be controlled through the WaveVision 5 register control panel. The particular frequency chosen is one that generates the least phase noise. It is not necessarily a round number but depends on the loop feedback of the PLL’s in the clock synthesis chip.

The clock source for the ADC can be selected between the on-board LMX2531 or an external clock source connected through the J11 SMA connector. The selection is performed through the WV 5 register panel. It is recommended that the external clock source should be connected and enabled before it is selected. ***For optimum performance, the external clock signal generator and the LMX2531 should not be enabled at the same time.*** This is because the RF relay used to select between them does not provide adequate isolation to keep one from affecting the other. Having both clocks on simultaneously will result in excessive spurious signals. The default setting for this board is the on-board LMX2531 clock source.

4.2.3 FPGA

The design employs a Xilinx Virtex-4 FPGA for capturing the digital data. While the board is powered up and configured, the FPGA is continually receiving data from the ADC. In response to a user command through the WV-5 software, the ADC captures the desired amount of data in its on-chip buffer (up to a maximum of 32K samples per-channel). The user can then command the FPGA to upload the captured data to the PC through the USB interface for further processing.

This board can support the ability to program the FPGA for specific requirements. A standard JTAG connector is provided for downloading FPGA object code from the Xilinx development environment.

Please note that National Semiconductor does not provide support for any user-designed FPGA functionality beyond the standard functionality that is shipped with the board.

Hardware Trigger: The board design supports an external hardware trigger that is connected to the FPGA. When the hardware trigger is enabled, an acquisition can be selected from the software, but the actual beginning of data capture will be postponed until the external trigger pulse is applied to the J26 SMA connector.

Auxiliary Port: Two Mictor 38-pin connectors form an auxiliary data port. With it, the user can program the FPGA to output high-speed continuous streaming data from the signal-path to the rest of the system.

This feature is currently not supported.

4.2.4 LM95233 Temperature Sensor

Using the National LM95233 temp sensor chip; the ambient, ADC10D1000/1500 and Xilinx FPGA temperatures can be monitored. The temperature readings are available through the WV-5 software.

5.0 Electrical Specification

Power Supply:	Nominal = 7.5V Minimum = 7.0V, Maximum = 8.0V *(Voltage above this level will cause damage!!)*
Power Consumption:	Nominal = 10 Watts Maximum = 20 Watts
ADC Input Signals:	Maximum Operating Voltage = +2.0V Recommended/initial (full scale) generator setting = 0 dBm Maximum generator setting = +5 dBm *(Voltage above this level will cause damage!!)*
Clock Input Signal:	Maximum Operating Voltage = +2.0V Recommended generator setting = 0 dBm Maximum generator setting = +5 dBm *(Voltage above this level will cause damage!!)*
USB Port:	USB 2.0 compliant

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