Application Note

Driving Multiple Loads With a Single LVCMOS Oscillator

Connor Lewis, William Pfennigwerth

ABSTRACT

In an effort to reduce cost and simplify BOM, designers of some systems want to drive multiple loads with a single clock source in applications where the signal integrity of the clock is not critical. Low frequency, single-ended LVCMOS clock signals can be a good target for this type of cost reduction since jitter requirements are usually relaxed and the cost of an oscillator can be relatively high relative to the receiver that it is clocking. However, this technique can raise a number of questions about the specific routing implementation and the affect on signal integrity. How does co-location of loads affect signal integrity? What is the longest acceptable trace length between multiple loads? How many receivers can a single clock source drive while maintaining acceptable rise or fall times, and how does this effect ringing and signal reflections? This application note discusses the transmission line effects of splitting a trace into multiple loads, and provides some recommended topologies based on IBIS simulation results using the *Low-jitter, high-performance, bulk-acoustic-wave (BAW) fixed-frequency LVCMOS oscillator.*

Table of Contents

Trademarks

1 Introduction and Test Methodology

When clocking a system at high frequencies or with long trace lengths, cables and PCB traces are usually treated as transmission lines and not just as a simple wire. As a general rule, the estimate is that transmission line effects need to be considered when the propagation delay through the trace or cable is greater than 0.25 times the signal's rise time. For example, a typical PCB made of FR-4 material can have a signal propagation delay of around 150ps/in. Assuming a signal rise time of 1ns, then any trace longer than around 1.5 inches can behave like a transmission line and can have signal integrity concerns if not addressed.

The following simulation results show the effects of driving multiple loads with a single LVCMOS oscillator using various routing schemes. To perform the simulations, we designed a 4-layered stackup in Altium Designer and determined the trace width needed to create a nominal 50Ω characteristic trace impedance. This particular stackup was chosen such that traces with a nominal 50Ω impedance can be closely matched to the pad size of 0201 passive components, resulting in minimal reflections when the signal passes through onboard resistors and capacitors.

With this stackup we designed a series of PCB layouts to emulate several different methods of routing a driver to multiple loads . The layout files were then converted for use in IBIS SI simulations using a 25MHz TI LMK6C BAW Oscillator as the driver.

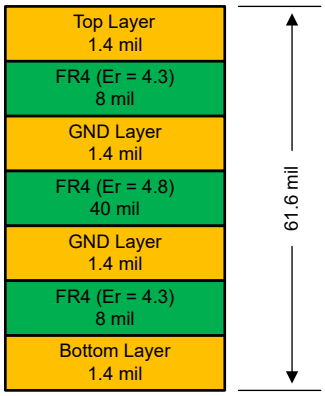

Figure 1-1. Stackup Used in Load Board Simulation

Table 1-1. Trace Impedance vs. Thickness Using Load Board Stackup

Trace Thickness (mil)	Characteristic Impedance (Z_0) of Trace
9	60Ω
13	50Ω
20	40Ω

When routing to multiple loads, line resistors can be placed for 50Ω impedance matching. Each routing scheme drives either one, two, or four loads with a combined capacitance of 10pF. The overall load capacitance was constant across all of the tests because to make sure that the routing topology was the only variable that was changed. Figure 1-2 demonstrates how increasing the overall capacitive load for the LMK6C LVCMOS oscillator can increase rise and fall times and can degrade performance. This factor was eliminated from the experiment by using a constant 10pF load to account for the worst case scenario of driving four loads, each with the nominal load capacitance of 2.5pF. Section 2 contains a more in-depth description of the various trace and load topologies that were tested.

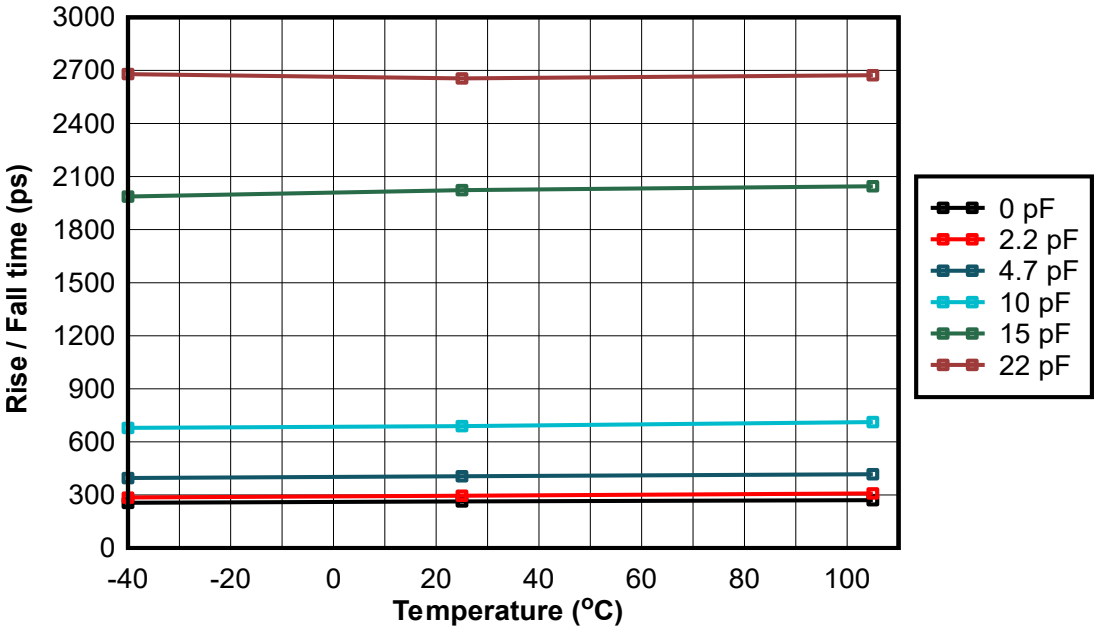

Figure 1-2. LMK6C Rise or Fall time (ps) vs Temperature and Load Capacitance for 25MHz Output Frequency, 3.3V Supply

2 Routing Topologies and Simulation Results

2.1 Single-Line

This is the typical configuration for a single-ended signal. The single line configuration is recommended for the best signal integrity since the number of nodes are reduced to only one load per line. The single-line, single-load configuration is used as a benchmark for the other topologies that were tested.

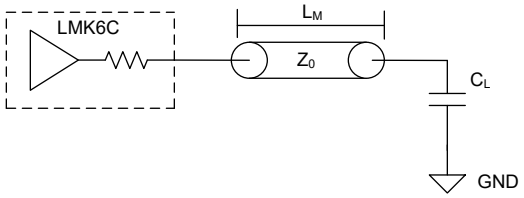

Figure 2-1. Single Line, Single Load Topology

The single-line, multi-load configuration is a good option for driving multiple loads when the separation between them is small. Some common use cases for this topology include driving two clock input pins on the same device, or multiple devices that are closely located. To be considered a single-line in the context of this study, the distance between loads need to be limited to under 1". The assumption is that each load is an equal distance from the main line, therefore L_S is the same length for each receiver.

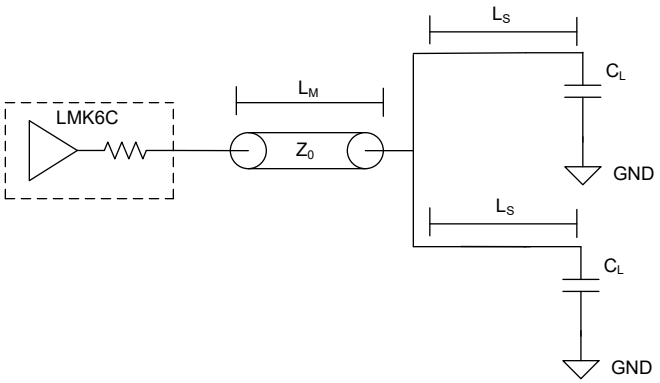

Figure 2-2. Single Line, Multiple Loads Topology

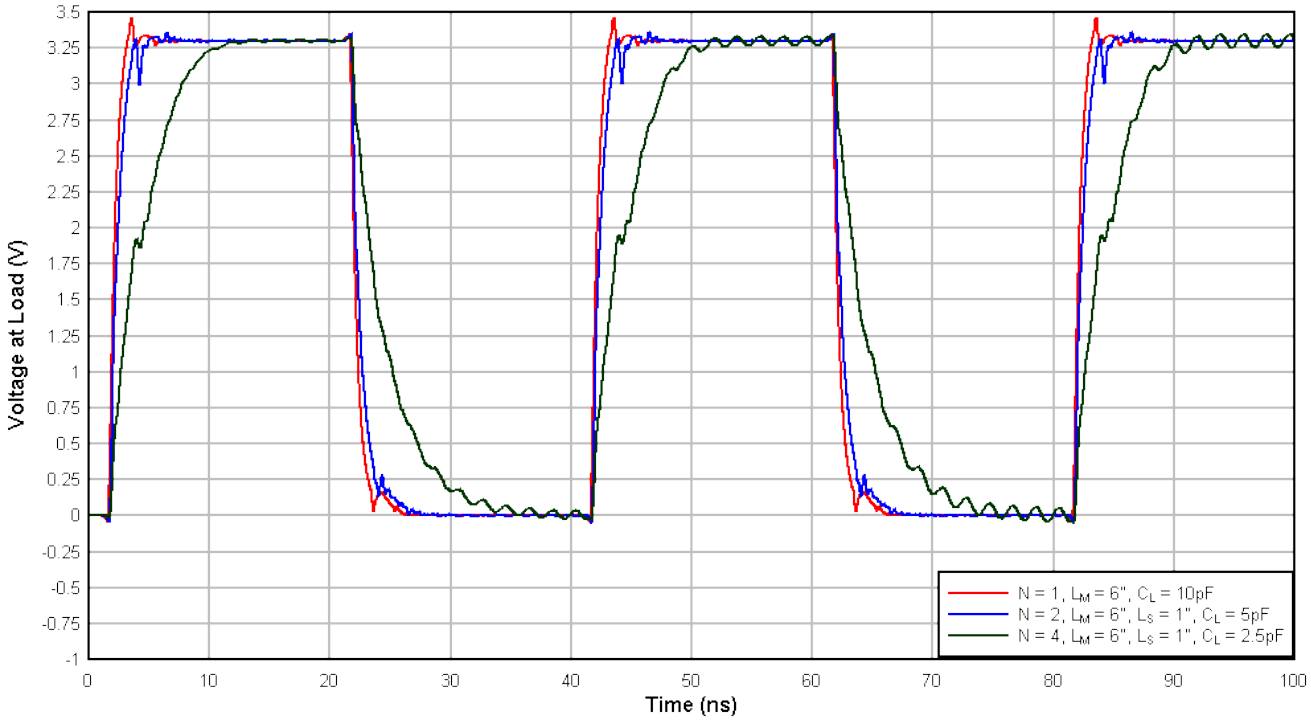

Figure 2-3. Single Line Simulation Results

Table 2-1. Single Line Rise or Fall Time

Number of Loads	Trace Length - L_M	Rise Time (ns)	Fall Time (ns)
1	6"	0.676	0.763
2	6"	0.938	1.105
4	6"	4.010	3.946

For single line configurations, driving two loads produces acceptable signal quality with only slightly longer rise and fall times and almost no measurable reflection artifacts.

With the addition of four loads, the rise/fall time slows significantly but there are still minimal reflections in the waveform.

2.2 Star Line

The star line configuration is an alternative design designed for when loads are not co-located on a board. This configuration starts out as a single output line from the driver, then splits off closer to the receiver side. Star line routing is similar to the single-line approach, but with receivers that are further than 1" apart.

Line resistors (R_t) are added to aid in impedance matching so the driver *sees* a continuous 50Ω impedance. R_t is calculated according to the formula in Equation 1.

$$R_t = \frac{N-1}{N+1} \times Z_0 \quad (1)$$

Where N is equal to the number of loads being driven and Z_0 is equal to the characteristic impedance of the trace.

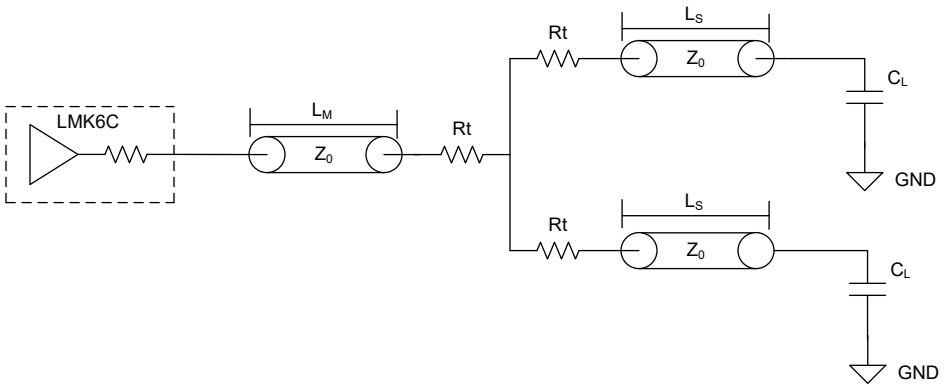

Figure 2-4. Star Line Topology

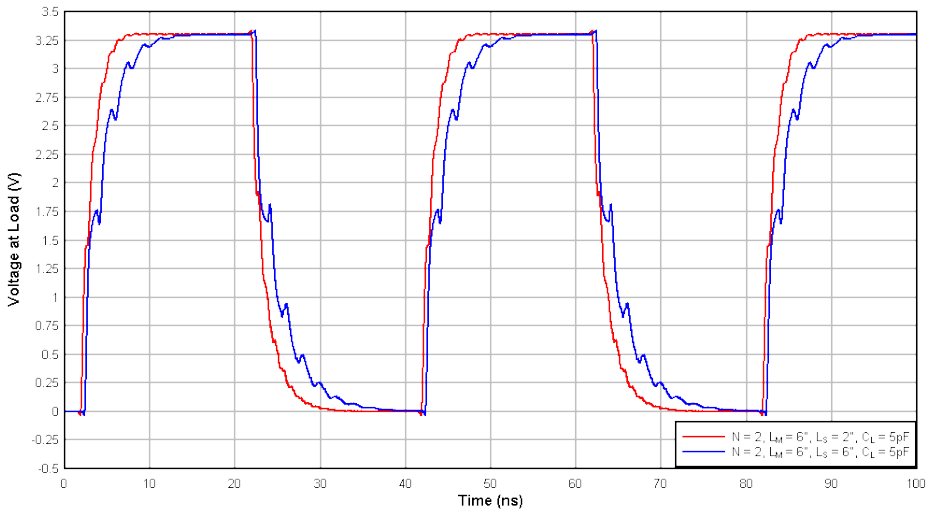

Figure 2-5. Star Line Simulation Results

Table 2-2. Star Line Rise/Fall Time

Number of Loads	Trace Length - L_S	Rise Time (ns)	Fall Time (ns)
2	2"	1.858	2.206
2	6"	2.839	3.980

For star line configurations, as it is similar to the single line configuration, with only 2" of split trace length we see the rise and fall times are increased with very slight rippling. As the trace length increases to 6", rippling worsens

and rise/fall time further increase. While this signal can be adequate to some receivers, increasing the split line length further can result in unacceptable signal integrity.

2.3 Split Line

The split line configuration can be used when loads are not co-located on a board. In this topology, the traces branch out close to the driver and behave as independent transmission lines for the majority of the trace distance.

Line resistors (R_t) are again added for impedance matching according to Equation 1.

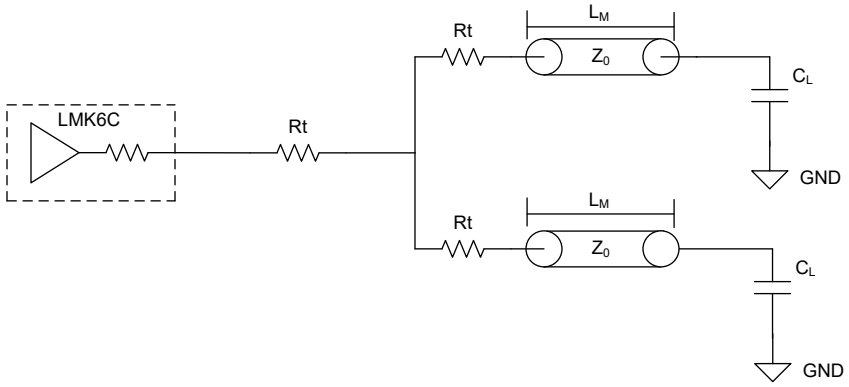

Figure 2-6. Split Line Topology

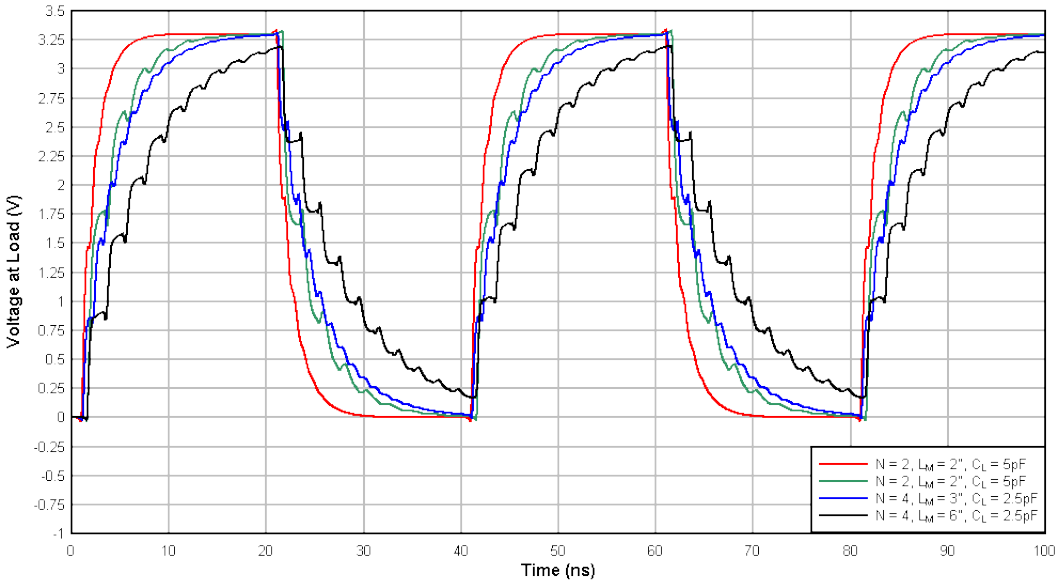

Figure 2-7. Split Line Simulation Results

Table 2-3. Split Line Rise or Fall Time

Number of Loads	Trace Length - L_M	Rise Time (ns)	Fall Time (ns)
2	2"	1.971	2.228
2	6"	3.762	4.556
4	3"	4.781	5.630
4	6"	7.998	10.16

For split line configurations, the number of loads and line length have a similar effect on signal integrity compared to the star line topology. As more loads are added an the trace length increases, the signal integrity worsens with more severe ringing and slower rise/fall times.

2.4 Star Line vs. Split Line

The star line and split line topologies were compared in a scenario driving two loads with a capacitance of 5pF each routed through a total of 8 inches of PCB traces. As shown in Figure 2-8, the star line approach results in better signal integrity and faster rise or fall times.

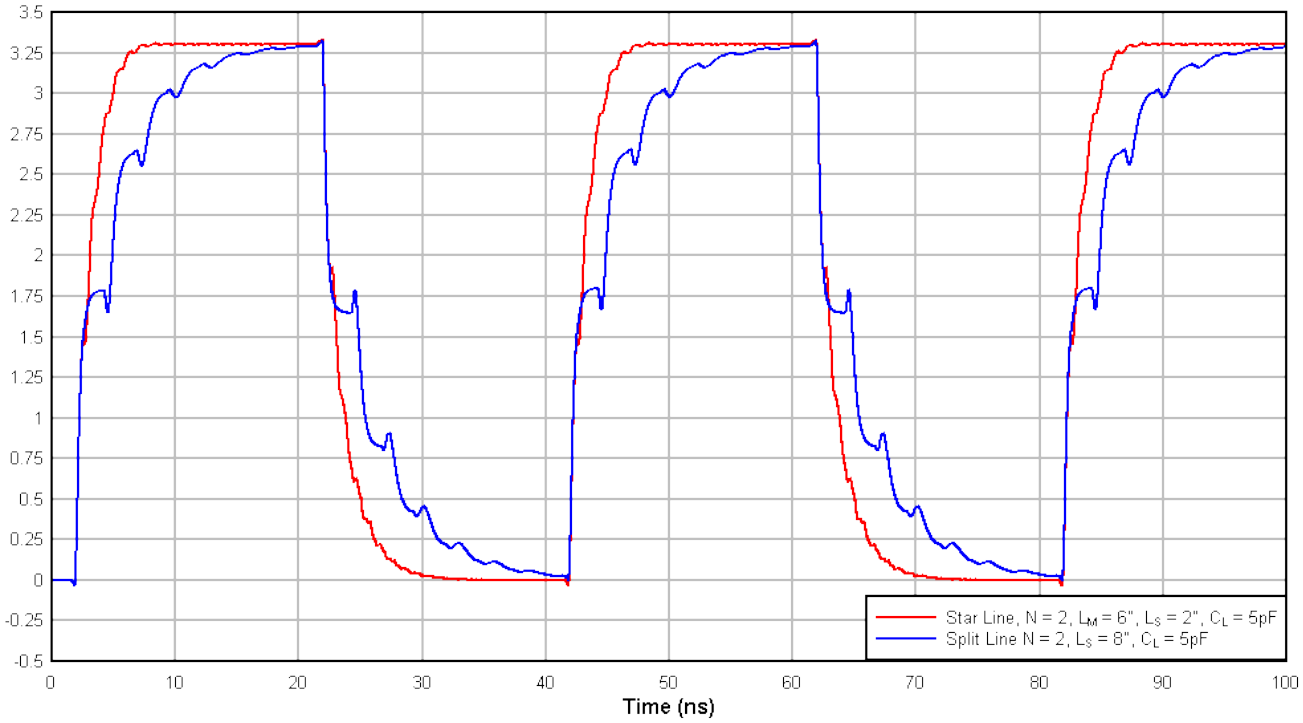

Figure 2-8. Star Line vs. Split Line Simulation Results

3 Summary

These simulations have shown some of the factors to determine if driving multiple loads with a single LVCMOS oscillator is feasible in a system. Driving multiple loads from a single LVCMOS oscillator can always degrade signal integrity in some way. For best performance one can limit the numbers of loads which needs to be directly driven out of LMK6C by using a *Clock buffer.*

Guidelines for driving multiple loads with a single oscillator:

- Limit the number of loads to 2
- Maximize common trace length before branching out to individual receivers as shown in Star Line topologies
- Limit total receiver capacitance to achieve fast rise/fall time

These guidelines can provide a basis for driving multiple loads in your system. By reducing the number of loads, reducing the brach trace length, and reducing the total parasitic and receiver capacitance, your system can be able to minimize the negative consequences of driving multiple loads with a single oscillator. The Star Line topology best models this kind of routing situation. If achieving absolute best performance is a priority, traces can never be split into multiple loads and instead a clock buffer like the 4-channel output LVCMOS 1.8-V buffer can be used to fanout the clock signal and drive multiple loads.

4 References

- Texas Instruments, LMK6x Low Jitter, High-Performance BAW Oscillator, data sheet.
- Texas Instruments, *LMK1C110x 1.8-V, 2.5-V, and 3.3-V LVCMOS Clock Buffer Family,* data sheet.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265