Application Report
SNAA308B–May 2017–Revised July 2017

LMK0461x Phase Noise Performance With DC-DC Converters

Puneet Sareen

ABSTRACT

The LMK0461x device family is the industry's highest performance with lowest power jitter cleaner family with dual PLLs called PLL1 and PLL2. PLL1 is a very low bandwidth PLL that uses an external VCXO as voltage control oscillator. PLL2 is a high bandwidth PLL with an integrated high performance LC oscillator. LMK04610 provides 10 differential outputs and the LMK04616 provides 16 differential outputs in addition to a pair of LVCMOS outputs.

To avoid coupling between different blocks, LMK046xx devices have a number of supply pins. A number of DC-DC converters are selected to power LMK04616 and their impact on the phase noise performance of the output clocks is analyzed in this document. Although all the LAB measurement results presented in this document are taken on LMK04616 EVM, they are also applicable to the LMK04610. The device is configured to accept a 122.88-MHz input clock frequency, 122.88-MHz VCXO and all output frequencies are programmed to 122.88 MHz.

Contents

List of Figures

List of Tables

1 Supply Pins in the LMK04616 and LMK04610 Devices

Figure 1 shows the different supply pins for LMK0461x. The description of the supply pins is given in Table 1.

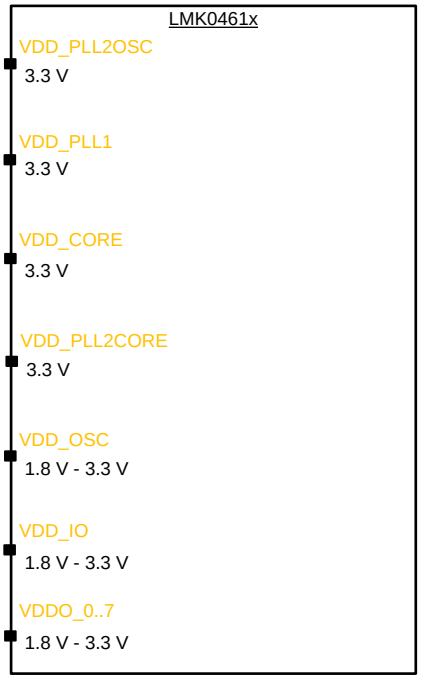


Figure 1. Supply Pins

Table 1. Supply Pin Descriptions

PIN NAME	LEVEL (V)	DESCRIPTION
VDD_CORE	3.3	Power supply for core
VDD_IO	1.8–3.3	Power supply for input block
VDD_OSC	1.8–3.3	Power supply for OSCout
VDD_PLL1	3.3	Power supply for PLL1
VDD_PLL2CORE	3.3	Power supply for PLL2
VDD_PLL2OSC	3.3	Power supply for PLL2 VCO
VDDO_X/Y	1.8–3.3	Power supply for CLKoutX and CLKoutY

Although each supply pin has on-chip LDO to provide additional decoupling and PSRR, ensure VDD_PLL1 is clean, because the VCXO control block directly runs on VDD_PLL1.

2 Recommended Power Supply Connections

The power supply connections, as shown in Figure 2, are recommended for the LMK04616 and LMK04610. For further details, refer to the corresponding EVM user guides.

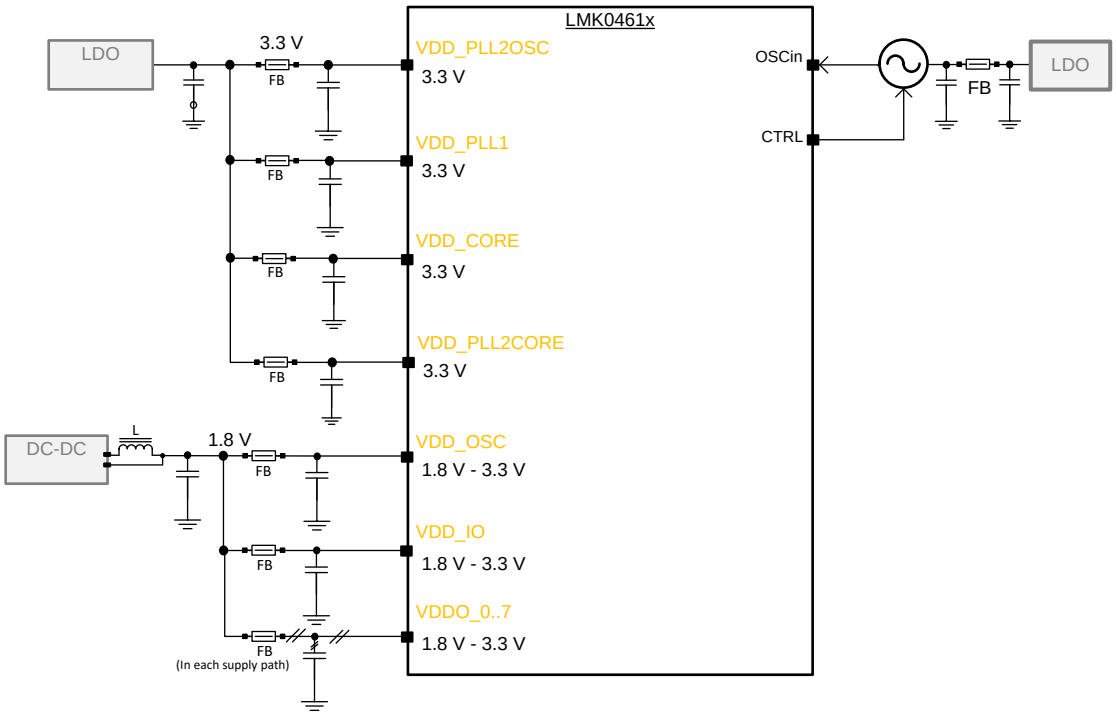


Figure 2. Recommended Power Supply Connections

3 Using DC-DC Power Supplies for LMK0461x

LMK0461x power pins can be suppled through an LDO and/or DC-DC converters. Impact of the DC-DC converters on the output clock phase noise is analyzed in this document. A number of low-noise DC-DC converters from Texas Instruments power products can be used with LMK046xx devices.

3.1 DC-DC Converters

The DC-DC converters in Table 2 are used for the clock phase noise bench measurements:

Table 2. Recommended DC-DC Converters

DC-DC CONVERTER PART NUMBER	OUTPUT VOLTAGE (V)
TPS62150	1.8-3.3
TPS62743	1.8-3.3
TPS62240	1.8
TPS62621	1.8
TPS62231-Q1	1.8
TPS62080	1.8
TPS54320	3.3
TPS54620	3.3
TPS54418	1.8
TPS54824	1.8

4 Bench Measurements

4.1 DC-DC Converter – TPS62150

TPS62150 DC-DC is mounted on the LMK04616 and LMK04610 EVMs provided by Texas Instruments. The DC-DC is configured like recommended in TPS62150EVM. The switching frequency is set to 1.25 MHz and output ripple is < 3 mV for I_{out} = 1 A as per the DC-DC data sheet. The phase noise results by using TPS62150 DC-DC converter supplying power to the LMK04616 are presented in the following sections.

4.1.1 All Output Supplies VDDO_X/Y Connected to DC-DC Converter (1.8 V)

The supply configuration shown in Figure 2 was used for the measurement and the output phase noise is shown in Figure 3.

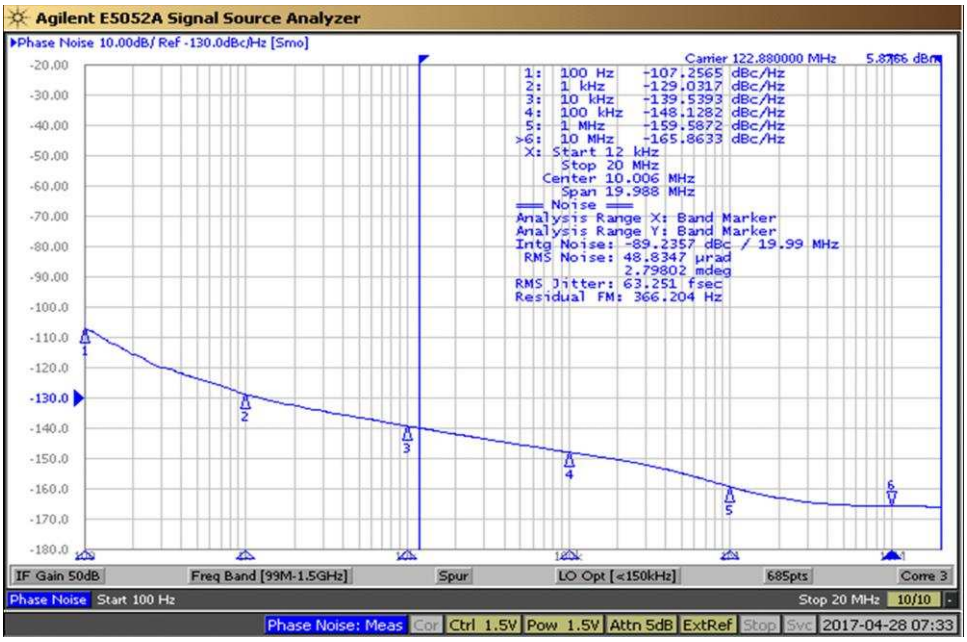


Figure 3. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 2

4.1.2 VDD_CORE Powered by the DC-DC Converter (3.3 V)

As shown in the supply configuration in Figure 4, VDD_CORE is connected to the DC-DC converter supplying 3.3 V, all other supplies are on LDOs. The output clock phase noise is shown in Figure 5. There is a marginal degradation in the phase noise performance below 1-KHz offset frequency.

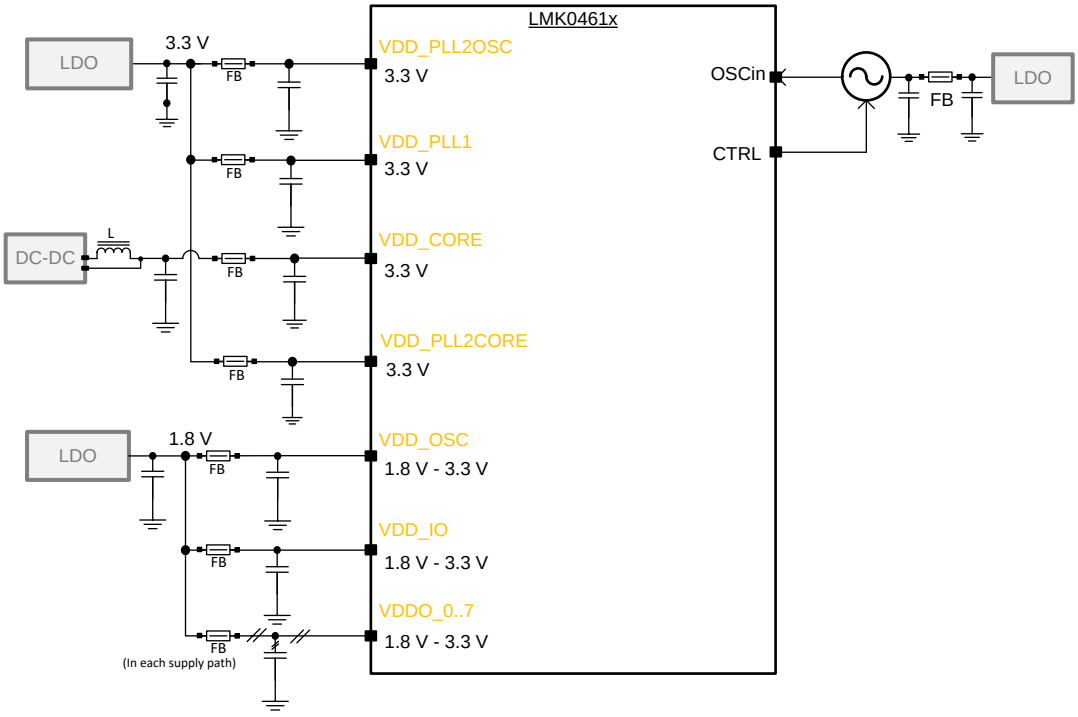


Figure 4. VDD_CORE is Powered by to the DC-DC Converter

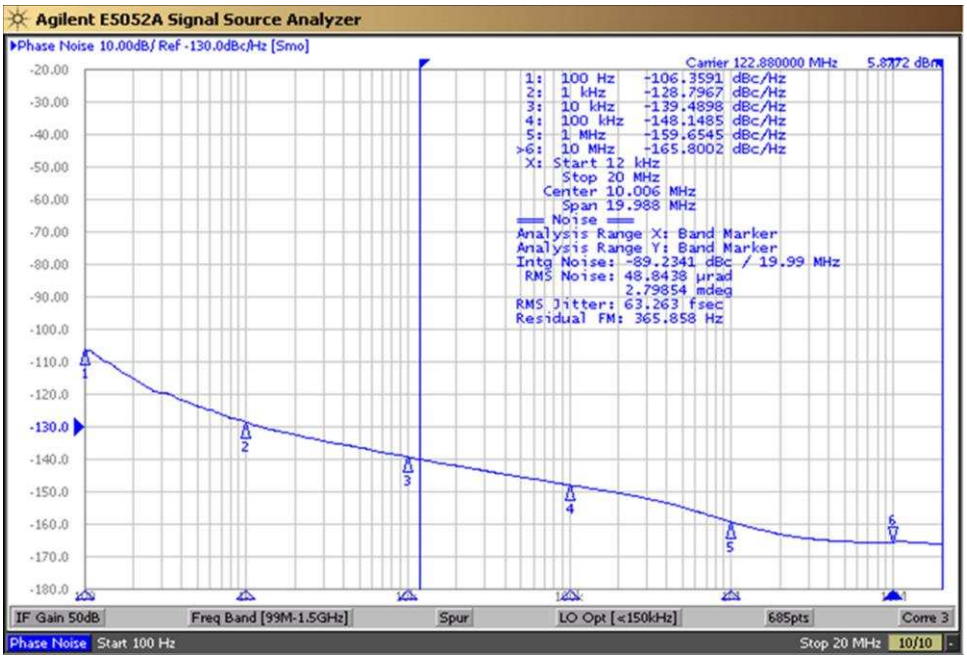


Figure 5. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 4

4.1.3 VDD_PLL1 Powered by the DC-DC Converter (3.3 V)

As shown in the Figure 6, only VDD_PLL1 is supplied with the DC-DC converter output at 3.3 V. There is a significant increase in phase noise at 100-Hz offset. Comparing the phase noise numbers in Figure 7 and Figure 3, the phase noise at 100-Hz offset degrades to –97.9 dBc/Hz when VDD_PLL1 is connected to the DC-DC converter, compared to –107.2 dBc/Hz when the VDD_PLL1 is connected to a low-noise LDO output.

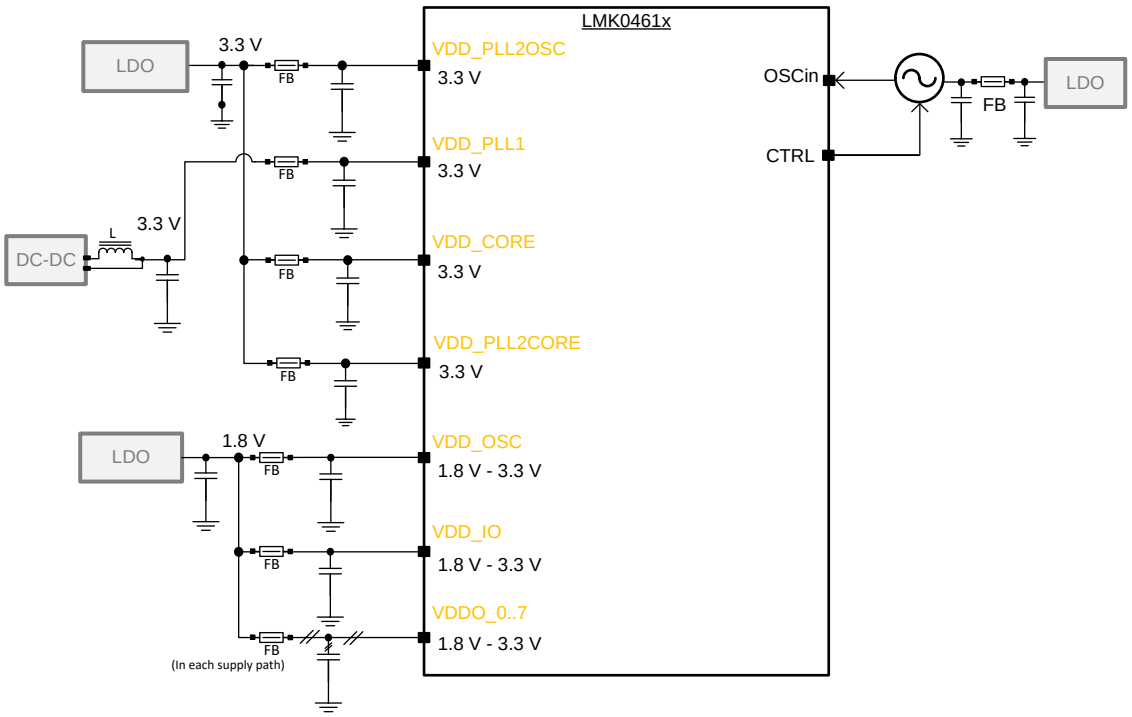


Figure 6. VDD_PLL1 Powered by the DC-DC Converter

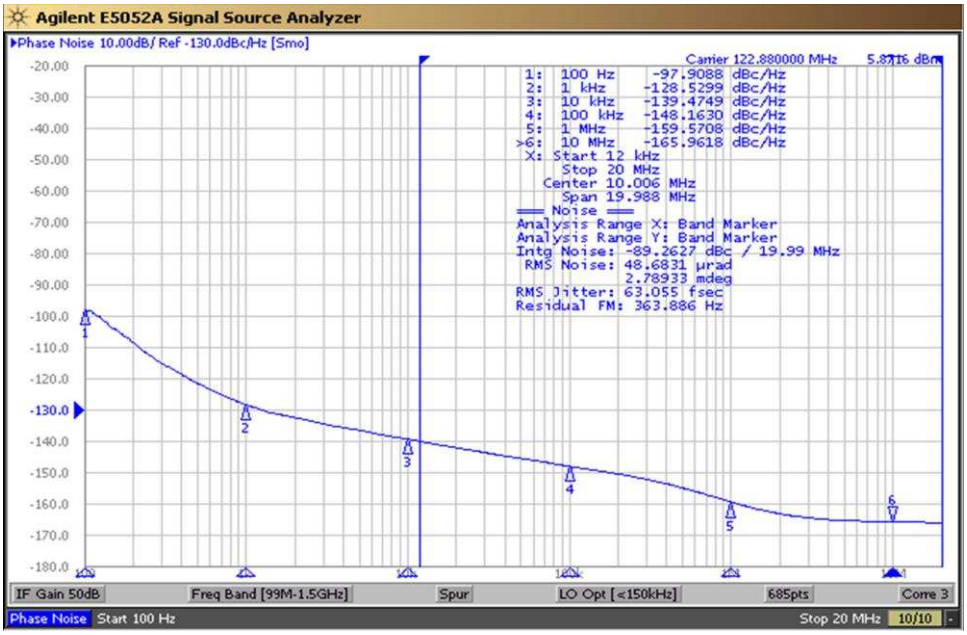


Figure 7. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 6

4.1.4 VDD_PLL2CORE Powered by the DC-DC Converter (3.3 V)

The supply connections are shown in Figure 8. Connecting the VCC_PLL2CORE to the DC-DC converter shows almost no degradation in the phase noise performance.

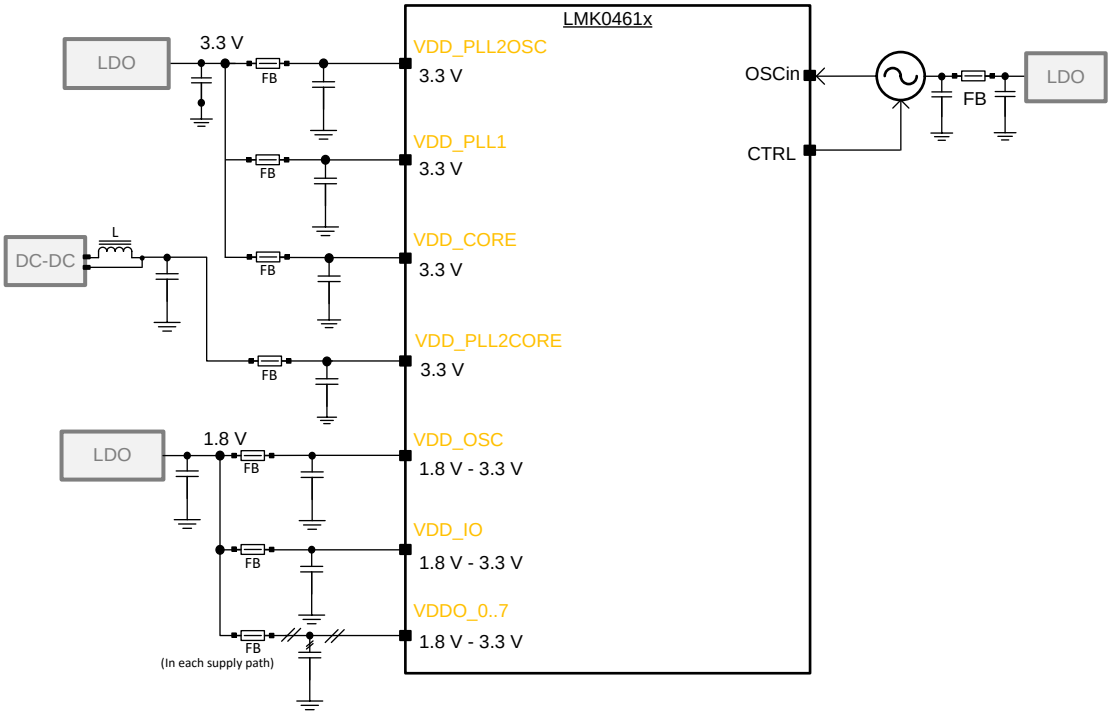


Figure 8. VDD_PLL2CORE Powered by the DC-DC Converter

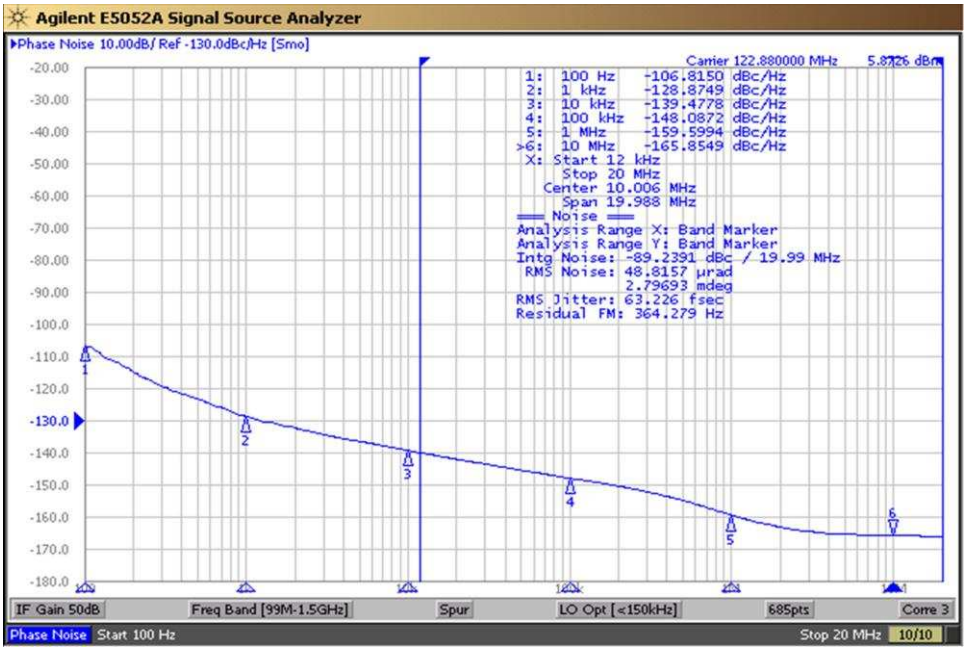


Figure 9. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 8

4.1.5 VDD_PLL2OSC Powered by the DC-DC Converter (3.3 V)

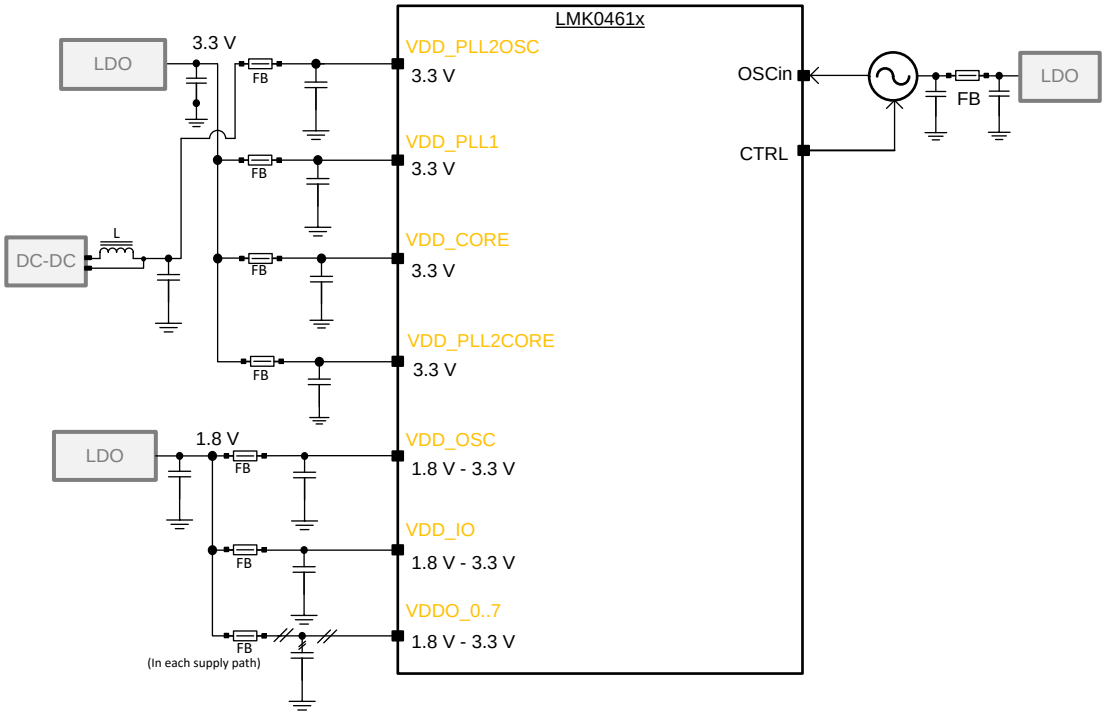


Figure 10. VDD_PLL2OSC Powered by the DC-DC Converter

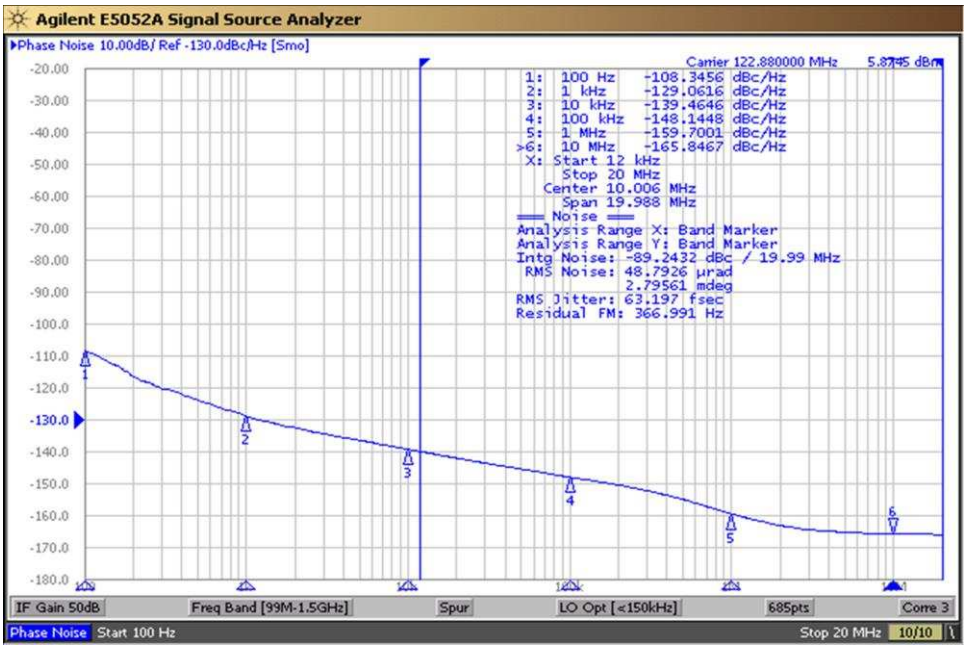


Figure 11. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 10

4.1.6 VDD_OSC Powered by the DC-DC Converter (3.3 V)

The supply configuration is shown in the Figure 12 where the VDD_OSC is connected to the DC-DC converter. No degradation in phase noise performance is observed as shown in Figure 13.

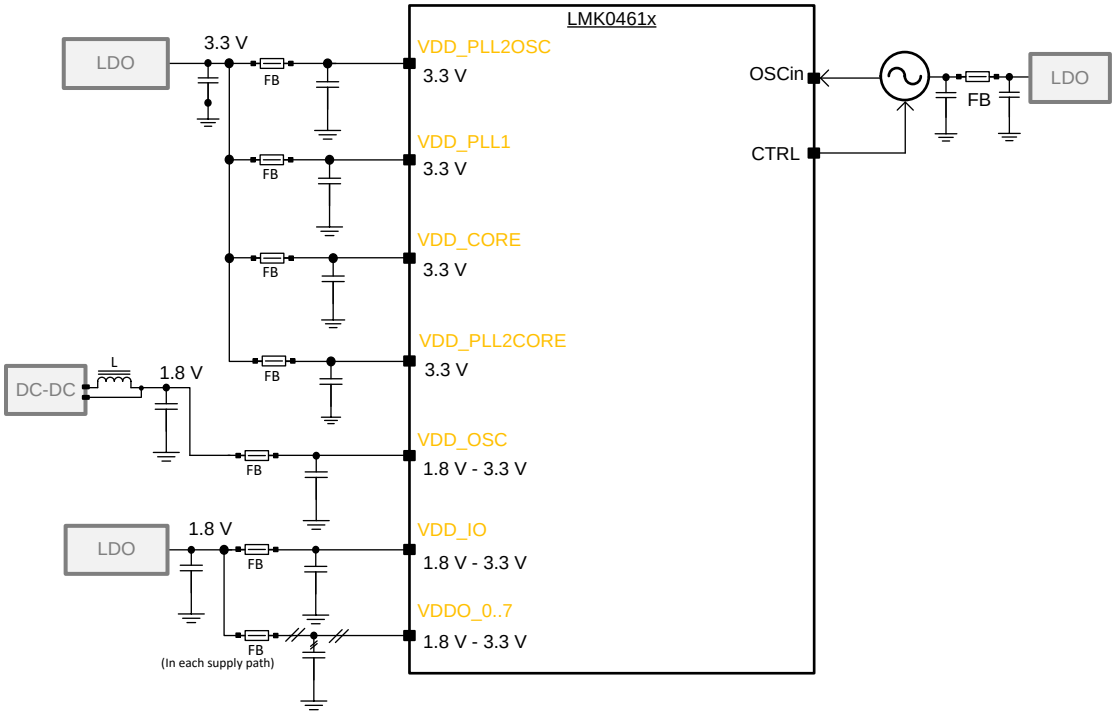


Figure 12. VDD_OSC Connected to DC-DC

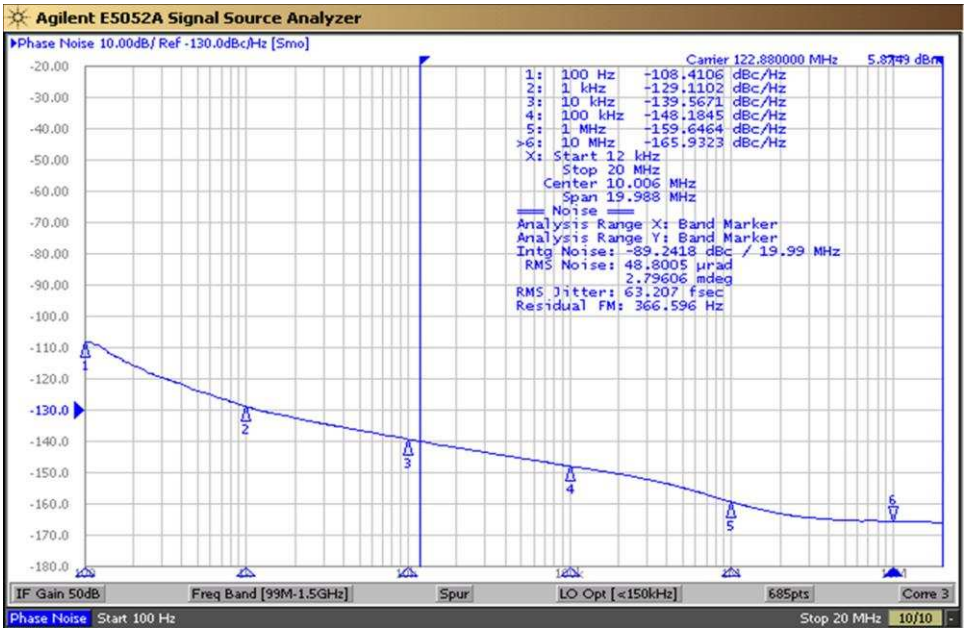


Figure 13. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 12

4.1.7 All LMK046xx Supplies and VCXO Supply Connected to DC-DC Converter (3.3 V)

In this test case, all supply pins of LMK04616 are connected to the DC-DC converter supplying the 3.3-V output. The VXCO is also connected to the same supply. As we can see in the phase noise plot in Figure 15, there is a significant degradation in the phase noise performance at offset frequencies below 100 KHz. This configuration is presented here as a test configuration only and should not be used.

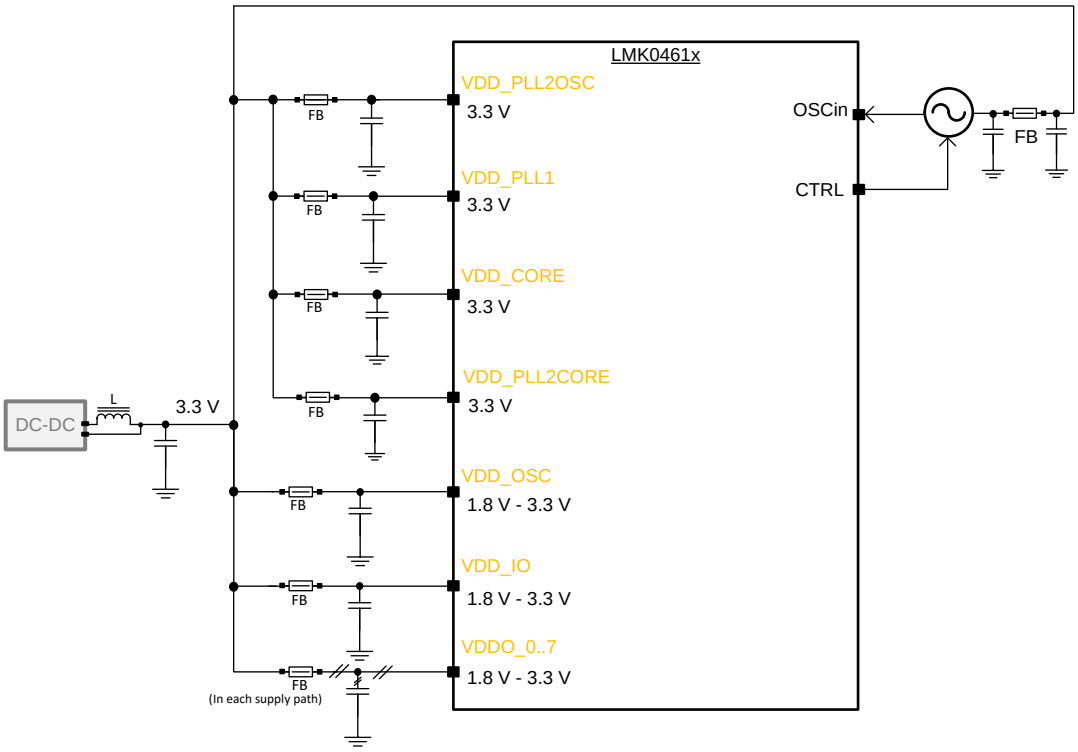


Figure 14. All LMK0461x Supplies and VCXO Supply Connected to DC-DC Converter

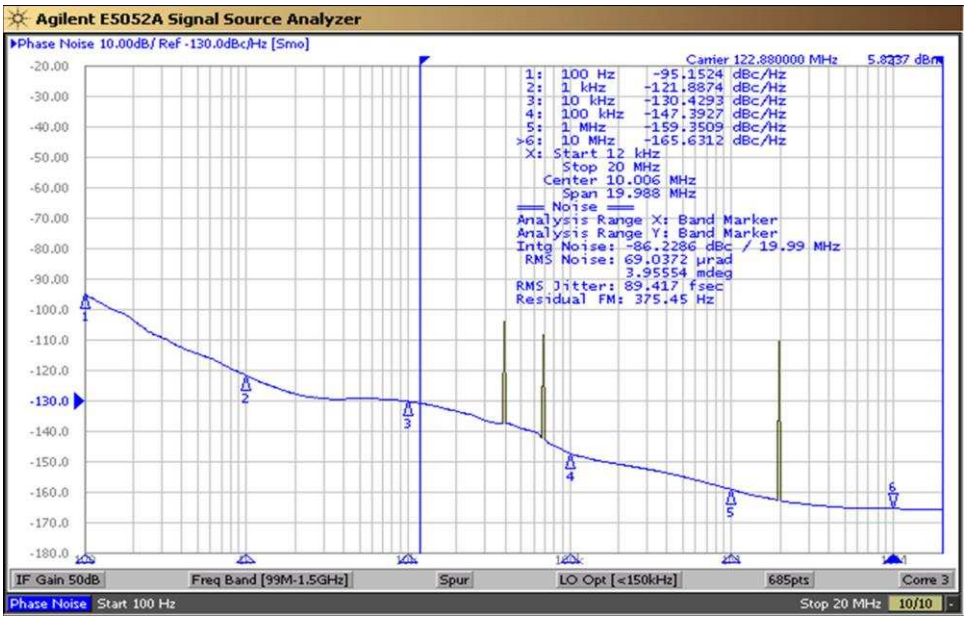


Figure 15. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 14

4.1.8 All LMK046xx Supplies Powered by the DC-DC Converter (3.3 V) and VCXO Connected to Separate LDO

The supply config is shown in Figure 16. Compared to the supply connections shown in Figure 14, the only difference is that the VCXO is supplied through a separate LDO and all the supply pins of the LMK04616 are supplied with the DC-DC converter at 3.3-V output voltage. The phase noise plot in Figure 17 shows degradation in phase noise at offset frequencies <10 KHz.

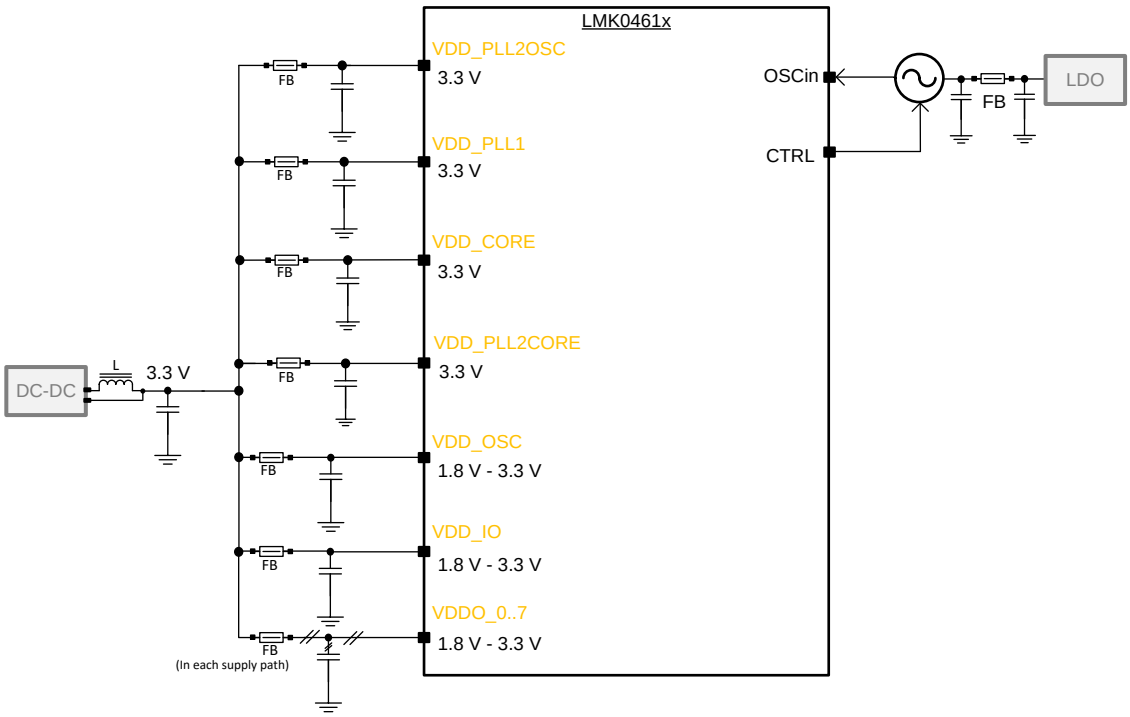


Figure 16. VCXO Connected to Separate LDO

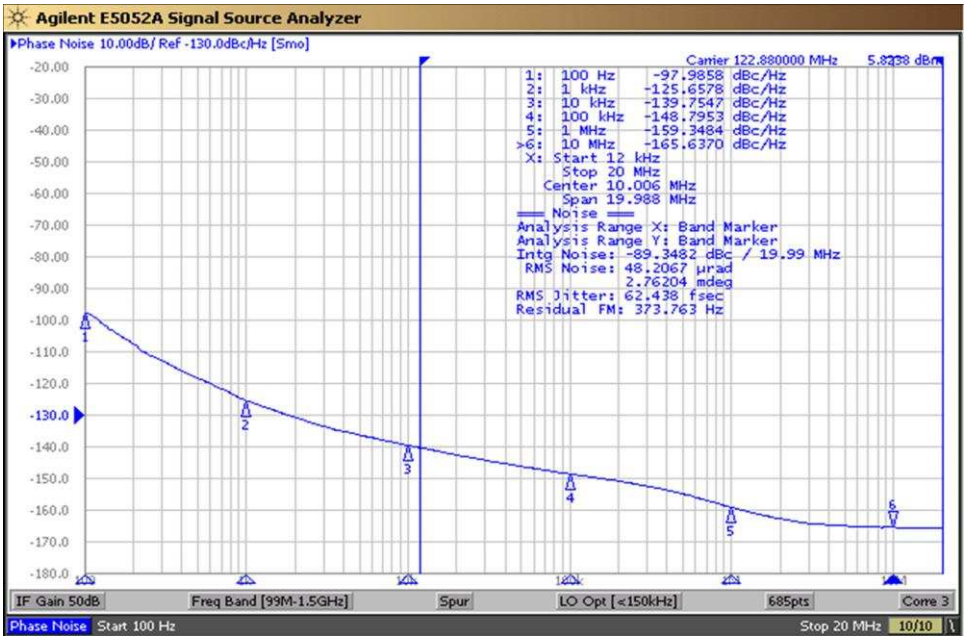


Figure 17. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 16

4.1.9 All LMK046xx Supplies Powered by the DC-DC Converter (3.3 V) Except VDD_PLL1

In this test configuration, the VDD_PLL1 is connected to the 3.3-V output from a low-noise LDO, and all the other supplies are connected to the 3.3-V output of the DC-DC converter (see Figure 18). Compared to the supply configuration shown in Figure 16, the phase noise at 100-Hz offset is better, but still worse for offset frequencies < 10 KHz when comparing against the phase noise plot shown in Figure 3.

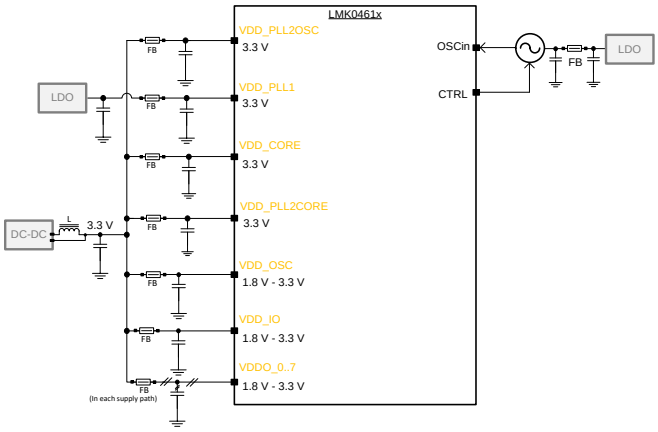


Figure 18. All LMK046xx Supplies Connected to DC-DC Converter (3.3 V) Except VDD_PLL1

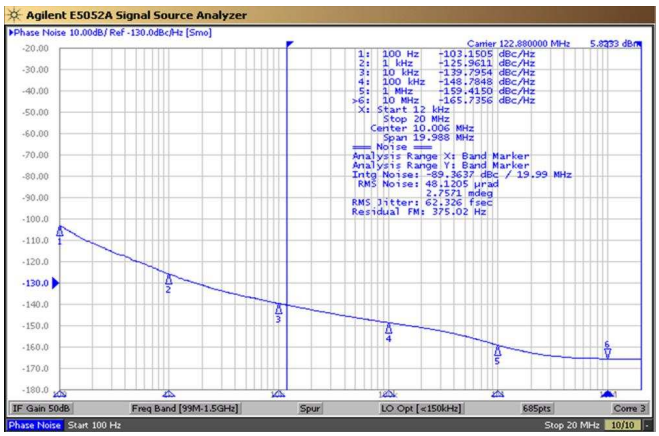


Figure 19. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 18

4.1.10 All LMK046xx Supplies Connected to DC-DC Converter (3.3 V) Except VDD_PLL1 and VDD_PLL2OSC

In this test configuration shown in Figure 20, both VDD_PLL1 and VDD_PLL2 are connected to the output of low-noise LDO, and all other supplies of the LMK04616 are connected to the output of the DC-DC converter. There is an improvement in the phase noise at 100-Hz offset compared to the supply configuration shown in Figure 18.

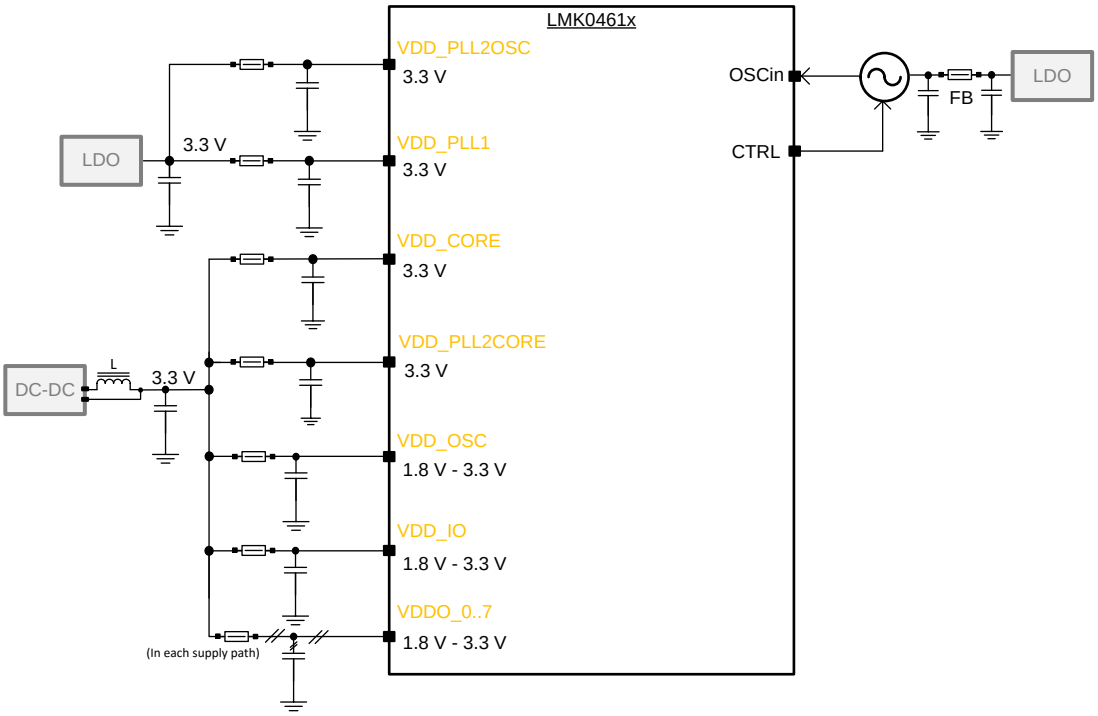


Figure 20. All LMK046xx Supplies Connected to DC-DC (3.3 V) Except VDD_PLL1 and VDD_PLL2OSC

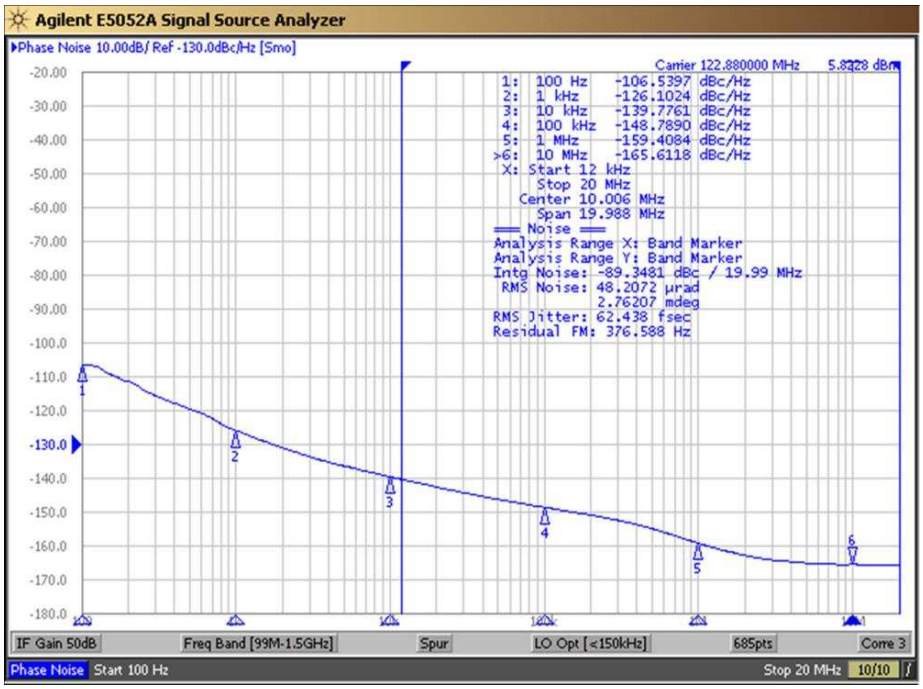


Figure 21. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 20

4.1.11 Without Ferrite Bead and Decoupling Capacitor on Output Supply

As shown in the Figure 22, the ferrite bead and the decoupling capacitor is removed from the VDDO_0 supply and the phase noise measurement is performed on OUT0/OUT0* output. The spurs from the DC-DC converter can be seen in the Phase noise plot of the clock output.

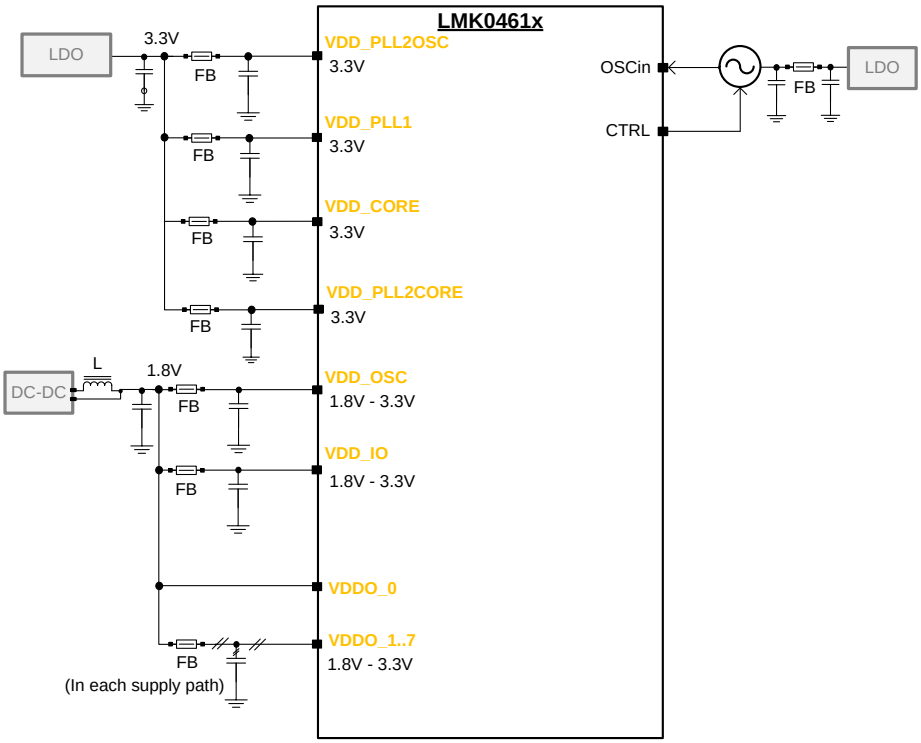


Figure 22. Removed Ferrite Bead and Decoupling Capacitor on Output Supply

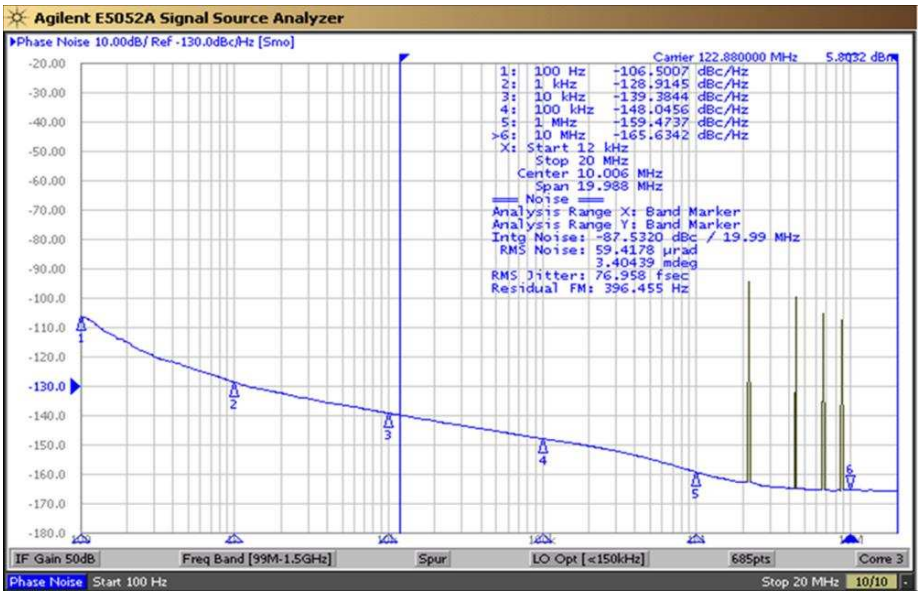


Figure 23. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 22

4.2 DC-DC Converter - TPS62743

The TPS62743 is a high-efficiency, step-down converter with ultra-low quiescent current of typical 360 nA. The output voltage can be programmed using the select pins. The typical switching frequency is 1.2 MHz and output ripple < 15 mV with C_{OUT} = 10 µF. The LMK04616 output clock phase noise measurements using TPS62743EVM as a supply source are shown in Section 4.2.1.

4.2.1 All Output Supplies VDDO_X/Y Powered by the DC-DC Converter (1.8 V)

All the output supplies are connected to the DC-DC converter 1.8-V output and other supplies are connected to the LDOs as shown in Figure 2. The phase noise performance of the output clock is shown in Figure 24.

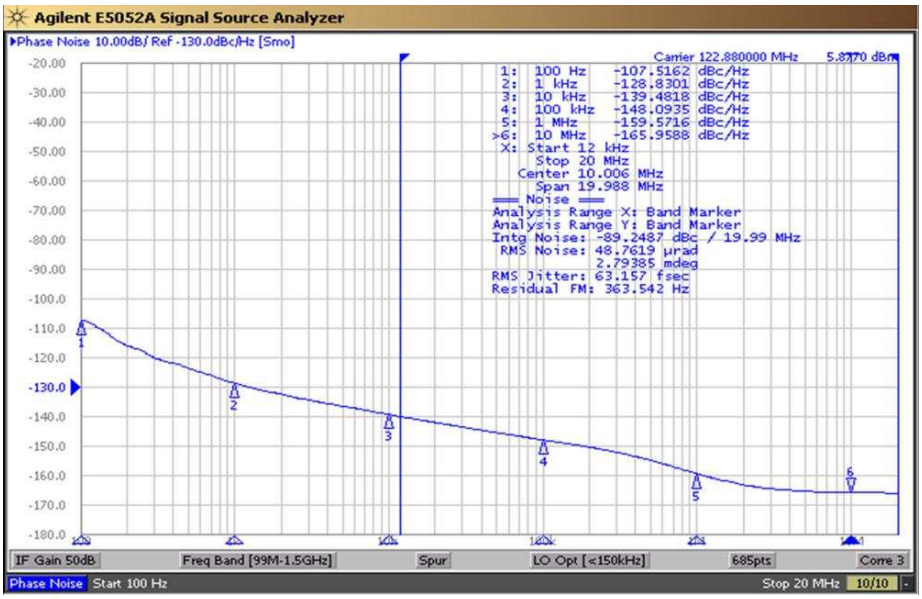


Figure 24. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 2 and TPS62743

4.2.2 All LMK046xx Supplies Powered by the DC-DC Converter (3.3 V)

In this test configuration, the DC-DC is configured for 3.3-V output voltage and all the LMK04616 supply pins are connected to the DC-DC converter output voltage. The supply configuration is shown in Figure 16. The noise plot in Figure 25 shows significant degradation for offset frequencies < 10 KHz.

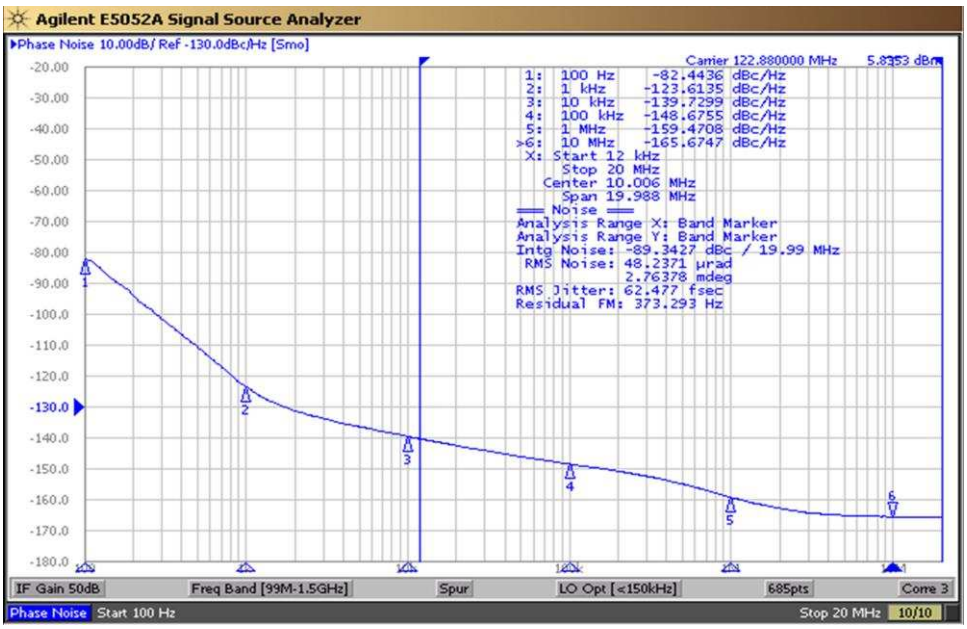


Figure 25. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 16 and TPS62743

4.2.3 All LMK046xx Supplies Except VDD_PLL1 Powered by the DC-DC Converter (3.3 V)

Compared to the supply configuration used in Figure 25, the VDD_PLL1 is excluded from the DC-DC converter and is supplied with the low-noise LDO. The supply configuration is shown in Figure 18. The phase noise plot in Figure 26 shows improvement compared to when all supplies are connected to the DC-DC converter, but still shows degradation compared to the phase noise when using the recommended supply configuration.

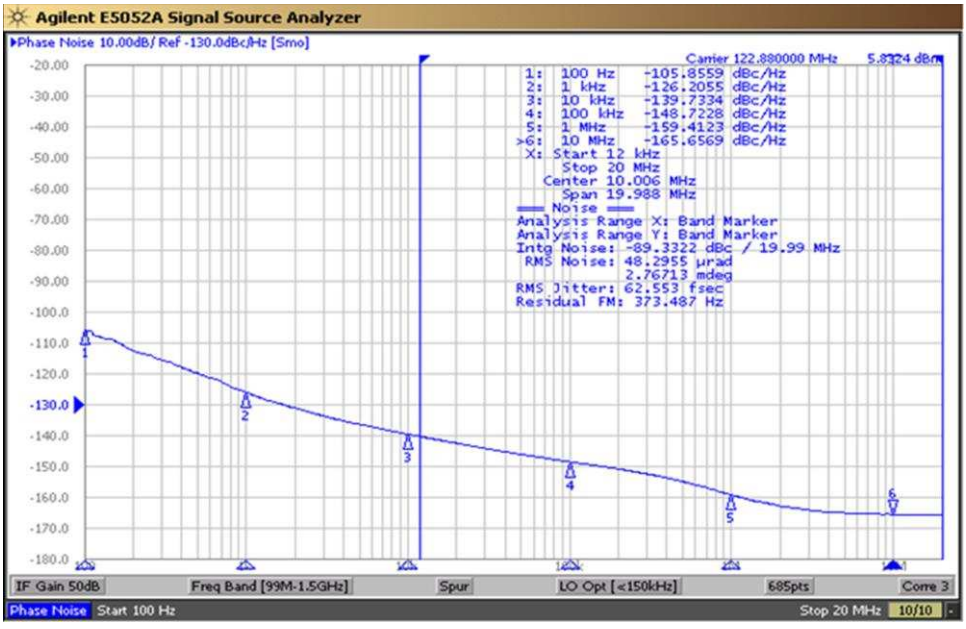


Figure 26. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 18 and TPS62743

4.3 DC-DC Converter - TPS62240

The TPS6224x device is a highly efficient 2.25-MHz synchronous, step-down DC-DC converter. The device provides up to 300-mA output current from a single Li-Ion cell.

4.3.1 All Output Supplies VDDO_X/Y Powered by the DC-DC Converter (1.8 V)

The TPS62240EVM provides the 1.8-V output voltage and the device is connected as shown in Figure 2 (recommended supply connections). The phase noise of the output clock is shown in Figure 27.

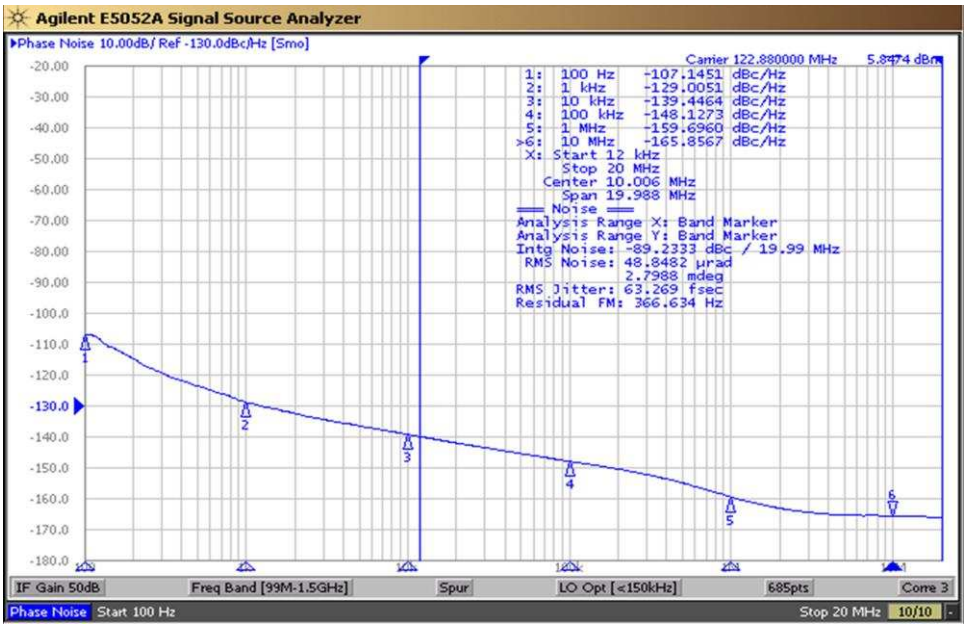


Figure 27. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 2 and TPS62240

4.4 DC-DC Converter - TPS62621

TPS62621 is a 6-MHz, synchronous, step-down DC-DC converter optimized for battery-powered, portable applications. Intended for low-power applications, the TPS62621 support up to 600-mA load current and allows the use of cost-effective chip inductor and capacitors. The output peak-to-peak ripple voltage is 5 mV at 300-mA load current.

4.4.1 All Output Supplies VDDO_X/Y Powered by the DC-DC Converter (1.8 V)

The TPS62621EVM is configured to supply 1.8-V output and the supply connection, as shown in Figure 2, and is used for this DC-DC converter, also. The phase noise plot is shown in Figure 28.

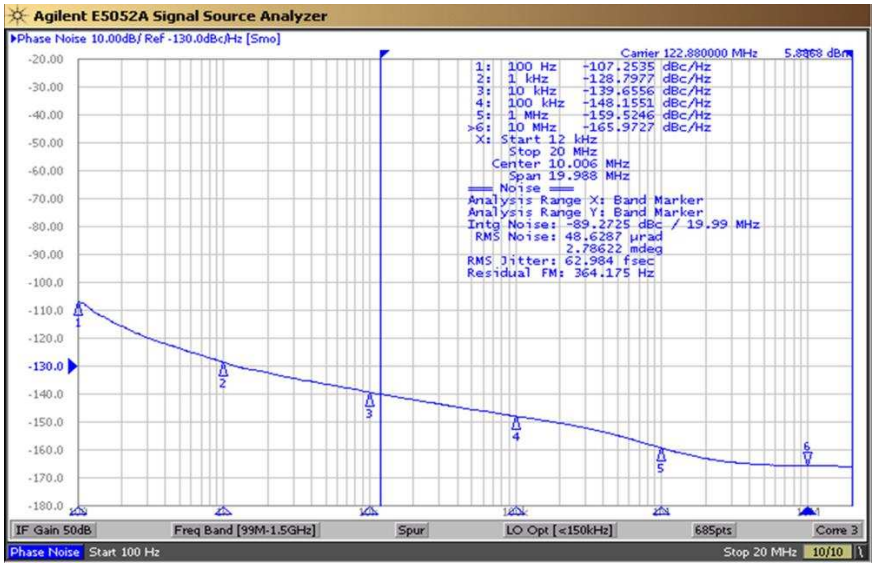


Figure 28. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 2 and TPS62621

4.5 DC-DC Converter - TPS62231

The TPS6223x device family is a 3-MHz, synchronous, step-down DC-DC converter ideal for space-optimized automotive and industrial applications. The peak-to-peak output ripple with L = 2.2 µH and C_O = 4.7 µF is < 10 mV at I_{OUT} = 300 mA. The device supports up to 500-mA output current and allows the use of tiny and cost-effective chip inductors and capacitors.

4.5.1 All Output Supplies VDDO_X/Y Powered by the DC-DC Converter (1.8 V)

The recommended supply configuration is used for the phase noise measurement with TPS62231EVM as shown in Figure 2. The output clock phase noise is shown in Figure 29.

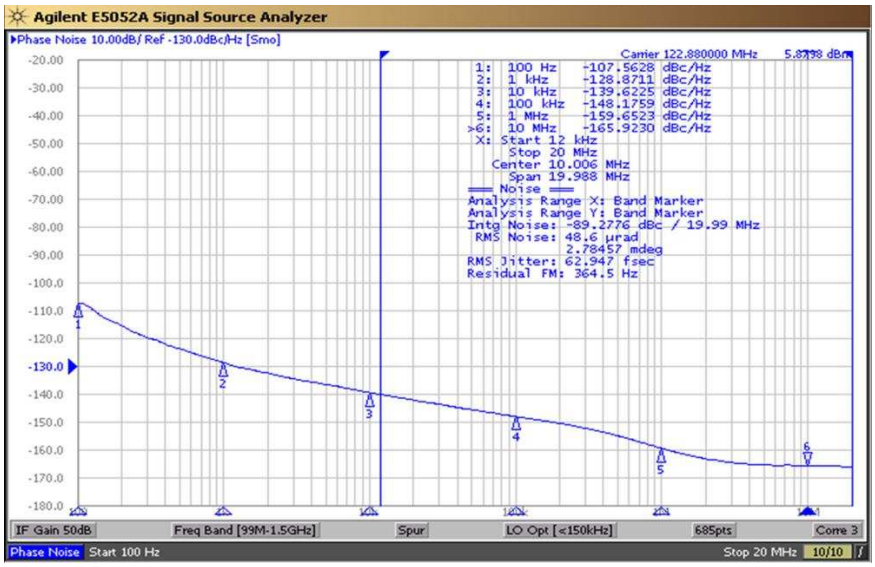


Figure 29. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 2 and TPS62231

4.6 DC-DC Converter - TPS62080

The TPS6208x devices are a family of high-frequency, synchronous, step-down converters. The converter focuses on high efficiency, step-down conversion over a wide output current range. At medium to heavy loads, the converter operates in PWM mode and automatically enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range. The DC-DC converter operates at a nominal frequency of 3 MHz.

4.6.1 All Output Supplies VDDO_X/Y Powered by the DC-DC Converter (1.8 V)

The recommended supply connection are used for TPS62080EVM as shown in Figure 2 and the phase noise results are shown in Figure 30.

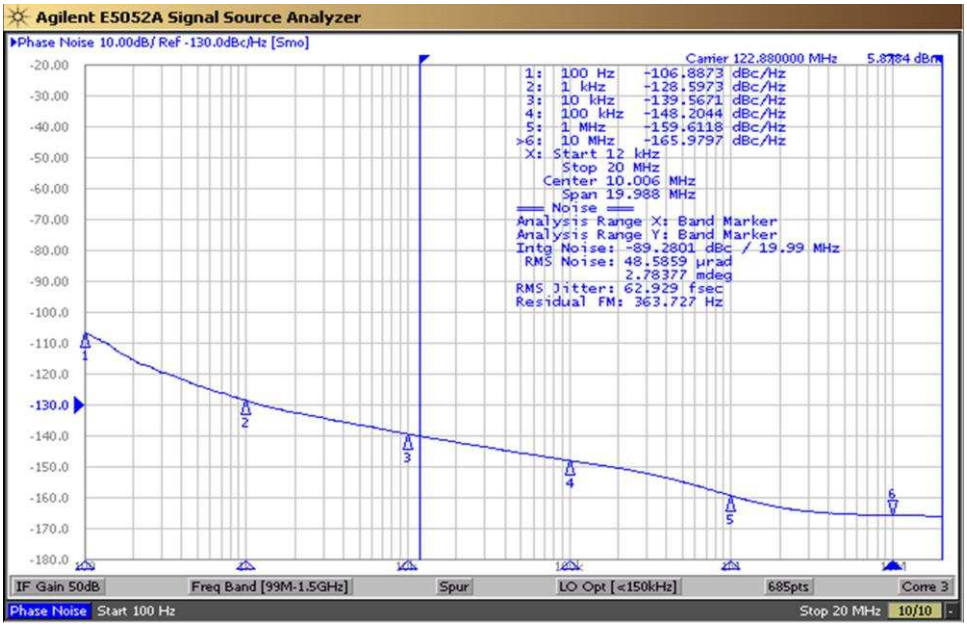


Figure 30. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 2 and TPS62080

4.7 DC-DC Converter - TPS54320

The TPS54320 is a full featured 17-V, 3-A synchronous step-down converter which is optimized for small designs through high efficiency and integrated high-side and low-side MOSFETs. The default EVM configuration of the TPS54320EVM is used for the LMK04616 measurements. The switching frequency on the TPS54320EVM is set at a nominal 480 kHz. The converter specifies an output ripple voltage of 10 mV_{pp} at I_{out} = 3 A.

4.7.1 All Output Supplies VDDO_X/Y Powered by the DC-DC Converter (3.3 V)

The recommended supply connection are used for to supply LMK04616 by the TPS54320EVM as shown in Figure 2 and the phase noise results are shown in

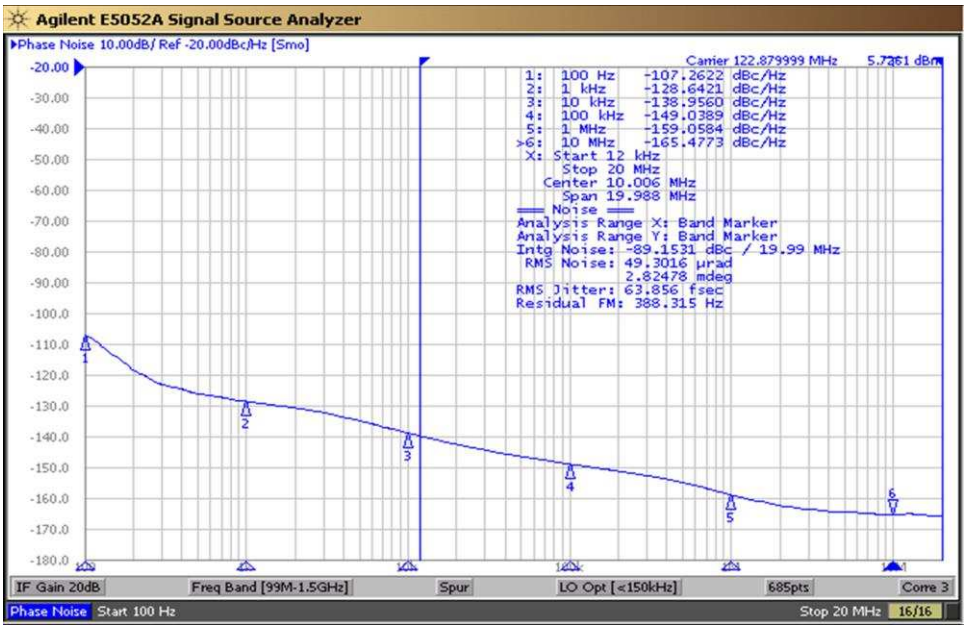


Figure 31. CLKoutX/X* Phase Noise for Supply Config Shown inFigure 2 and TPS54320

4.7.2 All LMK04616 Supplies and VCXO Supply Connected to DC-DC Converter (3.3 V)

All supply pins of LMK04616 are connected to the DC-DC converter supplying the 3.3-V output. The VXCO is also connected to the same supply. The supply configuration is shown in As we can see in the phase noise plot in , there is a significant degradation in the phase noise performance at offset frequencies below 100 KHz. This configuration is presented here as a test configuration only and is not recommended to be used.

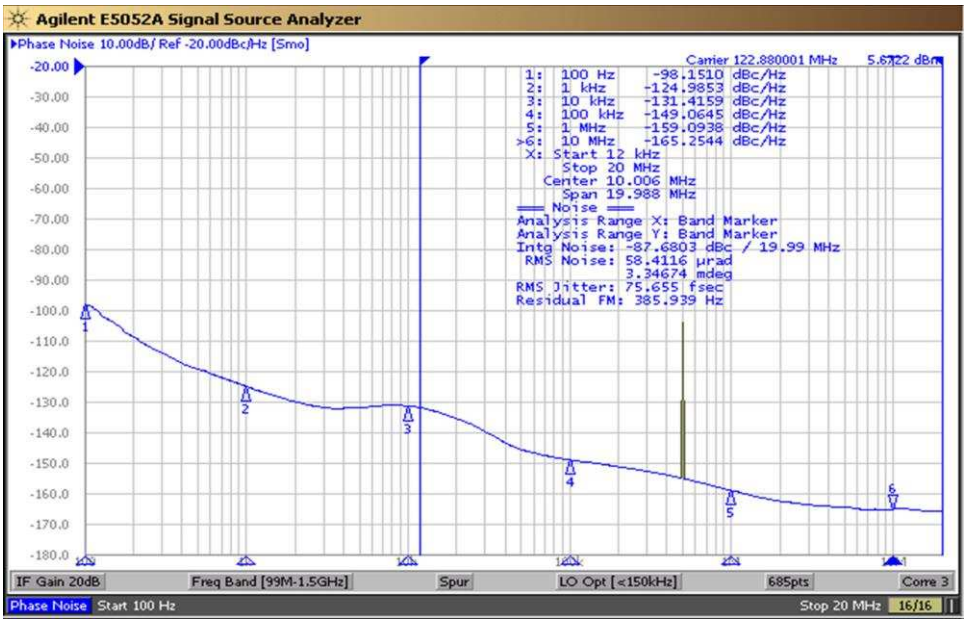


Figure 32. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 14

4.7.3 All LMK046xx Supplies Powered by the DC-DC Converter (3.3 V) and VCXO Connected to Separate LDO

The supply config is shown in Figure 16. Compared to the supply connections shown in Figure 14, the difference is that the VCXO is supplied through a separate LDO and all the supply pins of the LMK04616 are supplied with the DC-DC converter at 3.3-V output voltage. The phase noise plot in shows degradation in phase noise at offset frequencies < 10 KHz.

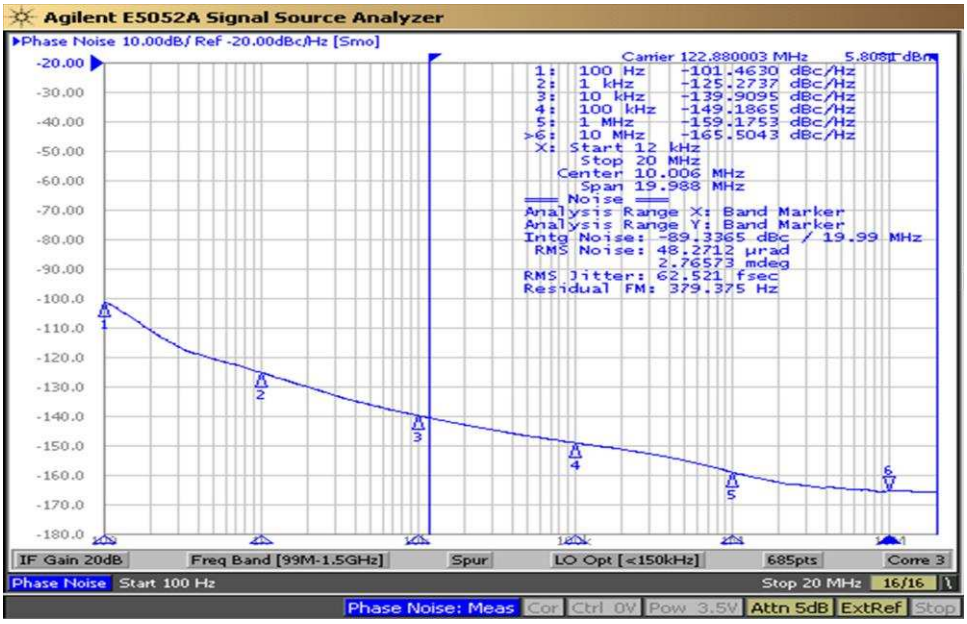


Figure 33. CLKoutX/X* Phase Noise for Supply Config Shown in Figure 16

4.8 DC-DC Converter - TPS54620

The TPS54620 in thermally enhanced 17-V, 6-A, synchronous, step-down converter which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. The default EVM configuration of the TPS54620EVM is used for the LMK04616 measurements. The switching frequency is externally set at a nominal 480 kHz. The output ripple is specified at 20-mV peak-to-peak at full load.

4.8.1 All Output Supplies VDDO_X/Y Powered by the DC-DC Converter (3.3 V)

The recommended supply connection are used to supply LMK04616 by the TPS54320EVM as shown in Figure 2 and the phase noise results are shown in

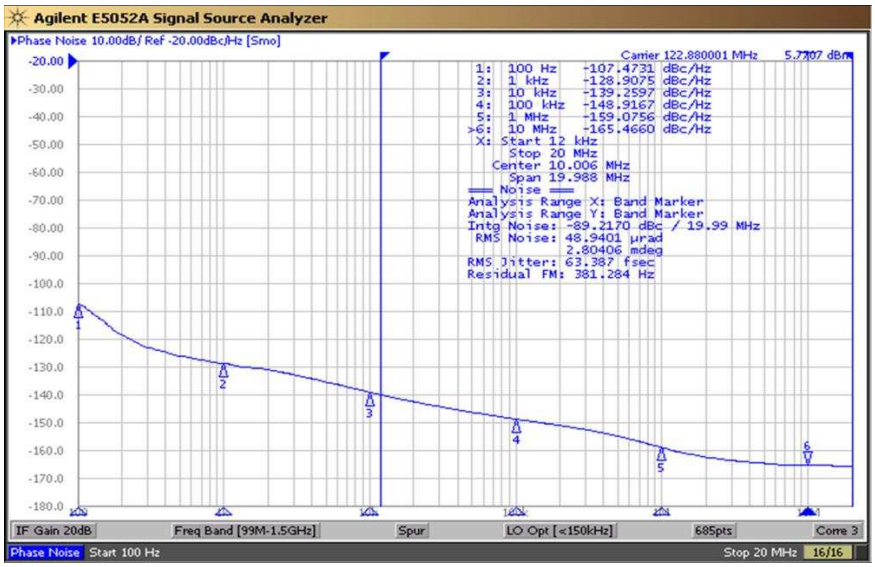


Figure 34. CLKoutX/X* Phase Noise for Supply Config Shown inFigure 2 and TPS54620

4.9 DC-DC Converter - TPS54418

The TPS54418 is a 2.95-V to 6-V Input, 4-A Output, 2-MHz , Synchronous Step-Down Switcher With Integrated FETs, and minimizing the device footprint with a small, 3 mm × 3 mm, thermally enhanced, QFN package. The output ripple at full load I_{OUT} is < 10-mV Peak-to-Peak as per the measurements in TPS54418EVM user guide.

4.9.1 All Output Supplies VDDO_X/Y Powered by the DC-DC Converter (1.8V)

The recommended supply connection are used to supply LMK04616 by the TPS54418EVM as shown in Figure 2 and the phase noise results are shown in

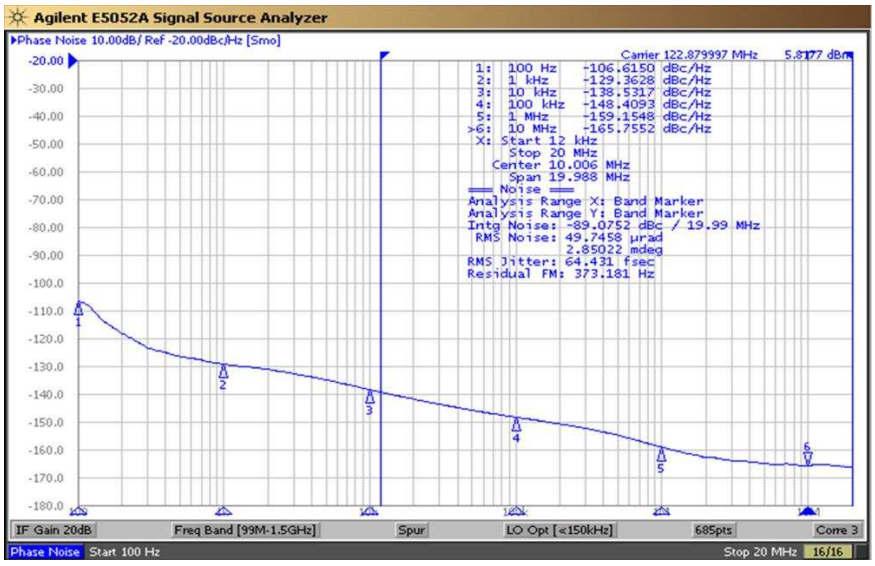


Figure 35. CLKoutX/X* Phase Noise for Supply Config Shown inFigure 2 and TPS54418

4.10 DC-DC Converter - TPS54824

The TPS54824 DC-DC converter is a synchronous buck converter designed to provide up to an 8-A output. The input (VIN) is rated for 4.5 V to 17 V. The RT/CLK pin is configured for 700-kHz switching frequency. The high-side and low-side MOSFETs are incorporated inside the TPS54824 package along with the gate-drive circuitry. The EVM is configured for VIN = 12 V and an output voltage of 1.8 V. The output voltage ripple is specified as 11 mV at 8-A output current.

4.10.1 All Output Supplies VDDO_X/Y Powered by the DC-DC Converter (1.8 V)

The recommended supply connection are used to supply LMK04616 by the TPS54824EVM as shown in

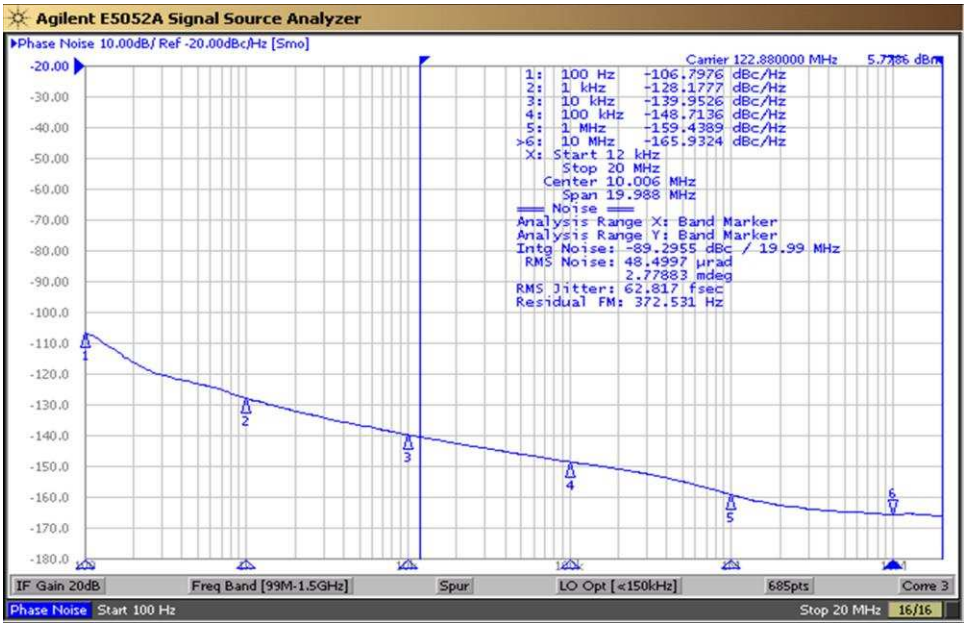


Figure 36. CLKoutX/X* Phase Noise for Supply Config Shown inFigure 2 and TPS54824

5 Conclusion

As seen in the previous sections, the LMK0461x output clock phase noise performance is very similar when selecting the DC-DC converters presented in Section 3.1 and using the recommended supply configuration. In addition, the impact of the LMK0461x phase noise performance while connecting the different supply pins to the DC-DC converter instead of the low-noise LDO is shown. As already seen, the phase noise performance for offset frequencies < 100 KHz degrades significantly when VCXO supply is powered by the DC-DC converter. Also, when all LMK0461x supply pins are connected to the DC-DC converter, there is a significant drop in the phase noise performance for offset frequencies < 10 KHz. The performance gets better when both VDD_PLL1 and VDD_PLL2OSC are connected to the low-noise LDO while all other pins are supplied through the DC-DC converter. The best performance is obtained when the DC-DC converter is used as shown in the recommended supply connections.

DC-DC EVM Schematics

A.1 TPS62150EVM

See *TPS62130EVM-505, TPS62140EVM-505, and TPS62150EVM-505 Evaluation Modules* (SLVU437) for more information.

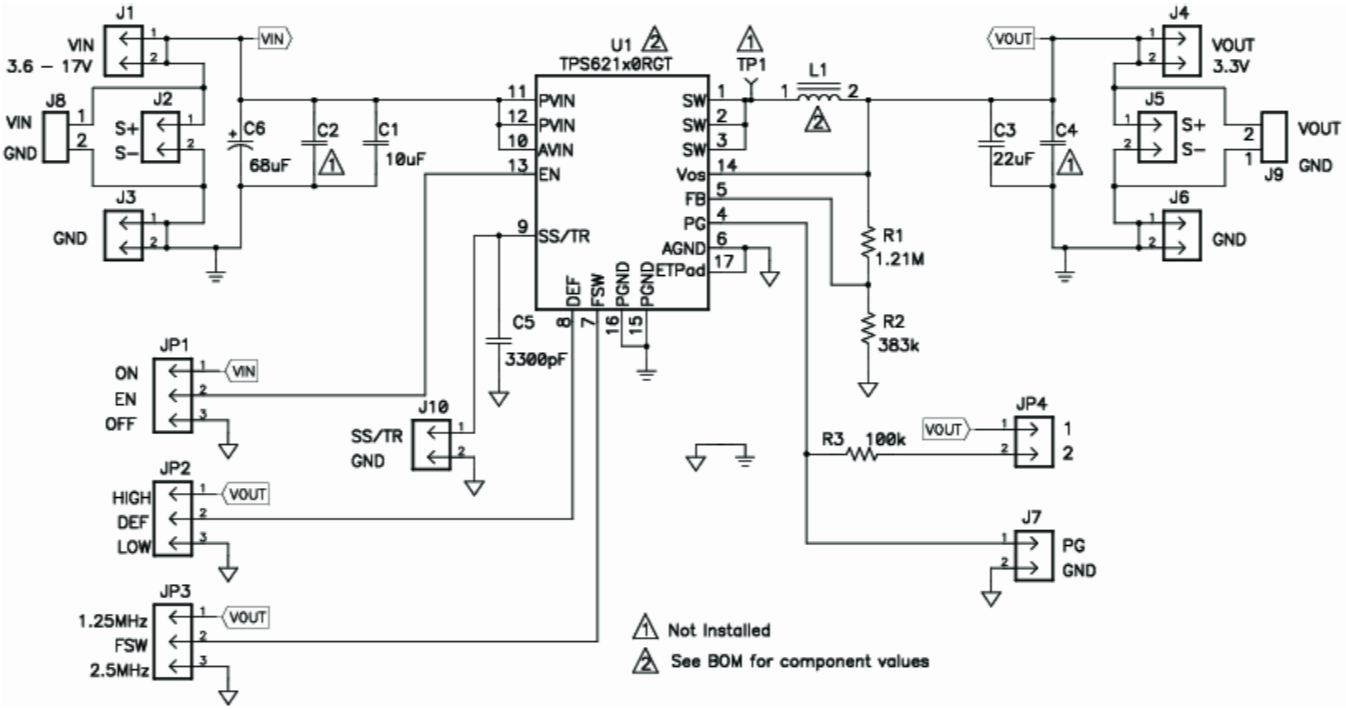


Figure 37. TPS62150 EVM Schematic

A.2 TPS62743EVM

See *TPS62743EVM-689 Evaluation Module User's Guide* (SLVUAF5) for more information.

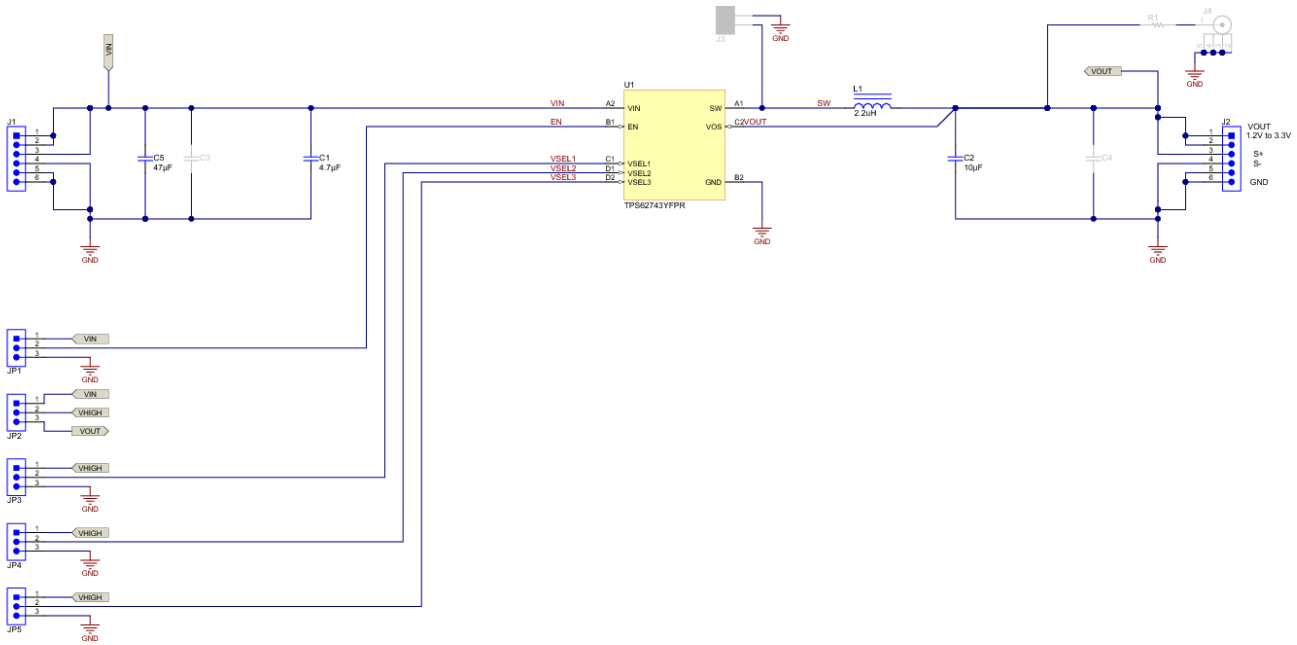


Figure 38. TPS62743 EVM Schematic

A.3 TPS62240EVM

See *TPS622x0EVM-229 User's Guide* (SLVU216) for more information.

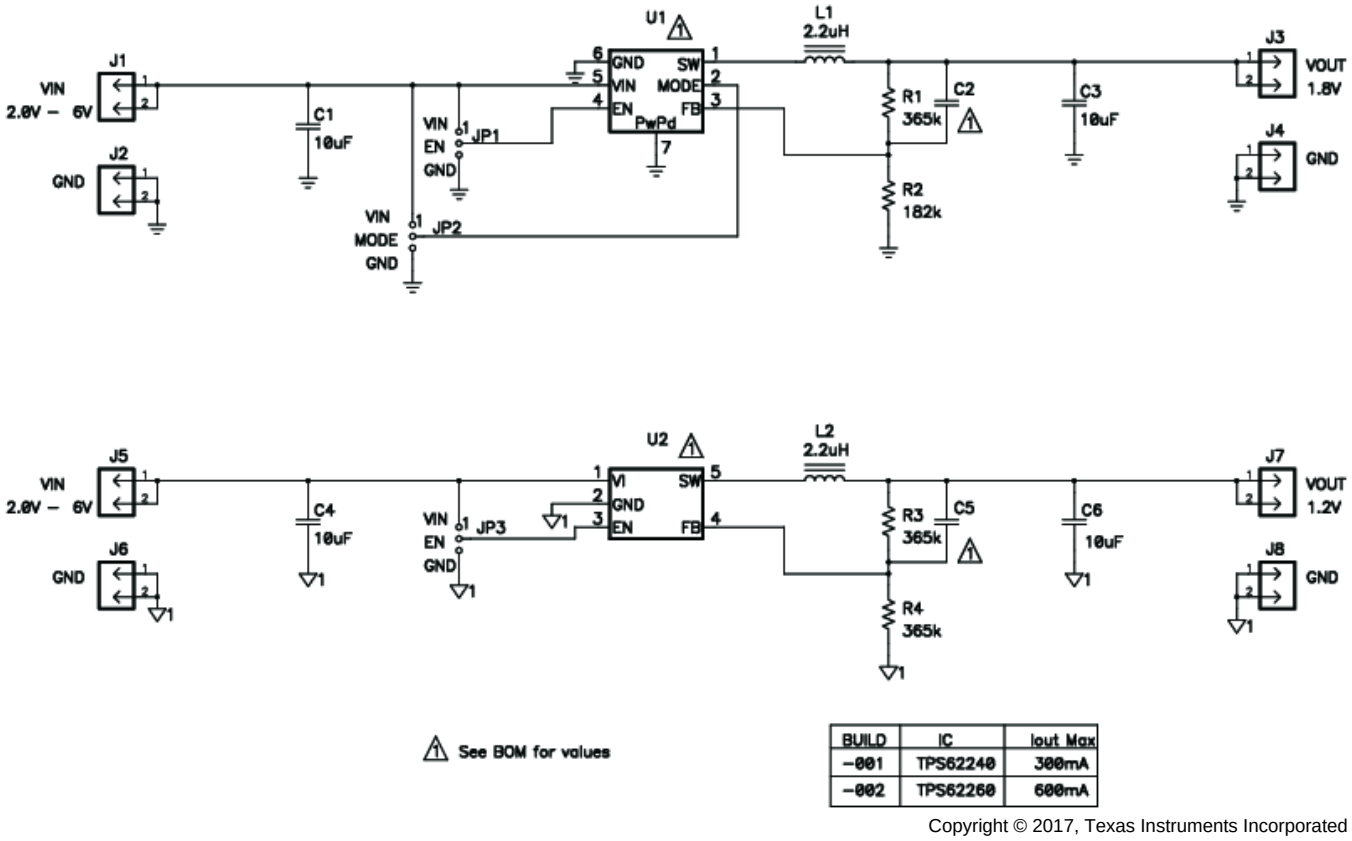


Figure 39. TPS62240 EVM Schematic

A.4 TPS62621EVM

See *TPS6261x/2x/6xEVM-419 User Guide* (SLVS292) for more information.

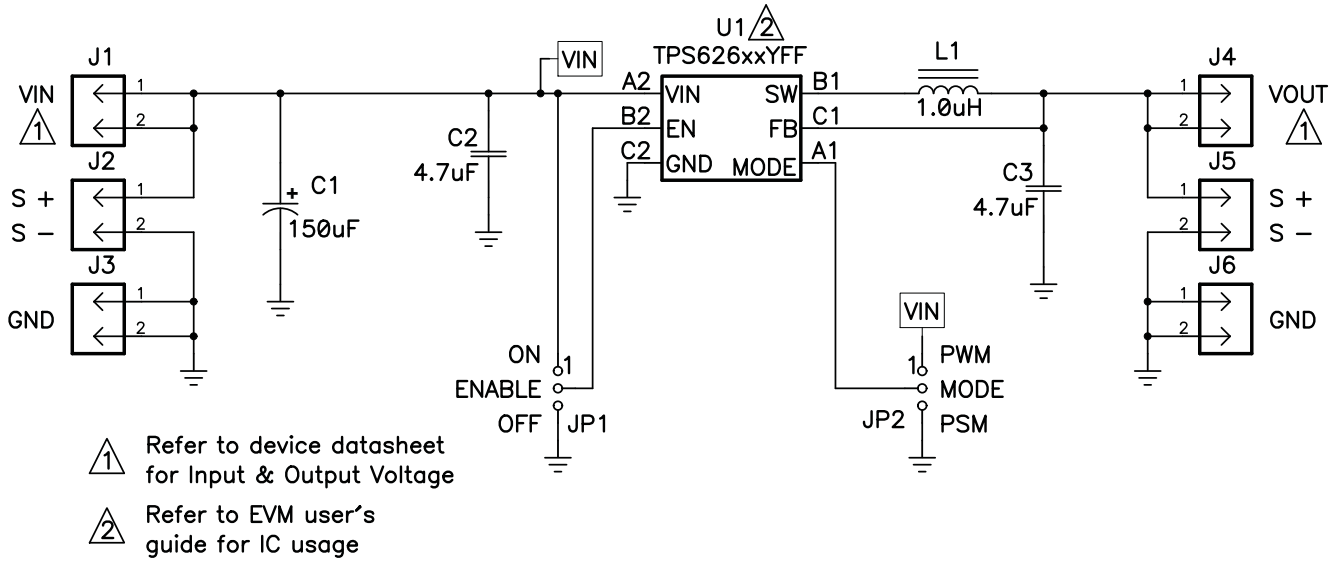


Figure 40. TPS62621 EVM Schematic

A.5 TPS62231EVM

See *TPS62230EVM-574 User's Guide* (SLVU426) for more information.

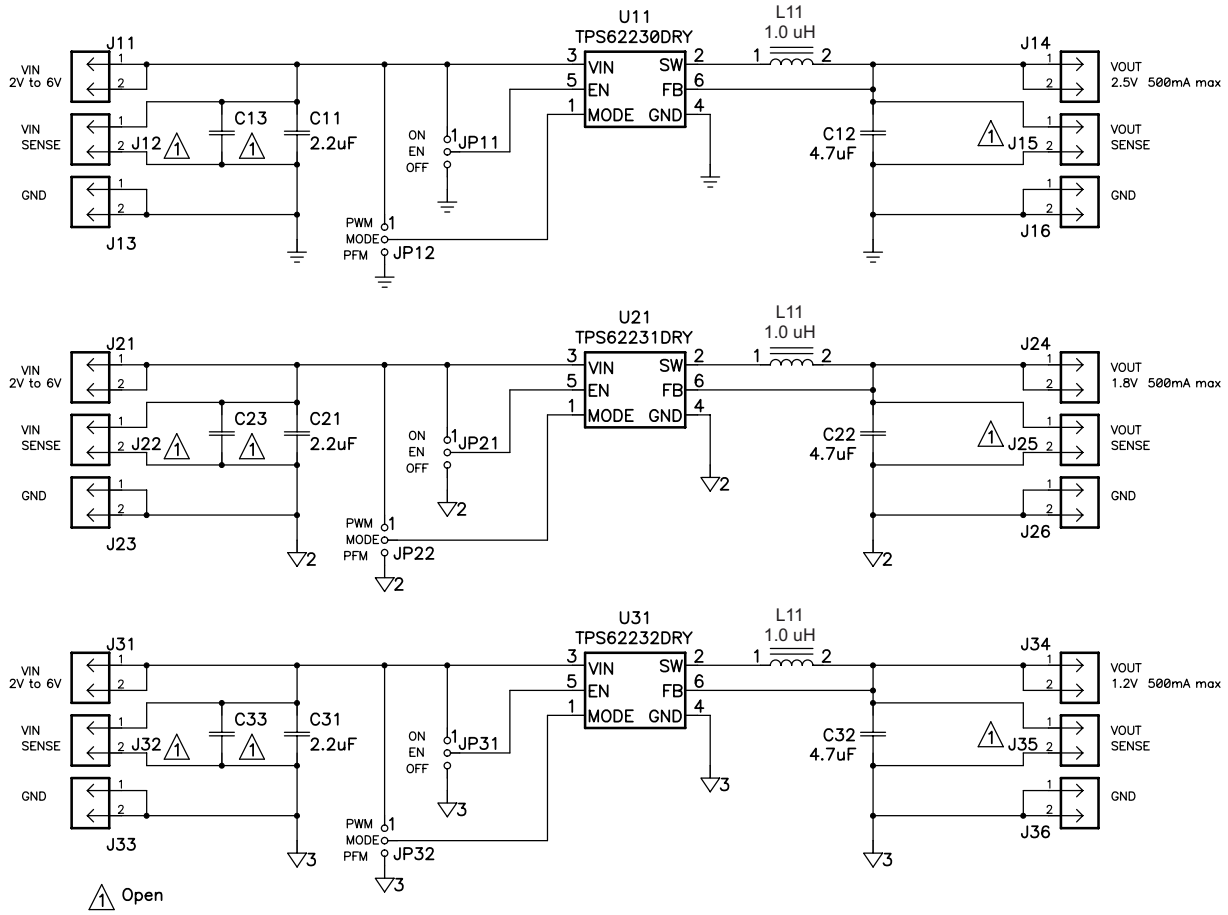


Figure 41. TPS62231 EVM Schematic

A.6 TPS62080EVM

See *TPS62080, 1.2A, High-Efficiency, Step-Down Converter in 2x2mm SON Package* (SLVU497) user's guide for more information.

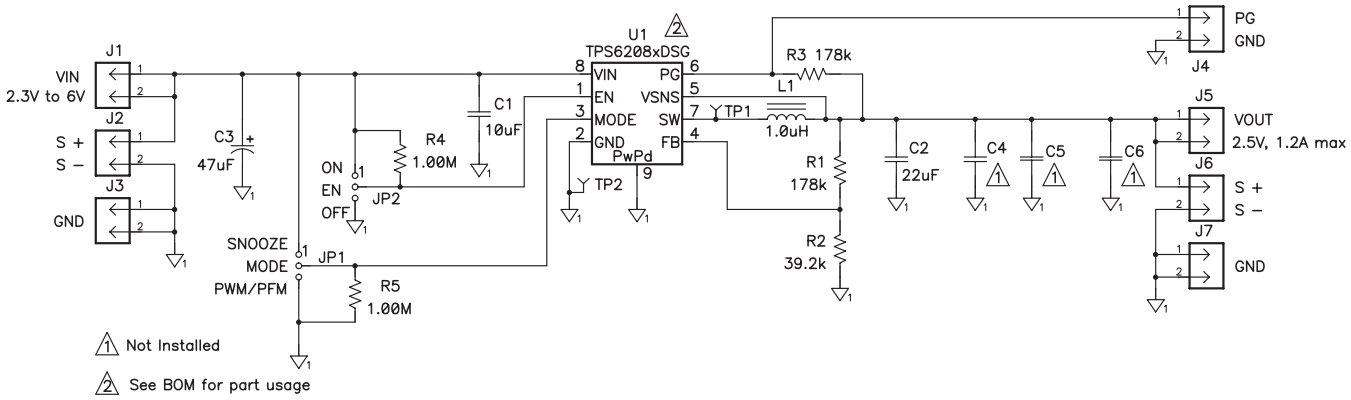


Figure 42. TPS62080 EVM Schematic

A.7 TPS54320EVM

See *TPS54320 User's Guide* (SLVU380) for more information.

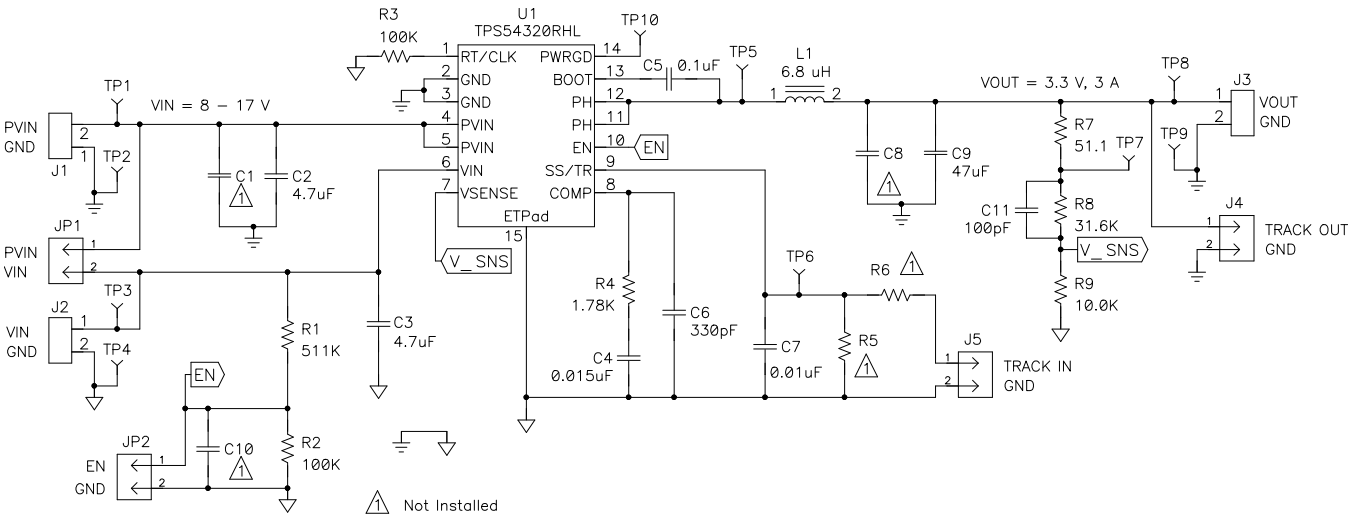


Figure 43. TPS54320 EVM Schematic

A.8 TPS54620EVM

See *TPS54620EVM-374 6-A, SWIFT Regulator Evaluation Module* (SLVU281) for more information.

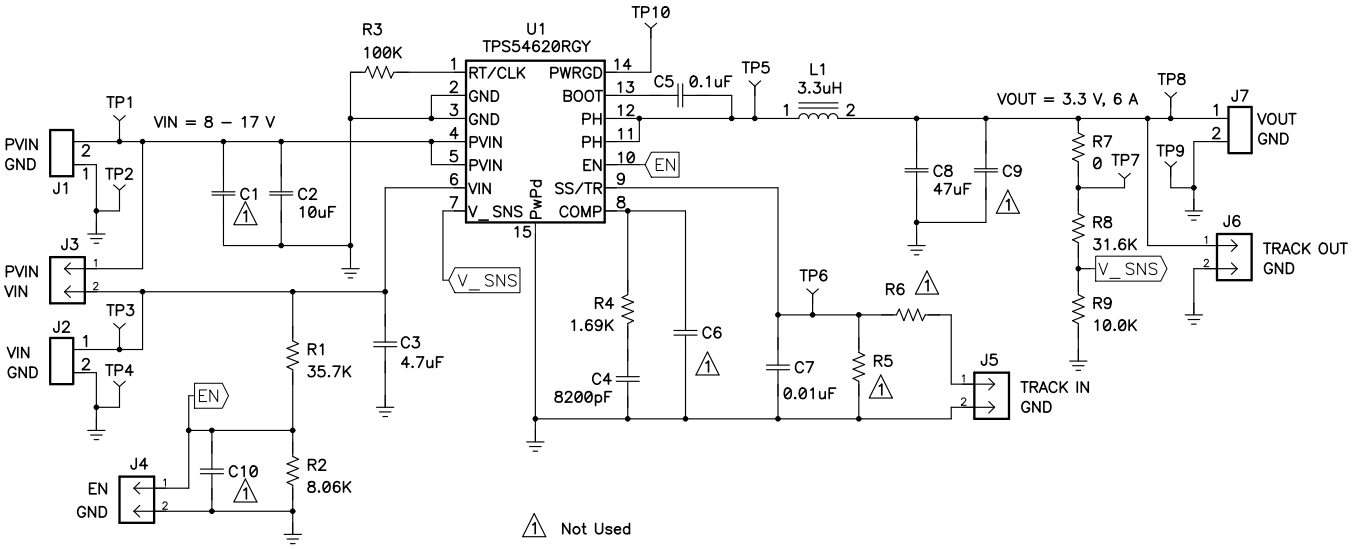
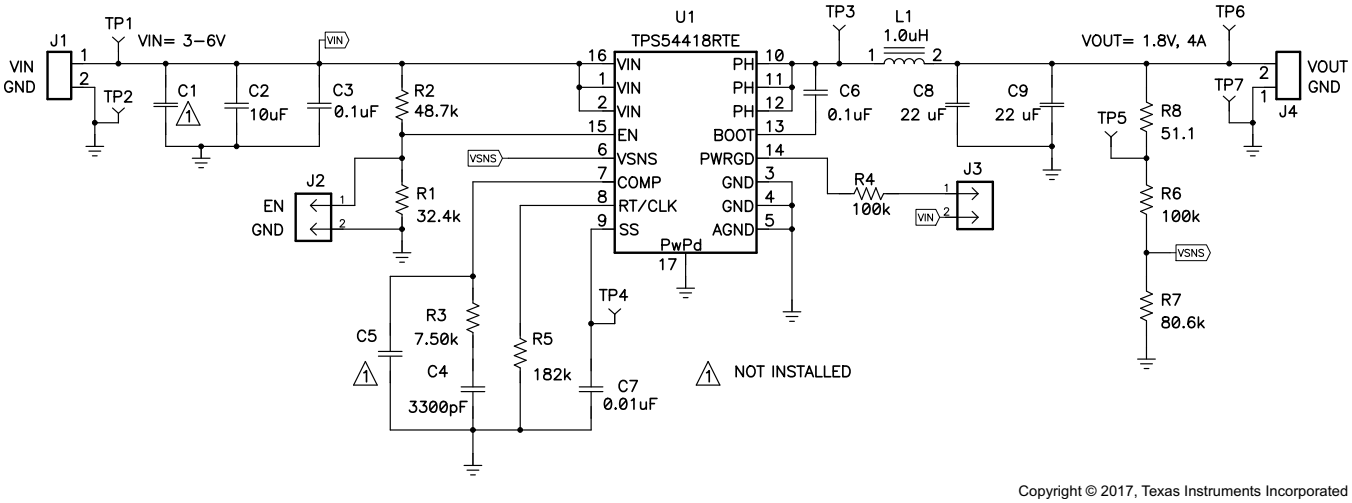


Figure 44. TPS54620 EVM Schematic

A.9 TPS54418EVM

See *TPS54418EVM-375 4-A, SWIFT™ Regulator Evaluation* (SLVU280) for more information.



Copyright © 2017, Texas Instruments Incorporated

Figure 45. TPS54418 EVM Schematic

A.10 TPS54824EVM

See *TPS54824EVM-779 8A, SWIFT™ Regulator Evaluation Module* (SLVUAX8) for more information.

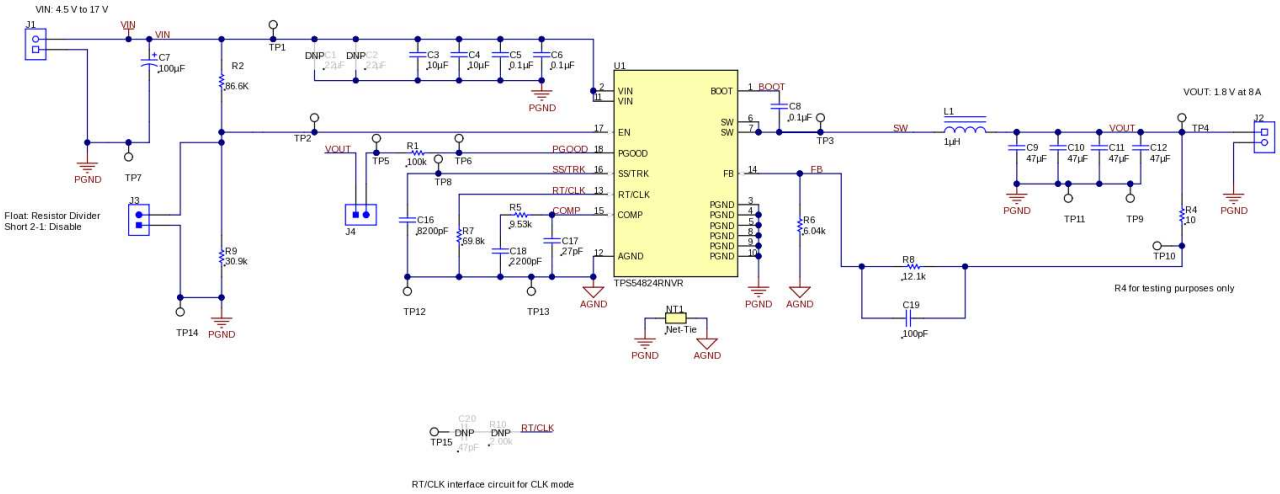


Figure 46. TPS54824 EVM Schematic

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (May 2017) to B Revision **Page**

- Updated waveform graphs with test conditions 5
- Landscaped schematics 24

Changes from Original (May 2017) to A Revision **Page**

- Added title to Table 2 4
- Changed the first row of DC-DC converter part number text from: EVM DCDC to: TPS62150 4

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265