Selecting output caps to optimize ripple and stability in PSR flyback converters

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Introduction

Primary-side regulation (PSR) is an observer-based approach to estimate the output voltage of a flyback converter using the reflected voltage on a primary-referenced winding. Previous Analog Design Journal articles[1, 2] have described the operation and switching behavior of an auxless PSR flyback DC/DC converter for automotive and industrial applications, where appropriately timed sensing of the primary switch voltage at its resonant knee position provides a suitable proxy for the output voltage. This magnetically-sensed regulation technique supports a sub-1% output-voltage accuracy across load, line and temperature ranges.[1] Moreover, it avoids the secondary-side optocoupler and error amplifier normally used for isolated feedback, thereby eliminating a component crossing the isolation barrier and enabling a cost-effective, high-reliability design with low component count.

Within this context, this article reviews the modes of operation and salient characteristics of a PSR flyback DC/DC converter and specifically examines output capacitor selection to meet system specifications for output voltage ripple and small-signal stability.

A PSR Flyback DC/DC Converter with Multimode Control

Figure 1 shows the schematic of a PSR flyback converter[3] with integrated primary switch and loop-compensation components. The converter supports magnetically-sensed regulation of the output voltage through the transformer's primary winding. **Equation 1** gives the output voltage setpoint:

$$V_{OUT} = \frac{V_{REF}}{N_{PS}} \times \frac{R_{FB}}{R_{SET}} - V_D \qquad (1)$$

where N_{PS} is the primary-to-secondary transformer turns ratio, V_{REF} is the internal bandgap reference voltage, and V_D is the flyback diode drop (at close to zero current).

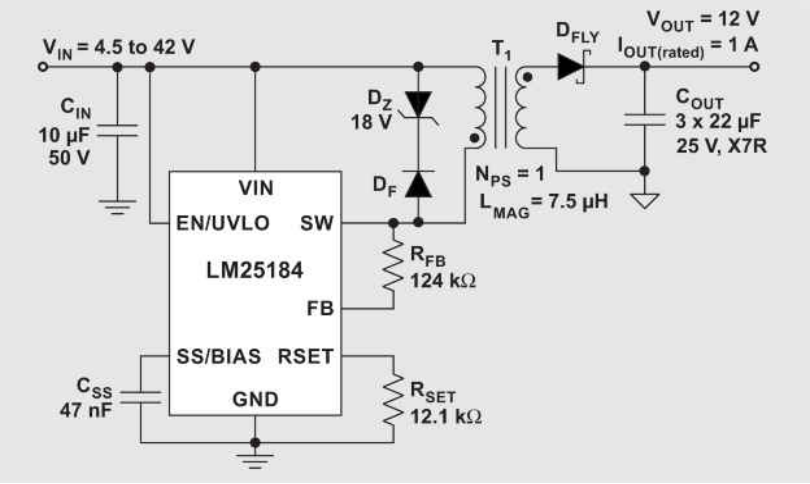

Figure 1. *Typical Schematic of an Auxless PSR Flyback Converter*

Using a variable switching-frequency-control law with peak current-mode control, the converter operates in boundary (BCM) or discontinuous (DCM) conduction mode depending on the load current, as depicted in

Figure 2.[4] Modulating the switching frequency and peak primary current amplitude helps maintain high efficiency across wide operating ranges of load and line.

More specifically, the converter operates in BCM at heavy loads, and the primary switch turns on with a resonant-half-period delay after switch voltage-knee detection (core reset) to achieve a quasi-resonant switching transition. As shown in **Figure 2**, the switching frequency in BCM increases as the load current decreases. To prevent high-frequency operation at medium load, the mode changes from BCM to DCM such that the switching frequency remains constant at its maximum value (350 kHz in this example). **Equation 2** gives the critical output current at the DCM-BCM boundary.

$$I_{OUT(DCM\text{-}BCM)} = \frac{V_{OUT}\, N_{PS}^2}{2 L_{MAG}\, f_{SW\text{-}DCM}} \left(\frac{V_{IN}}{V_{IN} + V_{OUT}\, N_{PS}} \right)^2 \quad (2)$$

Operation at light load changes to frequency-foldback mode (FFM), which is effectively DCM with a variable switching frequency and constant peak current. Because magnetic regulation relies on sensing the output voltage during switching cycles, it is necessary to maintain a certain minimum switching frequency at no load to continue sensing the output voltage (12 kHz in this example).

As shown in **Figure 2**, BCM has a lower switching frequency and a higher peak current than DCM. As such, BCM dictates the output capacitor sizing for a given ripple voltage specification. **Figure 3** shows the secondary-side waveforms in BCM.

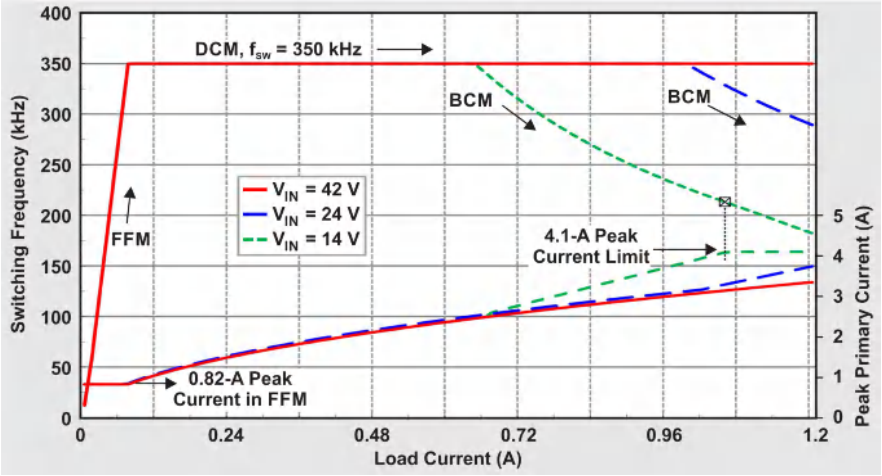

Figure 2. *Switching Frequency and Primary Peak Current vs. Load Current for the LM25184*

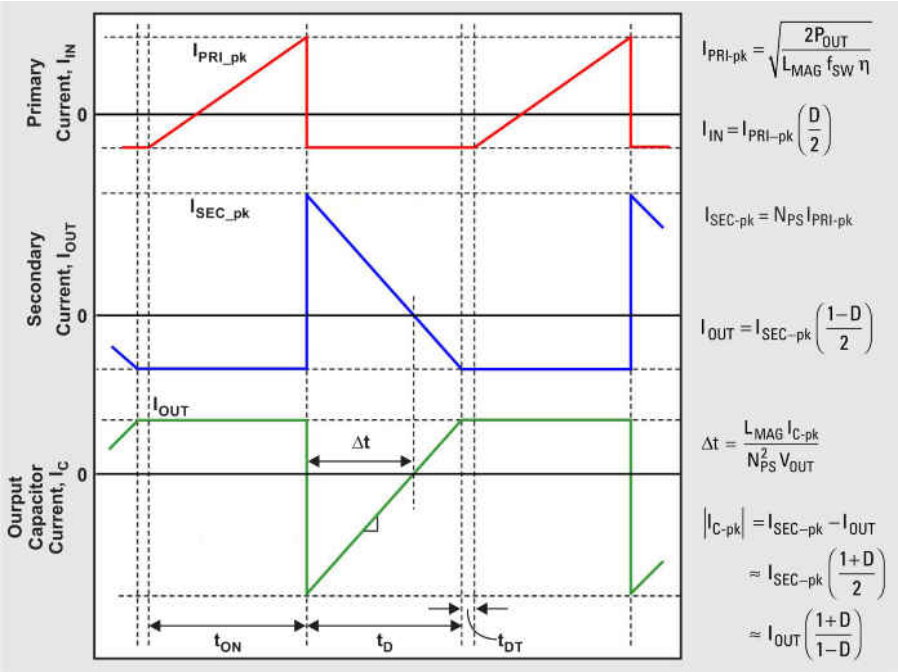

Figure 3. *Idealized Current Waveforms of a Flyback Converter in BCM*

Output Capacitor Sizing for Voltage Ripple

Based on the waveforms in **Figure 3**, **Equation 3** expresses the output capacitor peak-to-peak ripple voltage, ΔV_{OUT}, in BCM:

$$\begin{aligned}\Delta V_{OUT} &= \frac{I_{C\text{-}pk}\ \Delta t}{2C_{OUT}} = \frac{I_{C\text{-}pk}}{2C_{OUT}} \times \frac{L_{MAG\text{-}sec}\ I_{C\text{-}pk}}{V_{OUT}} \\ &\approx \frac{L_{MAG}\ I_{PRI\text{-}pk}^2}{2C_{OUT}\ V_{OUT}} \times \left(\frac{1+D}{2}\right)^2 \\ &= \frac{L_{MAG}\ I_{OUT}^2}{2C_{OUT}\ V_{OUT}\ N_{PS}^2} \times \left(\frac{1+D}{1-D}\right)^2\end{aligned} \tag{3}$$

Using the circuit values in **Figure 1**, **Equation 4** gives the required capacitance for 1% ripple on a 12-V output:

$$\begin{aligned}C_{OUT} &\geq \frac{7.5\,\mu H \times (4A)^2}{2 \times 120\,mV \times 12V \times 1^2} \times \left(\frac{1+0.47}{2}\right)^2 \\ &= 22.5\ \mu F\end{aligned} \tag{4}$$

Equation 5 defines the worst-case condition at maximum duty cycle (corresponding to the minimum input voltage):

$$\begin{aligned}D &= \frac{N_{PS}\left(V_{OUT} + V_D\right)}{V_{IN(min)} + N_{PS}\left(V_{OUT} + V_D\right)} \\ &= \frac{1 \times (12V + 0.4V)}{14\,V + 1 \times (12V + 0.4V)} = 0.47\end{aligned} \tag{5}$$

Equation 6 gives the output capacitor RMS current:

$$\begin{aligned}I_{COUT\text{-}RMS} &= I_{SEC\text{-}pk}\sqrt{\frac{1-D}{3}} = \sqrt{\frac{2I_{OUT}\ I_{SEC\text{-}pk}}{3}} \\ &= \sqrt{\frac{2 \times 1A \times 4A}{3}} = 1.6\ A\end{aligned} \tag{6}$$

Figure 4 shows the effective capacitance versus voltage and temperature of a 22-µF, 25-V multilayer ceramic capacitor (MLCC) from Murata.[5] Even though the name-plate capacitance is 22 µF, the effective value is 9.1 µF at 25°C and 7.2 µF at –40°C when applying a DC bias of 12 V. Meeting the ripple voltage specification therefore requires three such capacitors in parallel. The equivalent series resistance (ESR) of each MLCC is approximately 3 mΩ within the frequency range of interest, and represents a negligible contribution to output ripple.

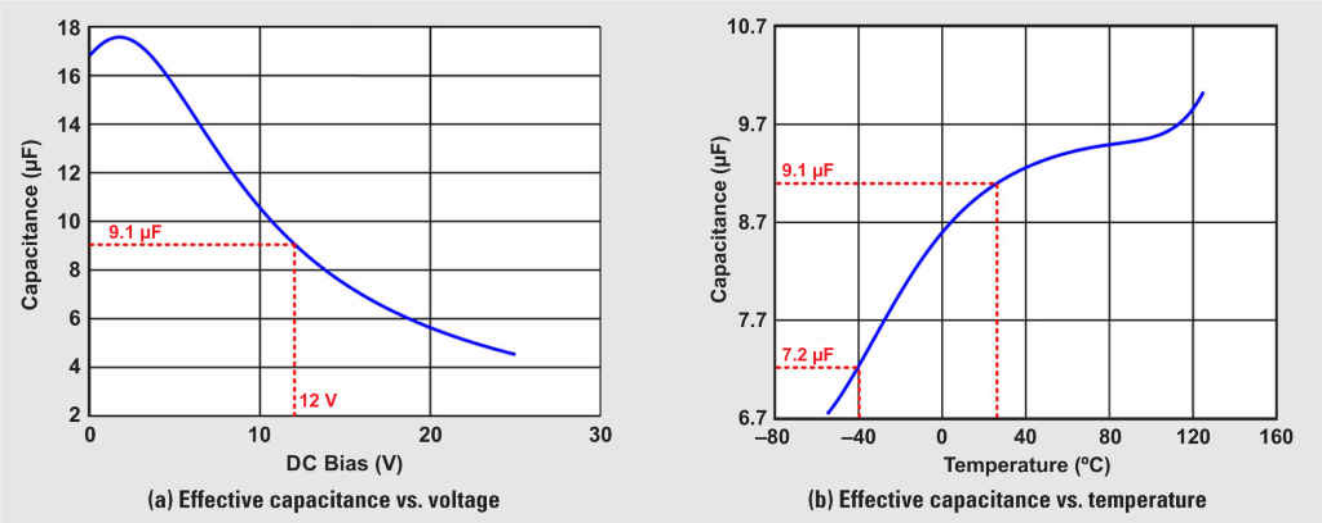

Figure 4. *MLCC Plots for a 22-µF, 25-V, 1210, X7R Capacitor*

Figure 5 shows the simulated primary and secondary currents, the primary switch voltage, and the output capacitor ripple voltage at input voltages of 14 V (BCM) and 42 V (DCM) with an effective output capacitance of 22 µF. For simplicity, the oscillatory effects of transformer parasitic leakage inductance were not included.

The × symbols in **Figure 5** mark the PSR sampling instants on the output voltage waveform. Sampling occurs at an instantaneous output voltage of 12 V close to the peak of the ripple waveform, but the DC output voltage is slightly lower given the total ripple amplitude.

Small-signal Stability Review

As the waveforms in **Figure 3** showed, the flyback converter delivers the entire magnetizing energy stored during the on-time (t_{ON}) to the output during the diode conduction time (t_D). And unlike DCM, where the control variable is the duty cycle, a converter in BCM regulates the output voltage by varying the t_{ON}, which then controls the average diode current (I_D). As a result, the duty cycle remains approximately constant, and I_D—through the effective impedance of the output filter and load—establishes the output voltage.

Neglecting high-frequency phase delays related to current-mode control and PSR sample and hold, **Equation 7** gives the overall loop gain as a product of the control to output (modulator and power stage), feedback, and compensator transfer functions:

$$T_V(s) = G_{VC}(s)G_C(s)G_{FB}(s) =$$

For BCM:

$$\left[\frac{N_{PS}R_L}{2R_i}\left(\frac{1-D}{1+D}\right)\left(\frac{1-s/\omega_{zRHP}}{1+s/\omega_p}\right)\right]\left[g_mR_{EA}\left(\frac{1+s/\omega_{z1}}{1+s/\omega_{p1}}\right)\right]\frac{V_{REF}}{V_{OUT}},$$

or for DCM:

$$\left[\frac{1}{R_i}\sqrt{\frac{L_{mag}f_{SW}R_L}{2}}\left(\frac{1-s/\omega_{zRHP}}{1+s/\omega_p}\right)\right]\left[g_mR_{EA}\left(\frac{1+s/\omega_{z1}}{1+s/\omega_{p1}}\right)\right]\frac{V_{REF}}{V_{OUT}},$$

or for FFM:

$$\left[\frac{K_{VCO}}{R_i}\left(\frac{N_{PS}V_{OUT}}{2f_{SW}}\right)\left(\frac{1-s/\omega_{zRHP}}{1+s/\omega_p}\right)\right]\left[g_mR_{EA}\left(\frac{1+s/\omega_{z1}}{1+s/\omega_{p1}}\right)\right]\frac{V_{REF}}{V_{OUT}} \quad (7)$$

where R_L is the load resistance, R_i is the effective current-sense resistance, ω_p is the power-stage load pole, ω_{p1} and ω_{z1} are the pole and zero of a type-2 compensator, g_mR_{EA} is the DC gain of the transconductance error amplifier, K_{VCO} is the gain from control voltage to switching frequency in FFM, and ω_{zRHP} is the right-half-plane zero (RHPZ) of the flyback power stage related to the phase-shift delay of the secondary current when the primary current changes. However, for DCM analysis, the RHPZ locates at sufficiently high frequency such that its effects can be ignored.

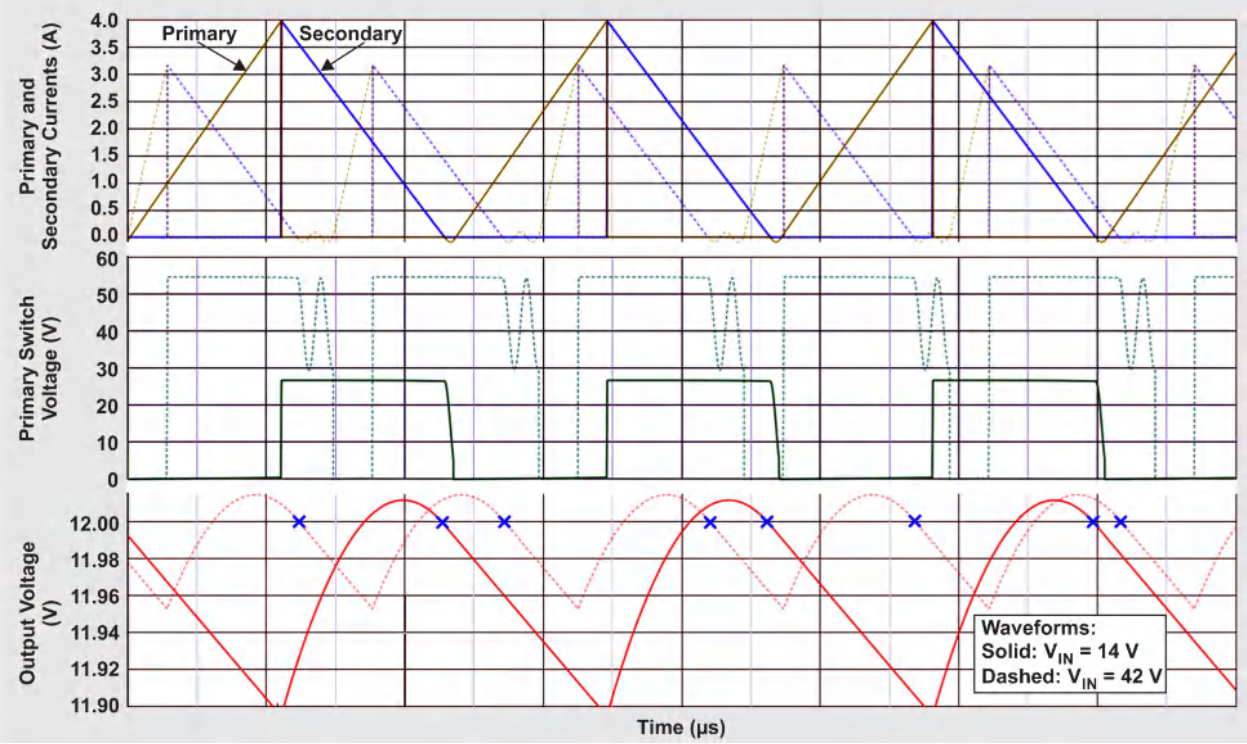

Figure 5. *PSR Flyback Converter Waveforms at Input Voltages of 14 V (Solid Lines, BCM) and 42 V (Dashed Lines, DCM)*

Equation 8 gives the power-stage dominant pole:

$$\omega_p = \begin{cases} \text{For BCM:} \\ (1+D)/R_L \times C_{OUT} \\ \text{or for DCM and FFM:} \\ 2/R_L \times C_{OUT} \end{cases} \quad (8)$$

Interestingly, as the PSR sample and hold occurs at an instantaneous secondary current of zero, the left-half-plane zero evident in the control-to-output transfer function—normally associated with the output capacitor and its ESR—shows no impact on the overall loop-gain transfer function and thus is not included here. In fact, the ESR zero is offset by a corresponding pole in the feedback sampler transfer function.

Figure 6 shows Bode plot simulations of the overall loop gain for the converter circuit in **Figure 1** at input voltages of 14 V and 42 V, assuming a total effective output capacitance of 22 µF. Simulation is mandatory here because practical measurements are not feasible with the integrated compensation design. Besides, the feedback node sees AC current based on the switch-voltage swing, making it unsuitable as an oscillator signal injection point for loop response measurements.

As evident from the plot in **Figure 6**, the frequency of the load pole is higher in DCM than BCM, and the gain of $G_{VC}(s)$ in DCM is generally higher. These two factors result in an increased loop gain in DCM and thus a higher crossover frequency (f_C). Accordingly, the operating condition in DCM at full load sets the output capacitance requirement with reference to loop stability. If the switching frequency in DCM is 350 kHz, a good target for maximum f_C is 35 kHz (10% of the switching frequency).

Output Capacitor Sizing for Small-signal Stability

From **Figure 6**, the loop gain generally presents as a slope of –20 dB per decade up to and beyond f_C, simplifying the determination of required output capacitance. From **Equation 7**, **Equation 9** gives a simplified loop gain expression in DCM:

$$T_V(s)\Big|_{s\to j2\pi f_C} \approx \frac{1}{R_i}\sqrt{\frac{L_{MAG}\, f_{SW}\, R_L}{2}}\left(\frac{2}{s\, R_L\, C_{OUT}}\right) \times\left(g_m\, R_{EA}\,\frac{s\, R_C\, C_C}{s\, R_{EA}\, C_C}\right)\frac{V_{REF}}{V_{OUT}} \quad (9)$$

where R_C and C_C denote the compensation resistance and capacitance, respectively.

Equation 9 further simplifies to yield an expression for C_{OUT} based on a target crossover frequency at unity gain (**Equation 10**):

$$C_{OUT} \approx \frac{1}{f_C}\times\frac{g_m\, R_C\, V_{REF}}{\pi\, R_i\, V_{OUT}}\sqrt{\frac{L_{MAG}\, f_{SW}}{2\, R_L}} \quad (10)$$

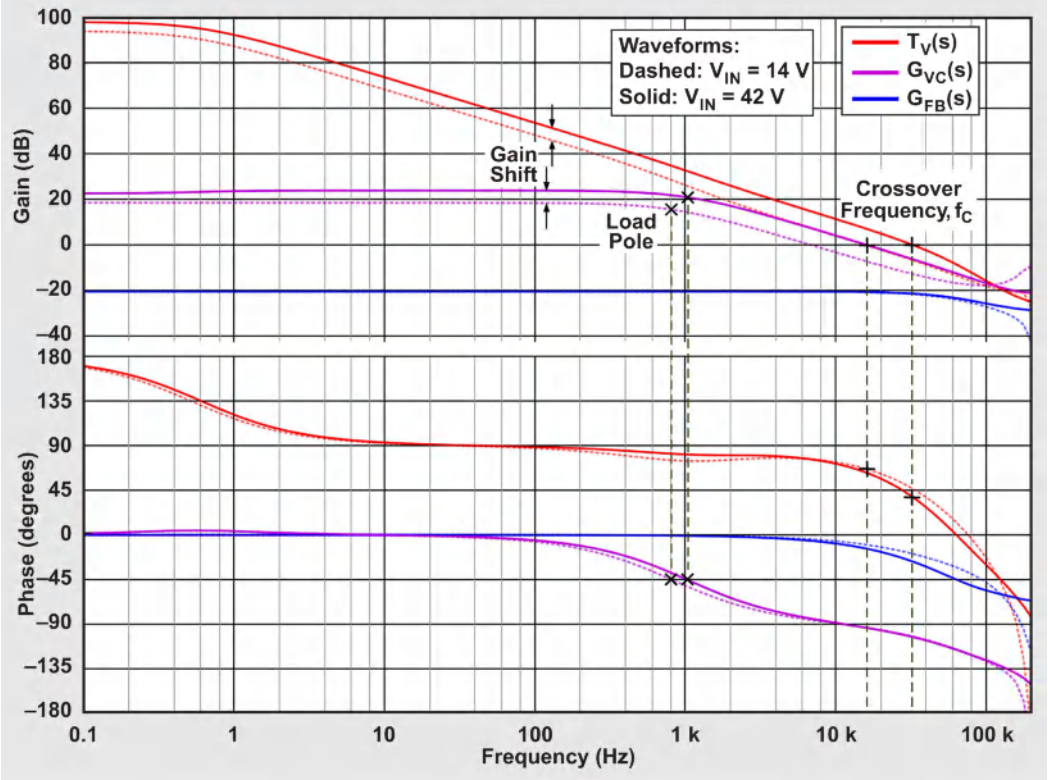

Figure 6. *Simulated Bode Plots at Input Voltages of 14 v (Dashed Lines, BCM) and 42 v (Solid Lines, DCM)*

Using parameters from the LM25184 circuit shown in **Figure 1**, **Equation 11** gives the output capacitance for a target crossover frequency of 35 kHz (10% of the switching frequency):

$$\begin{aligned} C_{OUT} &= \frac{1}{f_C}\times\frac{15}{V_{OUT}}\sqrt{\frac{L_{MAG}}{R_L}} \\ &= \frac{1}{35\,\text{kHz}}\times\frac{15}{12\,\text{V}}\times\sqrt{\frac{7.5\,\mu\text{H}}{12\,\Omega}} \\ &= 28\ \mu\text{F} \end{aligned} \quad (11)$$

overestimation given the attenuating contributions from the PSR sample-and-hold and the current-mode control high-frequency pole (although offset by the RHPZ gain) that may exist at a high f_C. The result also aligns with a generally satisfactory load transient response.

Conclusion

The proper selection of components for a flyback converter requires an understanding of mode behaviors and operating characteristics. This article examined the output capacitance requirement for a PSR flyback DC/DC converter as it pertains to peak-to-peak output ripple and small-signal stability. The worst case for output ripple is at a minimum input voltage and full load, which normally corresponds to operation in BCM. Distinctly, the capacitance requirement for loop stability occurs at a high input voltage and full load when operating in DCM.

References

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4. **LM25183 and LM25184 PSR flyback quickstart design tool, Texas Instruments Design resources (LM25183-LM25184DESIGN-CALC).**
5. **Murata online tool for MLCCs.**

Related Web Sites

Product Information:

LM5180

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