

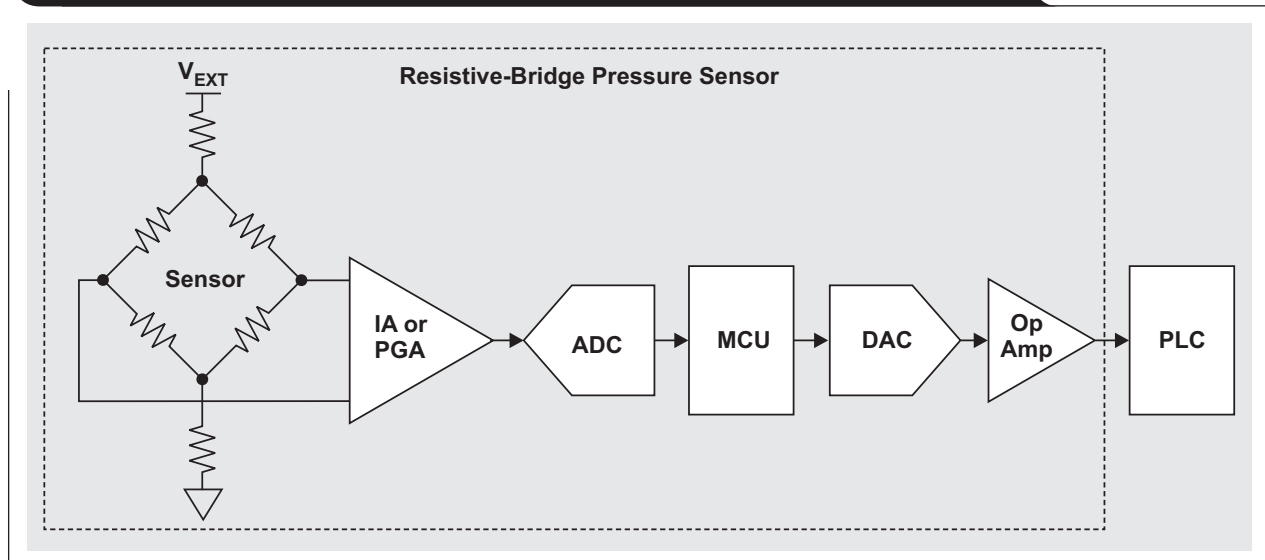
Design tips for a resistive-bridge pressure sensor in industrial process-control systems

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Figure 1. Resistive-bridge pressure sensor connection to process-control system



Introduction

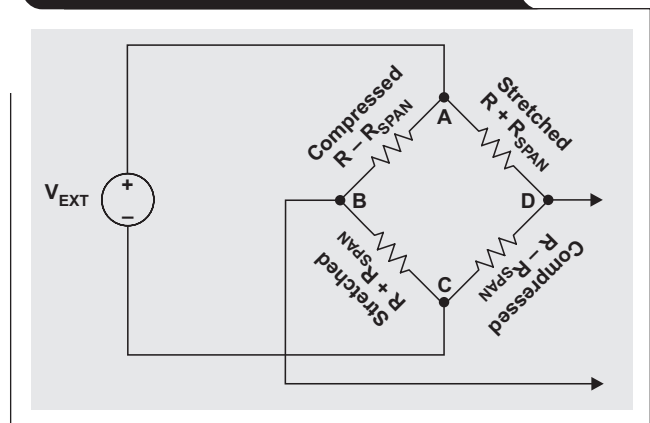
There are many physical parameters that need to be measured and controlled in industrial automation systems. Temperature, pressure, flow, and level are just a few of these physical parameters. Resistive-bridge sensors are commonly used in these applications. Figure 1 shows a typical diagram of a resistive-bridge pressure sensor in a process-control system. This article presents the primary design considerations for each block of the resistive-bridge pressure sensor.

Sensor basics

Industrial process-control systems commonly use resistive-bridge sensors to measure changes in resistance, which ultimately represent changes in physical parameters such as strain, pressure, temperature, humidity, and so on. There are numerous resistive-bridge topologies, but the Wheatstone bridge (Figure 2) is the most widely known and documented.

Each resistor in the pressure sensor either compresses or stretches (Figure 2). When pressure is applied to the sensor, the resistances of R_{AB} and R_{CD} decrease via compression while R_{AD} and R_{BC} increase by stretching. These changes in resistance yield a change in the

Figure 2. Resistive-bridge sensor with pressure applied



differential voltage, V_{BD} , which is amplified by a differential amplifier (Figure 1). Designers often use differential amplifiers with very large input impedance, such as instrumentation amplifiers (IAs) and programmable gain amplifiers (PGAs) when interfacing with bridge sensors.

Common-mode voltage versus output voltage range

The bridge's common-mode voltage (V_{CM}) is the average voltage present at the differential amplifier's input terminals.

$$V_{CM} = \frac{V_{BC} + V_{DC}}{2} \tag{1}$$

If the bridge is balanced, V_{CM} is half of the bridge excitation voltage, $V_{EXT} = V_{AC}$. For example, if $V_{AC} = 5\text{ V}$, then $V_{CM} = 2.5\text{ V}$. The common-mode voltage of the bridge is perhaps the most important design consideration for resistive-bridge sensors. This is because the output voltage range (V_{OUT}) of an IA depends on many factors, including common-mode voltage, gain, reference voltage, topology, and supply voltage.^[1] As an example, Figure 3 shows a V_{CM} versus V_{OUT} plot of an IA with three operational amplifiers (op amps).

Recall that $V_{AC} = 5\text{ V}$, then $V_{CM} = 2.5\text{ V}$. For unidirectional sensors, it is often desirable to power the IA with a single 5-V supply with V_{REF} connected to 0 V (GND). Unfortunately, this will limit the output swing of the IA. Using the INA826 as an example, notice in Figure 3 that if $V_{CM} = 2.5\text{ V}$, the output can only swing from 100 mV to approximately 3.2 V. As a result, the system cannot use the maximum resolution of the analog-to-digital converter (ADC) with a 5-V reference voltage. In this case, consider an alternate IA, select a different supply voltage and/or a different IA reference voltage, or modify the bridge common-mode voltage as shown in Figure 4.

Initial input offset voltage (V_{OS})

The input offset voltage is the DC error voltage between the differential amplifier's input terminals (for example, op amp, IA, PGA, and so on). For a traditional IA with three op amps, this voltage depends on the device's gain.^[2] The offset voltage contributes to the solution's overall offset error and if not calibrated, it also shifts the common-mode voltage. Therefore, a better choice may be a zero-drift IA or PGA (for example, a PGA900) which has a very low offset voltage.

Zero-drift is a term that applies to a chopper or devices with auto-zero topology that will internally correct for offset errors, such as initial input offset voltage, input offset voltage drift, power supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), and some others.

Input offset voltage drift ($\Delta V_{OS}/\Delta T$)

Input offset-voltage drift is the change in input offset voltage as the temperature deviates from room temperature (25°C). This offset error is in addition to the initial input offset voltage. Since most industrial systems must maintain accuracy over a wide temperature range, zero-drift IAs or PGAs are preferred. While the initial input offset voltage can be removed with a room temperature calibration, the offset-voltage drift requires a more complicated and time consuming over-temperature calibration routine. Each individual system must be

Figure 3. A V_{CM} versus V_{OUT} plot for the INA826 IA

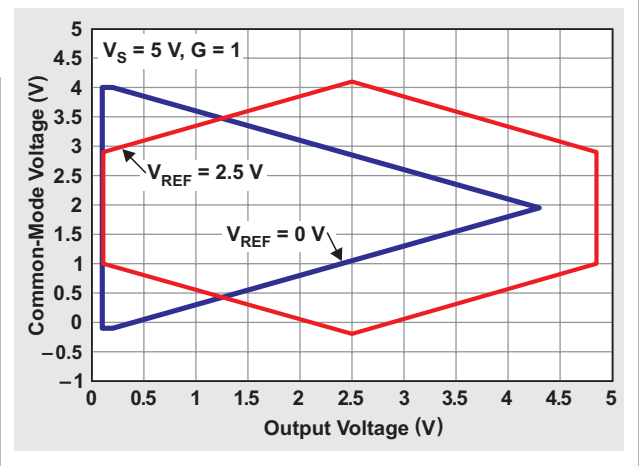
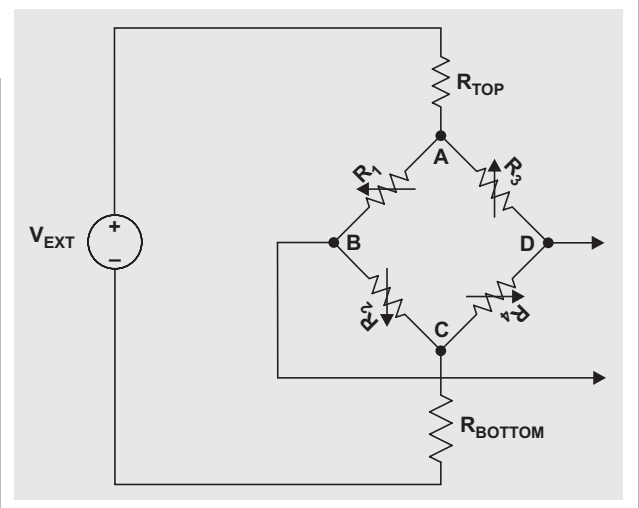


Figure 4. Adjust V_{CM} by adding R_{TOP} and/or R_{BOTTOM}



calibrated at various temperatures because each system component may drift in different directions. In some cases the error over temperature may actually increase if the system is calibrated at 25°C without calibration at other temperatures.^[3]

Noise

An amplifier's intrinsic noise is a primary concern when selecting the bridge amplifier. Of particular interest is the amplifier's low-frequency, or 1/f, noise because industrial systems are typically low-bandwidth. Noise generated by the amplifier sums with the noise of the ADC, which ultimately reduces the measurement's noise-free resolution. While zero-drift amplifiers may be preferred because the 1/f region of their noise spectral-density curve is flat, some non-zero-drift IAs may have better overall noise performance. Conduct a complete noise analysis to determine the amplifier's total noise contribution.

Analog-to-digital converter

High-resolution (24 bit) delta-sigma analog-to-digital converters (delta-sigma ADCs) can be used to measure resistive-bridge signals. Generally, these ADCs include a modulator and digital filter. The total quantization energy is very high for the delta-sigma modulator because the number of bits-per-sample is extremely low. The decimator must filter unwanted noise in the spectrum above the Nyquist band so that the noise is not aliased into the base-band by the decimation process.

The decimator filter implemented in most delta-sigma ADCs is a Sinc filter. This filter topology is popular because it is inherently stable and simple to implement. The order and decimation ratio of this sinc filter determine the performance of the ADC.^[4]

The ADC's noise-free code resolution is defined as the number of bits of resolution beyond which it is impossible to resolve individual codes. The noise-free resolution of the ADC can be calculated based on the total number of codes (2^N) and the peak-to-peak noise code measurement.

$$\text{Noise-free code resolution} = \log_2 \left(\frac{2^N}{\text{Peak-to-peak noise codes}} \right) \quad (2)$$

Effective resolution can be calculated by adding \log_2 (6.6), or approximately 2.7 bits to the calculated noise-free code resolution.

$$\text{Effective resolution} = \text{Noise-free code resolution} + 2.7 \text{ bits} \quad (3)$$

For example, the delta-sigma ADC in the PGA900 has a second-order modulator operating at a sampling frequency of 1 MHz, and a third-order Sinc filter with 128 oversamples. The noise performance shown in Figure 5 is for an output data rate of 7.8 kHz with a bandwidth of 3.9 kHz, and a step response of 384 μ s.

Applying additional digital filtering

It is common for the ADCs in this application to have data rates that are much higher than the required system bandwidth. Therefore, additional digital filtering can be applied to further reduce the ADC noise and therefore increase the noise-free resolution at the expense of the output data rate.

A simple averaging filter creates a low-pass filter that will lower the in-band noise by 3 dB and increase the measurement resolution by a half-bit for each two consecutive samples that are averaged. This is defined in Equation 4 where M is the number of consecutive samples averaged and W is the increase in output signal resolution.

$$W = \frac{1}{2} \log_2(M) \quad (4)$$

From Figure 5, a gain of 40 dB results in a noise-free output resolution of 13.84 bits. Applying a moving-average filter with $M = 32$ to the ADC output data should improve

Figure 5. Measured performance versus gain at output data rate of 7.813 kHz

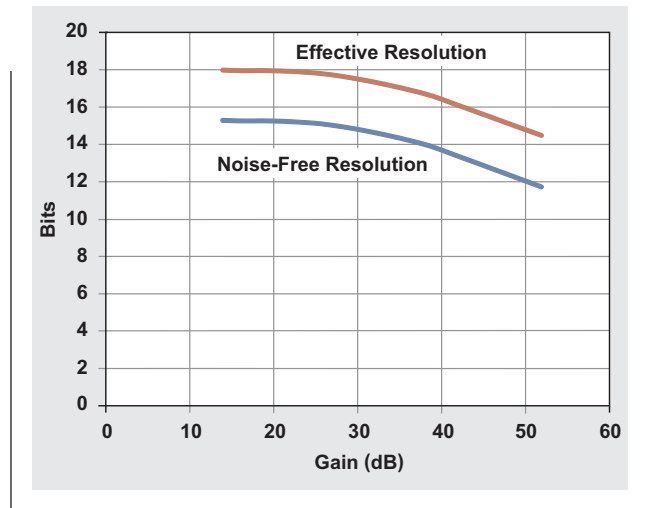
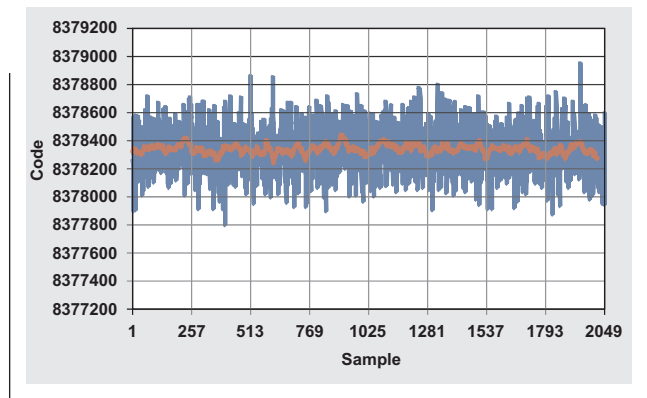


Figure 6. ADC output versus filter output



the noise-free output resolution by 2.5 bits as shown in Equation 5 and Figure 6.

$$W = \frac{1}{2} \log_2(32) = 2.5 \text{ bits} \quad (5)$$

Now the output noise-free resolution has increased from 13.84 to 16.34 bits. However, the data rate of the output signal decreases from 7.8 kHz to 244 Hz.

Analog output stage

Once the sensor signal has been acquired and processed, the next step is to create a linear analog-output signal that represents the sensor measurement from zero- to full-scale. The linear sensor output is transmitted over a 2-wire current loop or a 3-wire voltage output signal, depending on sensor transmitter requirements. The most common output range of a 2-wire sensor transmitter is 4 to 20 mA, although other output spans are occasionally

used. The most common 3-wire voltage output range is 0 to 10 V, but other output ranges can be implemented such as ±10 V, 0 to 5 V, and ±5 V.

The two main building blocks of the analog output stage are a digital-to-analog converter (DAC) and an op amp circuit configured to create the desired current or voltage output range. Be sure to match the performance of the analog output stage closely to that of the sensor acquisition circuitry; including resolution, offset, gain error, non-linearity and noise.

DAC considerations

The DAC commonly sets the performance capabilities for the analog output stage, so select it carefully. Many sensor transmitters are designed with 16-bit DACs, but systems with lower resolution requirements can use 12-bit DACs. Similar to the input stage and ADC, the DAC DC offset, gain and drift errors can be removed with calibration.

Integral non-linearity (INL) errors cannot be removed with a standard gain and offset calibration and set the post-calibration accuracy. Therefore, make sure that the DAC INL specification is well below the desired final system accuracy. A differential non-linearity (DNL) specification less than 1 LSB is almost always a requirement to ensure a monotonic output.

2-wire, 4- to 20-mA output op amp circuit

A standard 2-wire, 4- to 20-mA, transmitter op amp circuit is shown in Figure 7. This circuit requires an op amp with very-low quiescent current to minimize the impact on the limited 2-wire supply-current budget of 4 mA. A linear voltage regulator is typically used to lower the +24-V loop

supply voltage, which allows the use of low-voltage op amps.

The op amp input common-mode range must include the negative rail. To maximize the available output voltage swing, the output swing should include both rails. The output-current requirement is low because the op amp is only required to drive the base current of the bipolar junction transistor (BJT). The majority of the 4- to 20-mA current flows through the BJT from the collector to the emitter.

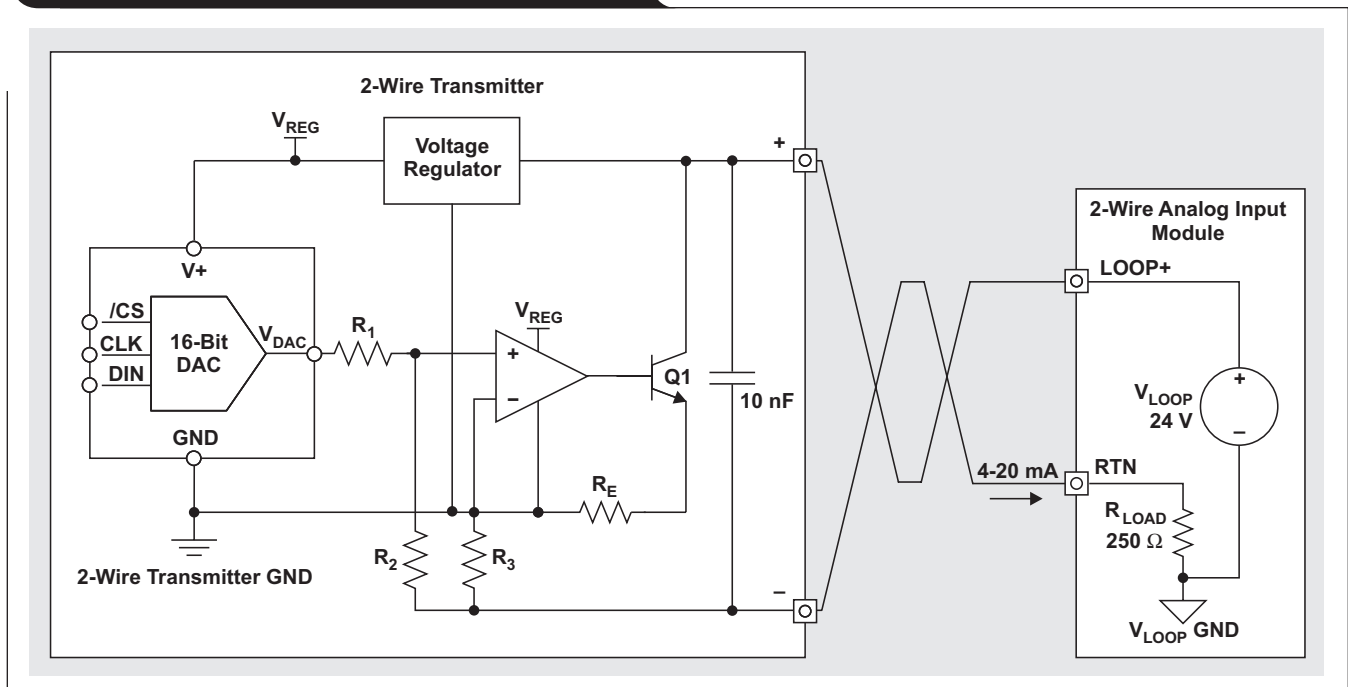
Select op amp performance specifications to match the DAC and the rest of the signal chain. The op amp must have low input offset voltage and drift. High CMRR and PSRR will improve DC performance and noise immunity of the design. eTrim™, laser trim and zero-drift (chopper/auto-zero) CMOS op amps are typically used to meet this circuit's performance requirements.

As shown in the transfer function in Equation 6, resistors R₁, R₂, and R₃ set the circuit's gain. Select precision resistors with low tolerance and temperature coefficients. Ratiometric tolerance and drift-matching the resistors greatly improves performance of the circuit over temperature.

$$I_{OUT} = \frac{V_{DAC}}{R_1 \times \left(1 + \frac{R_2}{R_3}\right)} \tag{6}$$

The circuit must maintain a stable output response to load transients and changes in the output current. Therefore, it is important to select the proper emitter resistor (R_E) based on the Q-point on the V-I curve load line.^[5] A properly selected value for R_E results in a stable feedback network.

Figure 7. Loop-powered 4- to 20-mA transmitter



3-wire voltage-output op amp circuit

A standard op amp circuit used to create a 3-wire voltage output is shown in Figure 8. High-voltage op amps are required for 3-wire circuits to meet the output voltage-range requirements. Single-supply, 0- to 10-V outputs require an input common-mode range that includes ground (GND) with a rail-to-rail output stage to reduce zero code errors in the system.^[6] Performance requirements for the op amp are the same as the 2-wire circuit; such as low-offset and drift with high CMRR and PSRR.

The gain is set by resistors R_F and R_G . Select them based on the same criteria as the gain-setting resistors in the 2-wire circuit.

$$V_{OUT} = V_{IN} \times \left(1 + \frac{R_F}{R_G} \right) \quad (7)$$

In a 3-wire voltage-output circuit, the op amp directly drives the system load, which can vary greatly depending on the final application. Therefore, a robust op amp output stage is required that can deliver upwards of ± 30 mA of output current into a wide range of capacitive loads. Few amplifiers can directly drive large capacitive loads, so the compensation network formed by R_{ISO} , R_F , C_F , and C_L is required for a stable output.^[7] To properly compensate the circuit, the op amp open-loop gain (A_{OL}) and open-loop output impedance (Z_O) must be known. Furthermore, the variations in the A_{OL} and Z_O curves over the system operating conditions need to be considered, or the design may become unstable.^[8, 9]

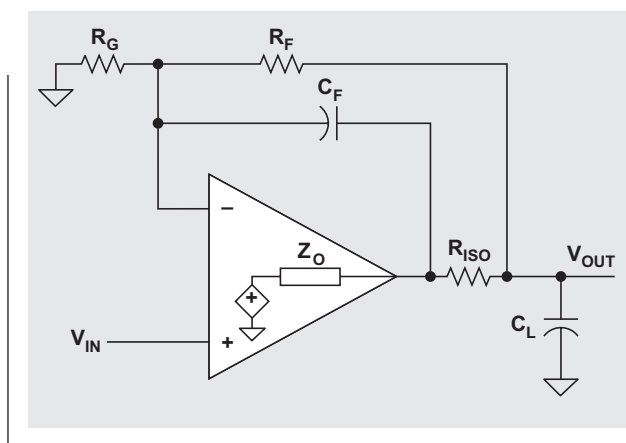
Conclusion

There are many design considerations for resistive-bridge pressure sensors in industrial process-control applications. Performance and specifications of the input signal-conditioning stage, the ADC, and the analog output stage must all be evaluated. This article presented primary design considerations for each of these stages of the signal chain and provided guidance to the designer when selecting components for the design.

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Figure 8. Compensation circuit for capacitive load drive



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