Clock jitter analyzed in the time domain, Part 1

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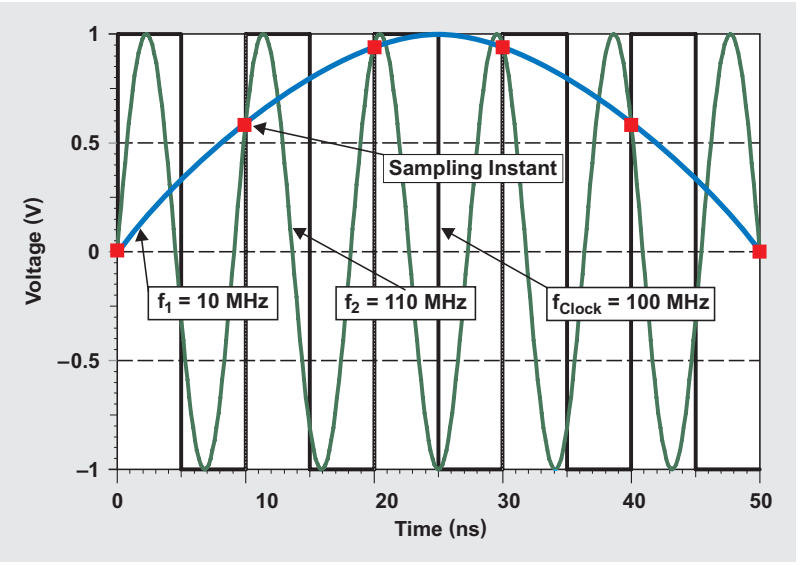
Introduction

Newer high-speed ADCs come outfitted with a large analog-input bandwidth (about three to six times the maximum sampling frequency) so they can be used in undersampling applications. Recent advances in ADC design extend the usable input range significantly so that system designers can eliminate at least one intermediate frequency stage, which reduces cost and power consumption. In the design of an undersampling receiver, special attention has to be given to the sampling clock, because at higher input frequencies the jitter of the clock becomes a dominant factor in limiting the signal-to-noise ratio (SNR).

Part 1 of this three-part article series focuses on how to accurately estimate jitter from a clock source and combine it with the aperture jitter of the ADC. In Part 2, that combined jitter will be used to calculate the ADC's SNR, which will then be compared against actual measurements. Part 3 will show how to further increase the SNR of the ADC by improving the ADC's aperture jitter, with a focus on optimizing the slew rate of the clock signal.

Figure 1. Two input signals sampled at 100 MSPS show the same sample points due to aliasing



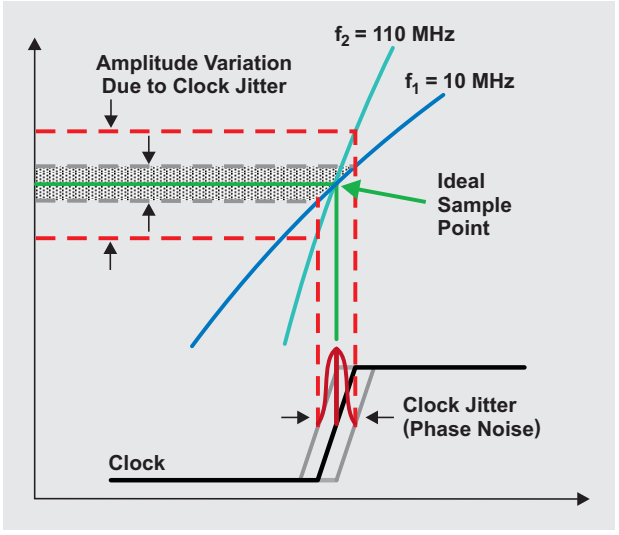
Review of the sampling process

According to the Nyquist-Shannon sampling theorem, the original input signal can be fully reconstructed if it is sampled at a rate that is at least two times its maximum frequency. Assuming that an input signal of up to 10 MHz is sampled at 100 MSPS, it doesn't matter whether the signal is located in the baseband (the first Nyquist zone) at 0 to 10 MHz or undersampled in a higher Nyquist zone at 100 to 110 MHz (see Figure 1). (Sampling in a higher [second, third, etc.] Nyquist zone is commonly referred to as undersampling or subsampling.) However, proper anti-aliasing filtering is required in front of the ADC to sample the desired Nyquist zone and to avoid confusion when the original signal is being reconstructed.

Jitter in the time domain

Looking closely at one sampling point reveals how timing uncertainty (clock jitter or clock phase noise) creates amplitude variation. As the input frequency increases due to undersampling in a higher Nyquist zone (e.g., from f_1 = 10 MHz to f_2 = 110 MHz), a fixed amount of clock jitter generates a larger amount of amplitude deviation (noise)

Figure 2. Clock jitter creates more amplitude error with faster input signals



from the ideal sample point. Furthermore, Figure 2 suggests that the slew rate of the clock signal itself has an impact on variations in the sampling instant. The slew rate

determines how fast the clock signal passes through the zero crossing point. In other words, the slew rate directly impacts the trigger threshold of the clock circuitry inside the ADC.

If there is a fixed amount of thermal noise on the internal clock buffer of the ADC, then the slew rate gets converted into timing uncertainty as well, which degrades the inherent aperture jitter of the ADC. As can be seen in Figure 3, the aperture jitter is completely independent of the clock jitter (phase noise), but those two jitter components combine at the sampling instant. Figure 3 also shows that the aperture jitter increases as the slew rate decreases. The slew rate is usually directly dependent on the clock amplitude.

SNR degradation caused by clock jitter

There are several factors that limit the SNR of the ADC, such as quantization noise (typically not noticeable in pipeline converters), thermal noise (which limits the SNR at low input frequencies), and clock jitter (SNR_{Jitter}) (see Equation 1 below). The SNR_{Jitter} component, which is limited by the input frequency, f_{IN} (depending on the Nyquist zone), and by the total amount of clock jitter, t_{Jitter}, can be calculated as

$$SNR_{Jitter}\left[dBc\right] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}). \quad (2)$$

As expected, with a fixed amount of clock jitter, the SNR degrades as the input frequency increases. This is illustrated in Figure 4, which shows the SNR of a 14-bit pipeline converter with a fixed clock jitter of 400 fs. If the input frequency increases by one decade, such as from 10 MHz to 100 MHz, the maximum achievable SNR due to clock jitter is reduced by 20 dB.

As already mentioned, another major factor that limits the ADC's SNR is the ADC's thermal noise, which doesn't change with input frequency. A 14-bit pipeline converter typically has a thermal noise of ~70 to 74 dB, also shown in Figure 4. The ADC's thermal noise, which can be found in the data sheet, is equivalent to the SNR at the lowest specified input frequency (10 MHz in this example), where clock jitter is not yet a factor.

Let's analyze the 14-bit ADC with a thermal noise of ~73 dB and a clock circuitry with 400 fs of jitter. At low input frequencies such as 10 MHz, the SNR of this ADC is pretty much defined by its thermal noise. As the input frequency increases, the 400-fs clock jitter gets more and more dominant until it completely takes over at ~300 MHz. Even though the SNR due to clock jitter at an input frequency of 100 MHz is reduced by 20 dB per decade compared to the SNR at 10 MHz, the total SNR is degraded by only

Figure 3. Clock jitter and ADC aperture jitter combine at sampling instant

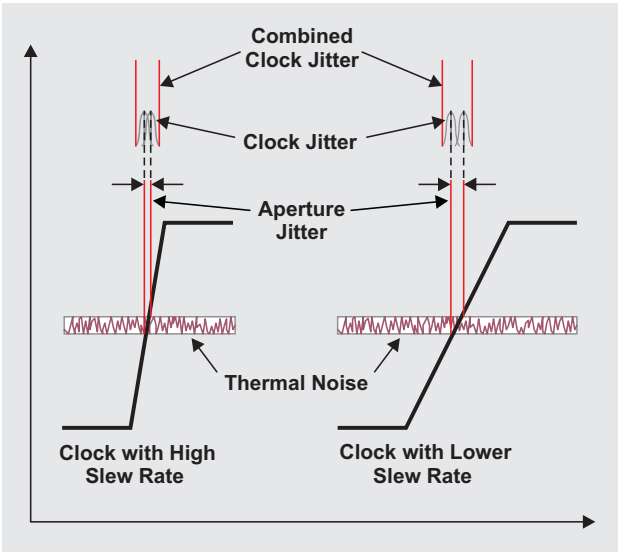
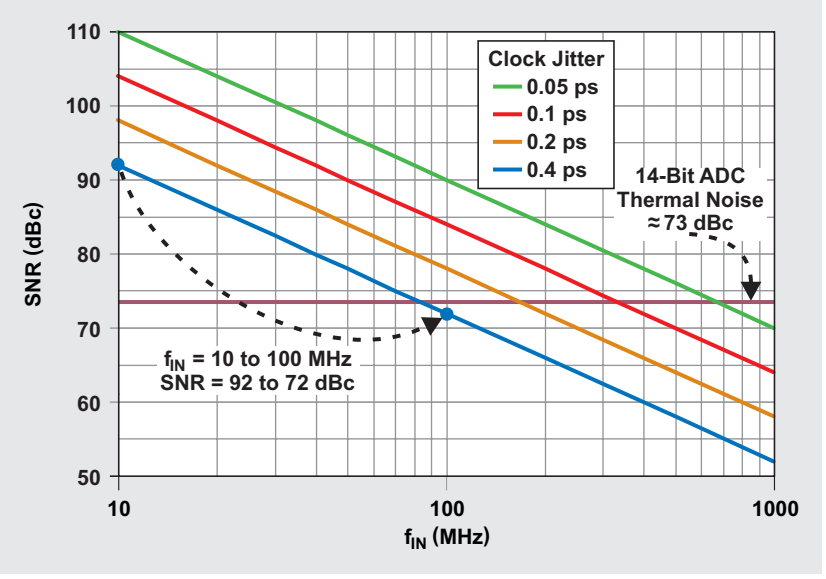
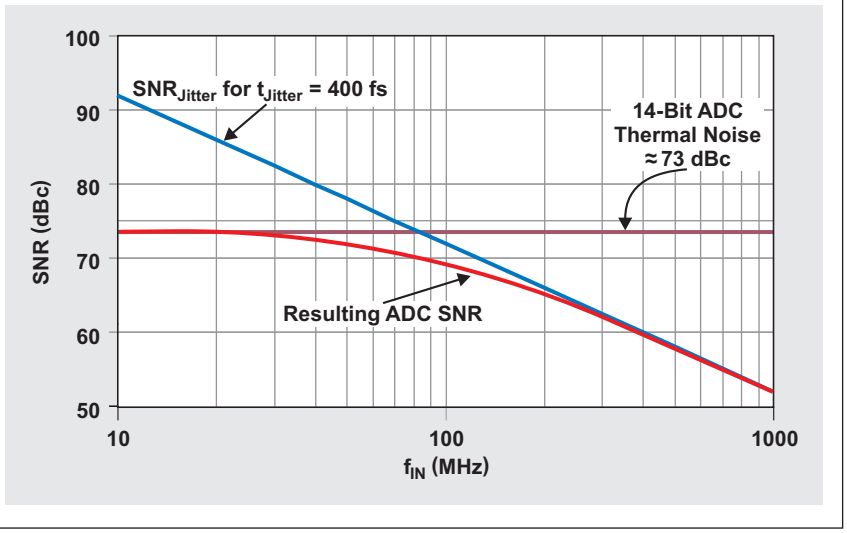


Figure 4. Fixed 400-fs clock jitter reduces SNR by 20 dB per decade



$$SNR_{ADC}\left[dBc\right] = -20 \times \log \sqrt{\left(10^{-\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

Figure 5. Resulting ADC SNR is limited by thermal noise and clock jitter



~3.5 dB (down to 69.5 dB) because of the 73-dB thermal noise (see Figure 5):

$$SNR_{Jitter} = -20 \times \log(2\pi \times 100\ \text{MHz} \times 400\ \text{fs}) = 72\ \text{dBc}$$

$$SNR_{ADC} = -20 \times \log\sqrt{\left(10^{-\frac{73\ \text{dBc}}{20}}\right)^2 + \left(10^{-\frac{72\ \text{dBc}}{20}}\right)^2} = 69.5\ \text{dBc}$$

Now it becomes obvious that if the ADC's thermal noise increases, the clock jitter will become very important when higher input frequencies are sampled. A 16-bit ADC, for example, has a thermal noise floor of ~77 to 80 dB. According to the curves in Figure 4, in order to minimize the effect of clock jitter on SNR at an input frequency of 100 MHz, the clock jitter needs to be on the order of 150 fs or better.

Determining the sample clock jitter

As demonstrated earlier, the sample clock jitter consists of the timing uncertainty (phase noise) of the clock as well as the aperture jitter of the ADC. Those two components combine as follows:

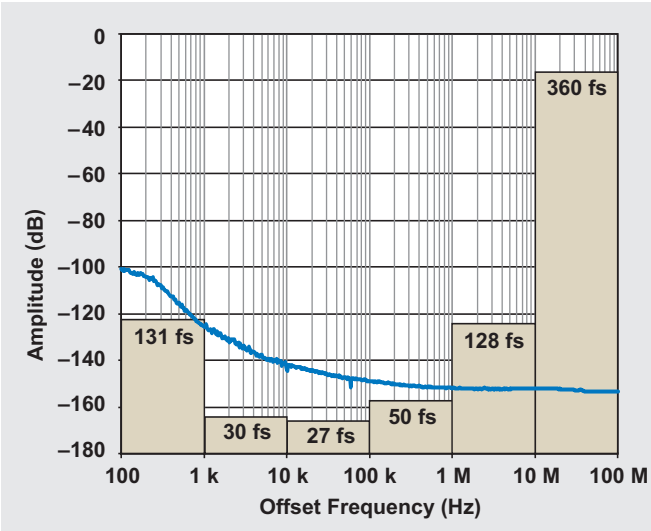
$$t_{Jitter} = \sqrt{(t_{Jitter,Clock\_Input})^2 + (t_{Aperture\_ADC})^2} \quad (3)$$

The aperture jitter of the ADC can be found in the data sheet. It is important to remember that this value is typically specified in combination with either clock amplitude or slew rate. Lower clock amplitudes result in slower slew rates and increase the aperture jitter accordingly.

Jitter from the clock input

The output jitter of devices in the clocking chain (oscillator, clock buffer, or PLL) is typically specified over a frequency range that is offset from the fundamental clock frequency by 10 kHz to 20 MHz—either in picoseconds or as a phase-noise plot, which can be integrated to obtain the jitter information. However, 10 kHz on the low end and 20 MHz on the high end are sometimes not the right boundaries to use, as they are highly dependent upon other system parameters, as will be explained later. The importance of setting the right integration limits is illustrated in Figure 6, where a phase-noise plot is overlaid with its jitter content per decade. It can be seen that the resulting jitter can be quite different if the lower limit is set to a 100-Hz or 10-kHz offset. Likewise, setting the upper integration limit to 10 or 20 MHz yields a drastically different result than setting it to 100 MHz, for example.

Figure 6. Jitter contribution from clock phase noise calculated per decade



Determining the proper lower integration limit

In the sampling process, the input signal gets mixed with the sampling clock's signal, including its phase noise. When an FFT analysis of the input signal is performed, the primary FFT bin is centered over the input signal. The phase noise around the sampled signal (either from the clock or the input signal) determines the amplitude of the bins adjacent to the primary bin, as illustrated in Figure 7. Therefore, all the phase noise with an offset frequency of less than half the bin size gets lumped into the bin of the input signal and doesn't add to the noise. Hence, the lower limit of the phase-noise integration bandwidth should be set to half the FFT bin size. The FFT bin size is calculated as follows:

$$\text{Bin Size} = \frac{\text{Sampling Rate}}{\text{FFT Size}}$$

To further illustrate this point, an experiment using the ADS54RF63 was set up with two different FFT sizes—131,072 and 1,048,576 points. The sampling rate was set to 122.88 MSPS, and the clock phase noise is shown in Figure 8. A 6-MHz, wide-bandpass filter was added to the clock input to limit the amount of wideband noise contributed to the jitter. A 1-GHz input signal was chosen to ensure that the SNR degradation was due solely to clock jitter. Figure 8 shows that the jitter results of the phase-noise integration from half a bin size to 40 MHz are drastically different for the two FFT sizes, and the SNR measurements in Table 1 reflect that as well.

Setting the proper upper integration limit

The phase-noise plot in Figure 6 had a jitter contribution of ~360 fs with the frequency offset between 10 and 100 MHz. This is far more than the entire jitter contribution of ~194 fs with the offset between 100 Hz and 10 MHz. Therefore, the chosen upper integration limit can drastically affect the calculated clock jitter and how well the predicted SNR will match the actual measurement.

To determine the right limit, one has to remember something very important from the sampling process: Noise and spurs on the clock signal alias in-band from other Nyquist zones just like they would if they were present on the input signal (see Reference 1). Hence, if the phase noise of the clock input is not band-limited and doesn't have a rolloff at a higher frequency, then the upper integration limit is set by the bandwidth of the transformer (if used) and the clock input of the ADC itself. In some cases the clock input bandwidth can be very large; for example, the ADS54RF63 has a clock input bandwidth of ~2 GHz to allow higher-order harmonics for very fast clock slew rates.

To verify that the clock phase noise needs to be integrated all the way up to the clock input bandwidth, another experiment was set up. The ADS54RF63 was again operated at 122.88 MSPS with an input signal of 1 GHz to ensure that the SNR jitter was limited. Broadband white noise of 50 MHz to 1 GHz was generated with

Figure 7. Close-in phase noise determines amplitude of FFT bins around primary bin

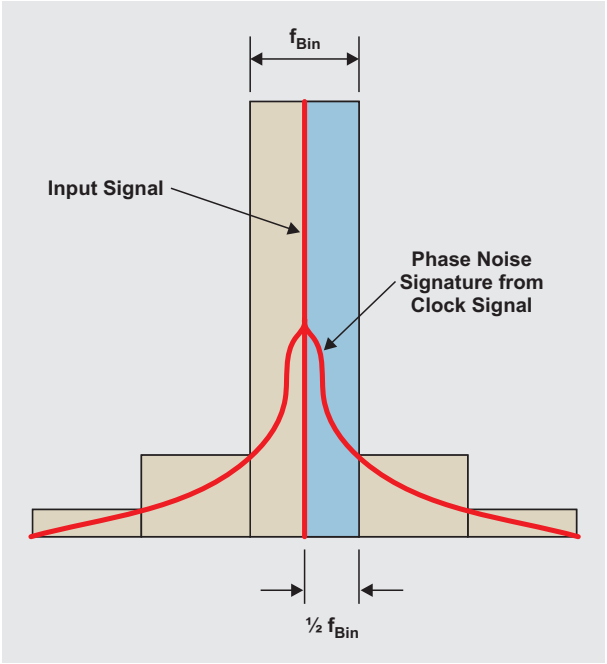


Table 1. SNR measurements for two FFT sizes

FFT SIZE (POINTS)	½ BIN SIZE (Hz)	SNR AT 1 GHz (dBFS)
131,072	469	60.4
1,048,576	59	51.9

Figure 8. Integrated jitter for two FFT sizes with different lower integration limits

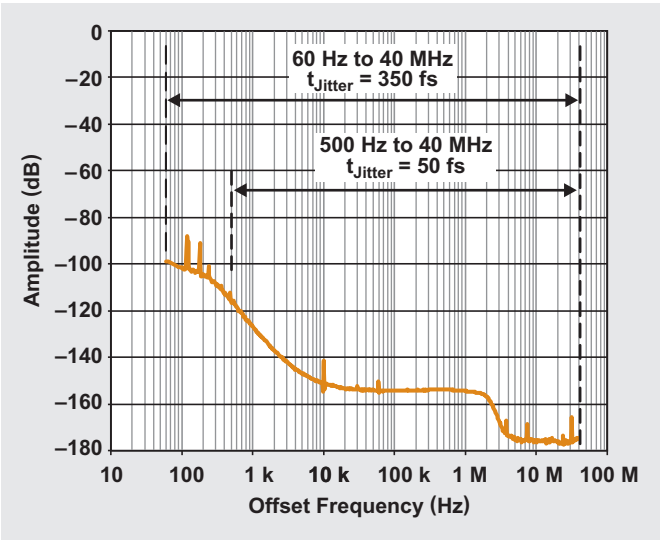
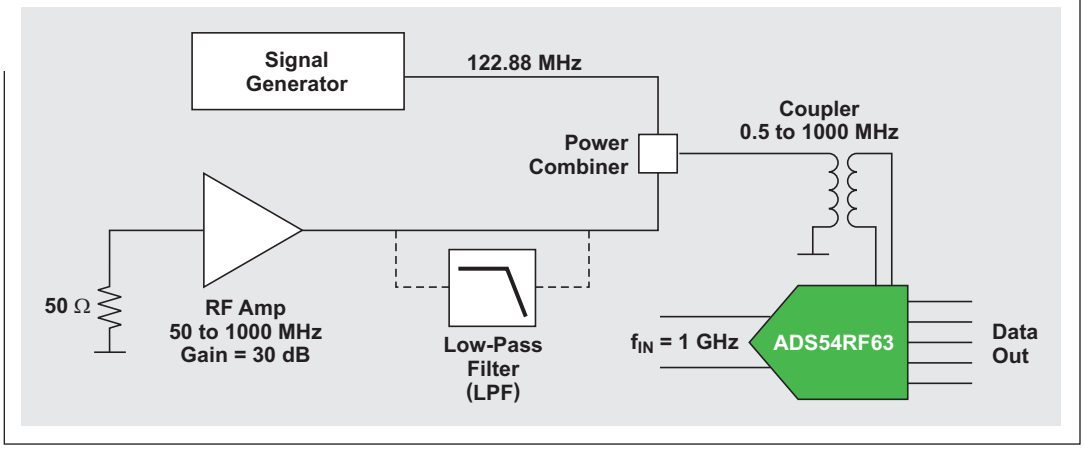


Figure 9. Test setup to verify clock input noise

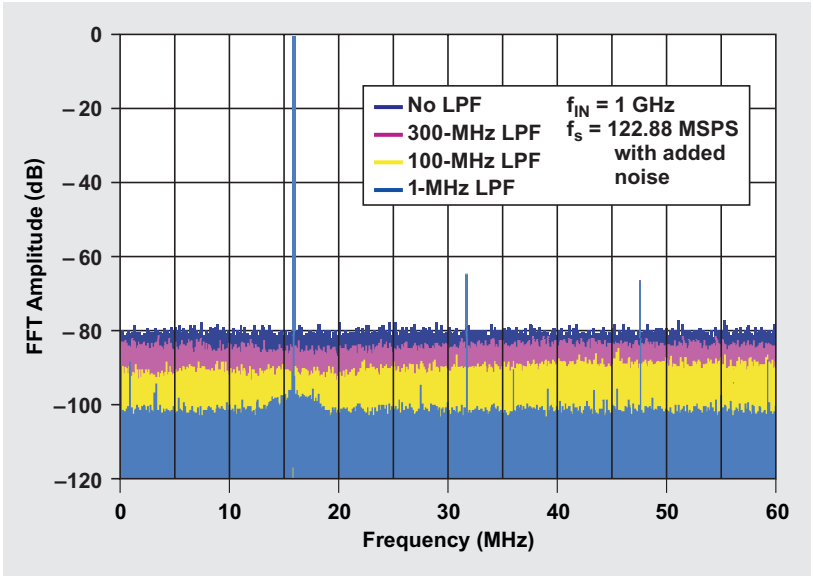


an RF amplifier and added to the sampling clock as shown in Figure 9. Then different low-pass filters (LPFs) were used to limit the amount of noise being added to the clock signal.

The clock input bandwidth of the ADS54RF63 is ~2 GHz, but since the RF amplifier and the transformer both have a 3-dB bandwidth of ~1 GHz, the effective 3-dB clock input bandwidth is reduced to ~500 MHz. The measured SNR results in Table 2 confirm that for this setup the clock input bandwidth indeed is around 500 MHz. A comparison of the FFT plots in Figure 10 further confirms how the wide-band noise from the RF amplifier limits the noise floor and degrades the SNR.

This experiment showed that the phase noise of the clock needs to be either very low or band-limited, ideally through a tight bandpass filter. Otherwise the upper integration limit, set by the clock bandwidth of the system, can degrade the ADC's SNR substantially.

Figure 10. Overlaid measured FFT plots with different noise contributions



Conclusion

This article has shown how to accurately estimate the sampling-clock jitter and determine the proper upper and lower integration boundaries. Part 2 will show how to use this estimation to derive the ADC's SNR and how this result compares against actual measurements.

Table 2. SNR measurements for setup in Figure 9

SETUP	SNR (dBFS)
No filter	39.9
300-MHz LPF	43.6
100-MHz LPF	49.4
1-MHz LPF	57.7

Reference

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1. Thomas Neu, "Impact of sampling-clock spurs on ADC performance," *Analog Applications Journal* (3Q 2009) slyt338

Related Web sites

dataconverter.ti.com
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