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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Amplifiers: Audio
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

How digital filters affect analog audio signal levels

By Jorge Arbona, *Applications Engineer,*
and Supriyo Palit, *Software Systems Engineer*

Introduction

Digital audio processing provides a great amount of flexibility to system designers. Multiple filter structures can be cascaded to form equalization (EQ), low-pass, high-pass, shelf, and many other filter combinations with relatively low power consumption and little PCB space. Infinite-impulse-response (IIR) filters can be used to easily simulate filter functions performed by analog counterparts.

Digital audio signals are represented as an array of bits with a fixed resolution. This means that the signal is discrete in nature, both in amplitude and in time. If the source of this data is analog, it is quantized and sampled at fixed intervals (sampling periods) by an analog-to-digital converter (ADC). An audio engineer has to be careful to ensure that the signal being recorded is not clipped, while maintaining the signal as loud as possible to maximize the signal-to-noise ratio (SNR). An ADC has an amplitude limit, which may be defined as a full-scale voltage, meaning that any signal above a certain amount of volts at the converter's input may result in clipping. Also, the signal is quantized into a number with a certain fixed resolution (which might also be close to the clipping point).

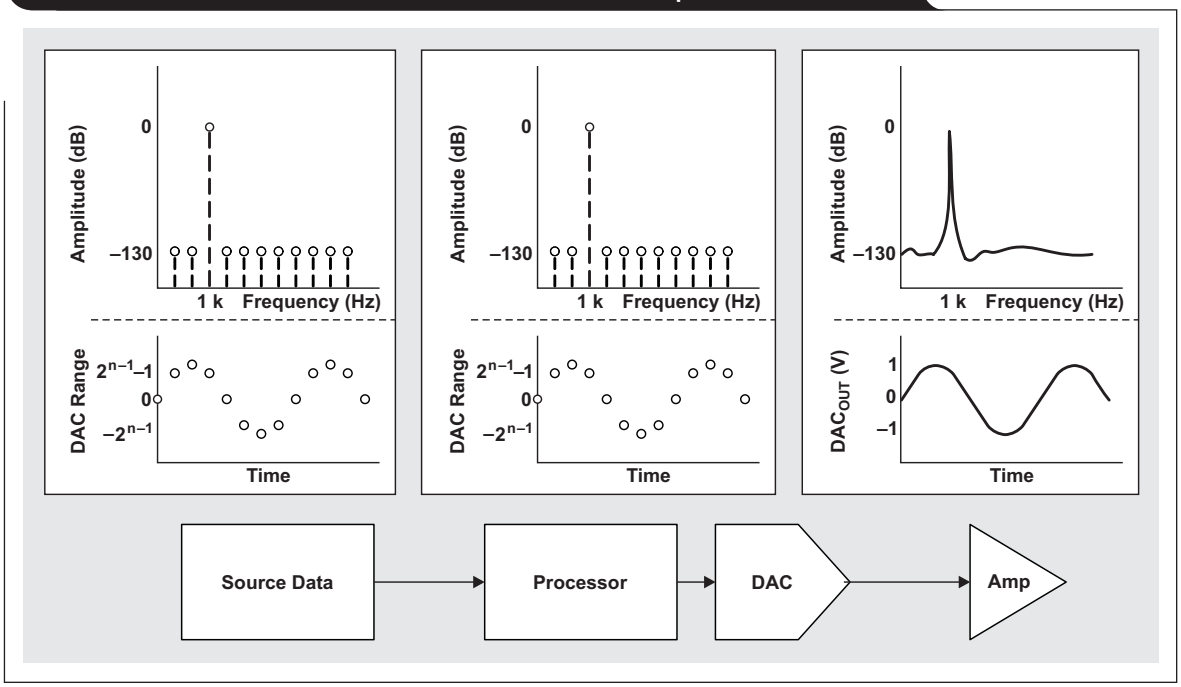
A mastering engineer also has to be careful when working with music in the digital domain. Some EQ can be added to boost certain frequencies as well as to achieve other effects. If there is an extravagant amount of headroom, the engineer can boost, boost, and boost. However, the final medium for the music is a CD (which is limited to 16-bit audio), so trade-offs have to be made because the rest of the music sounds too "quiet" compared to the SNR of the medium.

Boosting frequency bands in the digital domain can create certain problems when the bands are converted into the analog domain. Digital-to-analog converters (DACs) can also clip the signal if their digital input is larger than their full-scale voltage. Most processors allow a certain amount of headroom to work with intermediate values, but ultimately a DAC expects a certain data width bounded by maximum and minimum values. If the signal is scaled down and certain frequencies are then boosted to accommodate the higher peaks, then the SNR at the flat region(s) will suffer from a lower SNR.

Understanding the problem

A very important aspect to consider when digital filters are used is how the signal level is affected upon its conversion from the digital to the analog domain. Suppose that a system provides a digital signal to a processing unit and converts it to analog using an ideal DAC without any processing being applied, as shown in Figure 1. In this example, a 0-dBFS digital signal is provided to the DAC and converted

Figure 1. Full-scale digital signal represented as a 1-V_{peak} analog signal



into the analog domain. A relationship between the digital code and the analog output amplitude is provided in the specification of a codec as the full-scale amplitude. If the specification of the full-scale amplitude is 0.707 V_{RMS} (or 1 V_{peak}), this means that a full-scale 0-dBFS digital sinusoid will result in a 1-V_{peak} sinusoid, as shown in the figure.

If a DAC is bounded by -2^{n-1} and $2^{n-1} - 1$, amplifying a signal beyond these limits will distort the signal by clipping it at its output (assuming saturation logic), as shown in Figure 2. Note that it is typical for most signal processors to allow some amount of headroom before providing data to a DAC. It is important for the data within the processor's memory to remain undistorted. Figure 2 illustrates the DAC input limits where output clipping may occur if exceeded.

A solution to this problem would be to ensure that the signal is not amplified beyond the DAC's limits (i.e., ensure that positive gain is not applied to the source signal). However, there are cases for which the solution is not as obvious. Performing a boost relative to the full-scale amplitude of the DAC input at a specific frequency range will also cause adverse effects. In Figure 3, a 500-Hz signal is boosted by 6 dB. The distortion observed in the analog output is due to DAC clipping.

Figure 2. Excessive gain in the digital domain can make the signal exceed the DAC's upper and lower limits

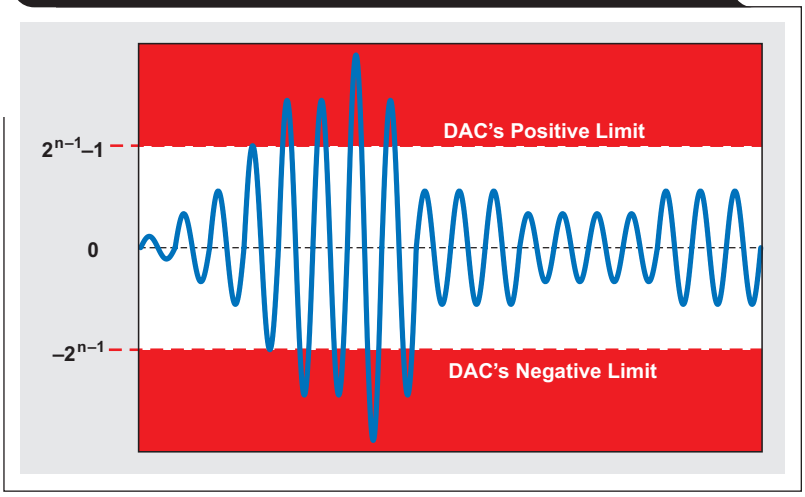
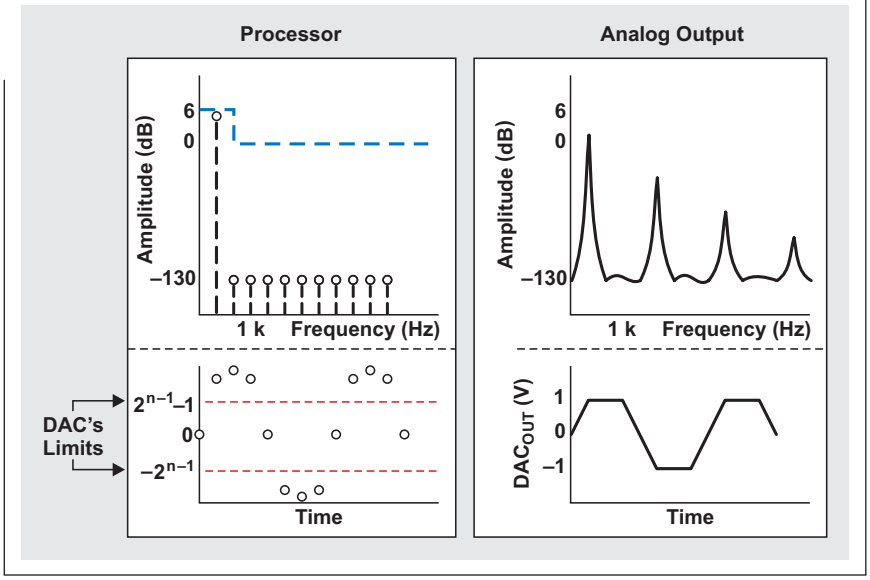
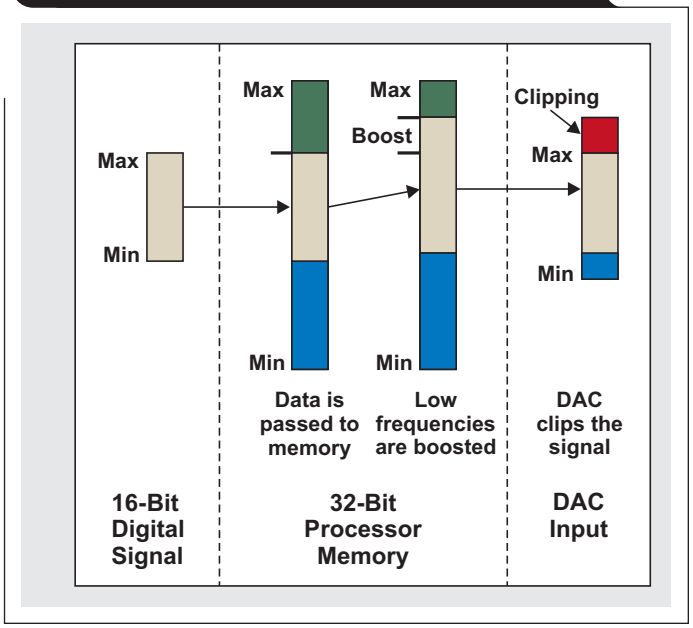


Figure 3. Possible effects of boost on a specific frequency band



This concept is also illustrated in Figure 4. Note that the noise from the source data is inherited when passed to the larger bus width of the processor's memory. As mentioned previously, data could be scaled down by the maximum amount of total boost to accommodate the boosted regions. However, as seen in Figure 5, even if the boost reference point is in a good position, the DAC signal might be affected by the output SNR. If the amount of boost does not compromise overall system SNR significantly, then simple scaling might be a viable solution. Some low-power codecs provide 100 dB of SNR, which allows some amount of scaling without sacrificing the SNR of the original 16-bit source.

Figure 4. Signal content throughout the digital signal chain



Quantization and number representation

In digital processing, a real number is represented as an integer value with a fixed precision. This is called quantization, and the quantized value is an approximation of the original value. The integer value can be represented as a fixed-point number or a floating-point number. An integer value represented as a fixed-point number is composed of magnitude bits and fractional bits. An integer value represented as a floating-point number is composed of exponent bits and mantissa bits. This discussion will henceforth be restricted to fixed-point numbers and fixed-point arithmetic.

A fixed-point number is represented as a twos-complement integer with a fixed number of digits after the radix point (or the decimal point). These digits make up the fractional part of the number. The digits before the radix point are the magnitude part and denote the range of the number. The magnitude part also contains the sign of the number.

Digital data coming into an audio processor is considered to be a real number lying between –1 and 1 – 1LSB. Assuming that the real value is represented as a 16-bit fixed-point number, the number –1 will be represented as 1000000000000000 in binary (or 0x8000 in hexadecimal). In twos-complement arithmetic, 0x8000 corresponds to an integer value equal to –32768. This means that dividing the integer number by 32768 will result in the quantized

Figure 5. Signal content with the use of scaling

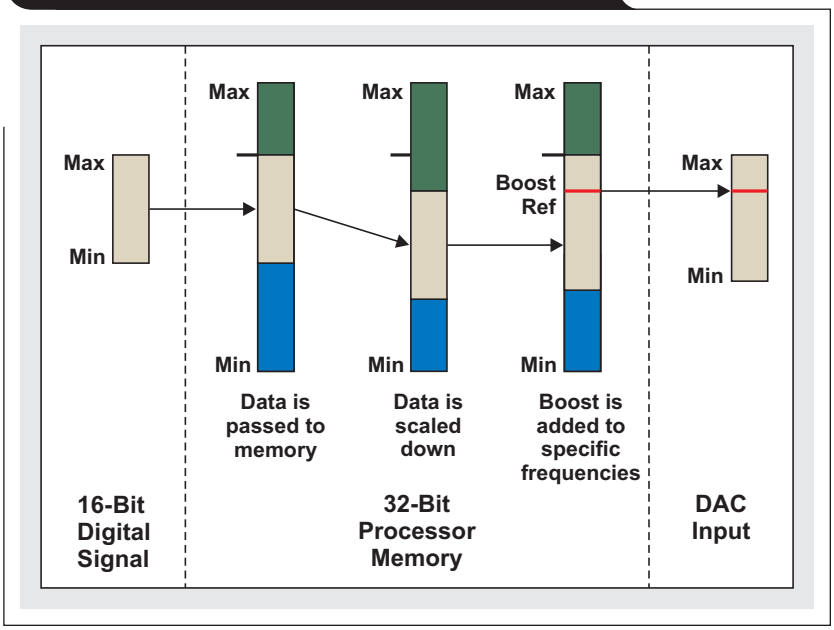
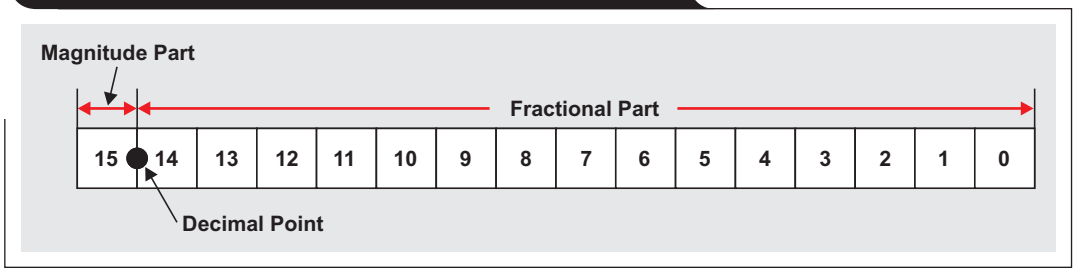


Figure 6. Fixed-point representation of a real number



approximation of the real value. The largest positive number in 16 bits is 0111111111111111 in binary (or 0x7FFF in hexadecimal). The corresponding integer value is 32767. Dividing this by the scale factor of 32768 produces the largest real number that can be represented in this format. The number is 32767/32768 = 0.999969482421875. The fixed-point representation is shown in Figure 6.

In this representation, there are 15 fractional bits and 1 magnitude bit, which is also the sign bit. This means that a real number must lie between –1 and 0.999969482421875 before quantization. If the real number is above or below this range, it cannot be represented in the given format because the 16-bit register will overflow. To accommodate larger real numbers, the magnitude part needs to be increased at the expense of a reduced fractional part. This format is also known as the 1.15 format (1 = magnitude bits, and 15 = sign bits). Input to a digital processor is always represented in 1.n format, where n is the number of fractional bits (15, 19, 23, or 31). A value of 0 dBFS corresponds to the RMS value of a full-scale sine wave whose amplitude is $(2^n - 1)/2^n$. The largest real number in the given format is represented by 2^n. The number of bits that are used to represent a signal is called the signal bit width or the data bit width.

Overflow and saturation

Overflow occurs when a processing unit's computation results in a value greater in magnitude than the data bit width. Overflow is typically associated with computation in the accumulator, where successive numbers of the same sign are added and stored. Accumulators usually keep accumulating even after overflow because the final result, if within bounds, will still come out correctly.

The output of the accumulator is saturated before it is stored as a signal value. Saturation is a process where a positive overflow is converted to the maximum positive number and a negative overflow is converted to the minimum negative number. Saturation is a nonlinear operation and results in severe harmonic distortion of the output. Headroom bits are used to prevent saturation.

Signal bits

Signal and noise bits affect the performance of a system. The digital audio processor adds quantization noise, and the overall performance will be the effect of both the analog circuit noise and the quantization noise. Assuming that both noise sources are the outcome of independent random processes, the overall system noise performance can be defined as

$$\mathrm{SNR} = 10\log_{10}\left(\frac{S^2}{N_C^2 + N_Q^2}\right),$$

where S is a uniformly distributed random signal, N_C is DAC circuit noise, and N_Q is quantization noise. Using a 100-dB DAC and a 120-dB signal processor will result in an overall SNR of 99.96 dB.

It should be noted that the overall SNR is also limited by the source—the input to the digital audio processor. If the input is provided as a 16-bit number, then the signal-to-quantization-noise ratio (SQNR) of the system can, at best, be 96 dB (assuming a uniformly distributed random signal, unweighted). So, even a higher-bit internal representation (lower N_Q) will not provide much improvement in this case.

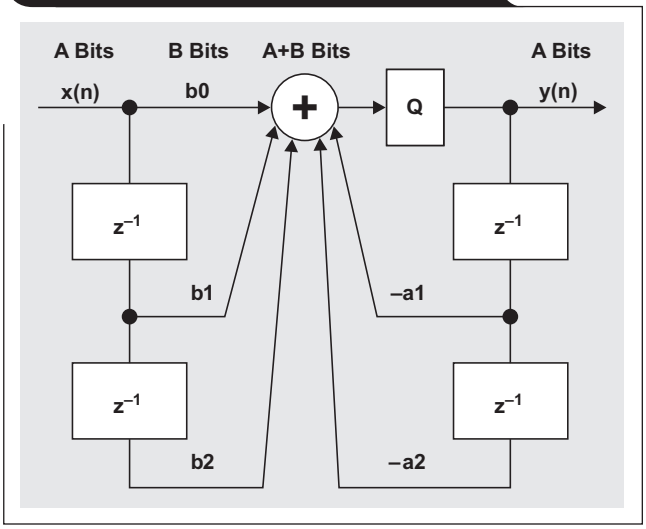
Noise bits

Earlier it was mentioned that the number of signal bits determines the performance of the digital audio system. More bits are sometimes needed for filter-response calculations.

A filter implementation consists of a data path through which the signal flows and is stored as delay elements for the filter. The signal and delay values are multiplied by the coefficients associated with the filter taps. Coefficient quantization also plays an important role in system performance. The product of the signal and coefficient values is stored in the accumulator, which usually has a higher bit width than that of the signal. Subsequent products are added in the accumulator (at a higher bit width), and the final filter output is then stored back in signal precision (at a lower bit width).

Consider the biquad filter implementation in Figure 7. In this figure, the input and output signals are represented by "A bits." The a and b coefficients are represented by "B bits." The input signal and its delay elements are multiplied by the coefficients and added at the accumulator. The multiplier and accumulator together are A + B bits wide. The output signal is then quantized by the Q block and stored as an A-bit number. This introduces a quantization error, which is a noise source for the digital filter; therefore extra bits are needed to ensure that the noise contribution from the digital filter is below the target SNR. These extra bits are called the noise bits. The effect of noise is more pronounced with IIR filters than with finite-impulse-response (FIR) filters. The number of noise bits also depends on the sampling frequency and the cutoff frequency of the digital filter. As the sampling frequency increases, the number of noise bits required increases. As the cutoff frequency decreases, the number of noise bits required increases. For a 48-kHz operation, 14 to 16 noise bits are enough to maintain the target SNR for a 40-Hz IIR filter.

Figure 7. Biquad filter implementation



Headroom bits

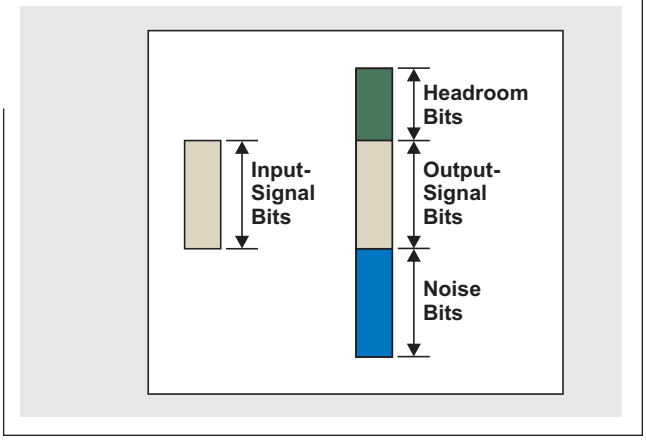
Other than signal and noise bits, additional bits are needed to prevent overflow. These bits are called headroom bits. An end-to-end audio-processing chain will usually preserve the signal level. This means that if a 0-dB signal is input to the signal chain, the output will measure 0 dB or less. (Usually there is a signal compressor that will limit the signal swing to a few decibels below zero.) If boost filters are used to amplify specific signal bands, the remaining bands are usually attenuated to prevent the signal from going above 0 dB. For the latter case, when the input-signal level is at 0 dB (also known as the neutral signal level), the output signal will be lower than 0 dB, and only the amplified bands will reach 0 dB at the output. This will reduce the average volume level of the audio signal.

In spite of the signal level being maintained at 0 dB, the signal can overflow at intermediate processing points. To prevent overflow, headroom bits—i.e., bits in addition to signal and noise bits—are needed.

There can be two sources of overflow:

1. An audio-processing chain can have a filter whose gain (at some specific frequency values) is greater than 0 dB. The filter can be part of a cascaded filter chain (e.g., low-pass, high-pass, and/or band-pass filters) whose overall gain is 0 dB, or it can be a frequency-selective filter that amplifies a specific frequency band relative to the neutral signal level (e.g., shelf and EQ filters). Note that if a real number is represented in 1.n format (where n is the number of fractional bits), the magnitude of the number is always less than 1. So, if a filter with a gain of more than 0 dB (a real number greater than 1) is used, then the output value from the filter is going to overflow if the input value is 0 dB (a real number equal to 1). To prevent overflow in such cases, more headroom bits are needed.

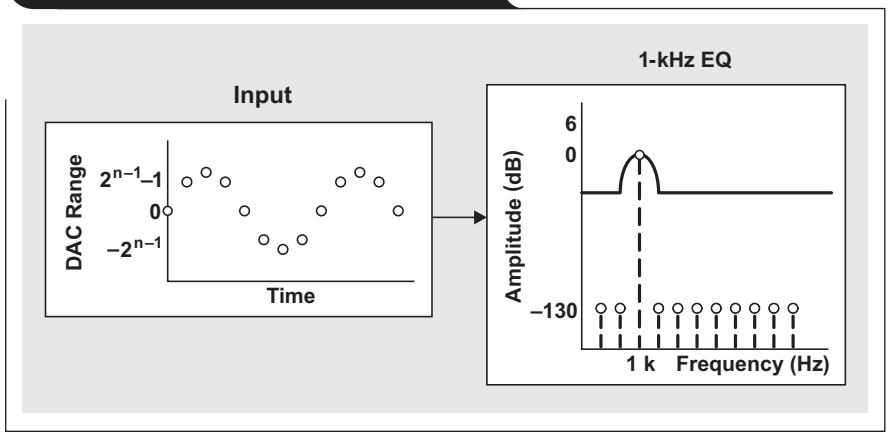
Figure 8. Representation of signal with headroom bits



2. A filter with a gain of less than or equal to 0 dB can have instantaneous real values greater than 1. To ensure that these instantaneous values do not overflow, headroom bits are needed.

A pictorial representation of the signal in the audio processor is shown in Figure 8. An important point to note is that headroom bits are primarily used to accommodate intermediate signal growth. It is expected that at the end of the final processing block, the output will fit within the signal bit width. Otherwise, for low-signal amplitudes, the output will still be within limits and not distort; but, for high-signal amplitudes, the output will get saturated and cause distortion. To prevent distortion, it is best to attenuate the signal prior to the final output.

Figure 9. Scaling the transfer function



Scaling

Scaling can be used to avoid saturation for filters with gain exceeding 0 dB. A boost filter can be used intentionally that will gain a particular frequency. Even a multisection low-pass filter can have a biquad section that actually gains certain frequencies that are higher than the available headroom (the overall response will still be 0 dB). In such a case, whether or not to use scaling can be determined by multiplying the input-signal level by the maximum gain of the total filter response. If the product is greater than the available DAC headroom, then scaling could be used to avoid saturation.

One method of scaling is to attenuate the system's transfer function by an amount equal to the maximum amplitude of the filter's transfer function. The scaling factor can be defined as

$$S = \max\left|H(e^{j\omega})\right|,$$

where $0 \le \omega \le \pi$. A second method is to scale the input signal by S. Figure 9 demonstrates the effect of scaling the transfer function. A full-scale sinusoid is input to the transfer function, which attenuates the flat frequencies by 6 dB. Relative to –6 dBFS, the 1-kHz signal is boosted by 6 dB.

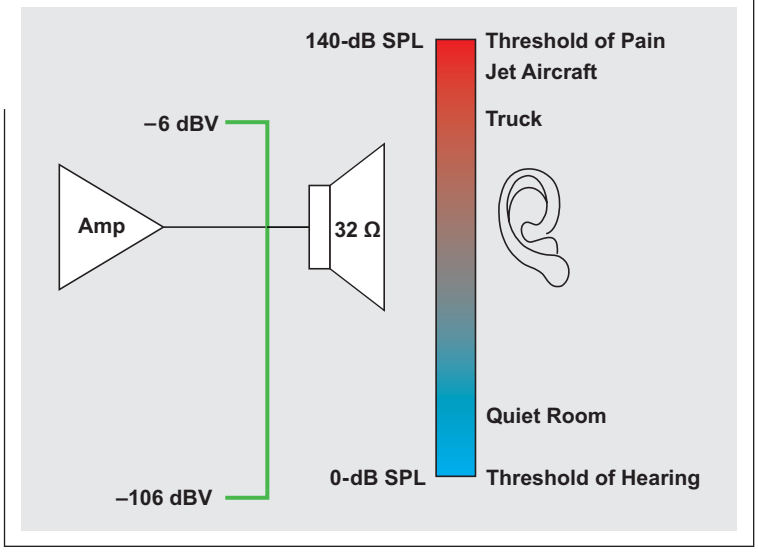
In some cases, due to the filter structure and the instantaneous signal sequences, the output of a filter can be more than 0 dB even though it does not have a gain of more than 0 dB. An FIR filter can increase the gain of a signal by a sum of the absolute value of the filter taps if the individual memory elements are at 0 dB with a sign opposite to that of the taps. The response of the filter may not exceed 0 dB, so additional headroom may be applied. Computing additional headroom for IIR filters is complex because they have feedback elements, and finding a closed-form expression to determine the upper limit for instantaneous gain is complex. In fact, one of the reasons signal processors provide additional headroom (above the DAC limit) is to allow headroom for instantaneous values. Measurements might be needed to compute additional headroom. In some cases, the SNR may need to be traded off for distortion that is due to saturation, and then an analog gain may need to be added to get the signal back to 0 dB.

When scaling is used, it is sometimes desirable to add additional gain (boost) in the analog output stage to compensate. Special care should be taken to ensure that the signal of the boosted regions does not saturate the output amplifiers as well, resulting in a distorted signal. Boost is also provided at the final output stage of the processor to compensate for scaling. This is required for multisection, 0-dB filters where scaling has been done to prevent overflow for one or more of the individual sections. For filters that gain frequencies above 0 dB (EQ and shelf filters), the neutral signal level is scaled below 0 dB. In this case, the final-stage boost is not required. The result is a loss of SNR for the flat regions.

A more elegant solution is to limit the amount of filter gain based upon the volume gain applied at the digital processor, which is very well-suited for headphone use. At higher volume levels, the frequency boost can be lowered and, ultimately, be flat at full volume.

In some cases, the frequency boost is kept constant, while the signal is compressed when the volume is high. This is the anti-clipping dynamic-range compressor (DRC) function: At low volume levels, the original SNR is maintained; but, as volume increases, the scaling is proportionately increased to prevent distortion.

Figure 10. Headphone volume relative to human hearing



Regardless of the method used, it is important to consider how humans perceive sound and noise. Human hearing has an outstanding dynamic range. Headphone amplifiers trade between noise floor and output power to best accommodate this range. For instance, the TLV320AIC3254 audio codec can deliver a very high sound-pressure level (SPL) with just 500 mV_{RMS} into a typical 32-Ω or 16-Ω headphone load, and at the same time can have a noise floor of 100 dB (A-weighted) below full scale, which can be below the threshold of hearing (see Figure 10). Sometimes, it is not even necessary to add additional amplification after scaling is performed, since the output power could be very well above the comfortable listening level.

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www.ti.com/digitalaudio
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Discrete design of a low-cost isolated 3.3- to 5-V DC/DC converter

By Thomas Kugelstadt
Senior Applications Engineer

Isolated 3.3- to 5-V converters are often required in long-distance data-transmission networks, where the bus-node controller operates from a 3.3-V supply to conserve power while the bus voltage is 5 V to maintain signal integrity and to provide high drive capability over long distances. Although isolated DC/DC converter modules for 3.3- to 3.3-V and 5- to 5-V conversion are readily available on the market, 3.3- to 5-V converters in integrated form are still hard to find. Even if a search for the latter proves successful, these specific converters—in particular, those with regulated outputs—often possess long lead times, are relatively expensive, and are usually limited to certain isolation voltages.

A discrete design can be a low-cost alternative to integrated modules if an application requires isolation voltages higher than 2 kV, converter efficiency higher than 60%, or reliable availability of standard components. The drawback of designing a discrete DC/DC converter is that it requires a great deal of work—choosing a stable oscillator structure and break-before-make circuit, selecting good MOSFETs that can be driven efficiently by standard logic gates, and performing temperature and long-term-reliability tests. This entire effort costs time and money. Therefore, before rushing into such a project, the designer should consider the following: Integrated modules have usually passed temperature tests and have met other industrial qualifications. These modules not only represent the most reliable solution but also provide a fast time to market.

Converters with unregulated output are priced at around $4.50 to $5.00 each in quantities of 1000 units, while converters with regulated output often cost twice as much, approximately $10.00 or more. Thus, it makes sense to purchase a converter with unregulated output and either buffer the output with bulk capacitance or feed it into a low-cost, low-dropout regulator (LDO) such as the Texas Instruments (TI) TPS76650 at around $0.50.

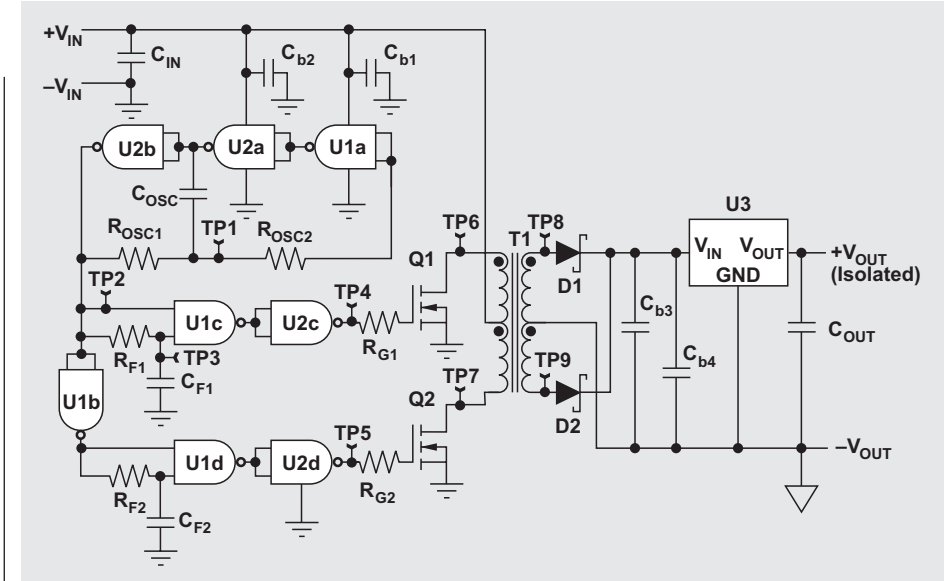
The discrete DC/DC converter design in Figure 1 uses only readily available, standard components (such as logic ICs and MOSFETs) for the transformer driver and an LDO for a regulated output voltage. While this circuit has been prototyped with through-hole components, thus making its form factor larger than that of integrated modules, the board space can be drastically reduced by using TI's Little Logic™ devices.

The main benefits of this design are its low bill of material (BOM) and the freedom to choose an isolation transformer for isolation voltages ranging from 1 to 6 kV. The goal is to offer a low-cost alternative to fully integrated DC/DC converters with regulated outputs, and to stand-alone transformer drivers (usually priced at around $1.80), by making the transformer-driver stage as inexpensive as possible.

Operation principle

Low-cost, isolated DC/DC converters are commonly of the push-pull driver type. The operation principle is fairly simple. A square-wave oscillator with a push-pull output stage drives a center-tapped transformer, whose output is rectified and made available in regulated or unregulated DC form. An important, functional requirement is that the square wave must have a 50% duty cycle to ensure

Figure 1. Isolated 3.3- to 5-V push-pull converter



symmetrical magnetization of the transformer core. Another requirement is that the product of magnetizing voltage (E) and magnetizing time (T), known as the ET product and measured in Vμs, must not exceed the transformer's characteristic ET product specified by its manufacturer. A break-before-make circuit following the oscillator must also be implemented to prevent the two legs of the push-pull output stage from conducting simultaneously and causing a circuit failure.

The discrete design

The well-known three-inverter-gate oscillator, consisting of U1a, U2a, and U2b, has been chosen because it is stable with supply variations. Its nominal frequency is set to 330 kHz through a 100-pF ceramic capacitor (C_{OSC}) and two 10-kΩ resistors (R_{OSC1} and R_{OSC2}). The oscillator possesses a duty cycle of close to 50% and a maximum frequency variation of less than ±1.5% across a 3.0- to 3.6-V variation in supply voltage. Figure 2 shows the waveforms at the summing point of R_{OSC1} and R_{OSC2} (TP1) and at the oscillator output (TP2). All voltages are measured with respect to circuit ground.

Two Schmitt-trigger NAND gates (U1c, U1d) perform a break-before-make function to avoid overlapping of the MOSFET's conducting phases. Two other NAND gates (U2c, U2d) are configured as inverting buffers, generating the correct signal polarity necessary to drive the n-channel MOSFETs (Q1, Q2). The complete break-before-make action is shown in Figure 3. To accommodate the limited drive capability of standard logic gates, the MOSFETs have been selected for their low total charge and their fast response times.

The isolation transformer (T1) has a secondary-to-primary winding ratio of 2:1, a primary inductance of 0.9 mH, and a guaranteed isolation voltage of 3 kV. The input and output waveforms of the transformer are shown in Figure 4.

Figure 2. Oscillator waveforms at TP1 and TP2

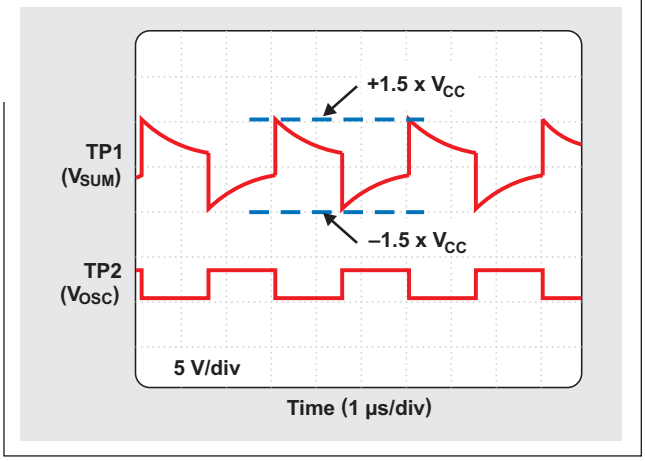


Figure 3. Break-before-make waveforms

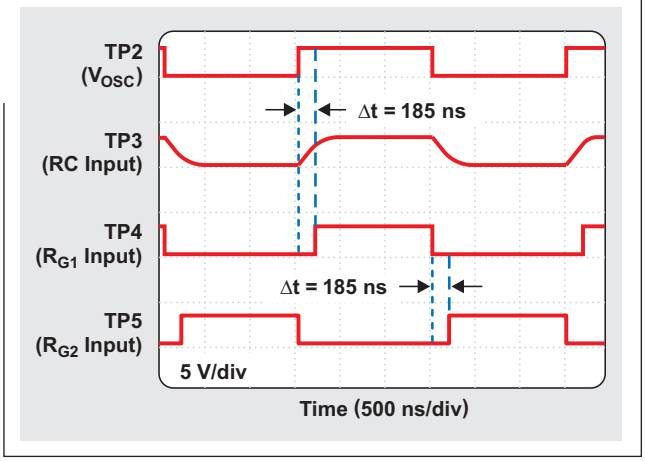
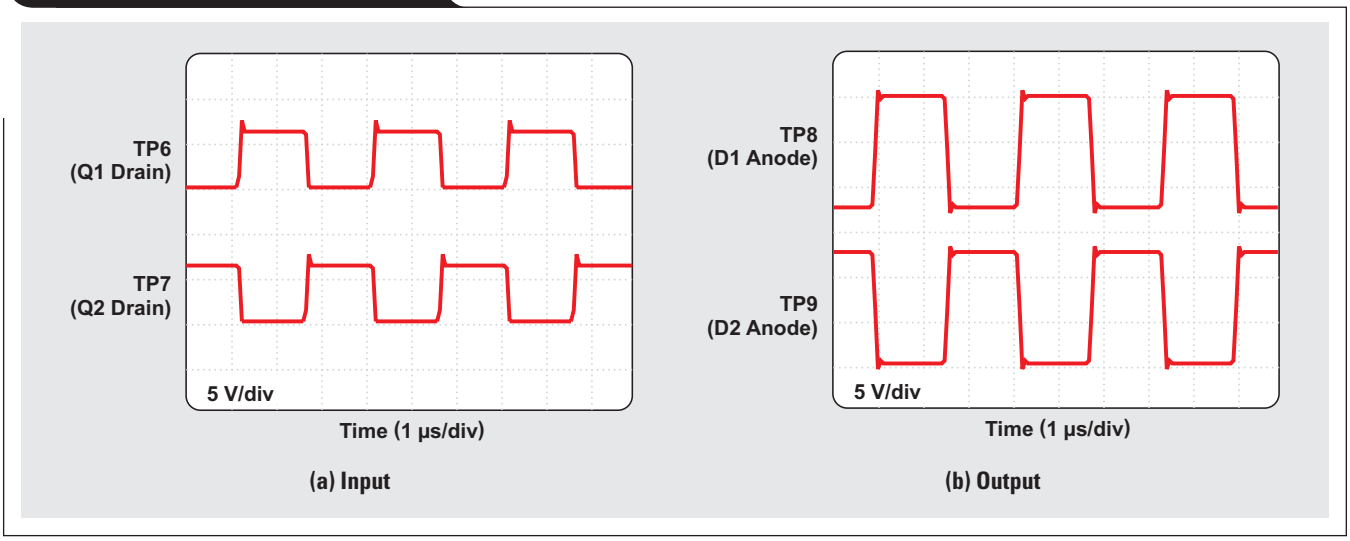


Figure 4. Transformer waveforms



The two diodes (D1, D2) are fast Schottky rectifiers performing a full-wave rectification while providing low forward voltage at full load current (V_{FW} < 0.4 V at 200 mA). It is possible to take the output voltage directly from a bulk capacitor (Cb3) following the diodes. In this case, the output is unregulated but provides the maximum efficiency of the DC/DC converter. However, the designer must ensure that the maximum supply of the affected circuitry is not exceeded, which can easily occur under low-load or open-circuit conditions. If the unregulated output voltage under minimum load proves to be too high, it is necessary to use a linear regulator after the full-wave rectifier to provide a stable output supply.

The main benefit of a linear regulator is the low ripple output. Other benefits include short-circuit protection and overtemperature shutdown. The main drawback, however, is a significantly reduced efficiency.

Figure 5 shows the ripple of the circuit in Figure 1 at an output voltage of 4.93 V, and Figure 6 compares the circuit's efficiency with that of an integrated DC/DC module with regulated output.

Table 1 on the next page provides an approximate BOM for the discrete converter. Note that the values of the bypass capacitors are larger than the 10 nF commonly implemented in low-speed applications. This is because high-speed CMOS technologies such as AHC, AC, and LVC possess high dynamic loading, so the values for bypass capacitors must be 0.1 µF or higher to assure proper operation. This is of particular importance for the inverter buffers driving the MOSFETs, where the bypass capacitor is 0.68 µF.

Conclusion

Where board-space constraints are not an issue, the discrete design of an isolated 3.3- to 5-V DC/DC converter with regulated output can present a viable low-cost alternative to an integrated DC/DC module with regulated output. A major benefit of the discrete design is the freedom to choose an isolation transformer for varying isolation-voltage requirements.

Related Web sites

power.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with SN74AC00, SN74AHC132, or TPS76650

Figure 5. Output ripple at V_{OUT} = 4.93 V

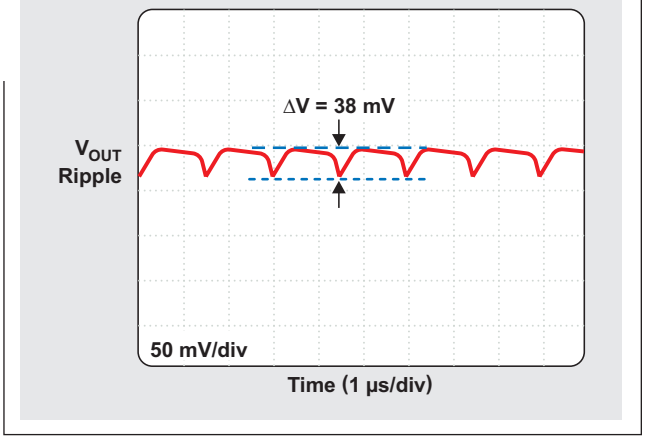


Figure 6. Efficiency comparison

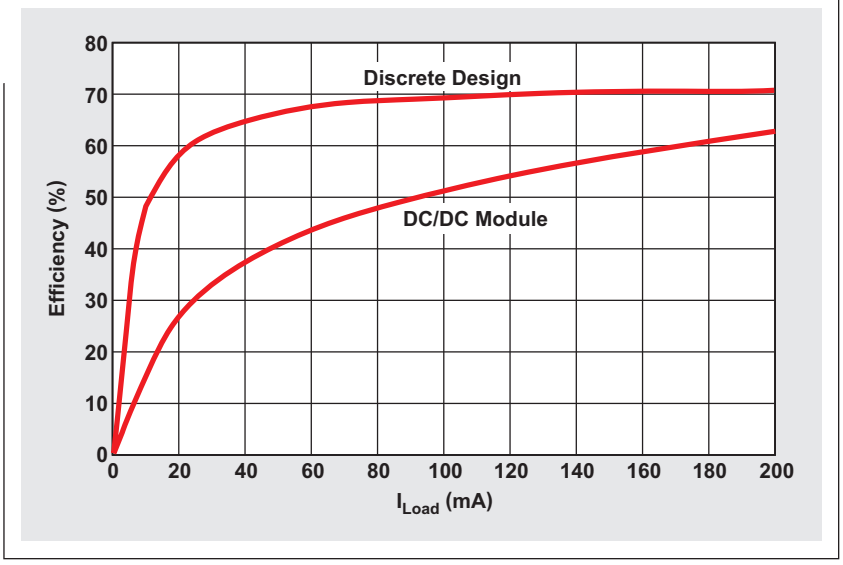


Table 1. BOM for discrete DC/DC converter

DEVICE LABEL	PART NUMBER OR VALUE	DESCRIPTION	COMPONENT PRICE* (EACH)	QUANTITY	TOTAL PRICE*	TRANSFORMER DRIVER PRICE*
U1	SN74AHC132	Quad Schmitt-trigger NAND	0.17	1	0.17	0.17
U2	SN74AC00	Quad NAND	0.17	1	0.17	0.17
U3	TPS76650	250-mA LDO	0.53	1	0.53	—
Q1, Q2	FDN335	n-channel power MOSFET	0.105	2	0.21	0.21
R_{OSC1}, R_{OSC2}	10 kΩ	OSC resistor	0.04	2	0.08	0.07
R_{F1}, R_{F2}	1.54 kΩ	Delay resistor	0.035	2	0.07	0.07
R_{G1}, R_{G2}	150 Ω	Gate-drive resistor	0.035	2	0.07	0.07
C_{OSC}	100 pF	Oscillator capacitor	0.04	1	0.04	0.04
C_{F1}, C_{F2}	47 pF	Delay capacitor	0.04	2	0.08	0.08
C_{b1}	0.1 µF	Bypass capacitor	0.02	3	0.06	0.02
C_{b2}	0.68 µF	Bypass capacitor	0.03	1	0.03	0.03
C_{b3}	0.1 µF	LDO input capacitor	0.02	1	0.02	—
C_{IN}, C_{b4}, C_{OUT}	4.7 µF	Bulk capacitor	0.12	3	0.36	0.12
D1, D2	MBR0520L	Schottky diode	0.045	2	0.09	—
T1	TGRTI-360NARL	1:2 transformer, 3 kV	2.31	1	2.31	—
				TOTAL	**4.28**	**1.09**

*Typical price in U.S. dollars in quantities of 1000 units.

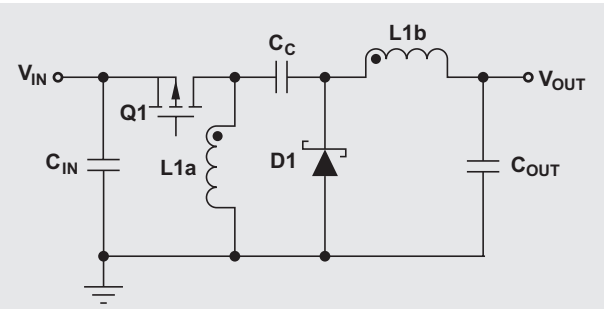
Designing DC/DC converters based on ZETA topology

By Jeff Falin
Senior Applications Engineer

Introduction

Similar to the SEPIC DC/DC converter topology, the ZETA converter topology provides a positive output voltage from an input voltage that varies above and below the output voltage. The ZETA converter also needs two inductors and a series capacitor, sometimes called a flying capacitor. Unlike the SEPIC converter, which is configured with a standard boost converter, the ZETA converter is configured from a buck controller that drives a high-side PMOS FET. The ZETA converter is another option for regulating an unregulated input-power supply, like a low-cost wall wart. To minimize board space, a coupled inductor can be used. This article explains how to design a ZETA converter running in continuous-conduction mode (CCM) with a coupled inductor.

Figure 1. Simple circuit diagram of ZETA converter



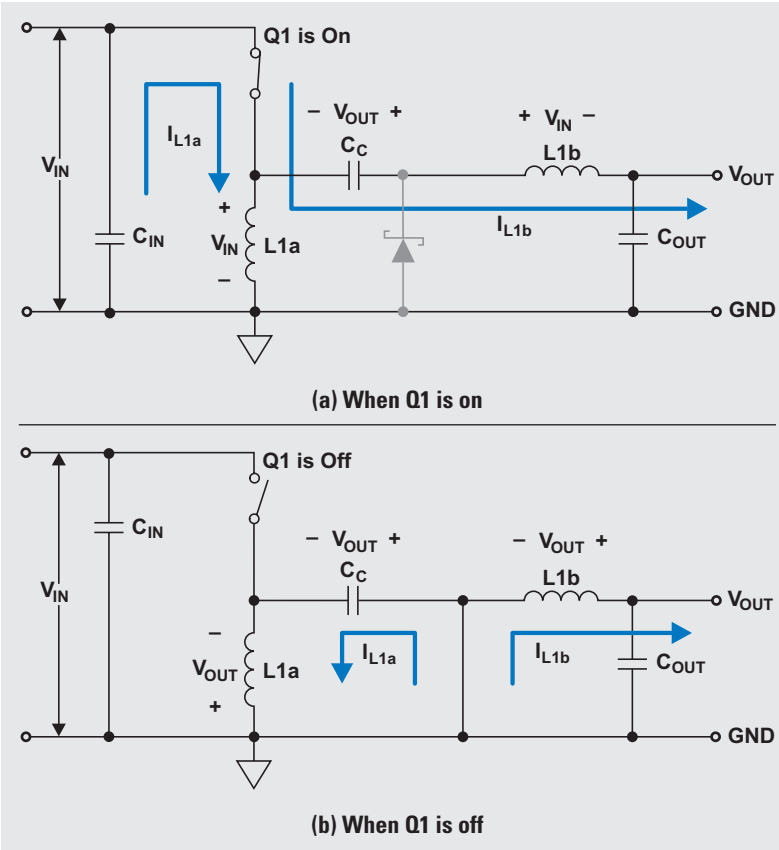
Basic operation

Figure 1 shows a simple circuit diagram of a ZETA converter, consisting of an input capacitor, C_{IN}; an output capacitor, C_{OUT}; coupled inductors L1a and L1b; an AC coupling capacitor, C_C; a power PMOS FET, Q1; and a diode, D1. Figure 2 shows the ZETA converter operating in CCM when Q1 is on and when Q1 is off.

To understand the voltages at the various circuit nodes, it is important to analyze the circuit at DC when both switches are off and not switching. Capacitor C_C will be in parallel with C_{OUT}, so C_C is charged to the output voltage, V_{OUT}, during steady-state CCM. Figure 2 shows the voltages across L1a and L1b during CCM operation.

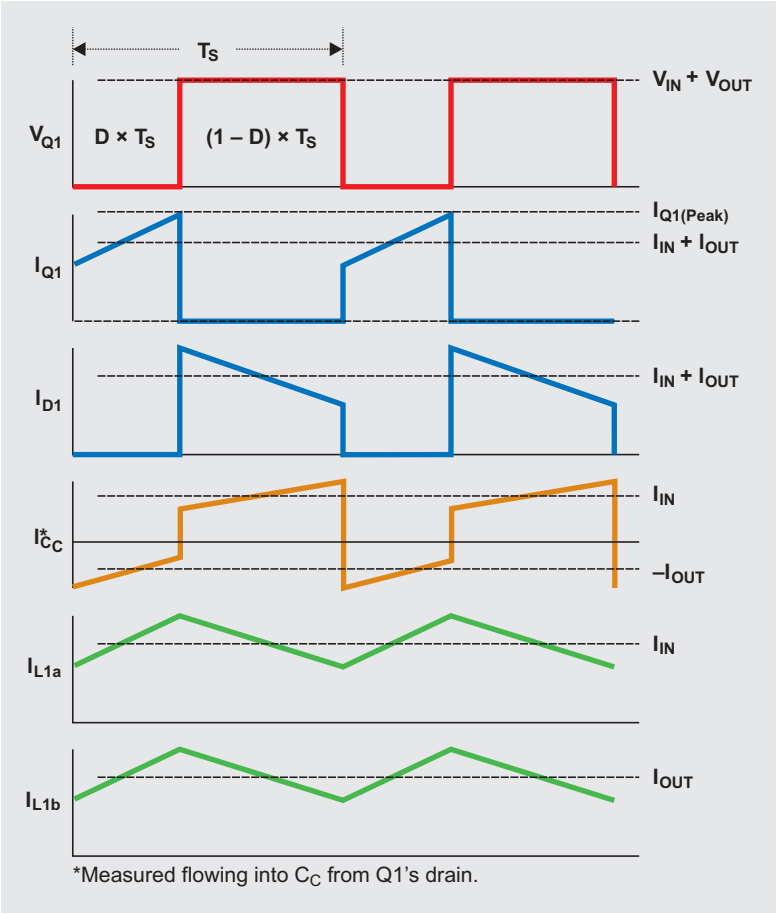
When Q1 is off, the voltage across L1b must be V_{OUT} since it is in parallel with C_{OUT}. Since C_{OUT} is charged to V_{OUT}, the voltage across Q1 when Q1 is off is $V_{IN} + V_{OUT}$; therefore the voltage across L1a is $-V_{OUT}$ relative to the drain of Q1. When Q1 is on, capacitor C_C, charged to V_{OUT}, is connected in series with L1b; so the voltage across L1b is $+V_{IN}$, and diode D1 sees $V_{IN} + V_{OUT}$.

Figure 2. ZETA converter during CCM operation



The currents flowing through various circuit components are shown in Figure 3. When Q1 is on, energy from the input supply is being stored in L1a, L1b, and C_C. L1b also provides I_{OUT}. When Q1 turns off, L1a's current continues to flow from current provided by C_C, and L1b again provides I_{OUT}.

Figure 3. ZETA converter's component currents during CCM



Duty cycle

Assuming 100% efficiency, the duty cycle, D, for a ZETA converter operating in CCM is given by

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}}. \quad (1)$$

This can be rewritten as

$$\frac{D}{1-D} = \frac{I_{IN}}{I_{OUT}} = \frac{V_{OUT}}{V_{IN}}. \quad (2)$$

D_{max} occurs at $V_{IN(min)}$, and D_{min} occurs at $V_{IN(max)}$.

Selecting passive components

One of the first steps in designing any PWM switching regulator is to decide how much inductor ripple current, $\Delta I_{L(PP)}$, to allow. Too much increases EMI, while too little may result in unstable PWM operation. A rule of thumb is to assign a value for K between 0.2 and 0.4 of the average input current. A desired ripple current can be calculated as follows:

$$\text{Desired } \Delta I_{L(PP)} = K \times I_{IN} = K \times I_{OUT} \times \frac{D}{1-D}. \quad (3)$$

In an ideal, tightly coupled inductor, with each inductor having the same number of windings on a single core, the coupling forces the ripple current to be split equally between the two coupled inductors. In a real coupled inductor, the inductors do not have equal inductance and the ripple currents will not be exactly equal. Regardless, for a desired ripple-current value, the inductance required in a coupled inductor is estimated to be half of what would be needed if there were two separate inductors, as shown in Equation 4:

$$L1a_{min} = L1b_{min} = \frac{1}{2} \times \frac{V_{IN} \times D}{\Delta I_{L(PP)} \times f_{SW(min)}} \quad (4)$$

To account for load transients, the coupled inductor's saturation current rating needs to be at least 1.2 times the steady-state peak current in the high-side inductor, as computed in Equation 5:

$$I_{L1a(PK)} = I_{OUT} \times \frac{D}{1-D} + \frac{\Delta I_L}{2} \quad (5)$$

Note that $I_{L1b(PK)} = I_{OUT} + \Delta I_L/2$, which is less than $I_{L1a(PK)}$.

Like a buck converter, the output of a ZETA converter has very low ripple. Equation 6 computes the component of the output ripple voltage that is due solely to the capacitance value:

$$\Delta V_{C_{OUT}(PP)} = \frac{\Delta I_{L1b(PP)} \text{ [at } V_{IN(max)}]}{8 \times C_{OUT} \times f_{SW(min)}}, \quad (6)$$

where $f_{SW(min)}$ is the minimum switching frequency. Equation 7 computes the component of the output ripple voltage that is due solely to the output capacitor's ESR:

$$\Delta V_{ESR\_C_{OUT}(PP)} = \Delta I_{L1b(PP)} \text{ [at } V_{IN(max)}] \times ESR_{C_{OUT}} \quad (7)$$

Note that these two ripple-voltage components are phase-shifted and do not directly add together. For low-ESR (e.g., ceramic) capacitors, the ESR component can be ignored. A minimum capacitance limit may be necessary to meet the application's load-transient requirement.

The output capacitor must have an RMS current rating greater than the capacitor's RMS current, as computed in Equation 8:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L1b(PP)} \text{ [at } V_{IN(max)}]}{\sqrt{3}} \quad (8)$$

The input capacitor and the coupling capacitor source and sink the same current levels, but on opposite switching cycles. Similar to a buck converter, the input capacitor and the coupling capacitor need the RMS current rating,

$$I_{C_{IN}(RMS)} = I_{C_C(RMS)} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN(min)}}}. \quad \textbf{(9)}$$

Equations 10a and 10b compute the component of the output ripple voltage that is due solely to the capacitance value of the respective capacitors:

$$\Delta V_{C_{IN}(PP)} = \frac{D_{max} \times I_{OUT}}{C_{IN} \times f_{SW(min)}} \quad \textbf{(10a)}$$

$$\Delta V_{C_C(PP)} = \frac{D_{max} \times I_{OUT}}{C_C \times f_{SW(min)}} \quad \textbf{(10b)}$$

Equations 11a and 11b compute the component of the output ripple voltage that is due solely to the ESR value of the respective capacitors:

$$\begin{aligned}\Delta V_{ESR\_C_{IN}(PP)} &= (I_{IN(max)} + I_{OUT}) \times ESR_{C_{IN}} \\ &= \frac{I_{OUT}}{1 - D_{max}} \times ESR_{C_{IN}}\end{aligned} \quad \textbf{(11a)}$$

$$\begin{aligned}\Delta V_{ESR\_C_C(PP)} &= (I_{IN(max)} + I_{OUT}) \times ESR_{C_C} \\ &= \frac{I_{OUT}}{1 - D_{max}} \times ESR_{C_C}\end{aligned} \quad \textbf{(11b)}$$

Again, the two ripple-voltage components are phase-shifted and do not directly add together; and, for low-ESR capacitors, the ESR component can again be ignored. A typical ripple value is less than 0.05 times the input voltage for the input capacitor and less than 0.02 times the output voltage for the coupling capacitor.

Selecting active components

The power MOSFET, Q1, must be carefully selected so that it can handle the peak voltage and currents while minimizing power-dissipation losses. The power FET's current rating will determine the ZETA converter's maximum output current.

As shown in Figure 3, Q1 sees a maximum voltage of $V_{IN(max)} + V_{OUT}$. Q1 must have a peak-current rating of

$$I_{Q1(PK)} = I_{L1a(PK)} + I_{L1b(PK)} = I_{IN} + I_{OUT} + \Delta I_L. \quad \textbf{(12)}$$

At the ambient temperature of interest, the FET's power-dissipation rating must be greater than the sum of the conductive losses (a function of the FET's $r_{DS(on)}$) and the switching losses (a function of the FET's gate charge) as given in Equation 13:

$$\begin{aligned}P_{D\_Q1} &= P_{r_{DS(on)}} + P_{SWG} + P_{Gate} \\ &= I^2_{Q1(RMS)} \times r_{DS(on)} \\ &+ (V_{IN(max)} + V_{OUT}) \times I_{Q1(PK)} \times Q_{GD} / I_{Gate} \times f_{SW(max)} \\ &+ V_{Gate} \times Q_G \times f_{SW(max)},\end{aligned} \quad \textbf{(13)}$$

where Q_{GD} is the gate-to-drain charge, Q_G is the total gate charge of the FET, I_{Gate} is the maximum drive current, and V_{Gate} is the maximum gate drive from the controller. Q1's RMS current is

$$\begin{aligned}I_{Q1(RMS)} &= (I_{IN(max)} + I_{OUT}) \times \sqrt{D_{max}} \\ &= \frac{I_{OUT} \times V_{OUT}}{V_{IN(min)} \times \sqrt{D_{max}}}.\end{aligned} \quad \textbf{(14)}$$

The output diode must be able to handle the same peak current as Q1, $I_{Q1(PK)}$. The diode must also be able to withstand a reverse voltage greater than Q1's maximum voltage ($V_{IN(max)} + V_{OUT}$) to account for transients and ringing. Since the average diode current is the output current, the diode's package must be capable of dissipating up to $I_{OUT} \times V_{FWD}$, where V_{FWD} is the Schottky diode's forward voltage at I_{OUT}.

Loop design

The ZETA converter is a fourth-order converter with multiple real and complex poles and zeroes. Unlike the SEPIC converter, the ZETA converter does not have a right-half-plane zero and can be more easily compensated to achieve a wider loop bandwidth and better load-transient results with smaller output-capacitance values. Reference 1 provides a good mathematical model based on state-space averaging. The model excludes inductor DC resistance (DCR) but includes capacitor ESR. Even though the converter in Reference 1 uses ceramic capacitors, for the following design example, the inductor DCR was substituted for the capacitor ESR so that the model would more closely match measured values. The open-loop gain bandwidth (i.e., the frequency where the gain crosses zero with an acceptable phase margin of typically 45°), should be greater than the resonant frequency of L1b and C_C so that the feedback loop can dampen the nonsinusoidal ripple on the output with fundamental frequency at that resonant frequency.

Design example

For this example, the requirements are for a 12-V, 1-W supply with $\eta = 0.9$ peak efficiency. The load is steady-state, so few load transients are expected. The 2-A input supply is 9 to 15 V. A nonsynchronous voltage-mode controller, the Texas Instruments TPS40200, was selected, running with a switching frequency between 340 and 460 kHz. The maximum allowed ripple at the input and flying capacitor is respectively 1% of the maximum voltage across each. The maximum output ripple is 25 mV, and the maximum ambient temperature is 55°C. Because EMI is not a concern, an inductor with a lower inductance value was selected by using the minimum input voltage. Table 1 on the next page summarizes the design calculations given earlier. Equations 7 through 9 and Equation 11 were ignored because low-ESR ceramic capacitors with high RMS current ratings were used.

Table 1. Computations for example ZETA-converter design

BASED ON DESIGN EQUATION	COMPUTATION (ASSUMING $\eta = 1$)	ADJUSTED FOR $\eta = 0.9$	SELECTED COMPONENT/RATING
Passive Components			
(1)	$D_{max} = \frac{12\ V}{12\ V + 9\ V} = 0.57$	N/A	N/A
(1)	$D_{min} = \frac{12\ V}{12\ V + 15\ V} = 0.44$	N/A	N/A
(2)	$I_{IN(max)} = 1\ A \times \frac{0.57}{1 - 0.57} = 1.33\ A$	$\frac{1.33\ A}{0.9} = 1.48\ A$	N/A
(3)	Desired $\Delta I_{L(PP)}$ [at $V_{IN(min)}$] $= 0.3 \times 1.33\ A = 0.4\ A$	$\frac{0.4\ A}{0.9} = 0.44\ A$	N/A
(4) using $V_{IN(min)}$	$L1a = L1b = \frac{1}{2} \times \frac{9\ V \times 0.57}{0.40\ A \times 340\ kHz} = 18.9\ \mu H$	$18.9\ \mu H \times 0.9 = 17.0\ \mu F$	Coilcraft MSD1260: 22 µH – I_{RMS} = 1.76 A in each winding simultaneously, I_{SAT} = 5 A
(4) at $V_{IN(min)}$	Actual $\Delta I_{L(PP)} = \frac{1}{2} \times \frac{9\ V \times 0.57}{22\ \mu H \times 340\ kHz} = 0.34\ A$	N/A	
(5)	$I_{L1a(PK)} = 1.33\ A + \frac{0.34\ A}{2} = 1.50\ A$	$1.48\ A + \frac{0.34\ A}{2} = 1.65\ A$	
(4) at $V_{IN(max)}$	Actual $\Delta I_{L(PP)} = \frac{1}{2} \times \frac{15\ V \times 0.44}{22\ \mu H \times 340\ kHz} = 0.45\ A$	N/A	N/A
(6)	$C_{OUT(min)} = \frac{0.44\ A}{8 \times 0.025\ V \times 340\ kHz} = 6.5\ \mu F$	N/A	Two 10-µF, 25-V X5R ceramics and one 4.7-µF, 25-V X5R ceramic to provide good load-transient response and to accommodate ceramic capacitor derating
(10a) for C_{IN}	$C_{IN(min)} = \frac{0.57 \times 1\ A}{0.01 \times 15\ V \times 340\ kHz} = 11.2\ \mu F$	$\frac{11.2\ \mu F}{0.9} = 12.4\ \mu F$	Two 10-µF, 25-V X5R ceramics and one 4.7-µF, 25-V X5R ceramic to accommodate ceramic capacitor derating
(10b) for C_C	$C_{C(min)} = \frac{0.57 \times 1\ A}{0.01 \times 12\ V \times 340\ kHz} = 14\ \mu F$	$\frac{14\ \mu F}{0.9} = 15.6\ \mu F$	Three 10-µF, 25-V X5R ceramics to accommodate ceramic capacitor derating
Active Components			
(12)	$I_{Q1(PK)} = 1.33\ A + 1\ A + 0.34\ A = 2.67\ A$	$1.48\ A + 1\ A + 0.34\ A = 2.82\ A$	N/A
(14)	$I_{Q1(RMS)} = \frac{1\ A \times 12\ V}{9\ V \times \sqrt{0.57}} = 1.77\ A$	$\frac{1.77\ A}{0.9} = 1.96\ A$	Fairchild FDC365P: –35-V, –4.3-A, 55-mΩ PFET
(13)	$P_{D\_Q1} = (1.96\ A)^2 \times 55\ m\Omega + (15\ V + 12\ V) \times 2.82\ A \times 2.2\ nC / 0.3\ A \times 460\ kHz + 8\ V \times 15\ nC \times 460\ kHz = 0.54\ W$	Included	
—	$P_{D\_D1} = 1\ A \times 0.5\ V = 0.5\ W$	N/A	MBRS340: 40 V, 3 A, SMC

Figure 4. ZETA-converter design with 9- to 15-V V_{IN} and 12-V V_{OUT} at 1 A

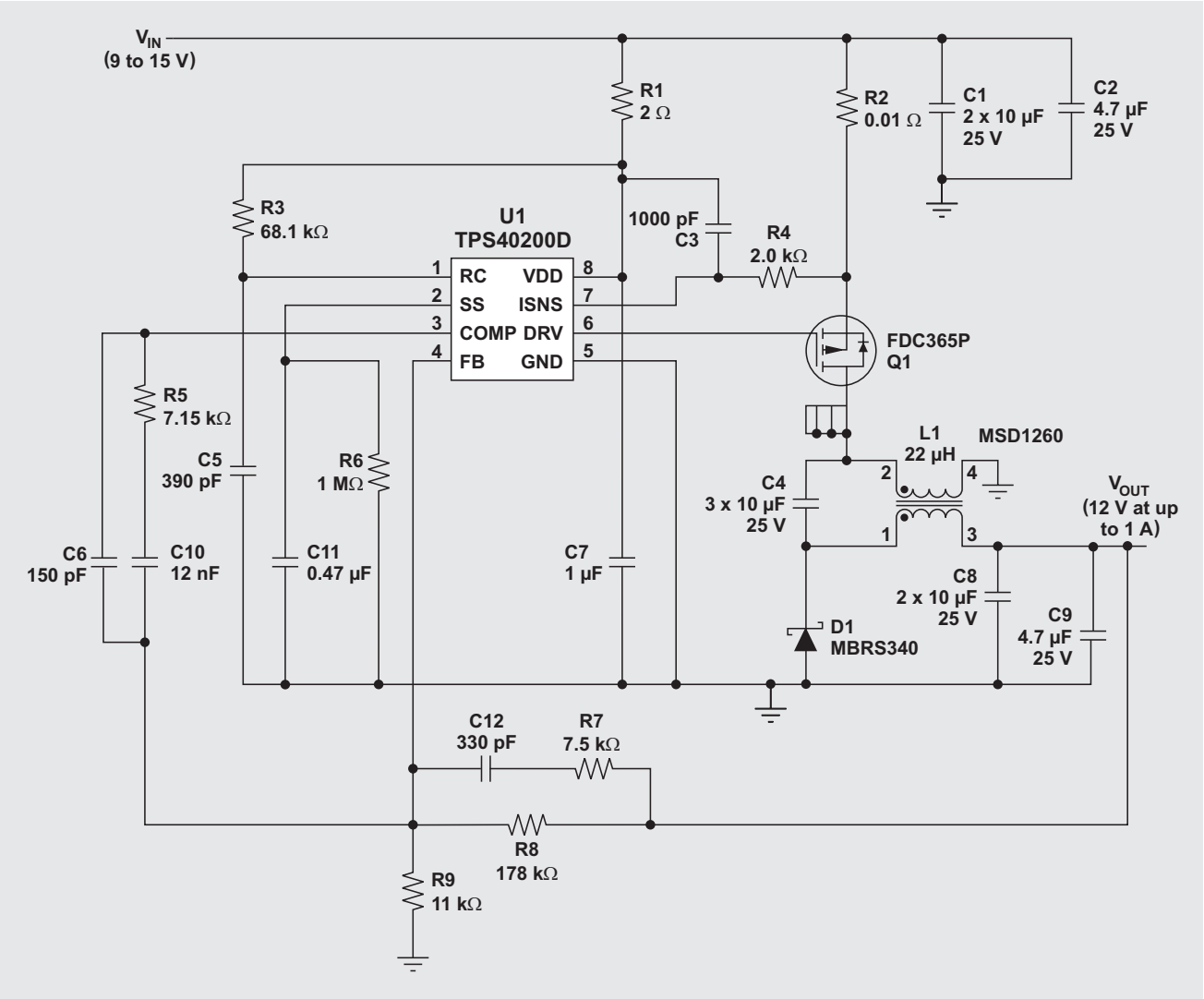
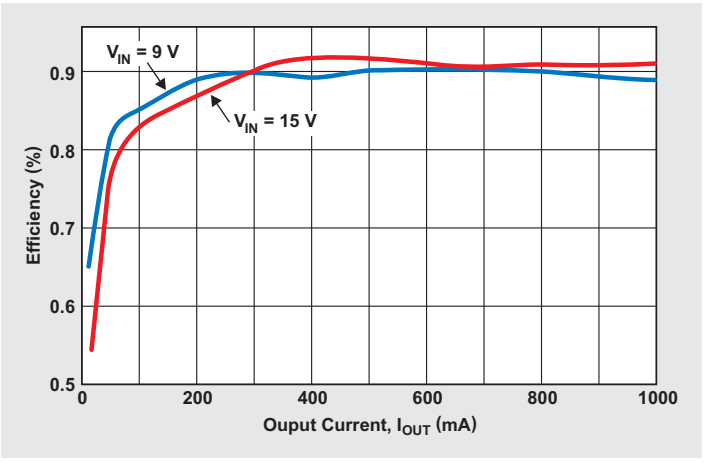


Figure 4 shows the schematic and Figure 5 the efficiency of the ZETA converter. On the next page, Figure 6 shows the converter's operation in deep CCM, and Figure 7 shows the loop response.

Conclusion

Like the SEPIC converter, the ZETA converter is another converter topology to provide a regulated output voltage from an input voltage that varies above and below the output voltage. The benefits of the ZETA converter over the SEPIC converter include lower output-voltage ripple and easier compensation. The drawbacks are the requirements for a higher input-voltage ripple, a much larger flying capacitor, and a buck controller (like the TPS40200) capable of driving a high-side PMOS.

Figure 5. Efficiency of example ZETA-converter design



Reference

1. Eng Vuthchhay and Chanin Bunlaksananusorn, "Dynamic modeling of a zeta converter with state-space averaging technique," *Proc. 5th Int. Conf. Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON) 2008,* Vol. 2, pp. 969–972.

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS40200

Figure 6. Operation at V_{IN} = 9 V and I_{OUT} = 1 A

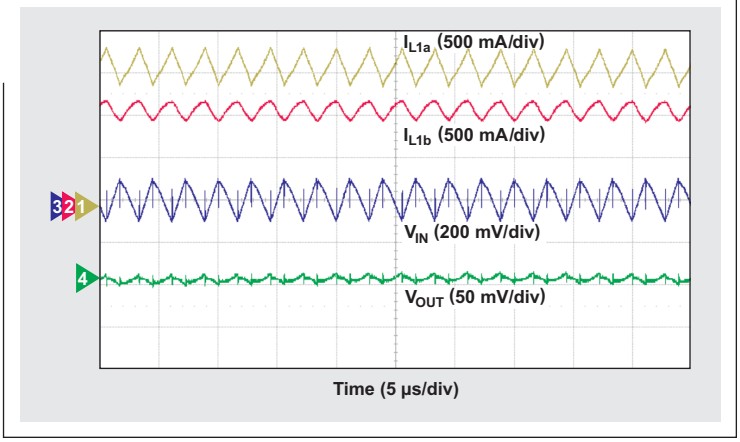
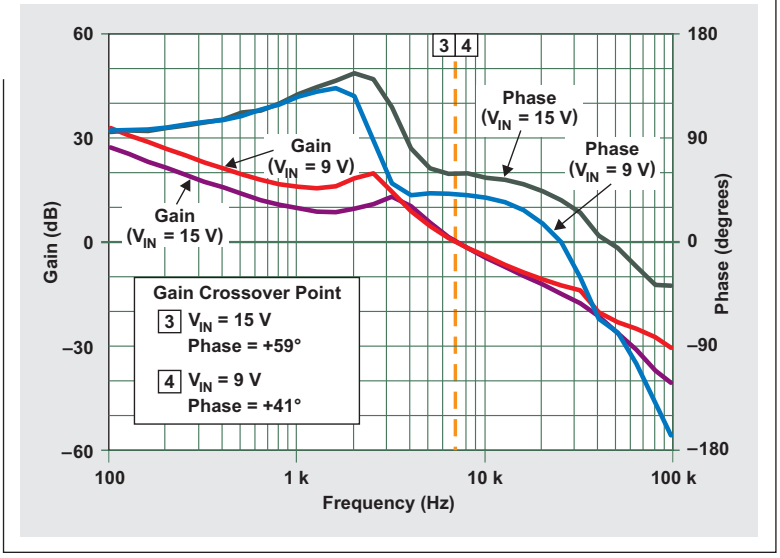


Figure 7. Loop response at V_{IN} = 9 V and 15 V, and I_{OUT} = 1 A



Precautions for connecting APA outputs to other devices

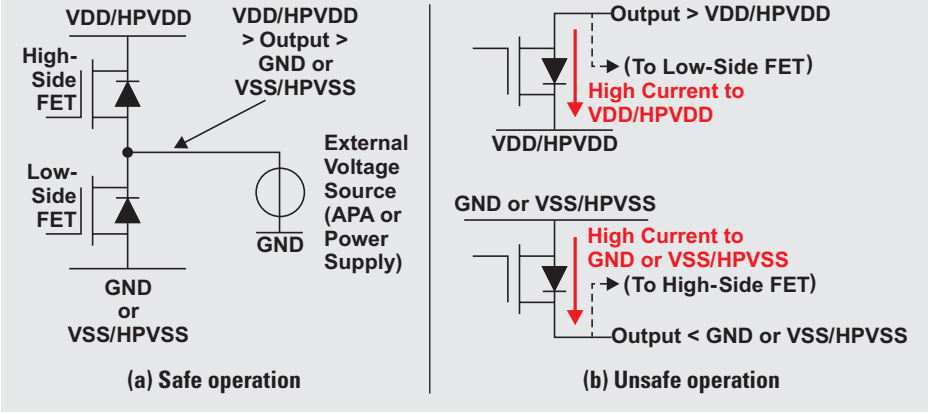
By Stephen Crump
Applications Engineer, Audio Power Amplifiers, Audio and Imaging Products

Multiple audio power amplifiers (APAs) may be connected to one output circuit by design, to multiplex different sources or to connect an external amplifier to save battery life. Also, one amplifier output may be connected to another or to a power supply by mistake. Any of these connections can force APA outputs to abnormal voltages, and this can damage an APA. This article explains limits that must be observed to avoid such damage.

Damage can occur whether an APA is active or shut down. The output of most APAs is protected with short-circuit protection (SCP) or overcurrent protection (OCP) when the APA is active, but the range of voltages the APA can tolerate is still the same. Generally, voltage forced into an APA output must be limited as follows to avoid APA damage:

- An APA output should not be forced more than 0.3 V above the APA's positive power-supply voltage (VDD or VCC), or more than –0.3 V below its negative power-supply voltage (ground or VSS).
- An APA output must never be forced beyond the Absolute Maximum Ratings for supply voltages given in the APA's data sheet.

Figure 1. Current conduction in forward-biased body diodes



How APAs respond to voltages forced into their outputs

When shut down, APAs have different resistances at their outputs, ranging from a few ohms to several kilohms to high impedance. If an external audio source connected to an APA output can drive the resistance there, it will force its voltage at the APA output.

When active, most class-AB devices have continuous-current limiting for SCP. This kind of APA holds its output at its intended output voltage until it is forced into SCP or OCP by the other source. Then it continues to draw its limit current, but its output voltage is controlled by the other source. If the APA continues to draw its limit current, it may overheat and go into thermal shutdown. Then its output voltage is controlled entirely by the other source. When the APA cools down enough, it will turn on again, and this cycle will continue as long as the external source is connected.

A typical Class-D APA holds its output at its intended output voltage until it is forced into SCP or OCP. Then it shuts down and its output voltage is controlled by the other source, without drawing significant current, as long as proper voltage limits are observed. A class-D APA with cycle-by-cycle OCP generally behaves like a continuous-current limiter until it shuts down.

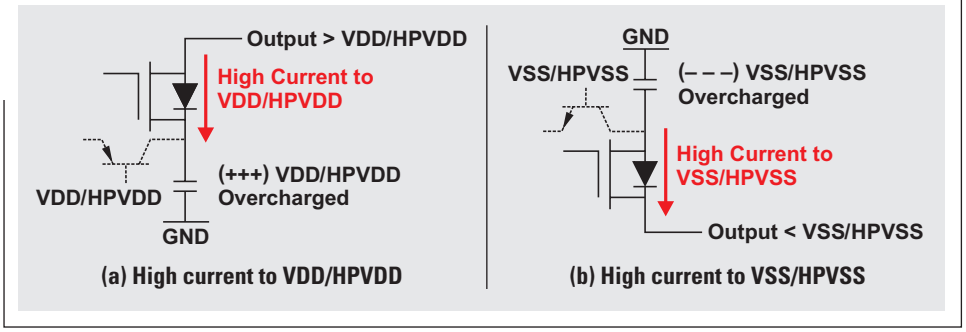
How damage occurs

If another source is connected to an APA output when it is shut down, it will force the APA output to follow its voltage. If the APA is active and the other source can supply enough current to force the APA into SCP or OCP, the other source will then force the APA output to follow its voltage. There are several different ways in which damage can be done.

Forward-biased body diode

Single-supply APAs operate between a positive power supply, usually called VDD or VCC, and ground. Output devices are FETs with body diodes that are reverse-biased in normal operation. Body diodes that are reverse-biased in normal operation (see Figure 1) can be damaged if one of the diodes becomes forward-biased and conducts excessive current. This can happen if an output of a single-supply APA is forced more than 0.3 V above VDD (or VCC) or more than –0.3 V below ground.

Figure 2. Pushing APA supply voltages beyond their limits



Texas Instruments (TI) DirectPath™ APAs operate between a positive power supply, usually called VDD, and a negative rail, usually called VSS, often generated from VDD with a switching circuit. The magnitude of VSS is generally less than the magnitude of VDD. Some DirectPath APAs regulate primary VDD to a lower level for their outputs, HPVDD, and generate a negative rail, HPVSS, from HPVDD, to control maximum output power. If an output of a DirectPath APA is forced more than 0.3 V above VDD/HPVDD or more than –0.3 V below VSS/HPVSS, one of the body diodes may become forward-biased and conduct excessive current, which can damage the diode.

Power-supply overvoltage

Even if external source currents do not damage a body diode, they may flow to VDD/HPVDD or VSS/HPVSS (see Figure 2). VDD/HPVDD and VSS/HPVSS typically only source current, so the diode currents may charge the supply voltages beyond their absolute maximum ratings and in turn may damage the APA and/or the supply components.

Table 1 may be helpful in understanding the different supplies for various DirectPath APAs. Supplies for devices not included here can be determined by comparing their data-sheet information to this table. Supply labels may be different from the labels shown in the table.

Related Web sites

www.ti.com/audio

www.ti.com/sc/device/*partnumber*

Replace *partnumber* with TPA4411, TPA6130A2, TPA6132A2, or TPA6136A2

Table 1. Comparison of supply-voltage limits for APA devices*

DEVICE	TPA4411	TPA6130A2	TPA6132A2	TPA6136A2
Positive Supply Voltage	SVDD = 1.8 to 4.5	VDD = 2.5 to 5.5	HPVDD = 1.8	HPVDD = 1.8
Negative Supply Voltage	SVSS ≈ –SVDD	CPVSS ≈ –VDD when VDD < 2.8 V** CPVSS ≈ –2.8 V when VDD ≥ 2.8 V	HPVSS = –1.8	HPVSS = –1.8

* APA outputs must never be forced beyond absolute maximum ratings for supply voltages.
- For single-supply APAs, this includes VDD (or VCC).
- For DirectPath APAs like TPA4411, this includes SVDD and SVSS.
- For DirectPath APAs like TPA6132A2, this includes HPVDD and HPVSS.
- Sometimes no absolute maximum rating is given for VSS/HPVSS. In these cases, the negative of the maximum recommended operating voltage for VDD/HPVDD should be used.

** When VDD < 2.8 V, CPVSS falls as VDD falls.

Operational amplifier gain stability, Part 2: DC gain-error analysis

By Henry Surtihadi, *Analog Design Engineer,*
and Miroslav Oljaca, *Senior Applications Engineer*

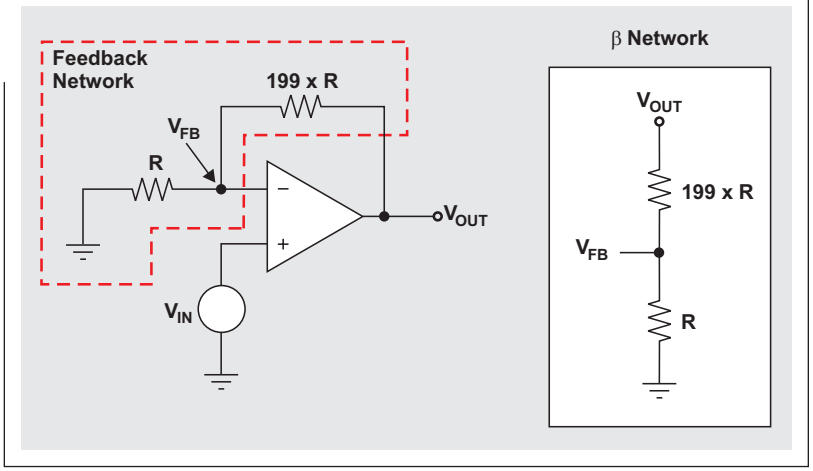
Introduction

The goal of this three-part series of articles is to provide readers with an in-depth understanding of gain accuracy in closed-loop circuits using two of the most common operational amplifier (op amp) configurations: non-inverting and inverting. Often, the effects of various op amp parameters on the accuracy of the circuit's closed-loop gain are overlooked and cause an unexpected gain error both in the DC and AC domains.

This article, Part 2, focuses on DC gain error, which is primarily caused by the finite DC open-loop gain of the op amp as well as its temperature dependency. This article builds upon the results obtained in Part 1 (see Reference 1), in which two separate equations were derived for calculating the transfer functions of non-inverting and inverting op amps. Part 2 presents a step-by-step example of how to calculate the worst-case gain error, starting with finding the pertinent data from the product data sheet. It then shows how to use the data in conjunction with the two aforementioned equations to perform the gain-error calculation.

In Part 3, the gain error for AC input signals will be calculated. In the AC domain, the closed-loop gain error is affected by the AC open-loop response of the op amp. Part 3 will discuss one of the most common mistakes that occur when the AC gain response is calculated.

Figure 1. Non-inverting op amp configuration with ideal closed-loop gain of +200



Transfer functions of non-inverting and inverting op amps

In Part 1 (Reference 1), the closed-loop transfer function of the non-inverting op amp configuration in the frequency domain was calculated. Specifically, the transfer function was derived with the assumption that the op amp had a first-order open-loop response. For calculating gain error, the magnitude response is of interest. For convenience, the result is repeated in Equation 1:

$$\left|A_{CL}(f)\right|_{dB} = 20\log\frac{\dfrac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}}}{\sqrt{1+\dfrac{f^2}{f_0^2}\times\dfrac{1}{(1+\beta\times A_{OL\_DC})^2}}}, \quad (1)$$

where β is defined as

$$\beta = \frac{V_{FB}}{V_{OUT}} = \frac{R_I}{R_I + R_F}. \quad (2)$$

Also derived in the same article was the equation for calculating the magnitude of the inverting configuration's closed-loop gain. The result is repeated in Equation 3:

$$\left|A_{CL}(f)\right|_{dB} = 20\log\frac{\alpha\dfrac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}}}{\sqrt{1+\dfrac{f^2}{f_0^2}\times\dfrac{1}{(1+\beta\times A_{OL\_DC})^2}}} \quad (3)$$

Equation 3 uses the same variable β defined by Equation 2. Additionally, the variable α is defined by Equation 4:

$$\alpha = \frac{V_{FB}}{V_{IN}} = \frac{R_F}{R_I + R_F} \quad (4)$$

At this point, the closed-loop gain for non-inverting and inverting amplifiers is represented by Equations 1 and 3, respectively. These equations will be used for subsequent analysis. The analysis of DC closed-loop circuits has been treated in slightly different ways in References 2 to 7; however, the results agree with this analysis.

DC gain error for non-inverting configuration

To illustrate the impact of an op amp's finite open-loop gain on the accuracy of DC closed-loop gain in a non-inverting configuration, a step-by-step example will be presented on how to calculate the gain error when the op amp is set in an ideal closed-loop gain. An ideal closed-loop gain of 200 (1/β = 200), as shown in Figure 1, will be used. This example focuses on using only the Texas Instruments (TI)

OPA211 op amp, but circuit designers can repeat the calculation with similar values from the data sheet of any other op amp they choose.

To calculate the DC closed-loop-gain error of a non-inverting op amp, Equation 1 is evaluated for zero frequency (f = 0 Hz):

$$A_{CL\_DC} = A_{CL}(0\ Hz) = \frac{A_{OL\_DC}}{1+\beta \times A_{OL\_DC}} \quad (5)$$

In the case of an ideal op amp with infinite open-loop gain, the DC closed-loop gain of the non-inverting configuration is reduced to

$$A_{CL\_DC(ideal)} = \lim_{A_{OL\_DC}\to\infty} \frac{A_{OL\_DC}}{1+\beta \times A_{OL\_DC}} = \frac{1}{\beta}. \quad (6)$$

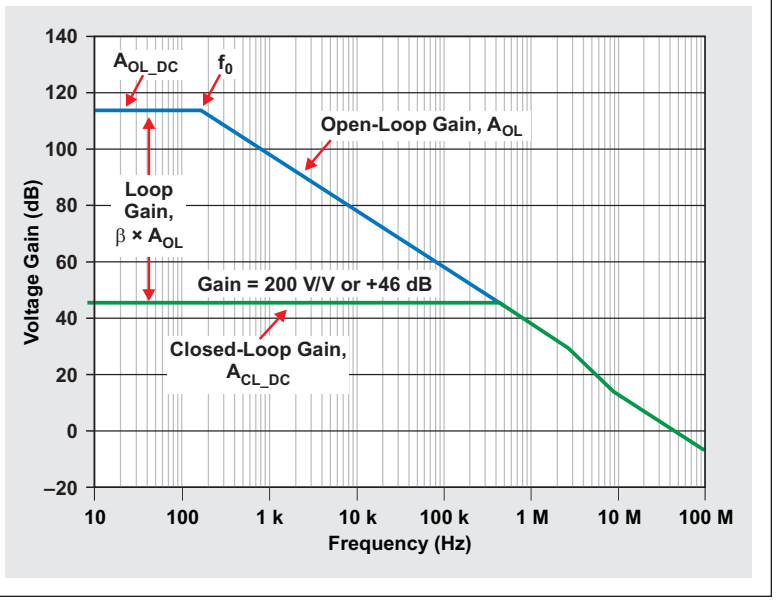
In other words, the DC closed-loop gain is entirely determined by the external feedback network.

From the closed-loop models of non-inverting and inverting amplifiers in Figures 3 and 6, respectively, in Part 1 (see Reference 1), it can be seen that the open-loop gain of the op amp is the ratio of V_{OUT} to the input-error voltage, V_{ERR}. V_{ERR} is the voltage difference between the inverting and non-inverting op amp inputs. It can also be seen as input offset voltage. In a product data sheet, the open-loop gain is typically expressed in decibels. In this case, the number represents the ratio of V_{OUT} to V_{ERR} in the logarithmic domain. For future calculation, A_{OL_DC} must always be converted from decibels to V/V. As an example, an op amp with an open-loop gain of 106 dB can be written in terms of V/V as

$$A_{OL\_DC}\big|_{V/V} = 10^{\frac{A_{OL\_DC}\big|_{dB}}{20}} = 10^{\frac{106\ dB}{20}} = \frac{V_{OUT}}{V_{ERR}} = 199{,}526\ \frac{V}{V}. \quad (7)$$

Figure 2 shows the simplified open-loop gain of the OPA211 along with the closed-loop gain in a non-inverting configuration. The difference between these two curves is the loop gain, $\beta \times A_{OL}$. Because the focus of this example is DC gain error, only the loop gain at low frequency ($\beta \times A_{OL\_DC}$) is of interest.

Figure 2. OPA211's simplified open-loop and closed-loop gain curves



When using the data from the typical curves, designers should consider possible variations. To calculate worst-case values, the open-loop-gain data provided in the product data sheet should be used. Such data are shown in Table 1 for the TI OPA211/2211 op amps. As the table shows, when the output signal is more than 200 mV from the supply rails and has a 10-kΩ load, the typical value for the DC open-loop gain is 130 dB, while the minimum ensured gain is 114 dB. To calculate the typical and the worst-case DC gain

Table 1. Excerpt from TI OPA211/2211 data sheet

ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V

BOLDFACE limits apply over the specified temperature range, T_A = –40°C to +125°C.
At T_A = +25°C, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	Standard Grade OPA211AI, OPA2211AI			High Grade OPA211I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	**A_{OL}**	**(V–) + 0.2V ≤ V_O ≤ (V+) – 0.2V, R_L = 10kΩ**	**114**	**130**		**114**	**130**		**dB**
	A_{OL}	(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 600Ω	110	114		110	114		dB
Over Temperature									
OPA211	**A_{OL}**	**(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, I_O ≤ 15mA**	**110**			**110**			**dB**
OPA211	**A_{OL}**	**(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, 15mA ≤ I_O ≤ 30mA**	**103**			**103**			**dB**
OPA2211 (per channel)	**A_{OL}**	**(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, I_O ≤ 15mA**	**100**						**dB**

errors at room temperature, the minimum A_{OL_DC} from the data sheet should be substituted into Equation 5. Note that in the OPA211 data sheet, "A_{OL_DC}" is written as "A_{OL}."

The first step in this process is to convert A_{OL_DC} from decibels to V/V:

$$A_{OL\_DC}\big|_{V/V} = 10^{\frac{130\ dB}{20}} = 3{,}162{,}278\,\frac{V}{V} \quad (8)$$

$$A_{OL\_DC}\big|_{V/V} = 10^{\frac{114\ dB}{20}} = 501{,}187\,\frac{V}{V} \quad (9)$$

A value for β of 1/200 (the ideal closed-loop gain of 200) can be used in Equation 5 to find the typical DC gain:

$$A_{CL\_DC}\big|_{130\ dB} = \frac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}} = \frac{3{,}162{,}278}{1+\frac{1}{200}3{,}162{,}278} = 199.98735 \quad (10)$$

The actual minimum ensured DC gain can be found in the same manner:

$$A_{CL\_DC}\big|_{114\ dB} = \frac{501{,}187}{1+\frac{1}{200}501{,}187} = 199.92022 \quad (11)$$

The DC gain error caused by the open-loop-gain value of the op amp can then be calculated:

$$\varepsilon_{typ} = \frac{A_{CL\_DC(ideal)} - A_{CL\_DC}}{A_{CL\_DC(ideal)}}\times 100 = \frac{200-199.98735}{200}\times 100 = 0.00632\% \quad (12)$$

$$\varepsilon_{max} = \frac{200-199.92022}{200}\times 100 = 0.0399\% \quad (13)$$

The actual DC closed-loop gain of 199.92 has an error of 0.0399% compared to the desired ideal gain of 200.

Over temperature, the OPA211 is characterized to ensure that A_{OL_DC} is higher than 110 dB over the specified temperature range and when loaded with less than 15-mA output current, which is the absolute worst case. For this value, in terms of V/V, 110 dB is equivalent to

$$A_{OL\_DC}\big|_{V/V} = 10^{\frac{110\ dB}{20}} = 316{,}228\,\frac{V}{V}. \quad (14)$$

This number can be substituted into Equation 5 to find the absolute worst-case condition for the DC closed-loop gain:

$$A_{CL\_DC}\big|_{110\ dB} = \frac{316{,}228}{1+\frac{1}{200}316{,}228} = 199.8736 \quad (15)$$

The gain error for this result, 0.063%, represents a slight degradation from the room-temperature case of 0.0399% previously calculated in Equation 13.

DC gain error for inverting configuration

To illustrate the impact of the op amp's finite open-loop gain on the accuracy of DC closed-loop gain in an inverting configuration, another step-by-step example will be presented of calculating the gain error when the op amp is set in an ideal closed-loop gain. This example will use an ideal closed-loop gain of –200 (–α/β = –200), as shown in Figure 3. So that results can be properly compared, the same op amp, OPA211, will be used.

Similar to the non-inverting case, to calculate the DC closed-loop-gain error of the inverting op amp, Equation 3 is first evaluated for zero frequency (f = 0 Hz):

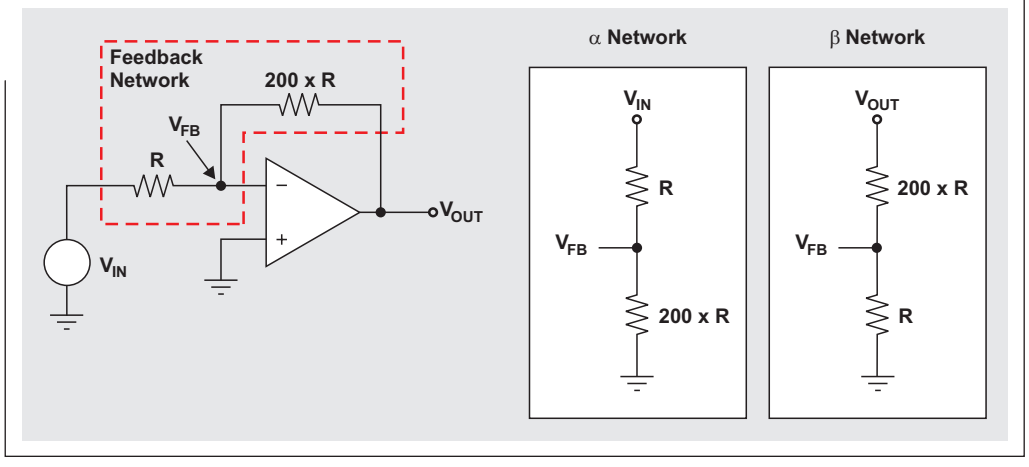
$$A_{CL\_DC} = A_{CL}(0\ Hz) = -\alpha\frac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}} \quad (16)$$

The negative sign indicates the inverting configuration.

In the case of an ideal op amp with infinite open-loop gain, the DC closed-loop gain of the inverting configuration is reduced to

$$A_{CL\_DC(ideal)} = \lim_{A_{OL\_DC}\to\infty} -\alpha\frac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}} = -\frac{\alpha}{\beta}. \quad (17)$$

Figure 3. Inverting op amp configuration with ideal closed-loop gain of –200



As in the non-inverting configuration, the DC closed-loop gain is entirely determined by the external feedback network.

With the same open-loop-gain specifications of 130 dB (typical) and 114 dB (minimum) at room temperature, and 110 dB (minimum) across the specified temperature range—i.e., the worst case—the same calculations can be done for the inverting configuration as were done for the non-inverting configuration. For an inverting amplifier with an ideal closed-loop gain of –200 ($-\alpha/\beta = -200$), the coefficients $\alpha = 200/201$ and $\beta = 1/201$ can be used for the following three gain calculations.

• Typical DC gain:

$$A_{CL\_DC}\Big|_{130\,dB} = -\alpha\frac{A_{OL\_DC}}{1+\beta\times A_{OL\_DC}} = -\frac{200}{201}\times\frac{3{,}162{,}278}{1+\frac{1}{201}\times 3{,}162{,}278} = -199.98729 \quad (18)$$

• Minimum ensured DC gain at room temperature:

$$A_{CL\_DC}\Big|_{114\,dB} = -\frac{200}{201}\times\frac{501{,}187}{1+\frac{1}{201}\times 501{,}187} = -199.9198 \quad (19)$$

• Worst-case DC closed-loop gain over temperature:

$$A_{CL\_DC}\Big|_{110\,dB} = -\frac{200}{201}\times\frac{316{,}228}{1+\frac{1}{201}\times 316{,}228} = -199.87296 \quad (20)$$

The DC gain error caused by the variation of the open-loop-gain value of the op amp can then be calculated:

$$\varepsilon_{typ} = \frac{A_{CL\_DC(ideal)} - A_{CL\_DC}}{A_{CL\_DC(ideal)}}\times 100 = \frac{200-199.98729}{200}\times 100 = 0.00636\% \quad (21)$$

$$\varepsilon_{max} = \frac{200-199.9198}{200}\times 100 = 0.0401\% \quad (22)$$

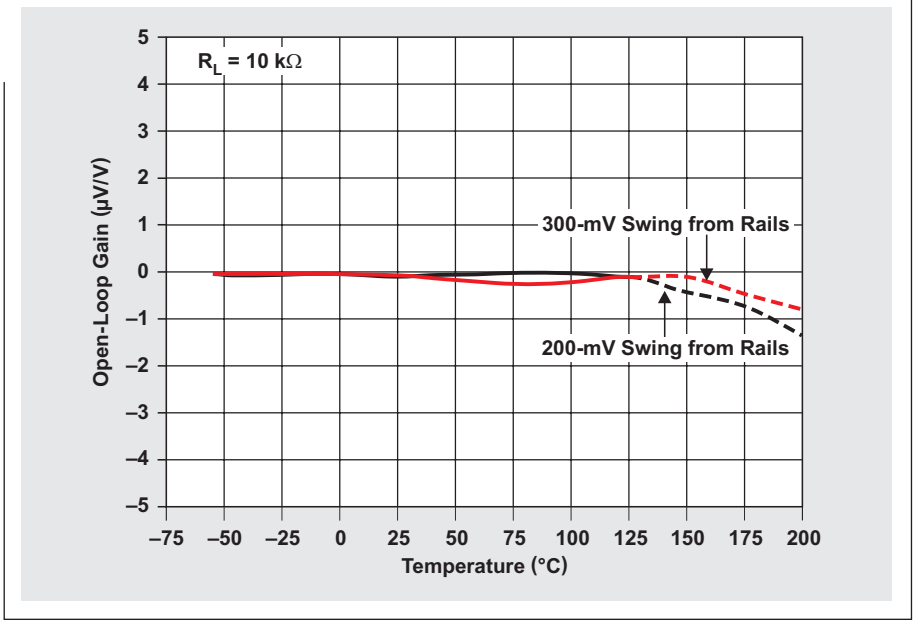
The calculated absolute worst-case condition over temperature for the DC closed-loop gain for the inverting configuration is 0.0635%, compared to 0.0632% for the non-inverting configuration. This example shows that the difference between the non-inverting and inverting configurations is minimal and in many cases can be ignored.

Normalized open-loop gain versus temperature

It should be clear at this point that the DC closed-loop gain is determined by the DC open-loop gain (A_{OL_DC}) of the op amp. Thus, the stability of the DC open-loop gain determines the stability of the DC closed-loop gain. The stability of the open-loop DC gain is determined by many factors, such as the power-supply rejection ratio (PSRR), the temperature, and process variations.

Figure 4 shows the OPA211's normalized DC open-loop gain versus temperature. Note that the changes in open-loop gain are shown in µV/V. As an alternative to representing changes in A_{OL_DC} with decibels as before, A_{OL_DC} can also be represented in terms of µV/V. This representation shows the ratio of the op amp's change in input voltage (error or offset) to the change in its output voltage. In

Figure 4. OPA211's normalized DC open-loop gain versus temperature



other words, the µV/V values have an inverse correlation to the decibel values. As an example, an op amp with an open-loop gain of 199,526 V/V can be written in terms of decibels as

$$A_{OL\_DC}\Big|_{V/V} = \frac{V_{OUT}}{V_{ERR}} = 199{,}526\,\frac{V}{V} \quad \textbf{(23)}$$

and

$$A_{OL\_DC}\Big|_{dB} = 20\log\frac{V_{OUT}}{V_{ERR}} = 20\log(199{,}526) = 106\text{ dB}. \quad \textbf{(24)}$$

In terms of µV/V, the same gain is written as

$$A_{OL\_DC}\Big|_{\mu V/V} = \frac{V_{ERR}}{V_{OUT}} = \frac{1}{199{,}526} = 5.012\,\frac{\mu V}{V}. \quad \textbf{(25)}$$

Figure 4 shows how the OPA211's A_{OL_DC} (in terms of µV/V) may change over temperature. For a device with a given A_{OL_DC} at room temperature (25°C), A_{OL_DC} will typically change less than 0.25 µV/V in the specified temperature range (–40°C to 125°C). For example, if the typical A_{OL_DC} performance is 130 dB, or 0.32 µV/V, at room temperature, then over the specified temperature range, A_{OL_DC} may typically vary between 0.32 µV/V and 0.57 µV/V. To ensure stable operation over temperature, the minimum gain is as follows:

$$A_{OL\_DC}\Big|_{V/V} = \frac{V_{ERR}}{V_{OUT}} = \frac{1}{0.57\ \mu V} = 1{,}754{,}386\,\frac{V}{V} \quad \textbf{(26)}$$

$$A_{OL\_DC}\Big|_{dB} = 20\log(1{,}754{,}386) = 124.88\text{ dB} \quad \textbf{(27)}$$

This is equivalent to an A_{OL_DC} ranging from 124.88 dB to 130 dB. Keep in mind that these are typical data. It is suggested that, during the circuit-design process, the designer not use typical values but instead use minimum ensured values published by the op amp's manufacturer.

Note that none of the calculations in this article include other factors that also affect A_{OL_DC}, such as the PSRR or the common-mode rejection ratio. The procedure to include these types of errors is similar: Simply add the additional error to the A_{OL_DC} term and recalculate the closed-loop DC gain.

Conclusion

Part 1 of this article series explored general feedback-control-system analysis and synthesis as they apply to first-order transfer functions. The analysis technique was applied to both non-inverting and inverting op amp circuits, resulting in a frequency-domain transfer function for each configuration. Part 2 has shown how to use these two transfer functions and manufacturer data-sheet specifications to analyze the DC gain error of a closed-loop op amp circuit. This analysis also took into consideration the temperature dependency of the open-loop gain as well as its finite value. Part 3 will explore the frequency dependency of the closed-loop gain, which will help designers avoid the common mistake of using DC gain calculations for AC-domain analysis.

References

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Document Title	**TI Lit. #**
1. Miroslav Oljaca and Henry Surtihadi, "Operational amplifier gain stability, Part 1: General system analysis," *Analog Applications Journal* (1Q 2010)	slyt367
2. Soufiane Bendaoud, "Gain error affects op amp choices," *Planet Analog* (July 14, 2006) [Online]. Available: http://www.planetanalog.com (Enter *bendaoud* in lower-case letters into the search field.)	
3. Ron Mancini, "Op-amp-gain error analysis," *EDN* (Dec. 7, 2000) [Online]. Available: http://www.edn.com	—
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amplifier.ti.com
www.ti.com/sc/device/OPA211

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