User's Guide

TPSI2072-Q1 EVM User's Guide

ABSTRACT

The TPSI2072Q1EVM helps designers evaluate the operation and performance of the TPSI2072-Q1. This user's guide provides the connectors, test point descriptions, operational modes, schematic, bill of materials, and board layout of the EVM. The TPSI2072-Q1 is a 3.75-kV_{rms} /5.3-kV_{DC} dual channel isolated switch. The inputs and output connections to the board are terminal blocks, which allow for easily wired connections. The TPSI2072Q1EVM contains multiple test points for monitoring the TPSI2072-Q1 functionality.

	**Danger**	**Do not use EVM to test Isolation above V_{IOWM} = 1414-V_{DC} High voltage**
	**Caution**	**Caution hot surface Contact can cause burns Do not touch!**
	**Caution**	**Read the user's guide before use**
	**Caution**	**Do not leave EVM powered when unattended**

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General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://ti.com/customer support for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:
   a. As a precautionary measure, it is always good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   b. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   d. Once EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment e.g. latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

1 Introduction

The TPSI2072-Q1 is a dual channel isolated solid state relay designed for high voltage automotive and industrial applications such as battery management systems, EV/HEV onboard chargers, mechanical relay replacement, DC link pre-charging, and more. The TPSI2072-Q1 seamlessly replaces relays without need for a secondary side supply while leveraging unique isolation technology integrated in a compact SOIC package. The entire primary side of the device requires only 9 mA of input current, enabling the user to drive the VDD, EN1, and EN2 pins from two microcontroller GPIO pins and eliminating the need for an external low side switch used in Photomos solutions. The secondary side consists of back-to-back MOSFETs with a standoff voltage of +/– 600 V from S1 to SM and S2 to SM. The TPSI2072-Q1 MOSFETs' avalanche robustness and thermally conscious package design allow it to survive system level dielectric withstand testing (HiPot) and DC fast charger surge currents of up to 2 mA without requiring any external components.

1.1 Features

- Isolation: 3.75-kVRMS, 1500-VDC
- Integrated avalanche rated MOSFETs with 600-V standoff voltage
- Qualified for automotive applications: AEC-Q100
- Low primary side supply current, 9-mA ON state, 1-µA OFF state (500-V, 105°C)
- Test points available for every pin and voltage supply to ensure correct functionality

1.2 Applications

- Solid state relay
- Hybrid, electric, and power train systems
- Battery Management Systems (BMS)
- Energy Storage Systems (ESS)
- Solar energy
- Onboard charger
- EV charging infrastructure
- See also the TI Reference Designs related to these applications.

1.3 Description

The TPSI2072Q1EVM is a six-copper layer board containing multiple test points and jumpers in order to fully evaluate the functionality of the device. The primary side consists of four differential drivers which deliver power and enable logic information to each of the internal MOSFETs on the secondary side. Each MOSFET on the secondary side has a dedicated full-bridge rectifier to form its local power supply. When the enable pin is brought HI, the oscillator starts and the drivers send power and a logic HI across the barrier. The avalanche robust MOSFETs and the thermal benefits of the widened pins on the 11 DWQ package enable the TPSI2072-Q1 to survive dielectric withstand testing (HiPot) and DC fast charger surge currents of up to 2 mA without requiring any external protection components.

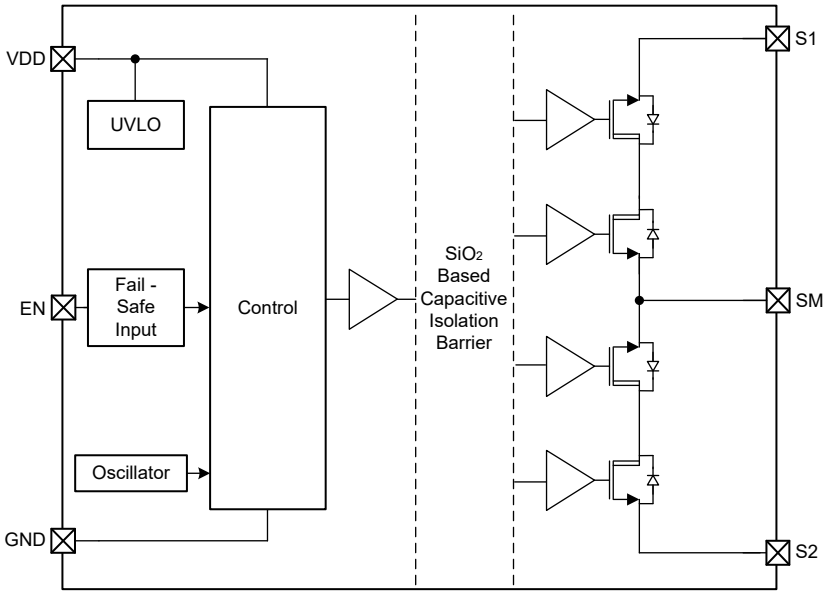

Figure 1-1. TPSI2072-Q1 Functional Block Diagram (need to update)

Table 1-1. Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPSI2072-Q1	SOIC 11 pin (DWQ)	10.3 mm × 7.5 mm

2 Connection Descriptions

Table 2-1 shows an overview of the input/output connectors. Table 2-2 shows the test points and jumpers.

Table 2-1. Input and Output Connector Descriptions

Connector	Label	Description
J1	HV1	Secondary side positive input 1
J2	SM	Voltage sense output
J3	HV–	Secondary side negative input
J4	VDD	Primary Side supply
J5	GND	Primary Side GND
J6	EN1_EXTERNAL	External Enable 1 Signal
J8	EN2_EXTERNAL	External Enable 2 signal
J10	HV2	Secondary side positive input 2

Table 2-2. Test Point and Jumper Descriptions

Test Point, Jumper	Label	Description
TP1	VDD	Primary side supply test point
TP2	EN1_EXTERNAL	EN1_EXTERNAL test point
TP3, TP4	GND	Primary side ground test point
TP5	S1	Secondary side HV1 voltage after resistor chain
TP6	SM	Thermal Pin
TP7	S2	Secondary side HV2 voltage after resistor chain
TP8	HV-	HV– secondary side test point
TP9	EN2_EXTERNAL	EN2_EXTERNAL test point
J7	EN1_X/EN1/VDD	Connects EN1_X to EN1, or EN1 to VDD. Allows for external enable signal to be used instead of EN1 being signaled by VDD
J9	EN2_X/EN2/VDD	Connects EN2_X to EN2, or EN2 to VDD. Allows for external enable signal to be used instead of EN2 being signaled by VDD
J11	Stitching Capacitor Jumper	Connects interlayer stitching capacitor (20 pF) between primary and secondary ground to improve EMI performance.

3 Test Equipment

The testing of the TPSI2072Q1EVM recommends the following equipment:

- Adjustable power supplies for the input
- Oscilloscope
- A function generator to toggle the EN pin

4 Recommended Test Setup

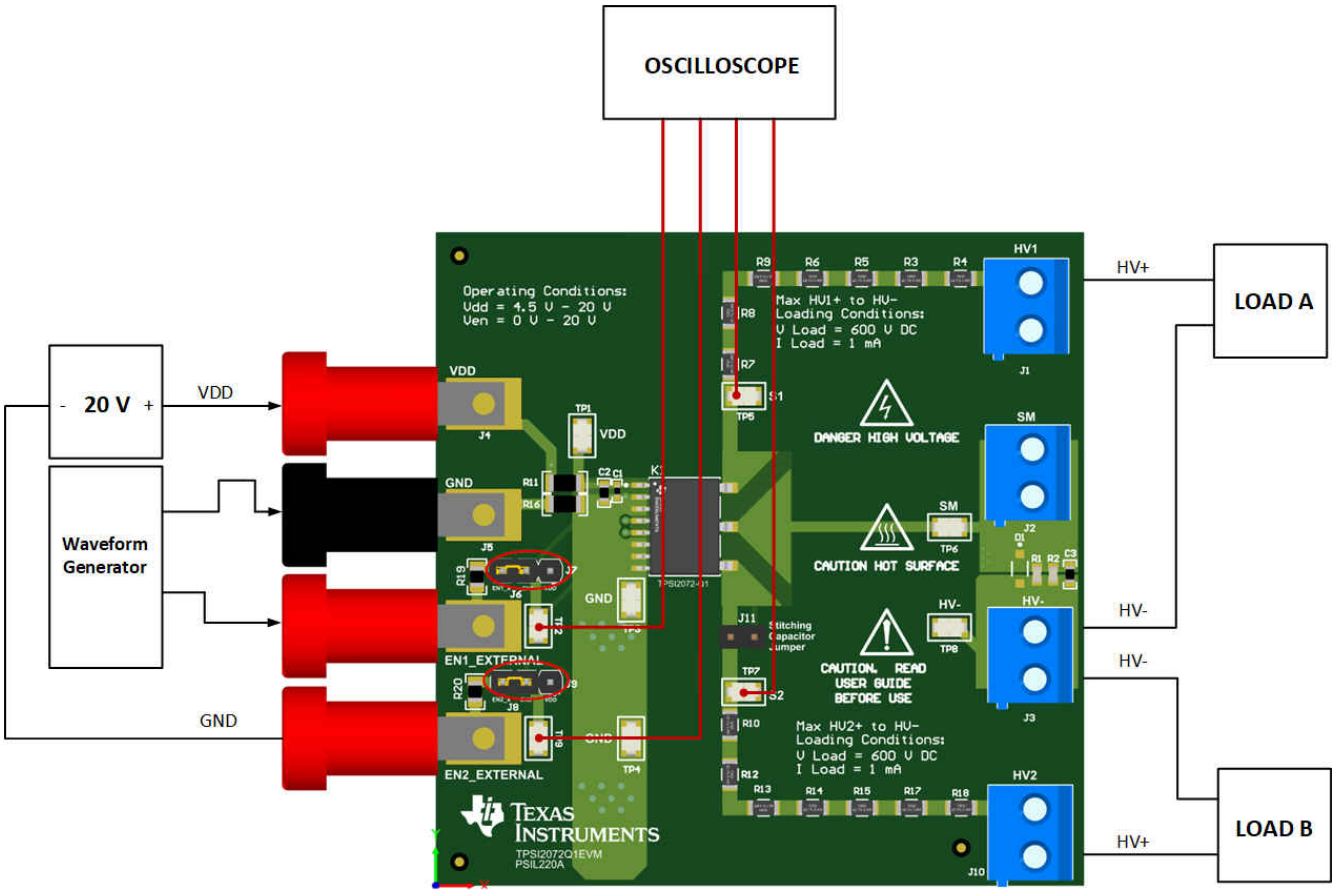

Figure 4-1. TPSI2072-Q1 EVM Test Setup

Ensure that the TPSI2072Q1EVM has the following setting on the jumpers:

1. J7 – Shunt is connecting EN1 and EN1_EXT.
2. J9 – Shunt is connecting EN2 and EN2_EXT.
3. If not using a waveform generator as shown above, alternate setting the shunts to be between VDD and EN1/EN2. This action causes EN1/EN2 to be high when VDD is powered.

4.1 Waveforms

If connected as described above, the following channels must be displayed in the waveforms below:

- CH 1 = EN1
- CH 2 = EN2
- CH 3 = S1-SM
- CH 4 = SM-S2

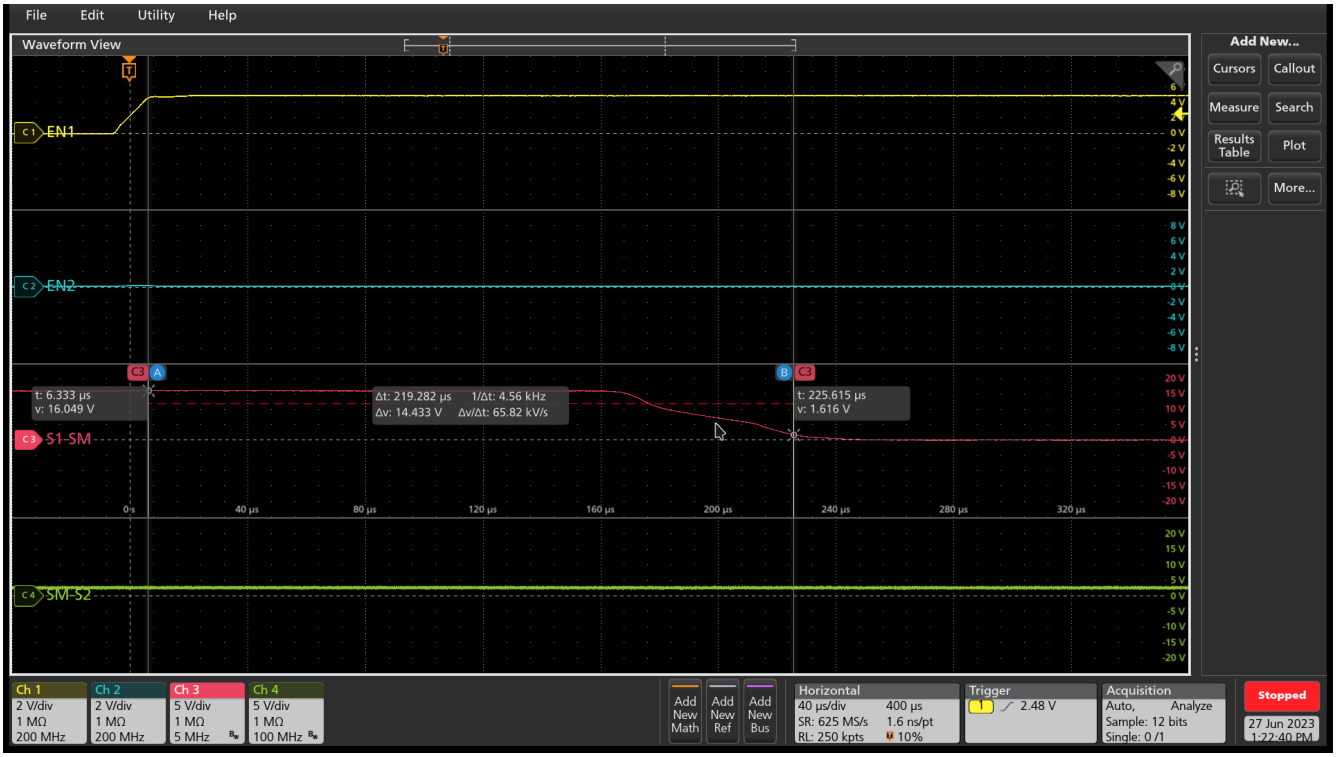

Figure 4-2. RN1 Rise Time

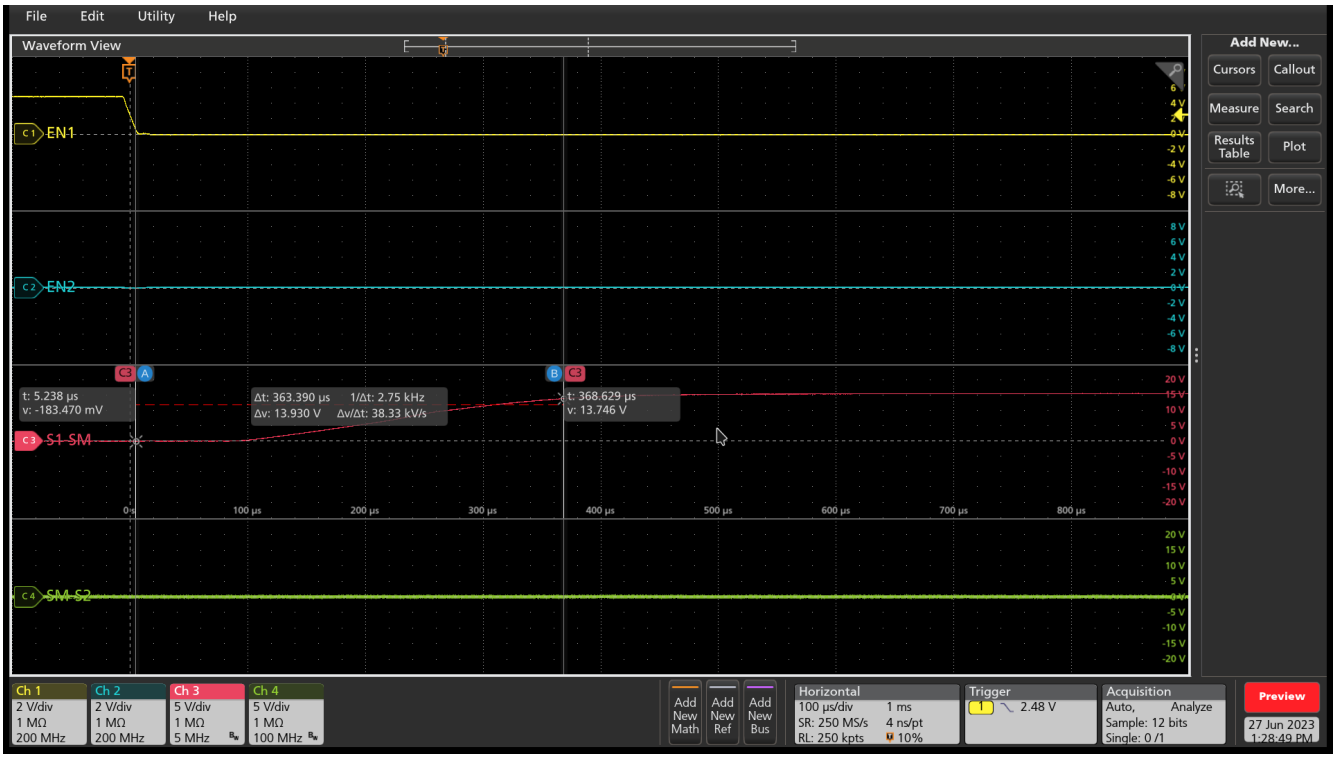

Figure 4-3. EN1 Fall Time

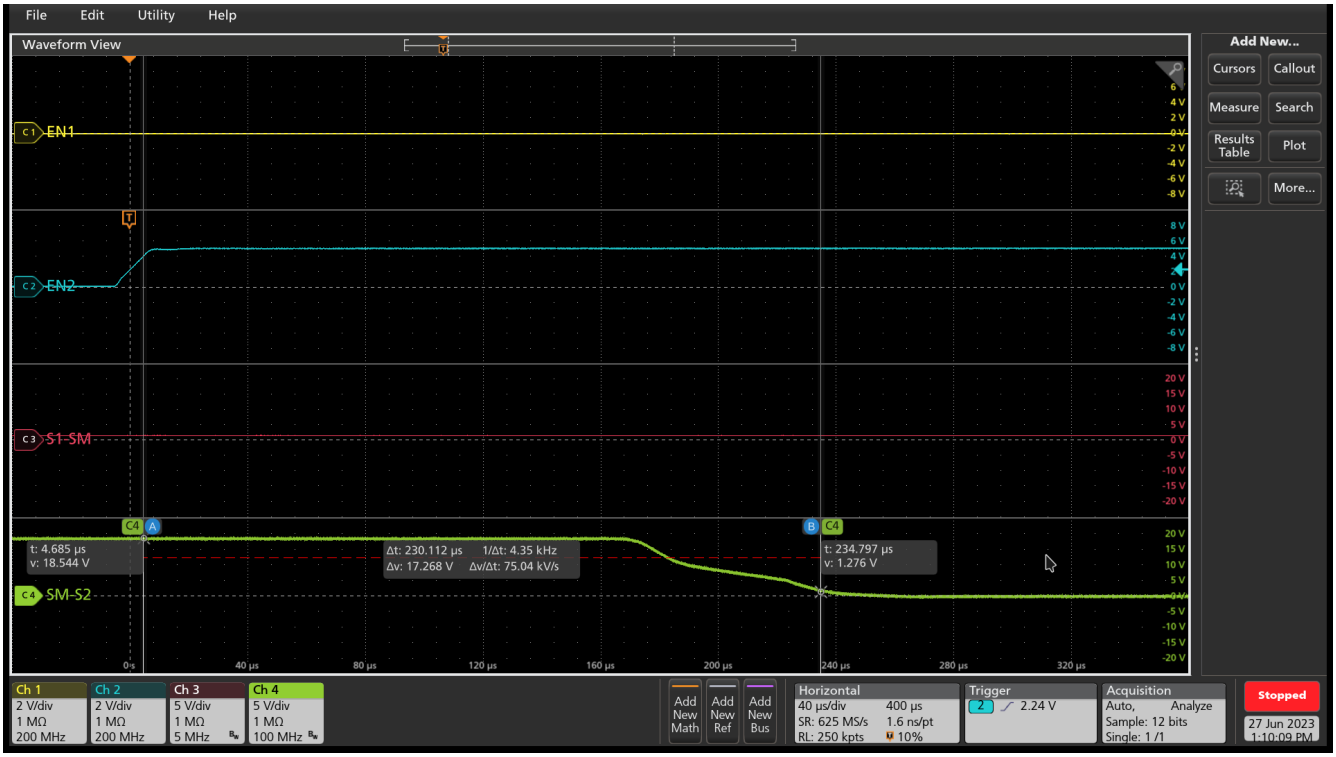

Figure 4-4. EN2 Rise Time

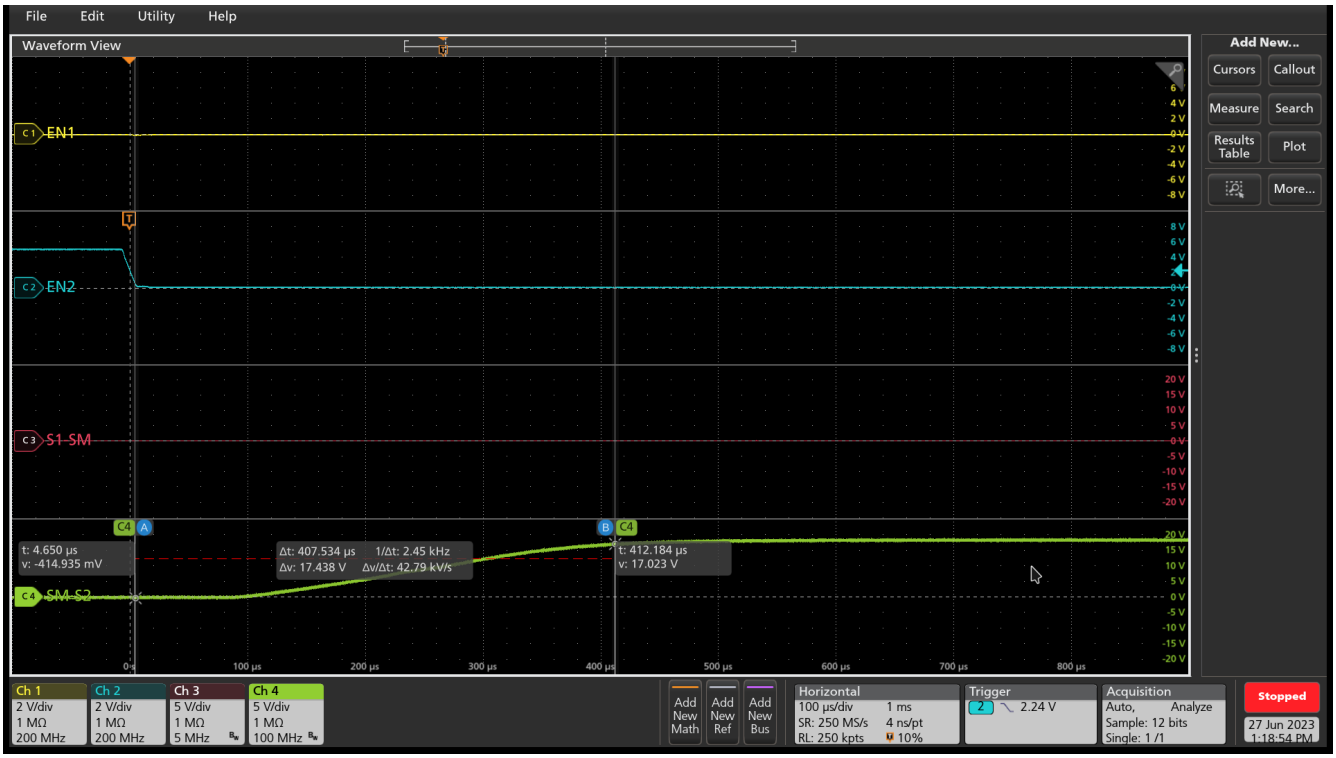

Figure 4-5. EN2 Fall Time

4.2 V_{S1_ADC} and V_{S2_ADC} Voltage Dividers

SM (TP6) will be the voltage divider measurement. The voltage measured is dependent on parallel resistors R1 and R2, and the resistor network R3-R9 or R10-R18. It can be calculated by the following equation:

$$V_{S1\_ADC} = \frac{R1||R2}{(R3 + R4 \ldots + R9) + (R1||R2)} \times V_{LOAD} \quad (1)$$

$$V_{S2\_ADC} = \frac{R1||R2}{(R10 + R12 + R13 + R14 + R15 + R17 + R18) + (R1||R2)} \times V_{LOAD} \quad (2)$$

5 Schematic

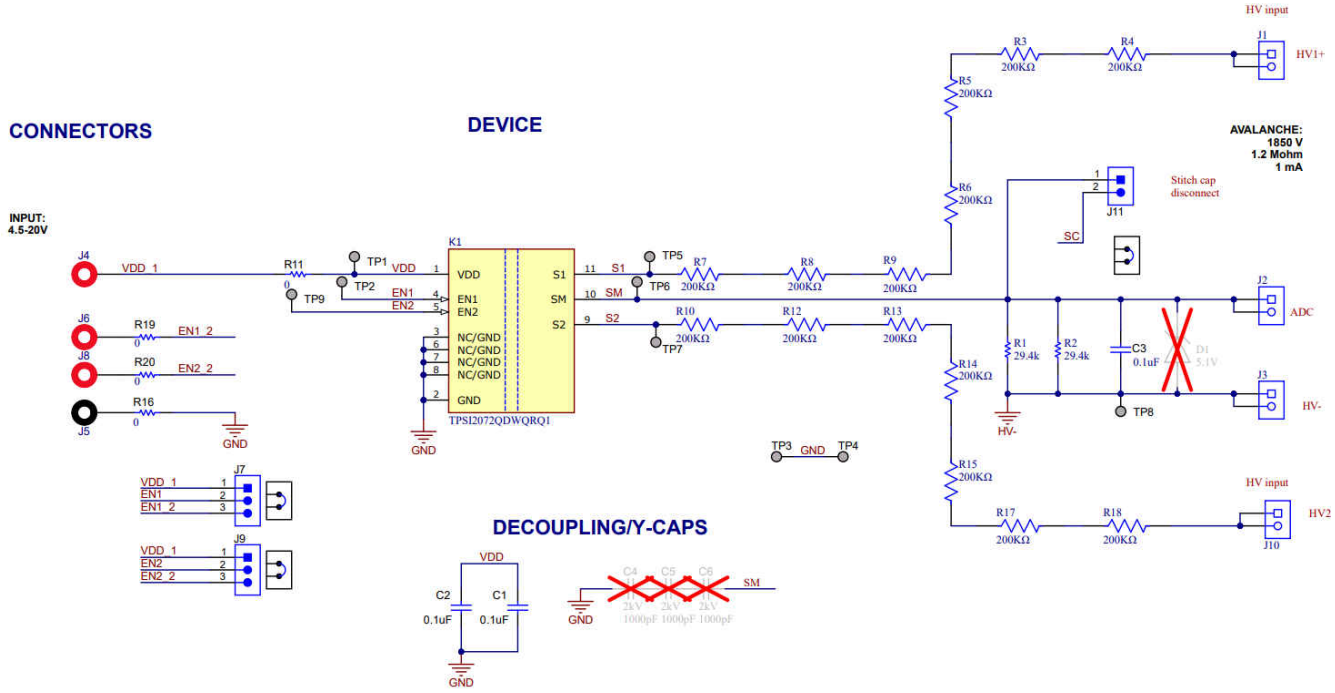

Figure 5-1. TPSI2072Q1EVM Schematic

6 PCB Layout

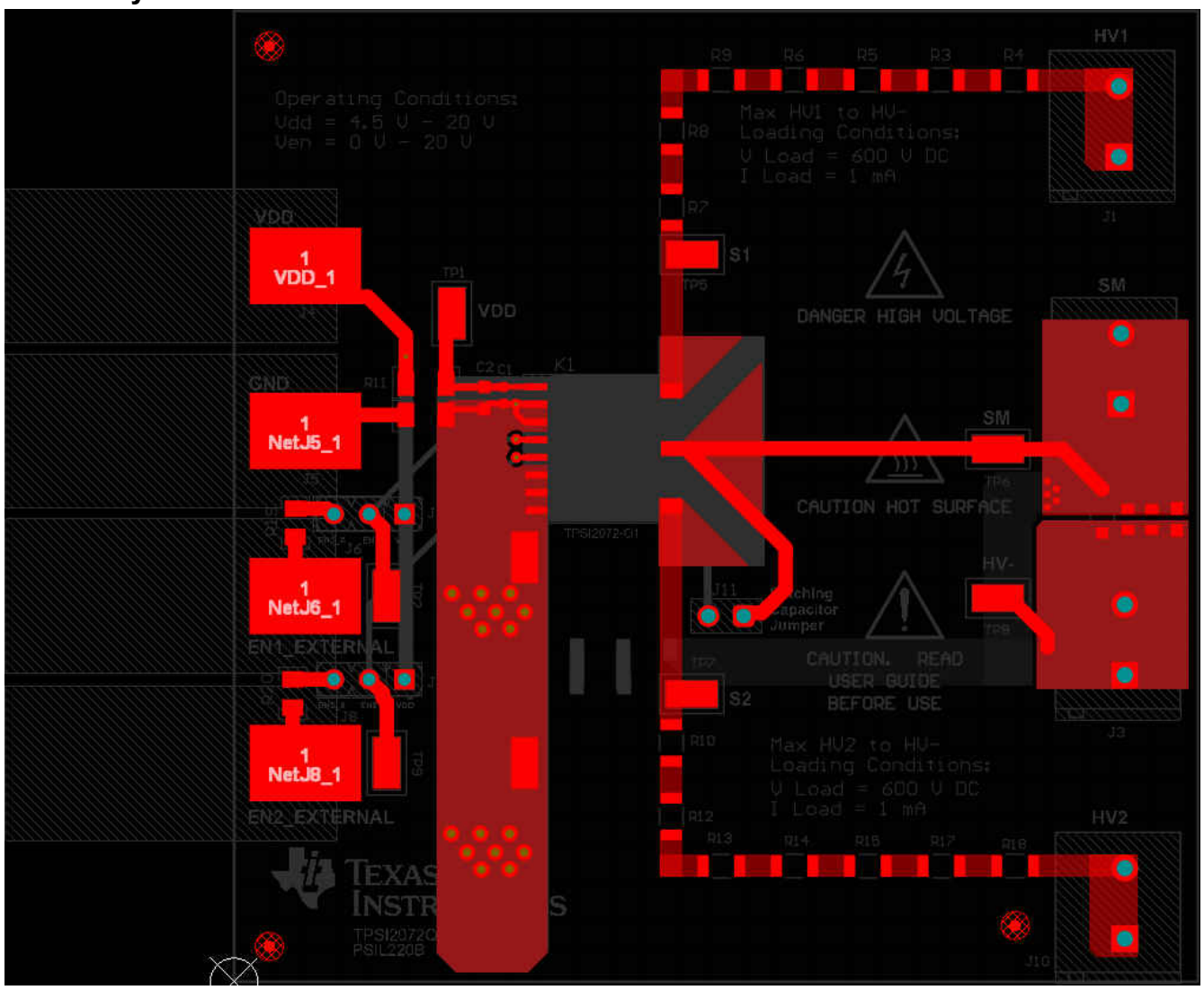

Figure 6-1. TPSI2072-Q1 EVM Layer 1

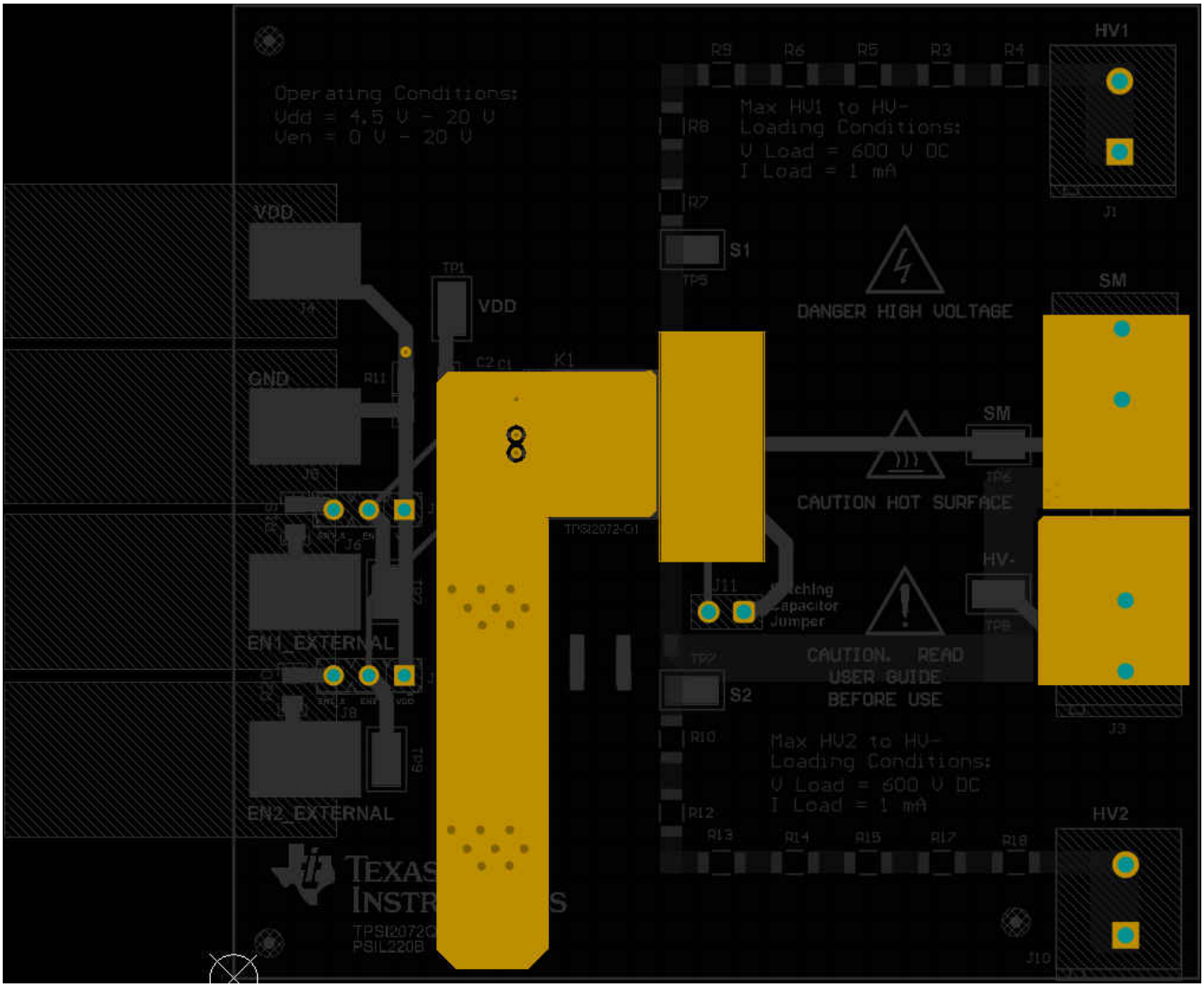

Figure 6-2. TPSI2072-Q1 EVM Layer 2

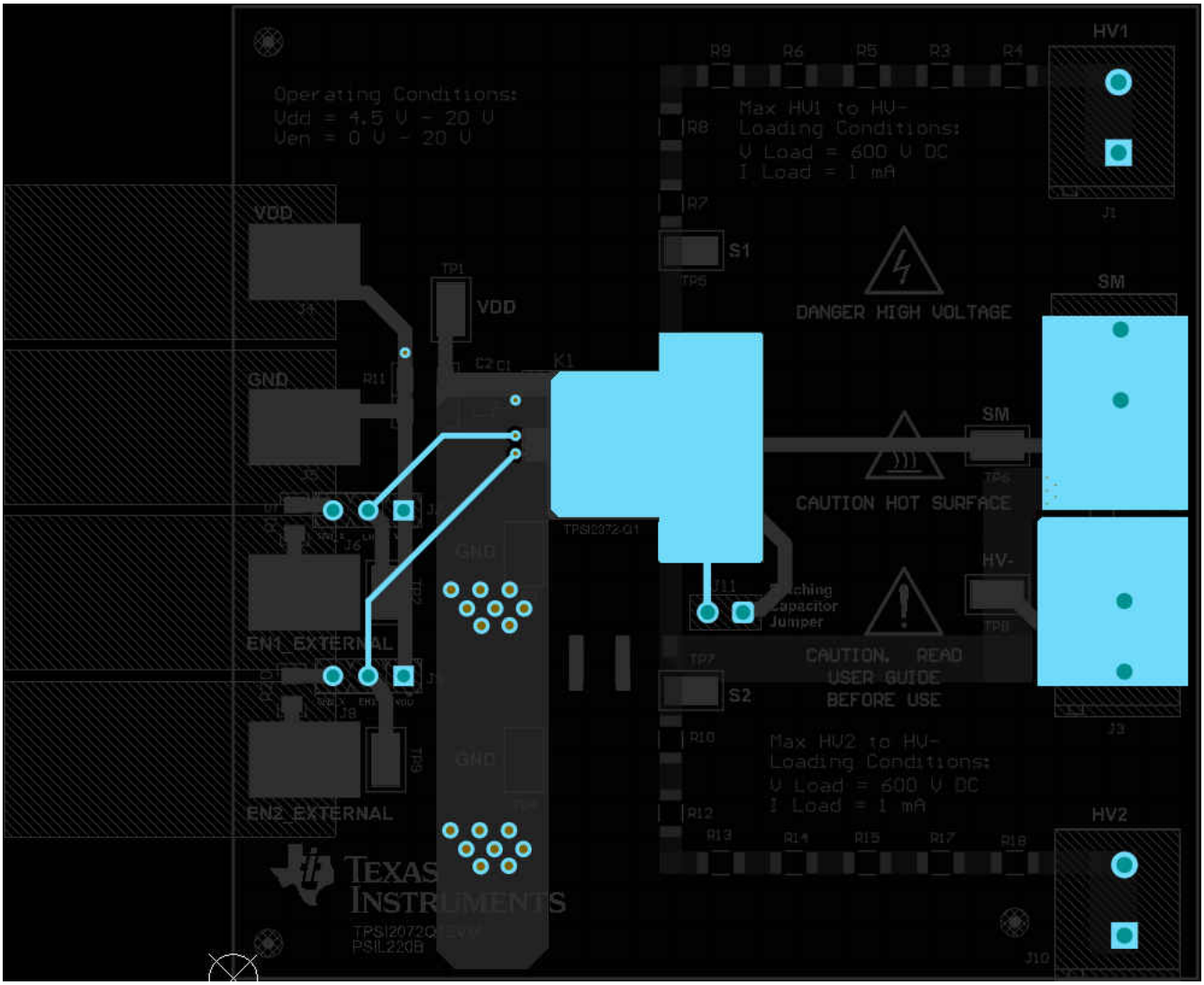

Figure 6-3. TPSI2072-Q1 EVM Layer 3

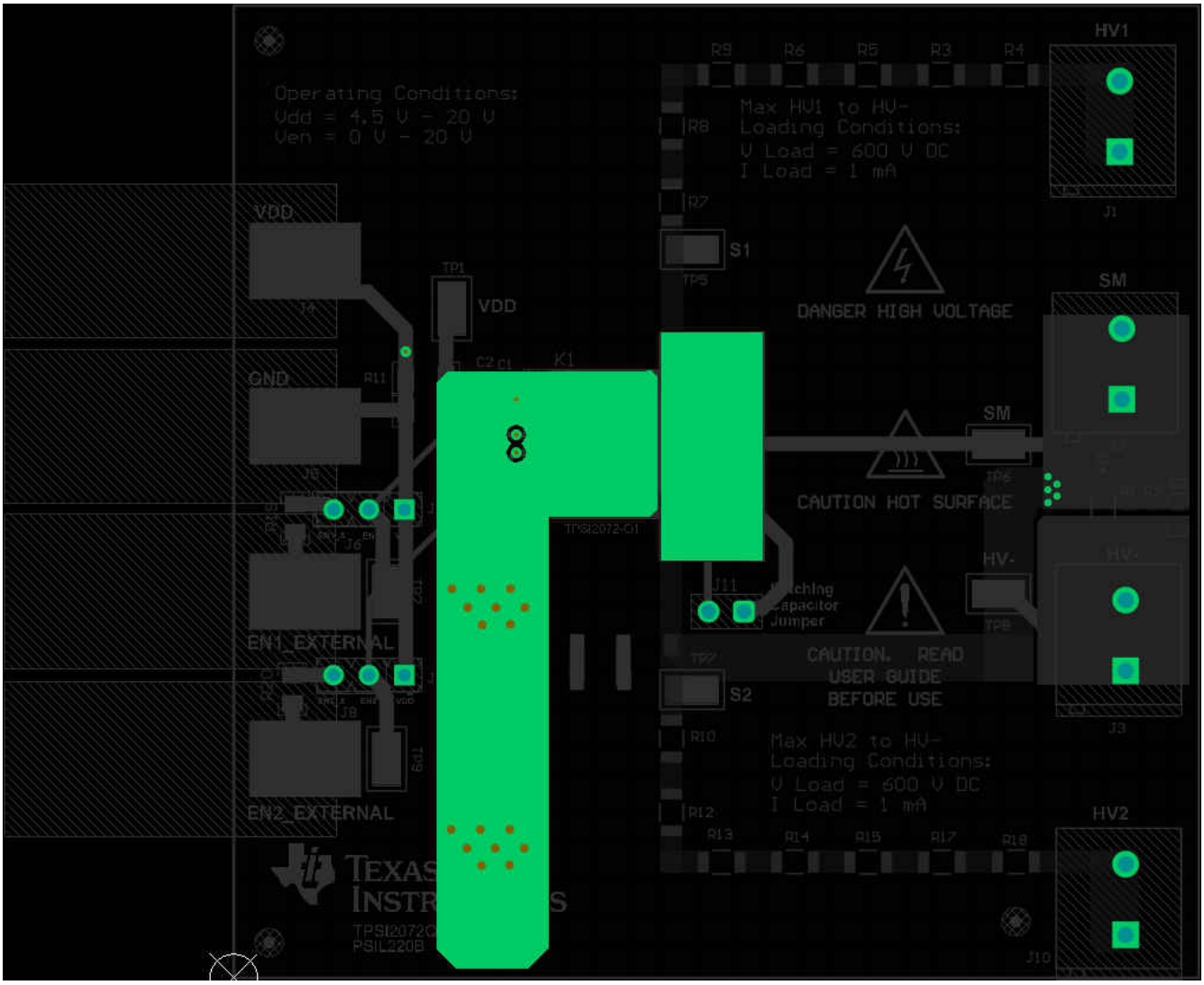

Figure 6-4. TPSI2072-Q1 EVM Layer 4

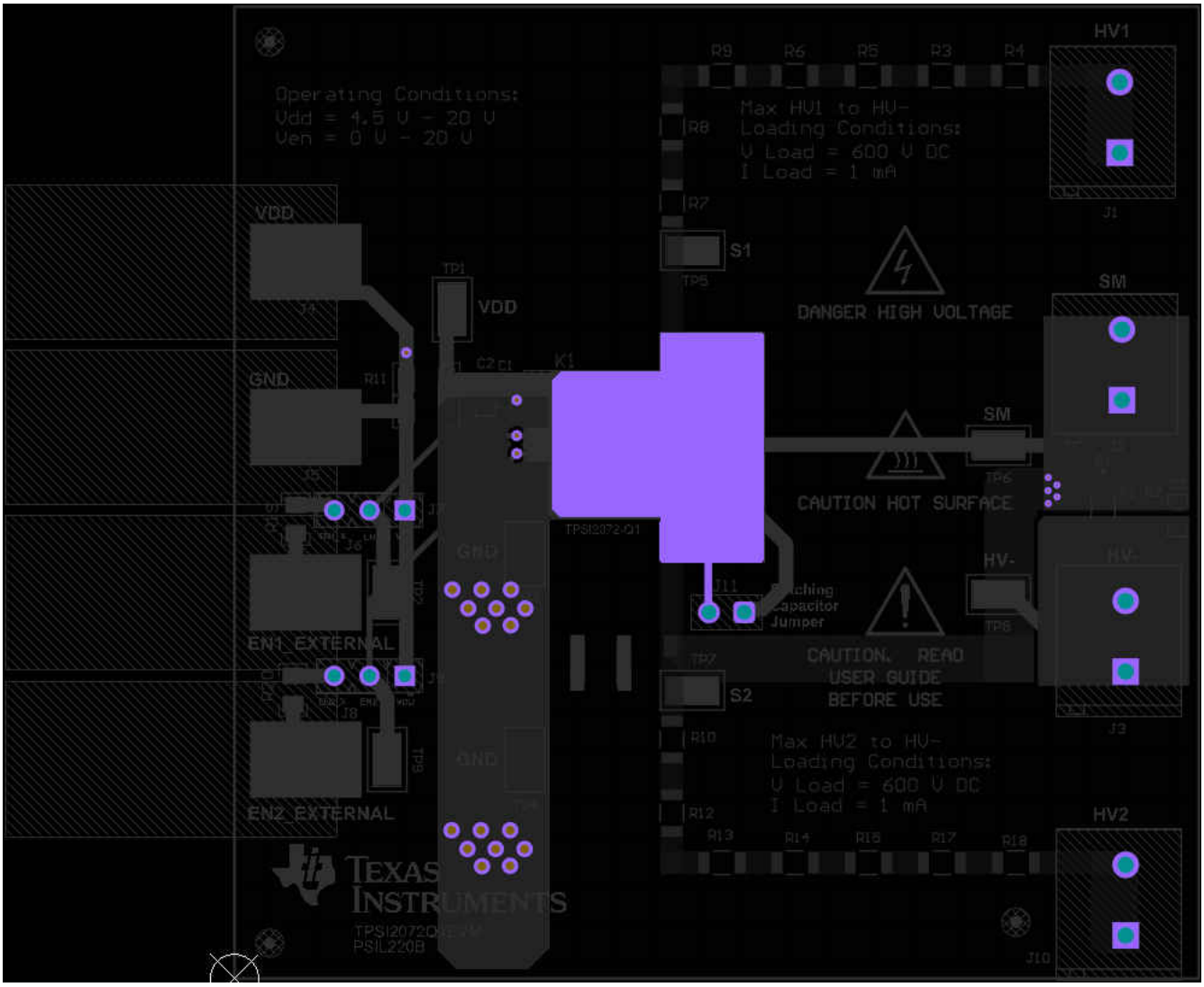

Figure 6-5. TPSI2072-Q1 EVM Layer 5

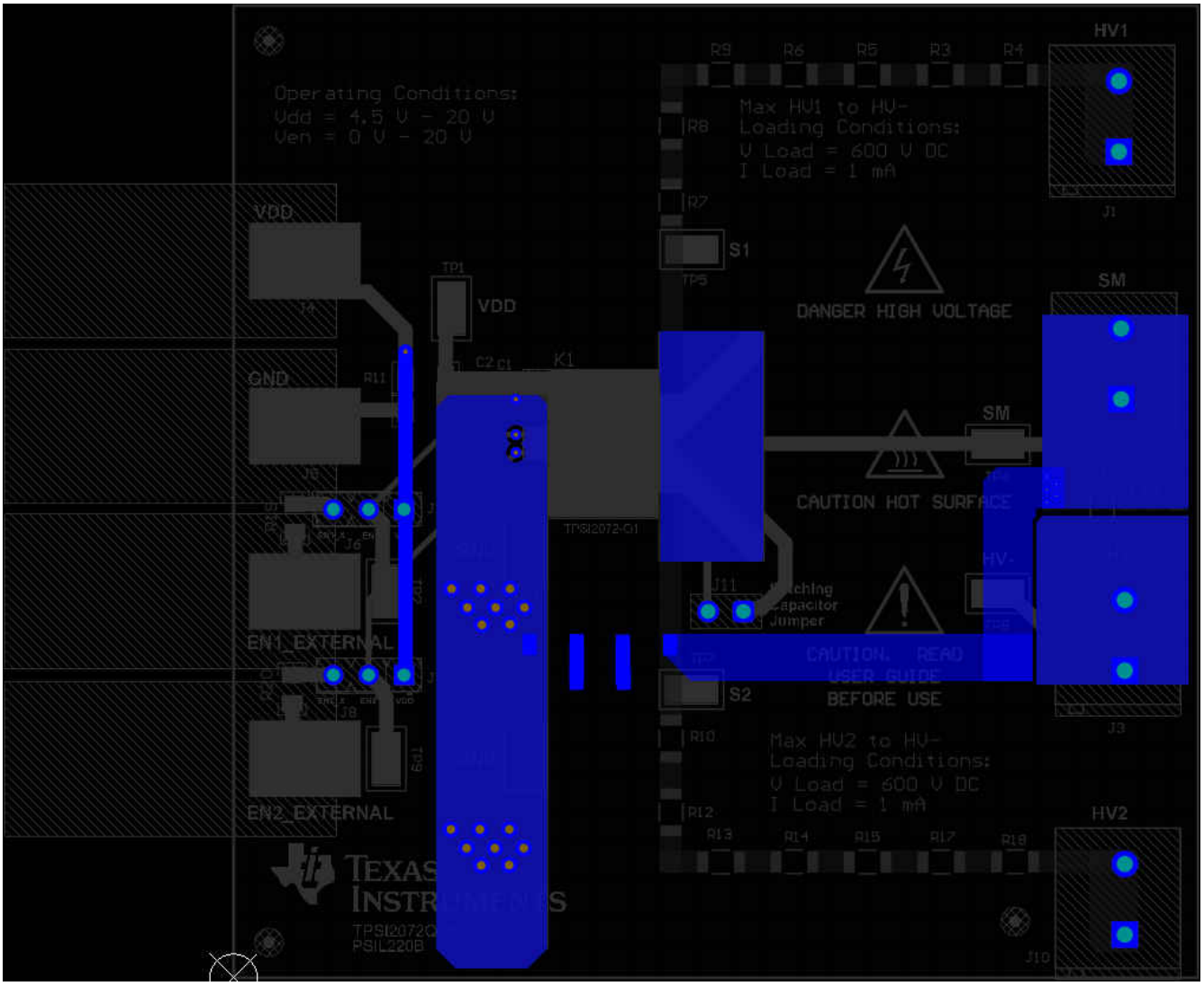

Figure 6-6. TPSI2072-Q1 EVM Layer 6

7 Interlayer Stitching Capacitor

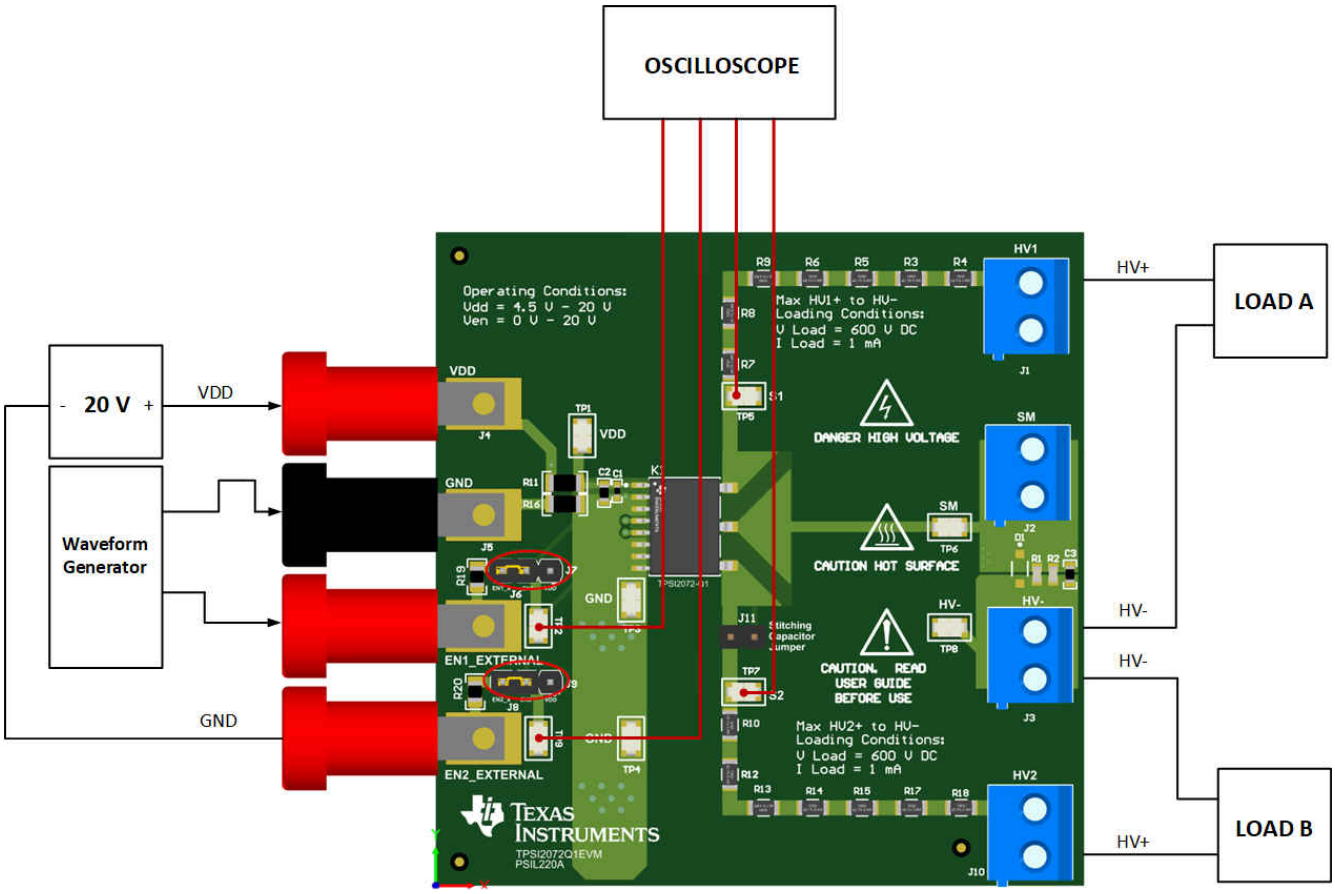

Figure 7-1. TPSI2072-Q1 EVM Test Setup

Ensure that the TPSI2072Q1EVM has the following setting on the jumpers:

1. J7 – Shunt is connecting EN1 and EN1_EXT.
2. J9 – Shunt is connecting EN2 and EN2_EXT.
3. If not using a waveform generator as shown above, alternate setting the shunts to be between VDD and EN1/EN2. This action causes EN1/EN2 to be high when VDD is powered.

7.1 Interlayer Stiching Capacitors & EMI Performance Improvements

Transient noise can couple through capacitive or magnetic isolation, creating a common-mode current between the primary and secondary sides. This emits EMI and can be exacerbated by a large return path. A Y-capacitor can connect the primary and secondary grounds together to minimize common-mode current return path size. The Y-capacitor effectively acts as a high-pass filter, creating a low impedance path for secondary-side high frequency signals to return back to the primary-side. The TPSI2072-Q1 EVM features an interlayer stitching capacitor by using the internal layers of the PCB to form a Y-capacitor (20 pF) across the primary and secondary side grounds. Connect the J11 jumper to enable the interlayer stitching capacitor. More about interlayer stitching capacitors can be read in the application report, Low-Emission Designs With ISOW7841 Integrated Signal and Power Isolator.

7.2 V_{S1_ADC} and V_{S2_ADC} Voltage Dividers

8 Bill of Materials

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
!PCB	1		Printed Circuit Board		PSIL220	Any
C1	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402	0402	GRM155R71E104KE14D	MuRata
C2	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E2X7R1E104K080AA	TDK
C3	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C104K3RACTU	Kemet
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J1, J2, J3, J10	4		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J4, J6, J8	3		Banana Jack Insul Nylon Red, TH	Banana Jack Insul Nylon Red, TH	108-0902-001	Cinch Connectivity
J5	1		Banana Jack Insul Nylon Black, TH	Banana Jack Insul Nylon Black, TH	108-0903-001	Cinch Connectivity
J7, J9	2		Header, 2.54mm, 3x1, Tin, TH	Header, 2.54mm, 3x1, TH	68001-403HLF	FCI
J11	1		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	61300211121	Wurth Elektronik
K1	1		Automotive Isolated Switch with 2-mA Avalanche Rating	SOIC11	TPSI2072QDWQRQ1	Texas Instruments
R1, R2	2	29.4k			RC0603FR-0729K4L	Yageo
R3, R4, R5, R6, R7, R8, R9, R10, R12, R13, R14, R15, R17, R18	14	200KΩ	RQ732B 1206 200KΩ 0.4W 10ppm/°C 0.1% 200V		RQ73C2B200KBTD	TE
R11, R16	2	0	RES, 0, 5%, 0.25 W, 1206	1206	RC1206JR-070RL	Yageo America
R19, R20	2	0	RES, 0, 5%, 0.125 W, 0805	0805	MCR10EZPJ000	Rohm
SH-1, SH-2, SH-3	3	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec

TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	9		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
C4, C5, C6	0	1000pF	CAP, CERM, 1000 pF, 2000 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206	C1206C102KGRACAUTO	Kemet
D1	0		DIODE ZENER 5.1V 500MW SOD123			Diodes

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2022) to Revision A (January 2023) **Page**

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