*User's Guide*

# *TPS7H1111EVM Evaluation Module (EVM)*


**ABSTRACT**

This user's guide describes operational use of the TPS7H1111EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7H1111-SEP and TPS7H1111-SP (QMLP), 1.5-A, Ultra-Low Noise, High PSRR, Space Enhanced Plastic, Lowdrop Out (LDO) regulators. This user's guide provides details about the EVM, its configuration, schematics, and bill of material (BOM).


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## Trademarks

# 1 Introduction

The TPS7H1111-SEP is an ultra-low noise, high PSRR, low dropout linear regulator (LDO) optimized for powering RF (radio frequency) devices in a space environment. It is capable of sourcing up to 1.5 A over a 0.85-V to 7-V input range with a 2.2-V to 14-V bias supply.

The EVM is configured with a default output resistor to regulate to a 1.8 V $V_{OUT}$, with a usable $V_{IN}$ range of (1.8 V + $V_{DO}$) to 7 V with $V_{BIAS}$ range of ($V_{OUT}$ + 1.6 V to 14 V). Worst case $V_{DO}$ ranges from 430mV for $V_{BIAS}$ ≥ ($V_{OUT}$ + 1.6 V) to 1.4 V with $V_{BIAS}$ = $V_{IN}$ at 1.5 A load. The EVM is intended to aid engineers in the evaluation of the operation and performance of the TPS7H1111-SEP linear regulator. The TPS7H1111-SEP low-dropout regulator allows input voltages from 0.85 V to 7 V and is capable of regulating any output voltage between 0.4 V and up to 5.5 V by changing the $V_{OUT}$ current setting resistor R8. The EVM is capable of delivering up to 1.5 A to a load. Achieving the maximum load depends on multiple variables, including the input-output power dissipation, board thermal dissipation, and heat removal.

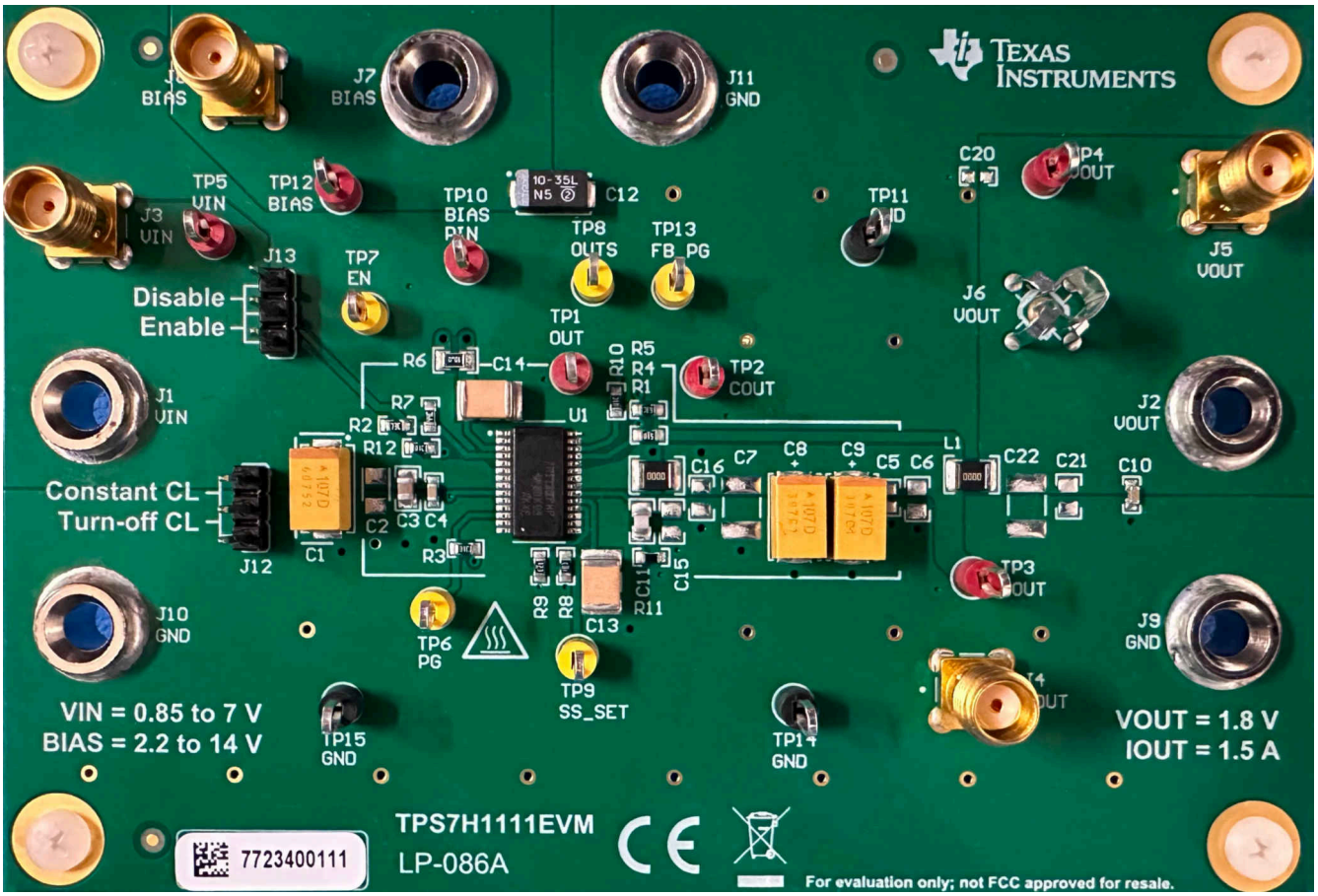


**Figure 1-1. TPS7H1111EVM (LP086A)**

## 1.1 Related Information

- TPS7H1111-SEP and TPS7H1111-SP data sheet (SLVSFT8)

## 1.2 Features of the TPS7H1111-SEP

- Device Radiation Characterization
  - Radiation characterized to a total ionizing dose (TID) of 50 krad(Si)
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune to linear energy transfer (LET) = 43 MeV-cm$^2$/mg
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized to LET = 43 MeV-cm$^2$/mg
  - Ultra-Low Noise: 1.71 $\mu V_{RMS}$ (typ), 10 Hz - 100 kHz
- High power-supply rejection ratio, PSRR (typ):
  - 109 dB at 100 Hz
  - 71 dB at 100 kHz
  - 66 dB at 1 MHz
- Input voltage range from 0.85 V to 7 V
- Bias supply of 2.2 V to 14 V to minimize power dissipation
- Output voltage as low as 0.4 V
- Up to 1.5-A output current
- Excellent output accuracy over line and load:
  - +1.1% / –1.3% across temperature
  - +0.9% / -0.7% at 25°C
- Low-dropout: 215 mV (typ) at 1.5 A
- Programmable soft start control (SS_SET)
- Open-drain power good (PG) indicator
- Configurable power good threshold (FB_PG)
- Exposed control loop with the external compensation STAB pin
- Internal current limit with configurable behavior
- Capable of current sharing to enable higher currents

## 1.3 Applications

- Satellite electrical power system (EPS)
- Power for high-speed and high-accuracy analog circuits
  - Data Converters: ADCs and DACs (analog-to-digital and digital-to-analog converters)
  - VCOs (voltage controlled oscillators)
  - PLLs (phase-lock-loops)
  - SerDes (serializer and deserializers)
  - Imaging sensors
- Accurate supply for FPGAs (field programmable gate arrays) and DSPs (digital signal processors)
- Radiation-hardened ultra-clean analog supply for space constrained areas

# 2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7H1111EVM.

## 2.1 Input/Output Connectors and Jumper Descriptions

### 2.1.1 Jumpers

Table 2-1 contains the list of jumpers and descriptions of their function(s).

**Table 2-1. Jumpers**

| Schematic Reference | Description |
|---|---|
| J1 | $V_{IN}$ Input power banana jack. 0.85 to 7 V. |
| J2 | $V_{OUT}$ Output regulated power banana jack. As configured $V_{OUT}$ = 1.8 V. |
| J3 | GND for $V_{IN}$ banana jack. |
| J4 | $V_{COUT}$ Output regulated power SMA. |
| J5 | $V_{OUT}$ Output regulated power SMA. |
| J6 | $V_{OUT}$ Output regulated power cold nose probe connector. |
| J7 | $V_{BIAS}$ Bias input power banana jack. 2.2 to 14 V. |
| J8 | $V_{BIAS}$ Bias input power SMA. |
| J9 | GND for $V_{OUT}$ banana jack. |
| J10 | GND for $V_{IN}$ banana jack. |
| J11 | GND for $V_{BIAS}$ banana jack. |
| J12 | Three pin current limit mode jumper selector. Selects "Constant current" or "Turn-off" current limit mode. |
| J13 | Three pin enable/disable jumper selector. Pulls EN signal to $V_{IN}$ "enable" or GND "disable". No jumper will enable LDO based on $V_{IN}$ R2/R7 divider reaching 600mV enable threshold. |

### 2.1.2 Test Points

Table 2-2 contains the list of test point and descriptions of their function(s).

**Table 2-2. Test Points**

| Schematic Reference | Description |
|---|---|
| TP1 | $V_{OUT}$ Test point. This test point is prior to 0 Ω R1, and directly connected to OUT pins of LDO. |
| TP2, TP3 | $V_{COUT}$ Test points. These test points are after the 0 Ω R1. They are on the COUT plane. TP2 is used for Bode signal injection along with TP8. |
| TP4 | $V_{OUT}$ Test point. This test point is after L1 (populated with 0 Ω) in the output path. This testpoint is outside the feedback loop. |
| TP5 | $V_{IN}$ Test point. |
| TP6 | PG power good test point. |
| TP7 | EN enable test point. |
| TP8 | Feedback OUTS test point. Used for Bode signal injection along with TP2. |
| TP9 | SS_SET test point. This node defines $V_{OUT}$ regulation, and soft start. |
| TP10 | Bias test point, located on device side of the bias filter defined by R6 and C14. |
| TP11 | GND test point. |
| TP12 | Bias test point, located on source side of the bias filter defined by R6 and C14. |
| TP13 | FB_PG test point. |
| TP14, TP15 | GND test points. |

## 2.2 Equipment Setup

The following procedure guides the setup and testing of the TPS7H1111EVM.

The following equipment is required for this testing:

1. Power supply PS1 capable of up to 7 V and 1.5 A for suppling $V_{IN}$.
   - If testing current limit functionality, PS1 should be capable of 3 A.
2. Power supply PS2 capable of up to 14 V and 100 mA.
3. Electronic load or resistive load capable of > 1.5 A (or desired test load).
4. Voltage meter and/or oscilloscope for monitoring $V_{OUT}$.

The following procedure describes the connectivity, supplies, and load setup:

1. With PS1 disabled, setup with 2.5 V, and 1.5 A current limit.
2. Connect PS1 positive supply with banana cable to $V_{IN}$ + jumper J1.
3. Connect PS1 negative supply with banana cable to $V_{IN}$ GND jumper J10.
   - Alternately, $V_{IN}$ can be supplied with SMA J3. Observe current ratings of SMA cable.
4. With PS2 disabled, setup with 5 V, and 100 mA current limit.
5. Connect PS2 positive supply with banana cable to $V_{BIAS}$ + jumper J7.
6. Connect PS2 negative supply with banana cable to $V_{BIAS}$ GND jumper J11.
   - Alternately, $V_{BIAS}$ can be supplied with SMA J8.
7. Connect oscilloscope to SMA jack J5 if desired to monitor $V_{OUT}$.
   - Alternatively, the cold nose connector J6 or TP4 may be used for $V_{OUT}$ monitoring.
8. Connect voltage meter to $V_{OUT}$ using TP4, J6, J5, or J2 if needed.
9. Connect desired (≤1.5 A) load between the $V_{OUT}$ connector J2, and the GND at connector J9.

**Note**

Large $V_{IN} – V_{OUT}$ differentials can lead to excessive internal power dissipation when operating at higher $I_{LOAD}$ currents. Internal power dissipation power can be estimated with $V_{IN} – V_{OUT} \times I_{LOAD}$. See SLVSFT8 for more information on power calculations

# 3 Operation

1. Set jumper J13 to the enable position.
   - J13 can also be left open, as a resistor divider is used with $V_{IN}$ to pull the enable pin up. Enable threshold is ~600mV. Resistor divider R2/R7 can be changed to achieve different turn on voltages for $V_{IN}$. By default, device will be enabled when $V_{IN}$ > ~1.8 V for default EVM. It can also be digitally controlled from a host through J13.
2. Enable PS1, and PS2. Sequence is not important.
3. $V_{OUT}$ should now read ~1.8 V.
   - $V_{OUT}$ at load will likely be lower than 1.8 V when load applied. The OUTS connection for feedback regulation is located on the $C_{OUT}$ plane closer to U1.
4. PG output (TP6) should also now be pulled up to $V_{OUT}$ and read 1.8 V.
5. Vary the load as necessary for test purposes.

# 4 Adjustable Operation

The nominal output voltage for the TPS7H1111-SEP is configured using equation $V_{SS\_SET} = V_{OUT} = I_{SET} \times R_{SET}$. Therefore, $R_{SET} = V_{SS\_SET} / I_{SET} = 1.8\ V / 100\ \mu A = 18\ k\Omega$. $I_{SET}$ is determined by $R_{REF}$, and is designed to be 100 uA using a precision 12 kΩ resistor. See Figure 4-1 for block diagram. See Figure 7-1 for $R_{SET}$ (R8), and $R_{REF}$ (R9) connectivity. See SLVSFT8 for more detailed information.

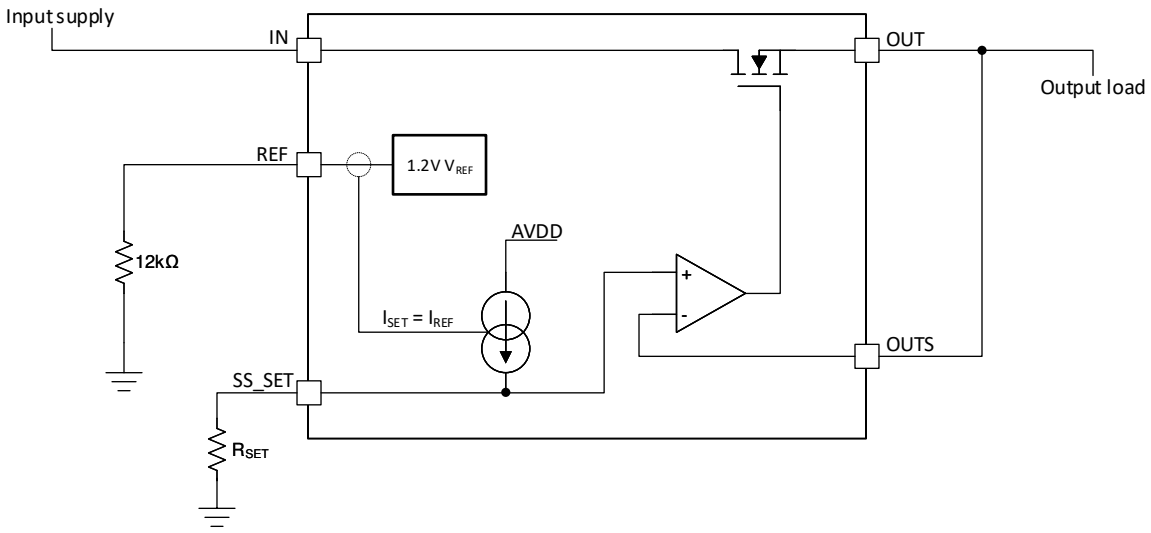


**Figure 4-1. Simplified Schematic to Configure Output Voltage**

It is also important to note that the TPS7H1111-SEP utilizes an adjustable power good PG output threshold FB_PG. When changing the output voltage, a suitable voltage divider needs to be set on the FB_PG pin in order for the LDO to assert PG when appropriate threshold achieved. Additionally when PG is asserted, this turns off internal fast charge circuit that is part of the soft start. Thus, setting appropriate divider is important for proper startup. See SLVSFT8 for more detailed information.

# 5 Test Results

This section provides typical performance waveforms for the TPS7H1111EVM with respect to stability, Noise Spectral Density (NSD), and PSRR. All performance data show is utilizing the the standard configuration of the EVM. The standard configuration is based on the following conditions: $V_{IN}$ = 2.5 V, $V_{BIAS}$ = 5 V, and $V_{OUT}$ = 1.8 V

**Note**

The datasheet for the TPS7H1111-SEP LDO contains a wide assortment of additional performance data under various input and output conditions. See SLVSFT8

## 5.1 Enable and Soft Start Timing

Figure 5-1 shows the enable and soft start characteristic where $V_{IN}$ is 2.5 V, $V_{BIAS}$ is 5 V, EN is toggled from ground to ~800 mV while the output drives a ~1.5 A resistive load. The waveforms for EN, $V_{OUT}$, SS_SET, and IOUT are shown for reference. $C_{SS}$ of 4.7uF results in a soft start time of approximately 3.7 ms.

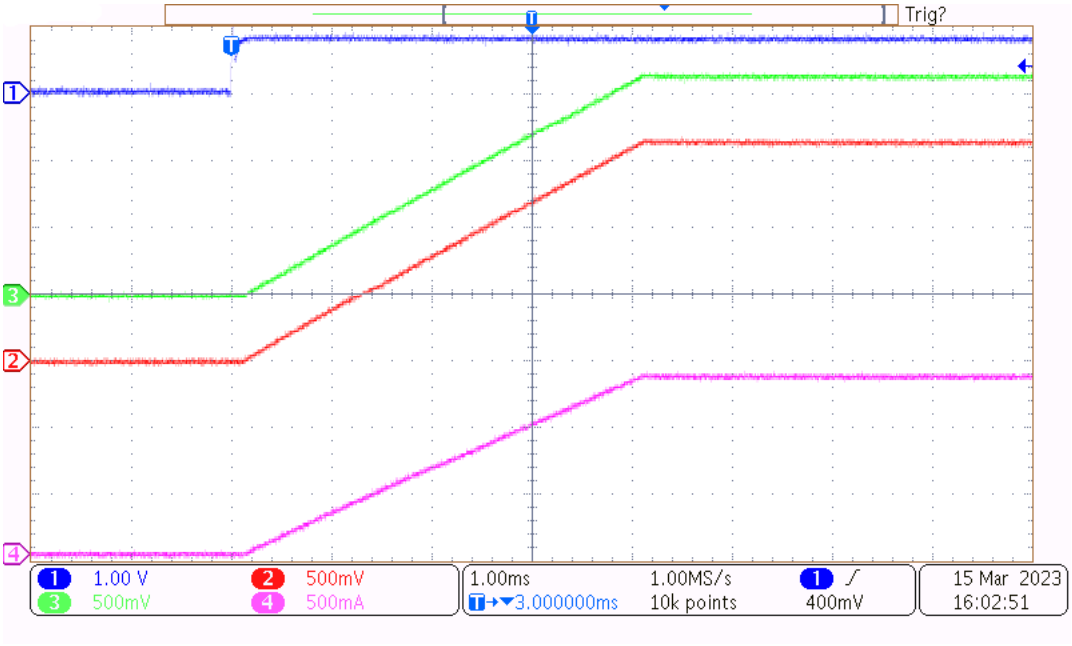


**Figure 5-1. TPS7H1111 Enable and Soft Start Timing**

## 5.2 PSRR

Figure 5-2 shows the typical PSRR performance of the TPS7H1111EVM with $I_{OUT}$ = to 1 A with the following conditions: $V_{IN}$ = 2.5 V, $V_{BIAS}$ = 5 V, $V_{OUT}$ = 1.8 V, $C_{IN}$ removed.

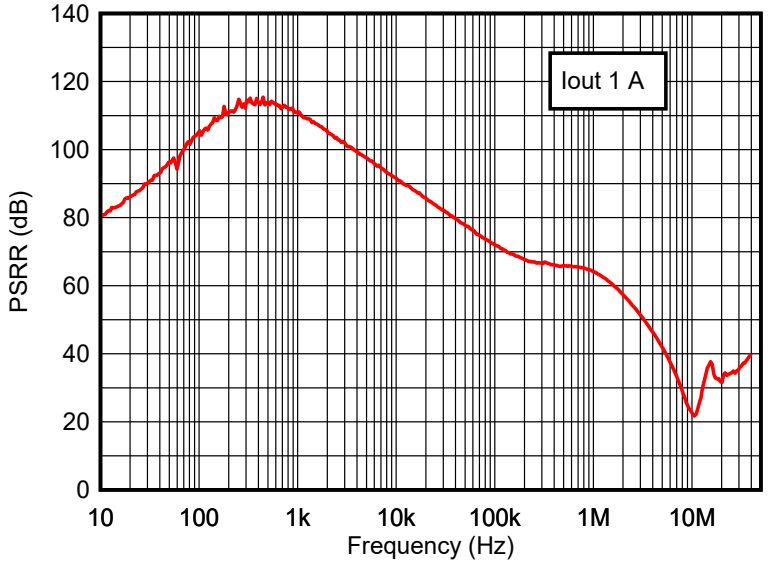


**Figure 5-2. TPS7H1111EVM PSRR**

Measuring ultra high PSRR on a device can be challenging. To obtain adequate results, the output of the LDO is fed to a wideband amplifier with approximately 50 dB of gain. Amplifying the output effectively lowers the noise floor of the measuring instrument. Once results are obtained, the gain curve of the amplifier in dBs is added to the results across the frequency span.

The injected signal on $V_{IN}$ was -10 dBm into a 50 Ω load. This results in a 200 mV pk-pk signal. Additionally a small variable amount of injected signal attenuation was used starting at 100 kHz to minimize signal distortion at higher frequencies. Final injected signal power used was -17 dBm at approximatly 2 MHz.

## 5.3 Stability

Figure 5-3 shows the typical Bode gain and phase plot versus frequency with a load of 1 A. Stability tests performed with the TPS7H1111EVM operating with the following conditions: $V_{IN}$ = 2.5 V, $V_{BIAS}$ = 5 V, $V_{OUT}$ = 1.8 V.

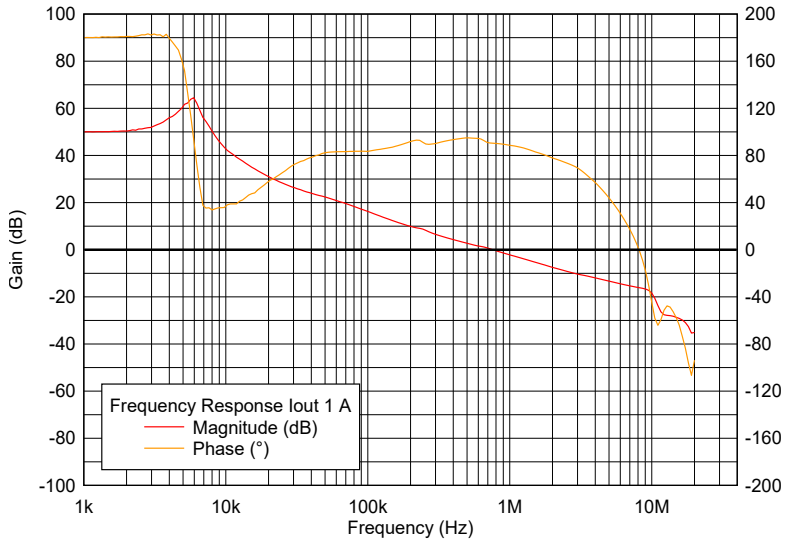


**Figure 5-3. TPS7H1111EVM Gain and Phase vs. Frequency (Bode Plot)**

Measuring accurate Bode response with a high bandwidth high gain LDO required using a very small injected signal. The signal injected used a shape for injected level with an injected signal reference level of -7 dBm. This reference level was reduced to -27 dBm from 10 kHz to 200 kHz. Additionally, the entire injected signal was externally attenuated with an inline attenuator by 26 dB. This was required to prevent overdriving the signal into feedback loop and keeping response within small signal behavior.

## 5.4 Noise Spectral Density

Figure 5-4 shows the typical Noise Spectral Density (NSD) performance of the TPS7H1111EVM operating with a 1 A load and the following conditions: $V_{IN}$ = 2.5 V, $V_{BIAS}$ = 5 V, $V_{OUT}$ = 1.8 V.

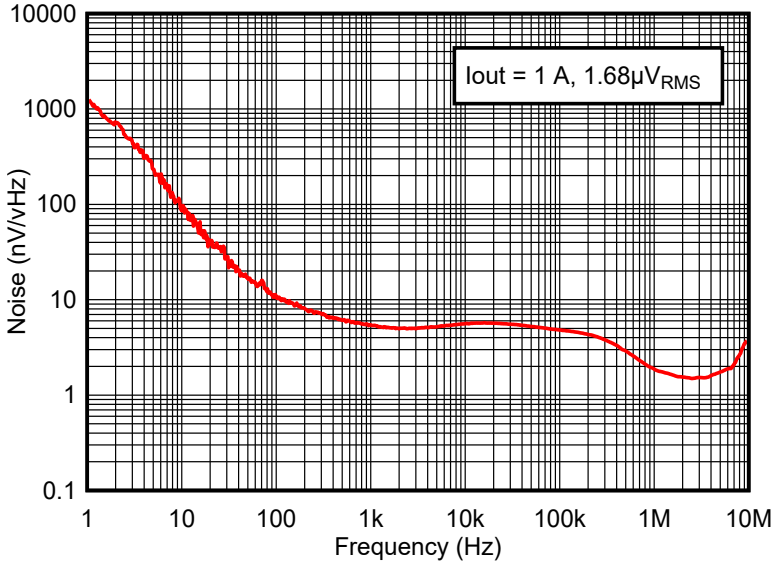


**Figure 5-4. Output Noise vs. Frequency (Noise Spectral Density)**

## 6 Board Layout

The following images represent the board design layers.

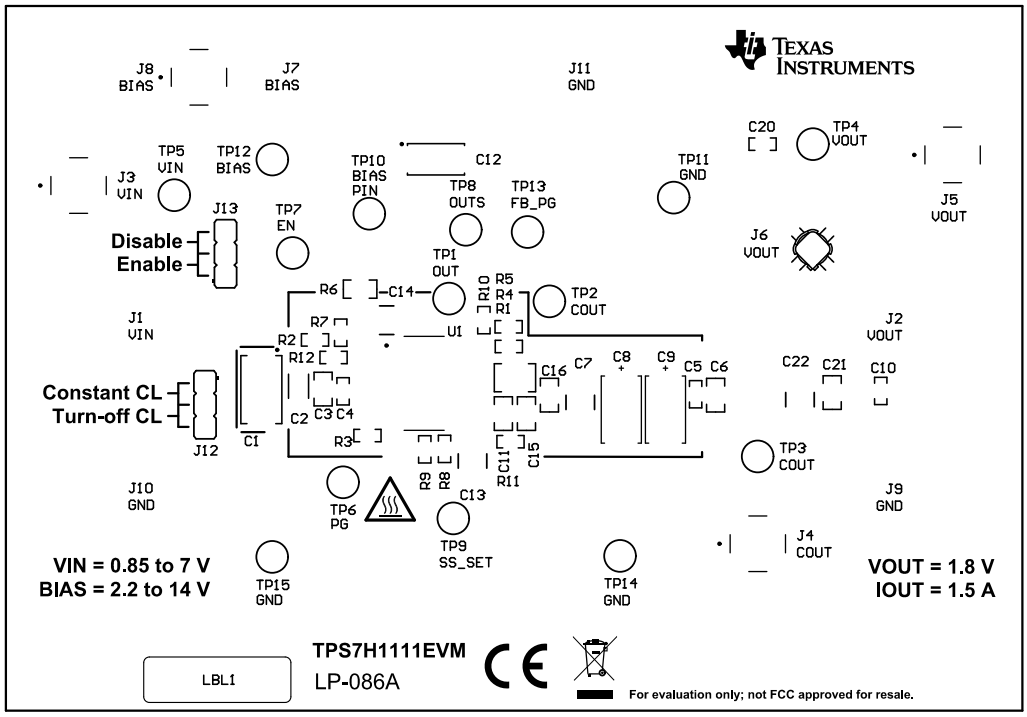


**Figure 6-1. Top Overlay Silkscreen**

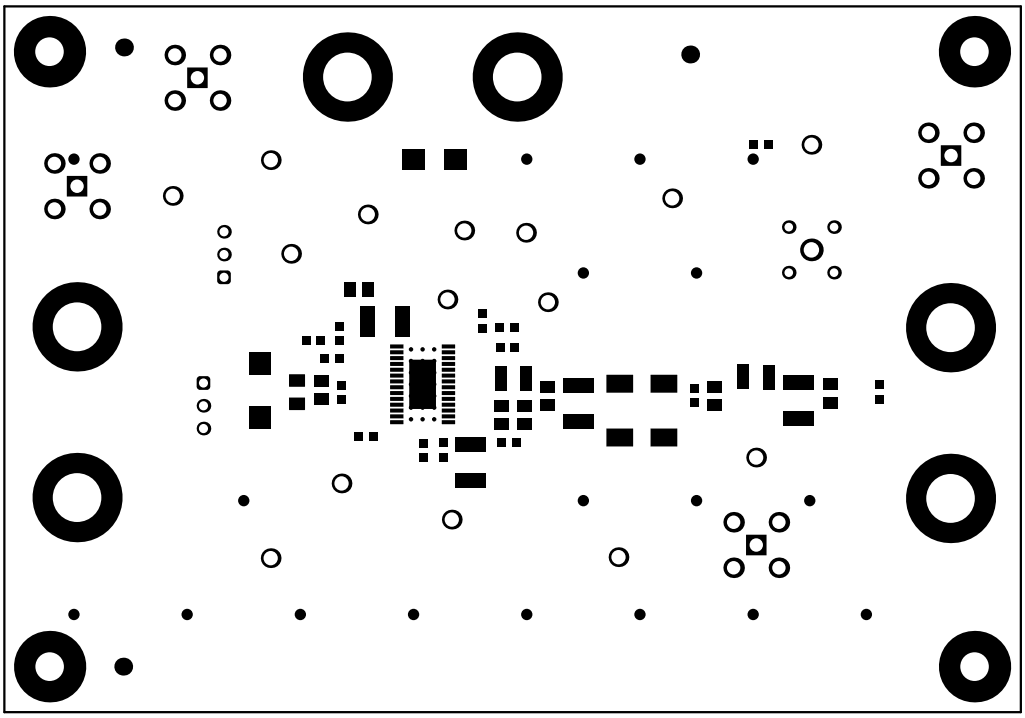

**Figure 6-2. Top Solder Mask**

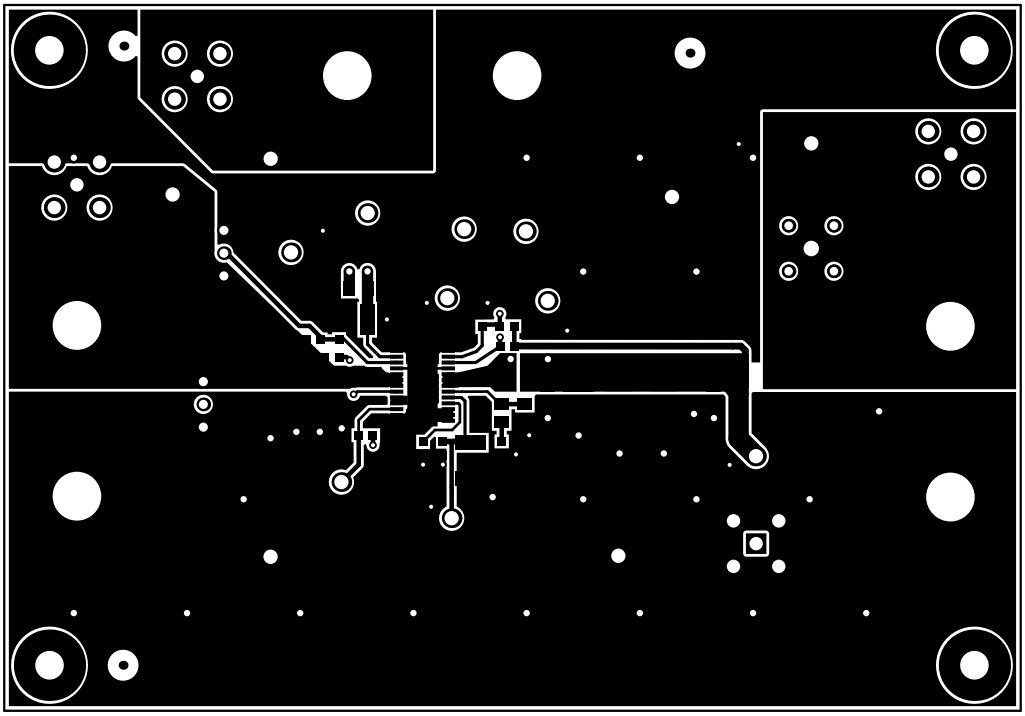

**Figure 6-3. Top Signal Layer**

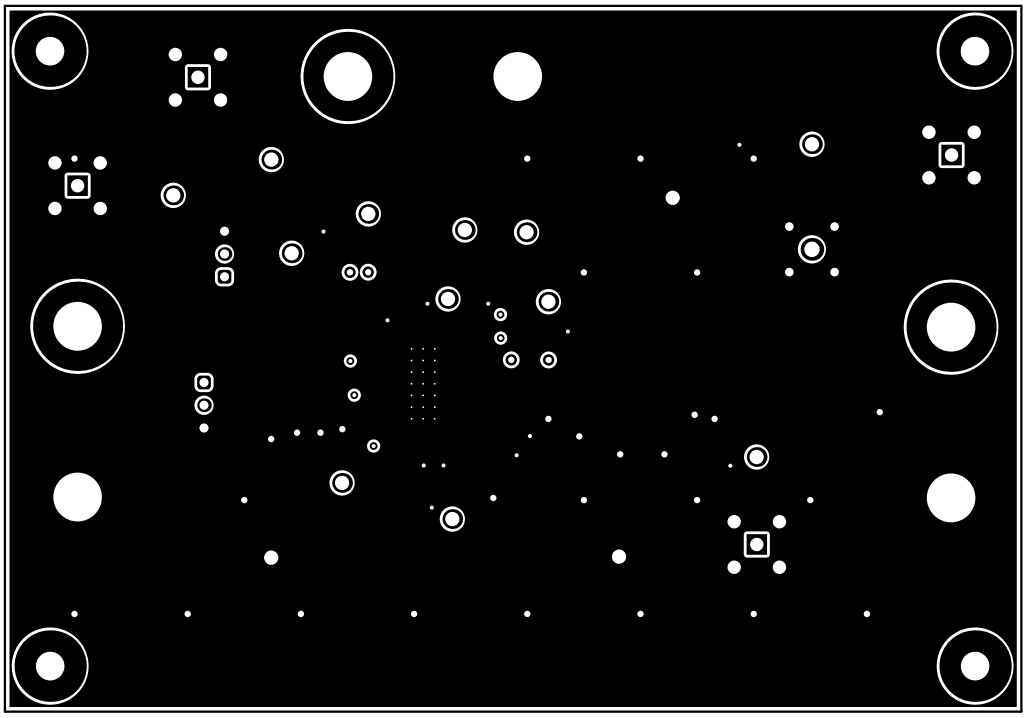

**Figure 6-4. Signal 1 Layer**

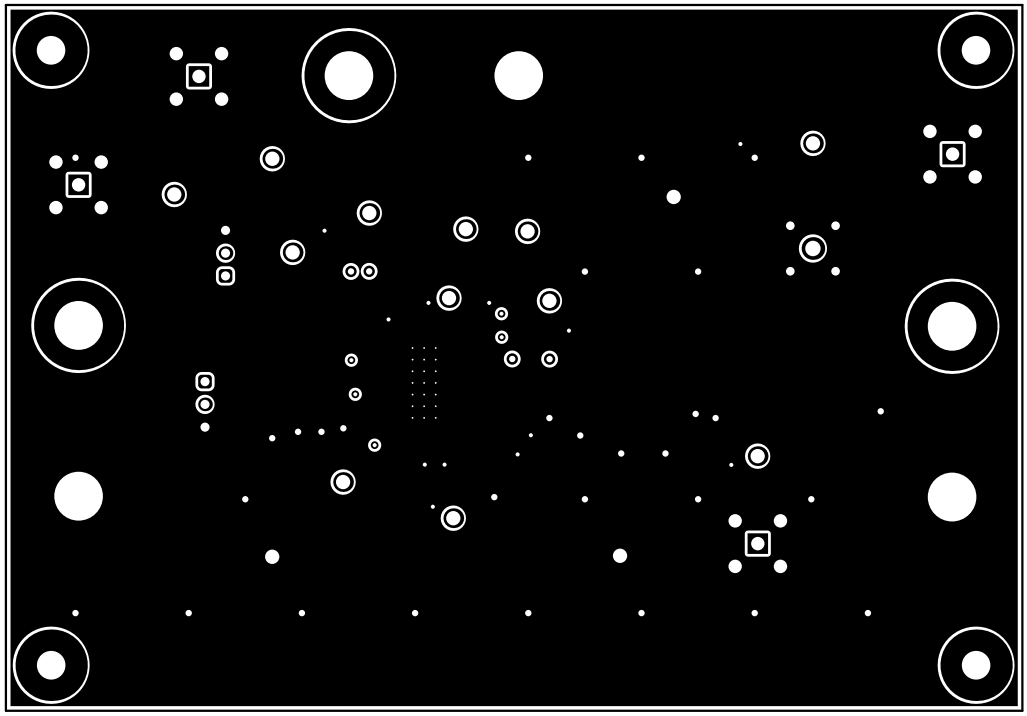

**Figure 6-5. Signal 2 Layer**

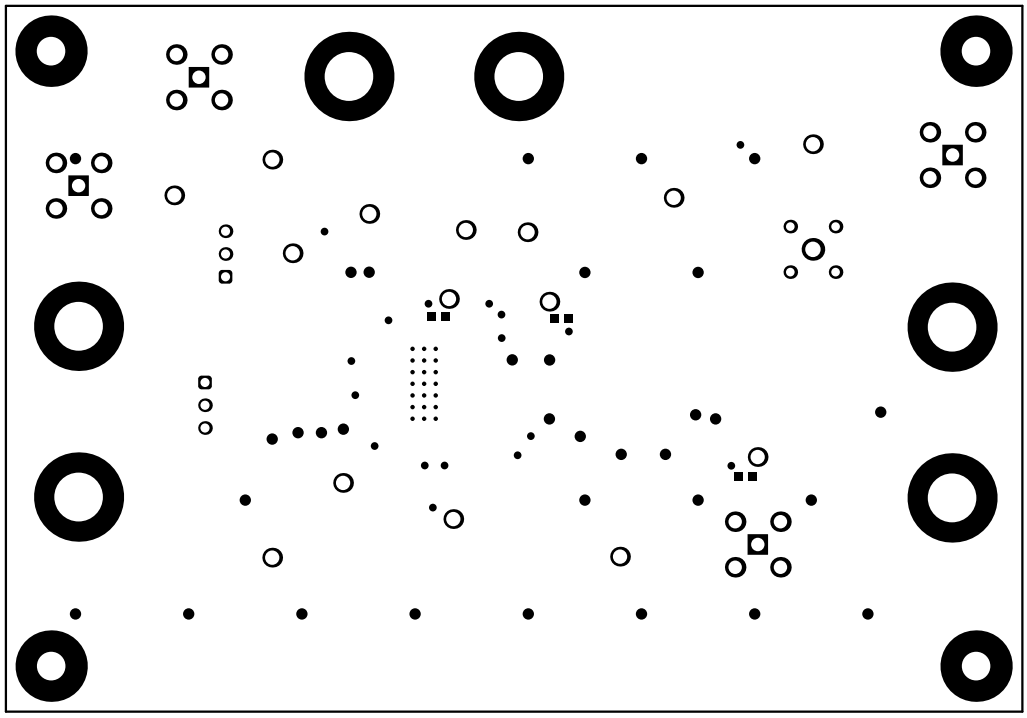

**Figure 6-6. Bottom Solder Layer**

# 7 Schematic

## TPS7H1111-SEP EVM - Schematic

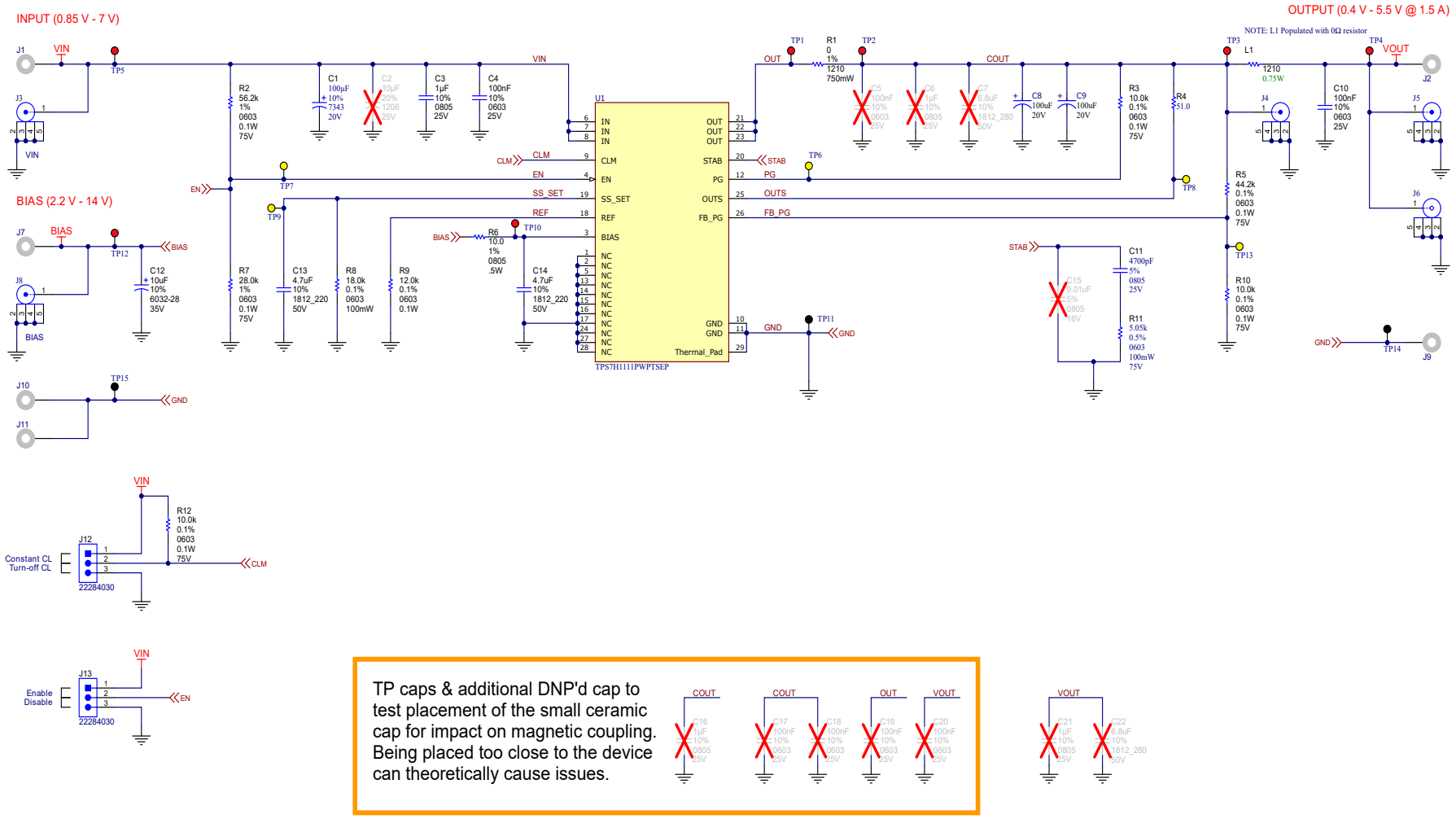


**Figure 7-1. TPS7H1111EVM (LP086A) Schematic**

# 8 Bill of Materials

**Table 8-1. Bill of Materials LP086A**

| Designator | Qty | Description | Part Number | Manufacturer |
|---|---|---|---|---|
| C1 | 1 | Capacitor, tantalum, 100 µF, 20 V, ±10%, 0.4 Ω, AEC-Q200 Grade 1, SMD, 7343-43 | TAJE107K020TNJV | AVX |
| C3 | 1 | Capacitor, ceramic, 1 µF, 25 V, ±10%, X7R, 0805 | TMK212B7105KG-T | Taiyo Yuden |
| C4 | 1 | Capacitor, ceramic, 0.1 µF, 25 V, ±10%, X7R, 0603 | 8.85012E+11 | Wurth Elektronik |
| C8, C9 | 2 | Cap Tant Solid 100uF 20V E CASE 10% (7.3 X 4.1 X 4.3mm) SMD 7343-43 0.035 Ohm 125°C T/R | TRME107K020R0035 | KYOCERA AVX |
| C11 | 1 | Capacitor, ceramic, 4700 pF, 25 V, ±5%, C0G/NP0, 0805 | 08053A472JAT2A | AVX |
| C12 | 1 | Capacitor, tantalum, 10 µF, 35 V, ±10%, 1.6 Ω, SMD, 6032-28 | 293D106X9035C2TE3 | Vishay-Sprague |
| C13, C14 | 2 | Capacitor, ceramic, 4.7 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, | CGA8M3X7R1H475K200KB | TDK |
| J1, J2, J7, J9, J10, J11 | 6 | Standard banana jack, uninsulated, 5.5 mm | 575-4 | Keystone |
| J3, J4, J5, J8 | 4 | SMA Connector Receptacle, Female Socket 50 Ω Through Hole Solder, PTH_RF_CONN | 733910060 | Molex |
| J6 | 1 | Compact Probe Tip Circuit Board Test Points, TH, 25 per, TH Scope Probe | 131-5031-00 | Tektronix |
| J12, J13 | 2 | Header, 2.54 mm, 3x1, tin, TH | 22284030 | Molex |
| L1, R1 | 2 | Resistor, 0 Ω, 1%, 0.75 W, AEC-Q200 Grade 0, 1210 | CRCW12100000Z0EAHP | Vishay-Dale |
| R2 | 1 | Resistor, 56.2 kΩ, 1%, 0.1 W, 0603 | RC0603FR-0756K2L | Yageo |
| R3, R10, R12 | 3 | Resistor, 10.0 kΩ, 0.1%, 0.1 W, 0603 | RT0603BRD0710KL | Yageo America |
| R4 | 1 | Resistor, 51.0 Ω, 1%, 0.1 W, 0603 | RC0603FR-0751RL | Yageo |
| R5 | 1 | Resistor, 44.2 kΩ, 0.1%, 0.1 W, 0603 | RT0603BRD0744K2L | Yageo America |
| R6 | 1 | Resistor, 10.0 Ω, 1%, .5 W, AEC-Q200 Grade 0, 0805 | ERJ-P6WF10R0V | Panasonic |
| R7 | 1 | Resistor, 28.0 kΩ, 1%, 0.1 W, 0603 | RC0603FR-0728KL | Yageo |
| R8 | 1 | Resistor, 18.0 kΩ, 0.1%, 0.1 W, 0603 | RT0603BRD0718KL | Yageo America |
| R9 | 1 | Resistor, 12.0 kΩ, 0.1%, 0.1 W, 0603 | RT0603BRD0712KL | Yageo America |
| R11 | 1 | Resistor, 5.05 kΩ, 0.5%, 0.1 W, 0603 | RT0603DRE075K05L | Yageo America |
| TP1, TP2, TP3, TP4, TP5, TP10, TP12 | 7 | Test point, multipurpose, red, TH | 5010 | Keystone Electronics |
| TP6, TP7, TP8, TP9, TP13 | 5 | Test point, multipurpose, yellow, TH | 5014 | Keystone Electronics |
| TP11, TP14, TP15 | 3 | Test point, multipurpose, black, TH | 5011 | Keystone Electronics |
| U1 | 1 | 1.5-A, Ultra-Low Noise, High PSRR Radiation Hardened LDO (SOP28) | TPS7H1111PWPTSEP | Texas Instruments |
| C2 | 0 | Capacitor, tantalum polymer, 10 µF, 25 V, ± 20%, 0.15 Ω, 3216-18 SMD | TCJA106M025R0150 | AVX |
| C5, C10, C17, C18, C19, C20 | 0 | Capacitor, ceramic, 0.1 µF, 25 V, ±10%, X7R, 0603 | C1608X7R1E104K080AA | TDK |
| C6, C16, C21 | 0 | Capacitor, ceramic, 1 µF, 25 V, ±10%, X7R, 0805 | TMK212B7105KG-T | Taiyo Yuden |
| C7, C22 | 0 | Capacitor, ceramic, 6.8 µF, 50 V, ± 10%, X7R, AEC-Q200 Grade 1, | CGA8P3X7R1H685K250KB | TDK |
| C15 | 0 | Capacitor, ceramic, 0.01 µF, 16 V, ±5%, C0G/NP0, 0805 | B37947K9103J62 | TDK |

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