Technical Reference Manual

TPS65917-Q1 Technical Reference Manual: O917A186TRGZRQ1 OTP Settings

ABSTRACT

This technical reference manual serves as an overview for the specific device settings of the O917A186TRGZRQ1.

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Trademarks

1 Introduction

This technical reference manual can be used as a guide for using the TPS65917-Q1 PMIC. This guide describes the power-up, power-down, and sleep entry and exit sequences along with the OTP configurations. In addition, this technical reference manual describes the initialization software and advises how to get started with the TPS65917-Q1 PMIC. This document does not provide details about the power resources, external components, or the functionality of the device. For such information, see the TPS65917-Q1 data sheet, *TPS65917-Q1 Power Management Unit (PMU) for Processor*.

In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the data sheet specification is the definitive source.

2 BOOT OTP Configuration

All TPS65917-Q1 resource settings are stored in the form of registers. Therefore, all platform-related settings are linked to an action altering these registers. This action can be a static update (register initialization value) or a dynamic update of the register (either from the user or from a power sequence).

Resources and platform settings are stored in nonvolatile memory (OTP). These settings are defined as follows:

Static platform settings	These settings define, for example, SMPS or LDO default voltages, and GPIO functionality. Most static platform settings can be overwritten by a power sequence or by the user.
Sequence platform settings	These settings define the TPS65917-Q1 power sequences between state transitions, such as the OFF2ACT sequence when transitioning from OFF mode to ACTIVE mode. The power sequence is composed of several register accesses that define which resources (and the corresponding registers) must be updated during the respective state transition. The state of these resources can be overwritten by the user after the power sequence completes execution.

3 Static Platform Settings

Each device has predefined values stored in OTP which control the default configuration of the device. The tables in this section list the OTP-programmed values for OTP 0x86, distinguished by the SW_REVISION.

3.1 System Voltage Monitoring

Table 3-1. System Voltage Monitoring OTP Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE	UNIT
VSYS_MON	VSYS_HI	System voltage rising-edge threshold	3.1	V
VSYS_LO	VSYS_LO	System voltage falling-edge threshold	2.75	V

Comparators that monitor the voltage on the VCC_SENSE, and VCCA pins control the power state machine of the TPS65917-Q1 device. For electrical parameters, refer to the data sheet.

POR When the supply at the VCCA pin is below the POR threshold, the TPS65917-Q1 device is in the NO SUPPLY state. All functionality is off. The device moves from the NO SUPPLY state to the BACKUP state when the voltage in VCCA rises above the POR threshold.

VSYS_LO When the voltage on the VCCA pin rises above VSYS_LO, the device enters from the BACKUP state to the OFF state. When the device is in an ACTIVE, SLEEP, or OFF state and the voltage on VCCA decreases below the VSYS_LO level, the device enters backup mode. The level of VSYS_LO is OTP programmable.

VSYS_MON During power up, the value of VSYS_HI OTP is used as a threshold for the VSYS_MON comparator which is gating PMIC start-up (that is, as a threshold for transition from the OFF state to the ACTIVE state). The VSYS_MON comparator monitors the VCC_SENSE pin. After power up, software can configure the comparator threshold in the VSYS_MON register.

VBUS_DET The VBUS_DET comparator is monitoring the VBUS_SENSE (secondary function of GPIO1) pin. This comparator is active when VCCA is greater than the POR threshold. Triggering the threshold level generates an interrupt. It can wake up the device from the SLEEP state, but can also switch on the device from the OFF state.

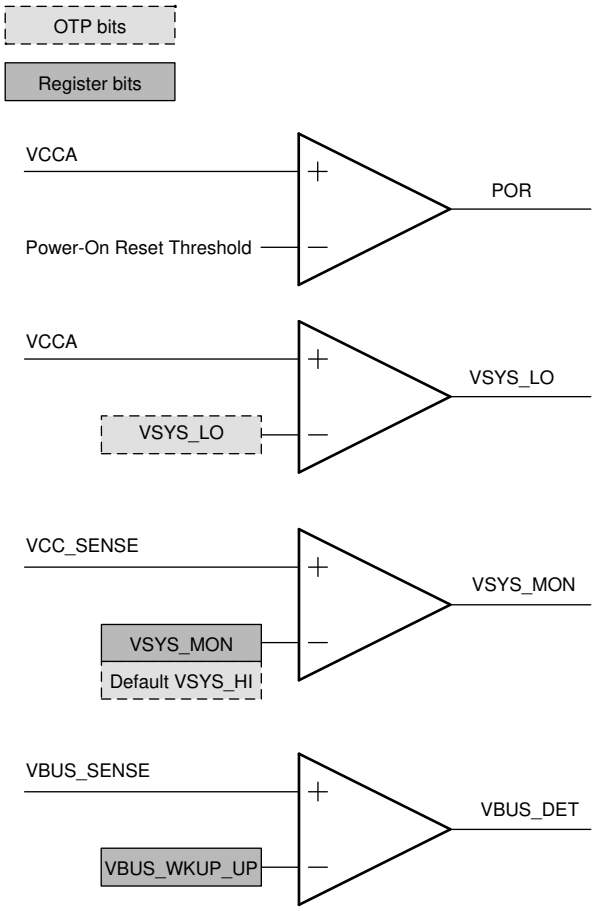

Figure 3-1. PMIC Comparators

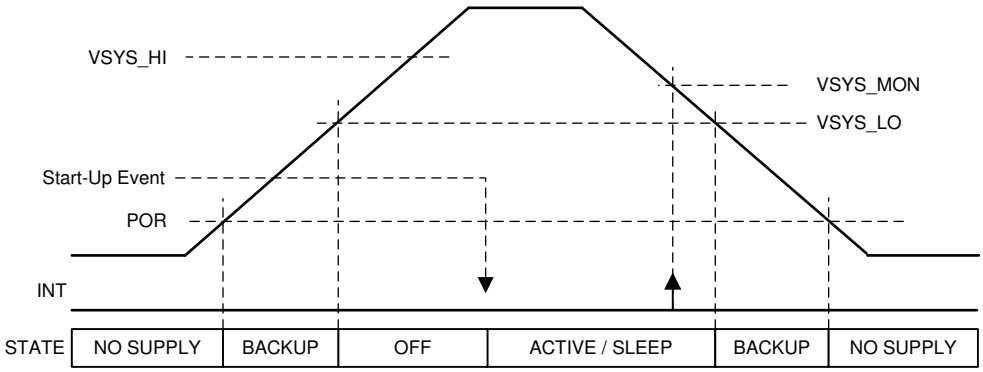

Figure 3-2. State Transitions

Note

The maximum input voltage of the VCC_SENSE pin depends on the OTP setting of PMU_CONFIG [HIGH_VCC_SENSE] as listed in the *Recommended Operating Conditions* table of the TPS65917-Q1 data sheet. This configuration is set as HIGH_VCC_SENSE = 0 with the VCC_SENSE and pins are connected to VCCA.

For the recommended operating conditions of the electrical parameters, see the TPS65917-Q1 data sheet, TPS65917-Q1 Power Management Unit (PMU) for Processor.

3.2 SMPS

This section describes the default voltage for each SMPS.

Table 3-2. SMPS OTP Settings

BIT	DESCRIPTION	OTP VALUE	UNIT
SMPS1_VOLTAGE	Default output voltage for the regulator	1.10	V
SMPS2_VOLTAGE	Default output voltage for the regulator	1.10	V
SMPS3_VOLTAGE	Default output voltage for the regulator	1.10	V
SMPS4_VOLTAGE	Default output voltage for the regulator	1.80	V
SMPS5_VOLTAGE	Default output voltage for the regulator	1.10	V
SMPS1_SMPS12_EN	SMPS12 single-phase or dual-phase configuration. 0: SMPS1 and SMPS2 single-phase 1: SMPS12 dual-phase	0	NA

3.3 LDO

This section describes the default output voltage for each LDO.

Table 3-3. LDO OTP Settings

BIT	DESCRIPTION	OTP VALUE	UNIT
LDO1_VOLTAGE	Default output voltage for the regulator	1.8	V
LDO2_VOLTAGE	Default output voltage for the regulator	1.8	V
LDO3_VOLTAGE	Default output voltage for the regulator	1.8	V
LDO4_VOLTAGE	Default output voltage for the regulator	Off	NA
LDO5_VOLTAGE	Default output voltage for the regulator	Off	NA

Note

LDO1 and LDO2 share a single input LDO12_IN and must by supplied by the same voltage. Refer to the input voltage parameter in the data sheet.

3.4 Interrupts

The interrupts are split into four register groups (INT1, INT2, INT3, and INT4). All interrupts are logically combined on a single output line, INT (default active-low). This line is used as an external interrupt line to warn the host processor of any interrupt event that has occurred within the device. The OTP settings in this section show whether each interrupt is enabled or disabled by default.

Table 3-4. INT1 OTP Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
INT1_MASK	VSYS_MON	Enable and disable interrupt from the VSYS_MON comparator	1: Interrupt generation disabled
	PWRDOWN	Enable and disable interrupt from the PWRDOWN pin	1: Interrupt generation disabled
	PWRON	Enable and disable interrupt from PWRON pin. A PWRON event is always an ON request.	1: Interrupt generation disabled
	LONG_PRESS_KEY	Enable and disable interrupt from long key press on the PWRON pin	1: Interrupt generation disabled
	HOTDIE	Enable and disable interrupt from device hot-die detection. The interrupt can be used as a pre-warning for processor to limit the PMIC load, before increasing die temperature forces shutdown.	0: Interrupt generated

Table 3-5. INT2 OTP Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
INT2_MASK	SHORT	Triggered from internal event of SMPS or LDO outputs failing. If an interrupt is enabled, it is an ON request.	0: Interrupt generated
	WDT	Enable and disable interrupt from watchdog expiration	1: Interrupt generation disabled
	FSD	Enable and disable First Supply Detection (FSD) interrupt	1: Interrupt generation disabled
	RESET_IN	Enable and disable interrupt from the RESET_IN pin	1: Interrupt generated disabled

Table 3-6. INT3 OTP Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
INT3_MASK	VBUS	Interrupt to detect rising or falling VBUS line	1: Interrupt generation disabled
	GPADC_EOC_SW	GPADC result ready from software-initiated conversion	1: Interrupt generation disabled
	GPADC_AUTO_1	GPADC automatic conversion result 1 above or below the reference threshold	1: Interrupt generation disabled
	GPADC_AUTO_0	GPADC automatic conversion result 0 above or below the reference threshold	1: Interrupt generation disabled

Table 3-7. INT4 OTP Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
INT4_MASK	GPIO_6	Enable and disable interrupt from the GPIO6 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_5	Enable and disable interrupt from the GPIO5 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_4	Enable and disable interrupt from the GPIO4 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_3	Enable and disable interrupt from the GPIO3 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_2	Enable and disable interrupt from the GPIO2 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_1	Enable and disable interrupt from the GPIO1 pin rising or falling edge	1: Interrupt generation disabled
	GPIO_0	Enable and disable interrupt from the GPIO0 pin rising or falling edge	1: Interrupt generation disabled

3.5 GPIO

TPS65917-Q1 integrates eight configurable general-purpose I/Os (GPIOs) that are multiplexed with alternative features. This section describes the default configuration of each GPIO, as well as the configuration of internal pullup or pulldown resistors on the GPIOs.

Table 3-8. GPIO Function OTP Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
PRIMARY_SECONDARY_PAD2	GPIO_6	Select pin function	REGEN3
	GPIO_5	Select pin function	POWERHOLD
	GPIO_4	Select pin function	REGEN2
PRIMARY_SECONDARY_PAD1	GPIO_3	Select pin function	SYNCDCDC
	GPIO_2	Select pin function	GPIO_2
	GPIO_1	Select pin function	RESET_IN
	GPIO_0	Select pin function	REGEN1

Note

The GPIO_0 pin is an open drain pin and therefore must be pulled up externally. TI does not recommend pulling the GPIO_0 pin up to any always-on signal such as VCCA or LDOVRTC_OUT. The GPIO_0 pin is configured as an input before the OTP memory is loaded at power up, and pulling the pin up to an always-on rail can cause a glitch on the GPIO_0 pin. Therefore, TI recommends pulling this signal up to a sequenced output, such as SMPS3 (1.8 V) or LDO4 (3.3 V).

Table 3-9 describes the pullup, pulldown, and open-drain settings for the corresponding GPIOs. These settings only apply in GPIO mode (example: GPIO_0), and do not apply to any of the secondary functions (example: REGEN1).

Table 3-9. GPIO Pullup, Pulldown, and Open Drain Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
PU_PD_GPIO_CTRL2	GPIO_6_PD	Configure pulldown for GPIO_6	0: Pulldown disabled
	GPIO_5_PD	Configure pulldown for GPIO_5	0: Pulldown disabled
	GPIO_4_PU	Configure pullup for GPIO_4	0: Pullup disabled
	GPIO_4_PD	Configure pulldown for GPIO_4	0: Pulldown disabled
PU_PD_GPIO_CTRL1	GPIO_3_PD	Configure pulldown for GPIO_3	0: Pulldown disabled
	GPIO_2_PU	Configure pullup for GPIO_2	0: Pullup disabled
	GPIO_2_PD	Configure pulldown for GPIO_2	0: Pulldown disabled
	GPIO_1_PD	Configure pulldown for GPIO_1	0: Pulldown disabled
	GPIO_0_PD	Configure pulldown for GPIO_0	0: Pulldown disabled

Table 3-9. GPIO Pullup, Pulldown, and Open Drain Settings (continued)

REGISTER	BIT	DESCRIPTION	OTP VALUE
OD_OUTPUT_GPIO	GPIO_4_OD	Configure GPIO_4 to be open-drain or push-pull	1: Open-drain
	GPIO_2_OD	Configure GPIO_2 to be open-drain or push-pull	0: Push-pull

Table 3-10 describes the polarity settings for each GPIO. These settings apply to both GPIO mode and secondary functions.

Table 3-10. GPIO Polarity Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
POLARITY_CTRL	GPIO_6_POLARITY	Enable or disable polarity inversion for GPIO_6	0: Inversion disabled
	GPIO_5_POLARITY	Enable or disable polarity inversion for GPIO_5	0: Inversion disabled
	GPIO_4_POLARITY	Enable or disable polarity inversion for GPIO_4	0: Inversion disabled
	GPIO_3_POLARITY	Enable or disable polarity inversion for GPIO_3	0: Inversion disabled
	GPIO_2_POLARITY	Enable or disable polarity inversion for GPIO_2	0: Inversion disabled
	GPIO_1_POLARITY	Enable or disable polarity inversion for GPIO_1	1: Inversion enabled
	GPIO_0_POLARITY	Enable or disable polarity inversion for GPIO_0	0: Inversion disabled

3.6 MISC

This section describes miscellaneous device configuration settings including pulldowns, polarity of signals, communication settings, and other functionality.

Table 3-11. MISC1 OTP Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
PU_PD_INPUT_CTRL1	RESET_IN_PD	Enable and disable internal pulldown for the RESET_IN pin	1: Pulldown enabled
	PWRDOWN_PD	Enable and disable internal pulldown for the PWRDOWN pin	1: Pulldown enabled

Table 3-12. MISC2 OTP Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
I2C_SPI	I2C_SPI	Selection of control interface, I^2C, or SPI	0: I^2C
	ID_I2C2	I2C_2 address for page access versus initial address (0H12)	0: Address is 0x12
	ID_I2C1	I2C_1 address for I^2C register access	I2C_1[0] = 1: 0x58 I2C_1[1] = 1: 0x59 I2C_1[2] = 1: 0x5A I2C_1[3] = 1: 0x5B
PMU_CONFIG	HIGH_VCC_SENSE	Enable internal buffers on VCC_SENSE to allow voltage sensing above 5.25 V	0: High VCC sense not enabled
	AUTODEVON	Automatically set DEV_ON bit after startup sequence completes	0: AUTODEVON disabled
	SWOFF_DLY	Delay before switch-off to allow host processor to save context. Device is maintained as ACTIVE until delay expiration then switches off.	00: No delay
PMU_CTRL2	INT_LINE_DIS	Configure INT output to be standard buffer or high-impedance buffer with pullup to VIO	0: Standard buffer: open-drain or push-pull
	WDT_HOLD_IN_SLEEP	Configure watchdog timer operation during device sleep state	1: Watchdog timer does not run in sleep state
	PWRDOWN_FASTOFF	Configure shut-down sequence from PWRDOWN pin event	0: PWRDOWN pin event triggers sequenced shut down
	TSHUT_FASTOFF	Configure shut-down sequence from thermal shutdown event	0: Thermal shutdown triggers sequenced shut down
OD_OUTPUT_CTRL2	RESET_OUT_OD	Configure RESET_OUT to be push-pull or open-drain	1: RESET_OUT is open-drain
	REGEN2_OD	Configure REGEN2 to be push-pull or open-drain	1: REGEN2 is open-drain
PMU_SECONDARY_INT	FSD_MASK	Secondary level of mask for FSD interrupt line	1: FSD_INT_SRC is masked
POLARITY_CTRL	INT_POLARITY	Configure polarity of INT line	0: INT line is low when interrupt is pending

Table 3-12. MISC2 OTP Settings (continued)

REGISTER	BIT	DESCRIPTION	OTP VALUE
PRIMARY_SECONDARY_PAD2	SYNCCLKOUT	Configure SYNCCLKOUT to output SYNCDCDCCLK or CLK32KGO	0: SYNCDCDCCLK

3.7 SWOFF_HWRST

This section describes whether each reset type is configured to generate a HWRST or SWORST.

Hardware reset (HWRST) A hardware reset occurs when any OFF request is configured to generate a hardware reset. This reset triggers a transition to the OFF state from either the ACTIVE or SLEEP state (execute either the ACT2OFF or SLP2OFF sequence).

Switch-off reset (SWORST) A switch-off reset occurs when any OFF request is configured to not generate a hardware reset. This reset acts as the HWRST, except only the SWO registers are reset. The device enters the OFF state, from either ACTIVE or SLEEP, and therefore executes the ACT2OFF or SLP2OFF sequence.
The power resource control registers for SMPS and LDO voltage levels and operating mode control are in SWORST domain. Additionally, some registers control the 32-kHz, REGENx and SYSENx, watchdog, and VSYS_MON comparator. This list is indicative only.

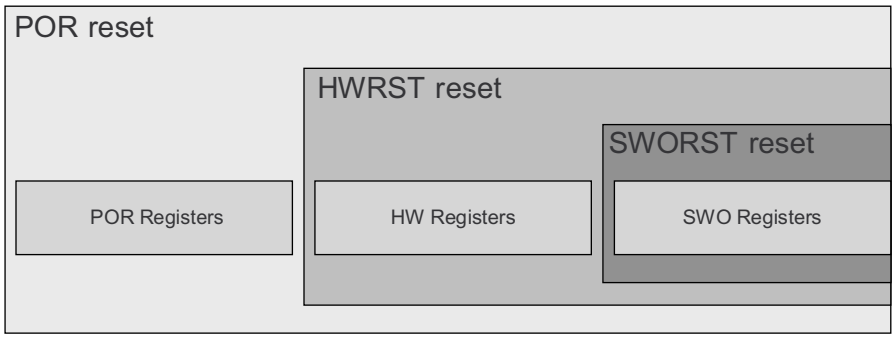

Figure 3-3. Reset Levels versus Registers

Table 3-13. SWOFF_HWRST OTP Settings

REGISTER	BIT	DESCRIPTION	0x30, 0x31, 0x32, 0x33 VALUE
SWOFF_HWRST	PWRON_LPK	Define if PWRON long key press is causing HWRST or SWORST	1: HWRST
	PWRDOWN	Define if PWRDOWN pin is causing HWRST or SWORST	0: SWORST
	WTD	Define if watchdog expiration is causing HWRST or SWORST	1: HWRST
	TSHUT	Define if thermal shutdown is causing HWRST or SWORST	1: HWRST
	RESET_IN	Define if RESET_IN pin is causing HWRST or SWORST	1: HWRST
	SW_RST	Define if register bit is causing HWRST or SWORST	1: HWRST
	VSYS_LO	Define if VSYS_LO is causing HWRST or SWORST	1: HWRST
	GPADC_SHUTDOWN	Define if GPADC event is causing HWRST or SWORST	0: SWORST

3.8 Shutdown_ColdReset

These OTP settings show whether each OFF request is configured to generate a shutdown request (SD) or cold reset request (CR).

- When configured to generate an SD, the embedded power controller (EPC) executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and remains in the OFF state.
- When configured to generate a CR, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and restarts, transitioning to the ACTIVE state (OFF2ACT power sequence) if none of the ON request gating conditions are present.

Table 3-14. Shutdown_ColdReset OTP Settings

REGISTER	BIT	DESCRIPTION	OTP VALUE
SWOFF_COLDRST	PWRON_LPK	Define if PWRON long key press causes shutdown or cold reset	0: Shutdown
	PWRDOWN	Define if PWRDOWN pin causes shutdown or cold reset	0: Shutdown
	WTD	Define if watchdog timer expiration causes shutdown or cold reset	1: Cold reset
	TSHUT	Define if thermal shutdown causes shutdown or cold reset	0: Shutdown
	RESET_IN	Define if RESET_IN pin causes shutdown or cold reset	1: Cold reset
	SW_RST	Define if SW_RST register bit causes shutdown or cold reset	1: Cold reset
	VSYS_LO	Define if VSYS_LO causes shutdown or cold reset	0: Shutdown
	GPADC_SHUTDOWN	Define if GPADC shutdown causes shutdown or cold reset	0: Shutdown

4 Sequence Platform Settings

A power sequence is an automatic preprogrammed sequence handled by the TPS65917-Q1 device to configure the device resources: SMPSs, LDOs, part of GPIOs, and REGEN signals into ON, OFF, or SLEEP state.

4.1 OFF2ACT Sequences

When an ON request occurs in the OFF state, the device is switched on and each resource is enabled based on the programmed OFF2ACT sequence.

OFF2ACT Sequence of O917A186TRGZRQ1 shows the OFF2ACT sequence of the O917A186TRGZRQ1 device.

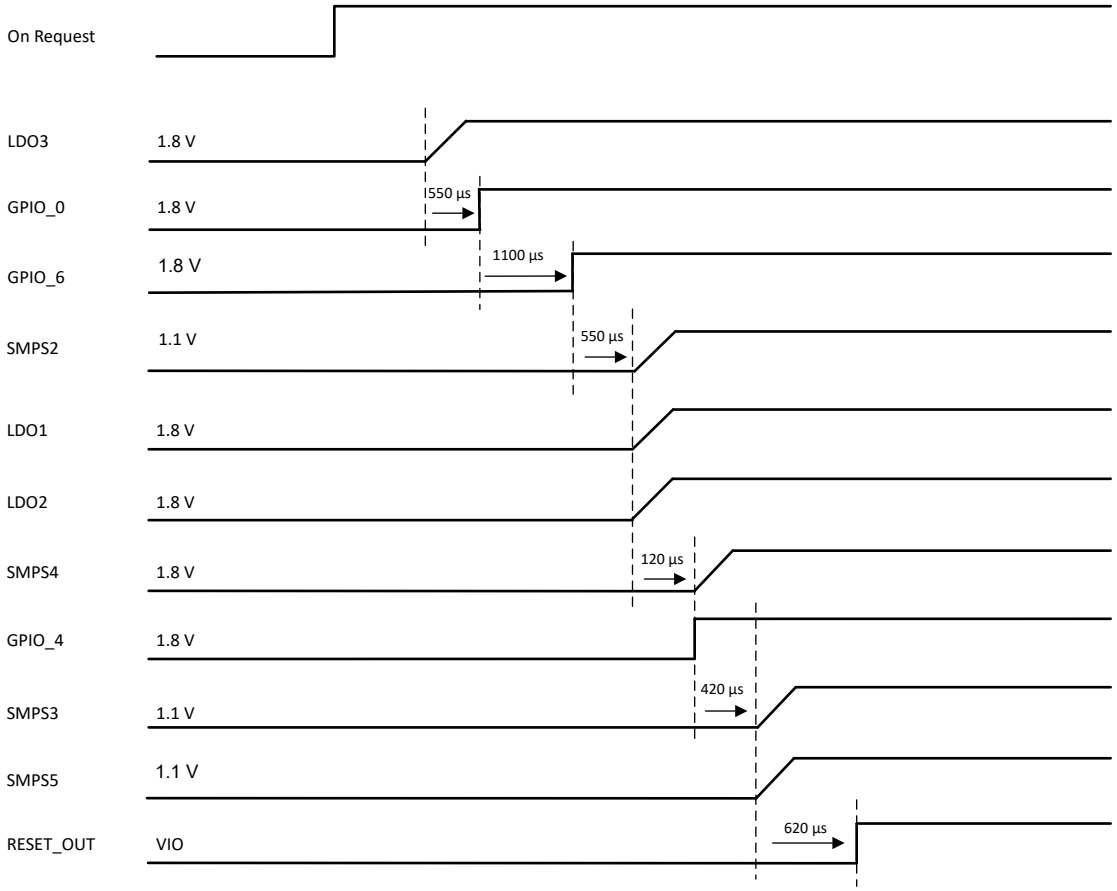

Figure 4-1. OFF2ACT Sequence of O917A186TRGZRQ1

4.2 ACT2OFF Sequences

When an OFF request occurs during active mode, each resource is disabled based on the programmed ACT2OFF sequence.

Figure 4-2 shows the ACT2OFF sequences of O917A186TRGZRQ1 device.

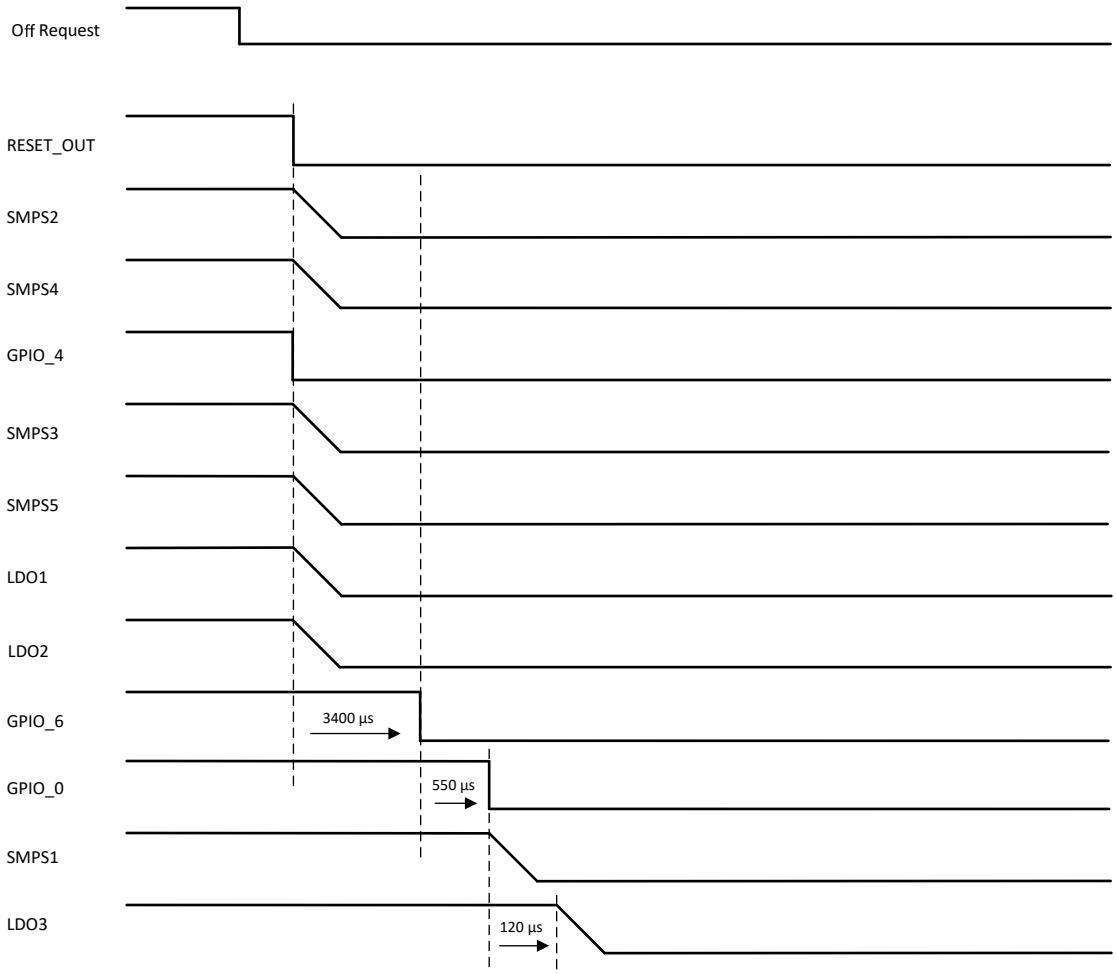

Figure 4-2. ACT2OFF Sequence of O917A186TRGZRQ1

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