User's Guide

TPS543320 SWIFT™ Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS543320EVM evaluation module (BSR101) and the TPS543320 dc/dc converter. Also included are the performance characteristics, schematic, and bill of materials for the TPS543320EVM.

Table of Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

1.1 Background

The TPS543320 dc/dc converter is a synchronous buck converter designed to provide up to a 3-A output. The input (VIN) is rated for 4 V to 18 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1.

The high-side and low-side MOSFETs are incorporated inside the TPS543320 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS543320 to achieve high efficiencies and helps keep the junction temperature low at the rated output current. Fixed frequency advanced current mode control allows you to synchronize the regulators to an external clock source. An external divider allows for an adjustable output voltage. The TPS543320 FSEL and MODE pins provide selectable switching frequency, soft start time, current limit, and internal compensation. Lastly, the TPS543320 includes an enable pin and a power good output which can be used for sequencing multiple regulators.

This evaluation module includes two designs with the TPS543320. The first design is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS543320 regulator. The small area design fits within 100 mm^2. The second design is designed to demonstrate the high efficiency that can be achieved when designing with the TPS543320 regulator. The second design also includes jumpers that can be used to easily evaluate the features of the TPS543320.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS543320EVM	V_{IN} = 4 V to 18 V	0 A to 3 A

1.2 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS543320EVM. Observe all safety precautions.

Warning The TPS543320EVM may become hot during operation due to dissipation of power in some operating conditions. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

1.3 Performance Characteristics Summary

A summary of the TPS543320EVM performance characteristics is provided in Table 1-2 and Table 1-3. The TPS543320EVM is designed and tested for V_{IN} = 4 V to 18 V. Characteristics are given for an input voltage of V_{IN} = 12 V and output voltages of 1.8 V and 3.3 V, unless otherwise specified. The ambient temperature is room temperature (20°C to 25°C) for all measurements, unless otherwise noted.

Table 1-2. TPS543320EVM Small Size (U1) Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			4	12	18	V
Input current	V_{IN} = 12 V, I_O = 0 A			12		mA
	V_{IN} = 5 V, I_O = 3 A			1.23		A
V_{IN} start voltage	Set by internal UVLO			3.95		V
V_{IN} stop voltage	Set by internal UVLO			3.8		V
Output voltage setpoint				1.8		V
Output current range	V_{IN} = 4 V to 18 V		0		3	A
Line and load regulation	V_{IN} = 4 V to 18 V, I_O = 0 A to 3 A			±0.1%		
Load transient response	I_O = 0.75 A to 2.25 A	Voltage change		–75		mV
		Recovery time to within ±0.5%		32		µs
	I_O = 2.25 A to 0.75 A	Voltage change		75		mV
		Recovery time to within ±0.5%		32		µs
Loop bandwidth	R_O = 0.72 Ω			117		kHz
Phase margin				51		degrees
Input ripple voltage	I_O = 3 A			18		mVPP
Output ripple voltage	I_O = 3 A			16		mVPP
Output rise time	Set by MODE pin resistor			1		ms
Current limit	Set by MODE pin resistor			High		
Switching frequency (f_{SW})	Set by FSEL pin resistor			1500		kHz
Peak efficiency	V_{IN} = 5 V, I_O = 1.5 A			94.7%		
	V_{IN} = 12 V, I_O = 2.5 A			91.6%		
IC case temperature	V_{IN} = 12 V, I_O = 3 A, 15-minute soak			35.1		°C

Table 1-3. TPS543320EVM High Efficiency (U2) Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			4	12	18	V
Input current	V_{IN} = 12 V, I_O = 0 A			21.8		mA
	V_{IN} = 5 V, I_O = 3 A			2.1		A
V_{IN} start voltage	Set by EN pin resistor divider			4.53		V
V_{IN} stop voltage	Set by EN pin resistor divider			3.98		V
Output voltage setpoint	J14 short pins 5 and 6			3.3		V
Output current range	V_{IN} = 4 V to 18 V		0		3	A
Line and load regulation	V_{IN} = 4 V to 18 V, I_O = 0 A to 3 A			±0.1%		
Load transient response	I_O = 0.75 A to 2.25 A	Voltage change		–200		mV
		Recovery time to within ±0.5%		28		µs
	I_O = 0.75 A to 2.25 A	Voltage change		200		mV
		Recovery time to within ±0.5%		28		µs
Loop bandwidth	R_O = 1.32 Ω, J18 short pins 3 and 4			56		kHz
Phase margin				48		degrees
Input ripple voltage	I_O = 3 A			130		mVPP
Output ripple voltage	I_O = 3 A			130		mVPP
Output rise time	Set by MODE pin resistor, All default J18 options			1		ms
Current limit	Set by MODE pin resistor, J18 short pins 1 and 2, 3 and 4, or 5 and 6			High		
Switching frequency (f_{SW})	Set by FSEL pin resistor, J17 short pins 3 and 4			1000		kHz
Peak efficiency	V_{IN} = 5 V, I_O = 1.75 A			96.09%		
	V_{IN} = 12 V, I_O = 2.5 A			93.71%		
IC case temperature	V_{IN} = 12 V, I_O = 3 A, 15-minute soak			33.2		°C

2 Configurations and Modifications

These evaluation modules are designed to provide access to the features of the TPS543320. The U2 design provides jumpers for testing different configurations. Jumper selections must be made prior to enabling the TPS543320.

If a desired configuration is not available, some modifications can be made to this module. When modifications are made to the components on the EVM, the internal compensation option selected with the MODE pin resistor can need to be changed. Changes to the f_{SW}, output voltage, output inductor, and output capacitors can require a change in the compensation. TPS543320 data sheet equations or WEBENCH can be used to calculate the output capacitor value, compensation, f_{SW}, and inductance. Ensure all components have sufficient voltage and current ratings.

2.1 Output Voltage

In the U1 design, the output voltage is set by the resistor divider network of R7 (R_{FBT}) and R8 (R_{FBB}). R8 is fixed at 1.00 kΩ to set the FB divider current at approximately 500 µA. To change the output voltage of the EVM, the value of resistor R7 must change. Changing the value of R7 can change the output voltage above the 0.5-V reference voltage (V_{REF}). The value of R7 for a specific output voltage can be calculated using Equation 1. After changing R7, the feedfoward capacitor (C8) can also need to be changed.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{1}$$

In the U2 design, there are a few ways to set the output voltage. First, jumper J14 can be used to select between the options shown in Table 2-1. If the desired output voltage is not available, a resistor must be changed. For output voltages less than 0.8 V, TI recommends leaving J14 open and increasing R21. R21 becomes R_{FBB} and the required value for can be calculated with Equation 2, where R_{FBT} is R15. For output voltages greater than 0.8 V, the jumper output voltage options can be changed by changing one of the resistors R23-R26. The R_{FBJ} resistor value to get a desired equivalent R_{FBB} resistance can be calculated with Equation 3. To use J14 for output voltages 3.3 V or larger, R20 should be reduced to 499 Ω.

$$R_{FBB} = R_{FBT} \times \frac{V_{REF}}{V_{OUT} - V_{REF}} \tag{2}$$

$$R_{FBJ} = \frac{R_{FBB} \times (R20 + R21) - R20 \times R21}{R21 - R_{FBB}} \tag{3}$$

Table 2-1. VOUT Selection

JUMPER SETTING	EQUIVALENT BOTTOM FB RESISTOR (R_{FBB})	NOMINAL OUTPUT VOLTAGE
Open	R21 = 20.0 kΩ	1.2 V
1 to 2 pin shorted	(R23+R20)||R21 = 6.08 kΩ	1.8 V
3 to 4 pin shorted	(R24+R20)||R21 = 4.67 kΩ	2.5 V
5 to 6 pin shorted(1)	(R25+R20)||R21 = 3.67 kΩ	3.3 V
7 to 8 pin shorted	(R26+R20)||R21 = 2.54 kΩ	5.0 V

(1) Default Setting

2.2 Switching Frequency (FSEL Pin)

In the U2 design, jumper J17 can be used to select between the switching frequency options shown in Table 2-2. If the desired option is not available, change one of the resistors to the value which sets the desired option.

In the U1 design, change the FSEL resistor to the value which sets the desired option.

Table 2-2. FSEL Selection

JUMPER SETTING	FSEL RESISTOR	SWITCHING FREQUENCY
1 to 2 pin shorted	17.4 kΩ	750 kHz
3 to 4 pin shorted(1)	11.8 kΩ	1000 kHz
5 to 6 pin shorted	8.06 kΩ	1500 kHz
7 to 8 pin shorted	4.99 kΩ	2200 kHz

(1) Default Setting

2.3 Current Limit, Soft-Start Time, and Internal Compensation (MODE Pin)

In the U2 design, jumper J18 can be used to select between the current limit, soft-start time, and internal compensation options shown in Table 2-3. If the desired option is not available, change one of the resistors to the value which sets the desired option.

In the U1 design, change the MODE resistor to the value which sets the desired option.

Table 2-3. MODE Selection

JUMPER SETTING	MODE RESISTOR	CURRENT LIMIT	SOFT-START TIME	RAMP
1 to 2 pin shorted	2.21 kΩ	High	1 ms	1 pF
3 to 4 pin shorted(1)	4.87 kΩ	High	1 ms	2 pF
5 to 6 pin shorted	11.3 kΩ	High	1 ms	4 pF
7 to 8 pin shorted	60.4 kΩ	Low	1 ms	2 pF

(1) Default Setting

2.4 Adjustable UVLO

The undervoltage lockout (UVLO) for U2 can be adjusted externally using R14 (R_{ENT}) and R17 (R_{ENB}). See the for detailed instructions for setting the external UVLO.

In the U1 design, the EN pin is floating, so only the internal UVLO of the device is used.

3 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS543320EVM evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start-up, and current limit modes. Measurements are taken with the following conditions unless otherwise noted.

- 12-V input
- Room temperature (20°C to 25°C)
- U2 with the default setting output voltage of 1 V, switching frequency of 1000 kHz, and maximum current limit setting
- With the other converter disabled

3.1 Input/Output Connections

The TPS543320EVM is provided with input connectors, output connectors, and test points as shown in Table 3-1 and Table 3-2.

To support the minimum input voltage with the full rated load on both outputs with the default EVM, a power supply capable of supplying greater than 3 A must be connected to J8 through a pair of 20-AWG wires or better. Banana jacks J5 and J9 provide an alternative connection to input power supply.

For U1, the load must be connected to J2 and for U2, the load must be connected to J7. A pair of 20-AWG wires or better must be used for each connection. With the maximum current limit setting, the maximum load current capability is near 5 A before the TPS543320 goes into current limit. Wire lengths must be minimized to reduce losses in the wires.

Test point TP11 provides a place to monitor the V_{IN} input voltage with TP19 providing a convenient ground reference. TP2 is used to monitor the output voltage of U1 with TP5 as the ground reference. TP15 is used to monitor the output voltage of U2 with TP17 as the ground reference.

If modifications are made to the TPS543320EVM, the input current may change. The input power supply and wires connecting the EVM to the power supply must be rated for the input current.

Note

For the FSEL pin of the TPS543320 to detect and set the correct switching frequency, the pin must either detect the resistor to ground or an external clock must applied to the pin before enabling the regulator. If starting up without an external clock, to properly detect the FSEL resistor value connected to ground, the buffers on the EVM need to be in high impedance mode. The shunts on J15 and J16 must be removed to put the buffers in high impedance mode for startup without an external clock.

Table 3-1. Connectors and Jumpers

REFERENCE DESIGNATOR	NAME	RELATED IC	FUNCTION
J2	VOUT	U1	VOUT screw terminal to connect load to output
J4	EN_OFF	U1	2-pin header for enable. Add shunt to connect EN to ground and disable device.
J5, J9	VIN	Both	Banana jack for positive terminal and negative terminal of input power supply
J7	VOUT	U2	VOUT screw terminal to connect load to output
J8	VIN	Both	VIN screw terminal to connect input voltage (see Table 1-1 for V_{IN} range)
J11	RDIV_VIN	U2	2-pin header for enable divider. Remove shunt to disconnect EN pin divider for U2 from VIN. If J11 shunt is removed and J13 shunt is populated, U2 EN pin is pulled to ground through bottom resistor in divider disabling U2.
J13	EN_RDIV	U2	2-pin header to connect enable divider to U2. Remove shunt to float EN pin of U2 to use internal UVLO to enable U2.
J14	VOUT Select	U2	VOUT selection header. Use shunt to set output voltage. See Table 2-1.
J15	ENSYNC_U1	U1	2-pin header to connect U1 buffer output enable to ground. Populate shunt to enable output of buffer. Remove shunt to make buffer output high impedance.
J16	ENSYNC_U2	U2	2-pin header to connect U2 buffer output enable to ground. Populate shunt to enable output of buffer. Remove shunt to make buffer output high impedance.
J17	FSEL Select	U2	FSEL selection header. Use shunt to select FSEL resistor. See Table 2-2.
J18	MODE Select	U2	MODE selection header. Use shunt to select MODE resistor. See Table 2-3.

Table 3-2. Test Points

REFERENCE DESIGNATOR	NAME	RELATED IC	FUNCTION
TP1	VIN_U1	U1	VIN test point. Use this for efficiency measurements.
TP2	VOUT_U1	U1	VOUT test point. Use this for efficiency, output regulation, and bode plot measurements.
TP3	SW_U1	U1	SW node solder mask opening
TP4	PGND_U1	U1	PGND test point
TP5	PGND_EFF_U1	U1	PGND test point. Use this for efficiency measurements.
TP6	PGOOD_U1	U1	PGOOD test point
TP7	EN_U1	U1	EN test point. If applying an external voltage, it must be kept below the absolute maximum voltage of the EN pin of 6 V.
TP8	AGND_U1	U1	AGND test point
TP9	BODE_U1	U1	Test point between voltage divider network and output voltage. Used for Bode plot measurements.
TP10	VOUT_U1	U1	SMB connector to measure output voltage. When using this test point, the scope should be set for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.
TP11	VIN	Both	VIN test point near input terminals
TP12	VIN_U2	U2	VIN test point. Use this for efficiency measurements.
TP13	SW_U2	U2	SW node solder mask opening
TP14	SW_U2	U2	SW node test point
TP15	VOUT_U2	U2	VOUT test point. Use this for efficiency, output regulation, and bode plot measurements.
TP16	PGND_U2	U2	PGND test point
TP17	PGND_EFF_U2	U2	PGND test point. Use this for efficiency measurements.
TP18	PGOOD_U2	U2	PGOOD test point
TP19	PGND	Both	PGND test point near input terminals
TP20	AGND_U2	U2	AGND test point
TP21	BP5_U2	U2	BP5 test point
TP22	BODE_U2	U2	Test point between voltage divider network and output voltage. Used for Bode plot measurements.
TP23	EN_U2	U2	EN test point. If you are applying an external voltage, it must be kept below the absolute maximum voltage of the EN pin of 6 V.
TP24	VO_ADJ	U2	Test point for injecting current into the FB divider to adjust the DC output voltage or inject a step to FB to test OVP
TP25	VO_2NDSTG	U2	Test point to measure output voltage after second stage filter if added to EVM.
TP26	SYNC	Both	SYNC test point. Supply an external clock to this test point to synchronize both regulators to it.
TP27	FSEL	U2	FSEL test point
TP28	SW_U2	U2	SMB connector to measure SW node. When using this test point, the scope should be set for 50-Ω termination. The combination of 50-Ω termination and 450-Ω series resistance creates a 10:1 attenuation.
TP29	VOUT_U2	U2	SMB connector to measure output voltage. When using this test point, the scope should be set for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.
TP30	VO_2NDSTG	U2	SMB connector to measure output voltage after second stage filter if added to EVM. When using this test point, the scope should be set for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.
TP31	FGEN	Both	Test point to connect function generator to load transient circuit. Slowly increase amplitude and vary slew rate of function generator for desired load step.
TP32	ISNS	Both	Test point to measure current in load transient circuit. Gain is 10 A/V.
TP33	PGND	Both	PGND test point for load transient circuit
TP34	MODE	U2	MODE test point

3.2 Efficiency

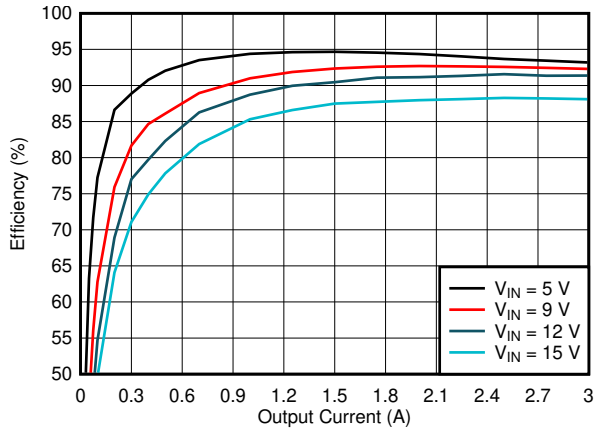
Figure 3-1 through Figure 3-4 show the efficiency for both designs on the TPS543320EVM. Using the selection jumpers for U2, the results for different output voltage and switching frequency combinations are included. The test points listed in Table 3-3 are used for the efficiency measurement. Use these test points to minimize the contribution of PCB parasitic power loss to the measured power loss.

The following are some additional test setup considerations to minimize external sources of power dissipation.

- Disable the other regulator to avoid including the switching quiescent current of the other regulator in the efficiency measurement.
- Do not measure the SW pin of U2 with TP28 while measuring the efficiency of U2. Measuring the SW pin with this test point loads this node with 500 Ω and the efficiency measurement will include the power lost in this external resistance.
- Remove the shunts from J11 and J13 as a small amount of power is dissipated in the EN resistor divider connected to U2.

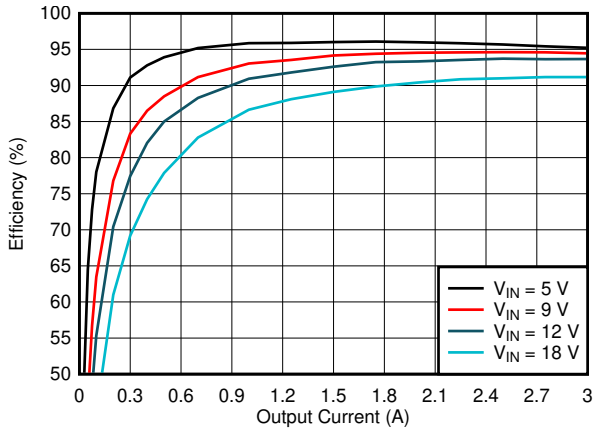
Table 3-3. Efficiency Measurement Test Points

RELATED IC	TEST POINT NAME	REFERENCE DESIGNATOR	FUNCTION
U1	VIN_U1	TP1	Input voltage test point connected near pins of U1
	VOUT_U1	TP2	Output voltage test point near output inductor of U1
	PGND_EFF_U1	TP5	PGND reference test point for both input and output voltages Kelvin connected near U1
U2	VIN_U2	TP12	Input voltage test point connected near pins of U2
	VOUT_U2	TP15	Output voltage test point near output inductor of U2
	PGND_EFF_U2	TP17	PGND reference test point for both input and output voltages Kelvin connected near U2



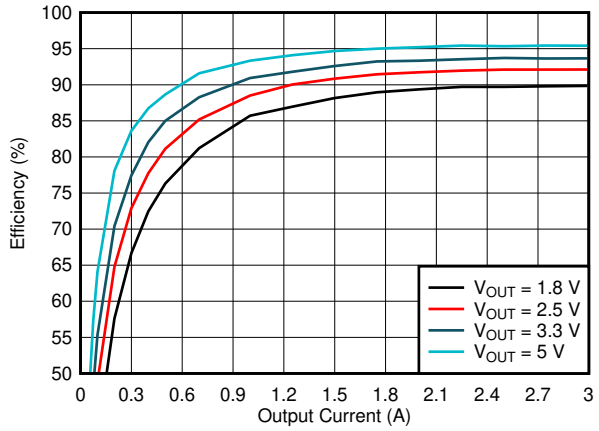
V_{OUT} = 1.8 V f_{SW} = 1500 kHz

Figure 3-1. U1 Efficiency



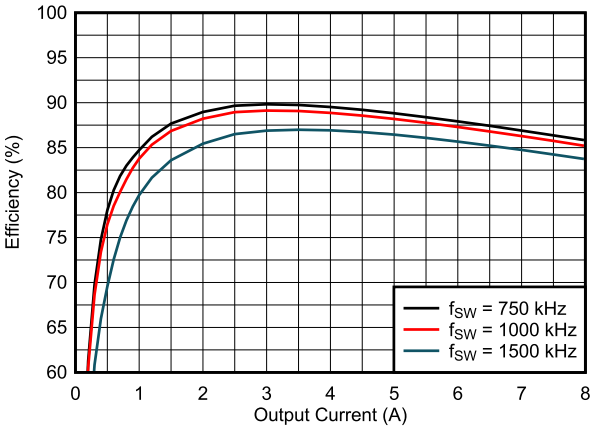
V_{OUT} = 3.3 V f_{SW} = 1000 kHz

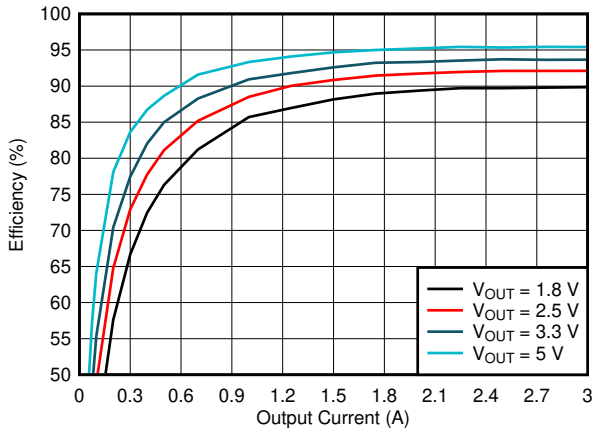
Figure 3-2. U2 Efficiency – Default Configuration



V_{IN} = 12 V f_{SW} = 1000 kHz

Figure 3-3. U2 Efficiency – 1000-kHz Switching Frequency with Different Output Voltages



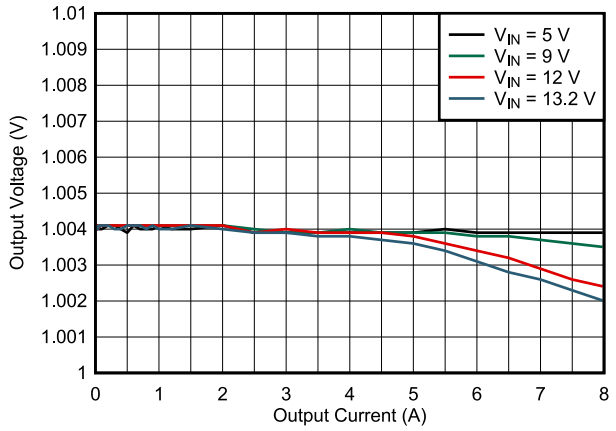


V_{IN} = 9 V V_{OUT} = 3.3 V

Figure 3-4. U2 Efficiency – 3.3-V Output with Different Switching Frequencies

3.3 Output Voltage Regulation

Figure 3-5 and Figure 3-6 show the load and line regulation for U1. Figure 3-7 and Figure 3-8 show the load and line regulation for U2.



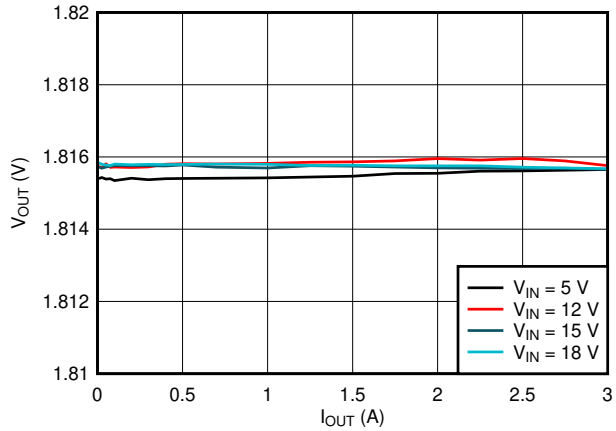


Figure 3-5. U1 Load Regulation

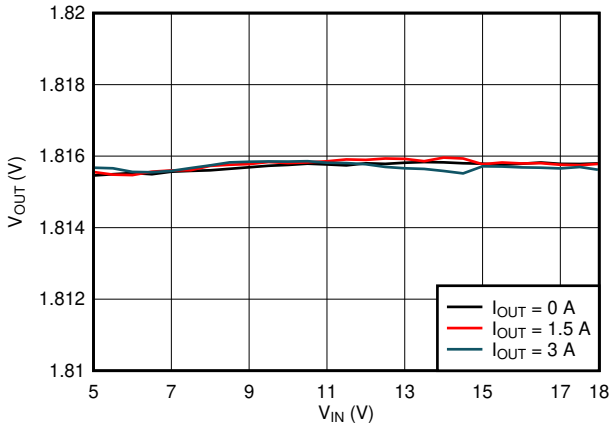


Figure 3-6. U1 Line Regulation

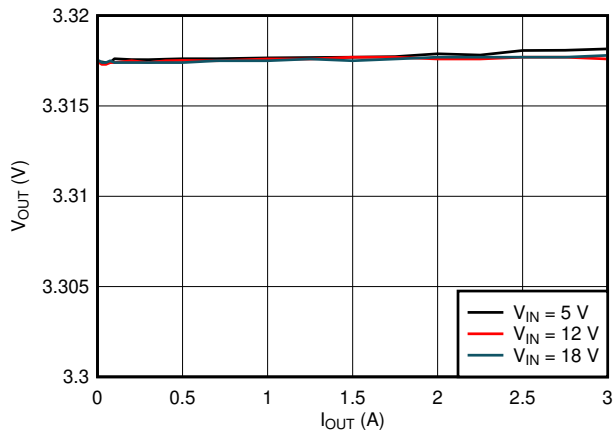


Figure 3-7. U2 Load Regulation

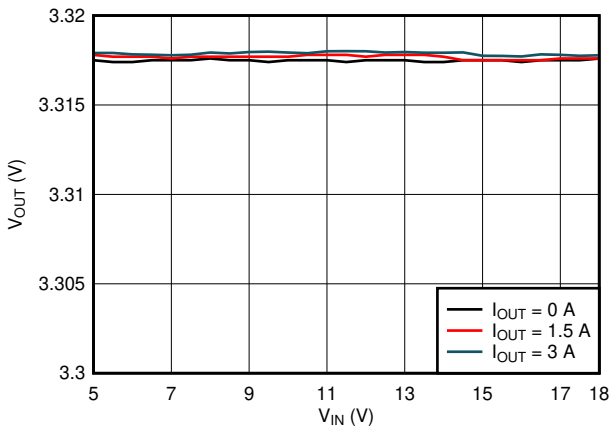


Figure 3-8. U2 Line Regulation

3.4 Load Transient and Loop Response

Figure 3-9 and Figure 3-10 show the response to load transients for both designs. The current step is from 0.75 A to 2.25 A and the current step slew rate is 1 A/µs. An electronic load is used to provide a DC 0.75-A load and the load transient circuit on the EVM is used to provide a 1.5-A step. The VOUT voltage is measured using TP10 for U1 and TP29 for U2.

When using the load transient circuit included on the TPS543320EVM, slowly increase amplitude of function generator for desired load step amplitude then vary the rise and fall times for the desired slew rate. The current for the load step can be sensed with the ISNS test point. The default resistors on the EVM provide a gain of 10 A/V. With this gain, a 1.5-A step will result in 150-mV at the ISNS test point.

Note

To use the load transient circuit with U1, move R27 to R28.

Figure 3-11 and Figure 3-12 show the loop characteristics for both designs. Gain and phase plots are shown for V_{IN} voltage of 12 V and a 0.72-Ω or 1.32-Ω resistive load.

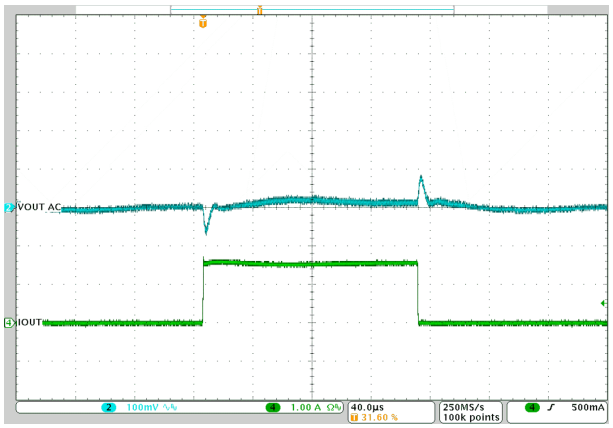


Figure 3-9. U1 Transient Response

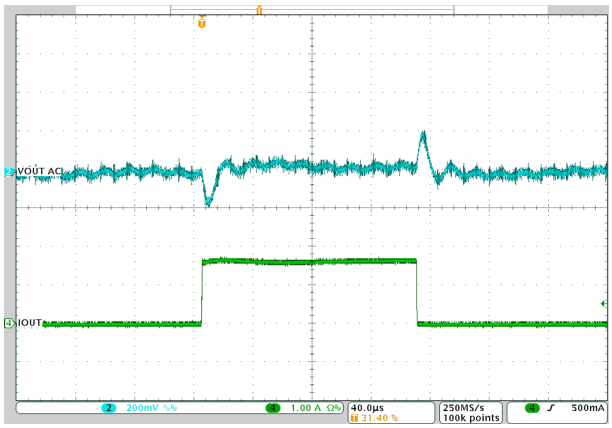


Figure 3-10. U2 Transient Response

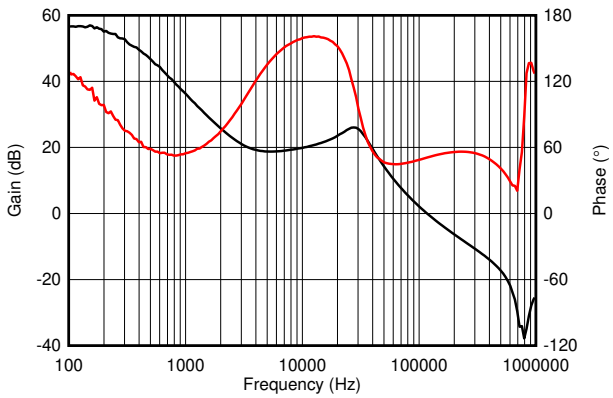


Figure 3-11. U1 Bode Plot

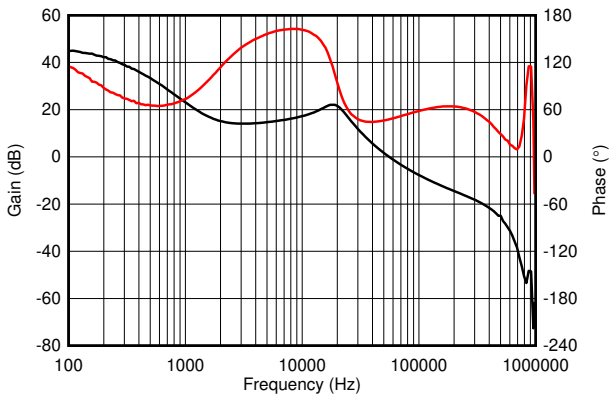


Figure 3-12. U2 Bode Plot

Figure 3-13 and Figure 3-14 shows the loop characteristics for U2 with the 3 different ramp settings.

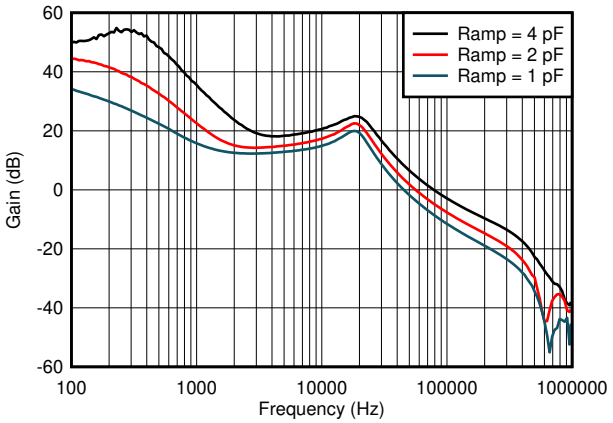


Figure 3-13. U2 Loop Gain with Different Ramp Settings

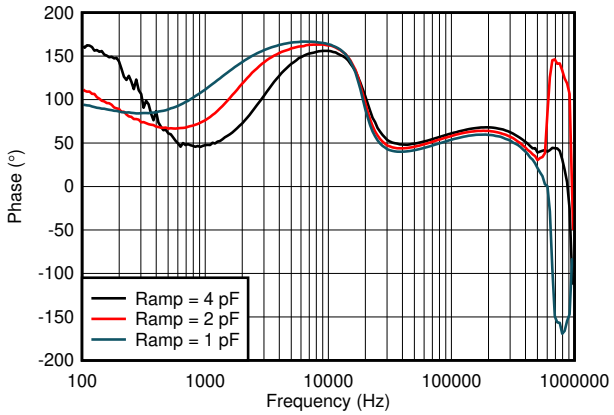


Figure 3-14. U2 Loop Phase with Different Ramp Settings

3.5 Output Voltage Ripple

Figure 3-15 through Figure 3-18 show the TPS543320EVM output voltage ripple. The load currents are no load and 3 A. V_{IN} = 12 V. The VOUT voltage is measured using TP10 for U1 and TP29 for U2.

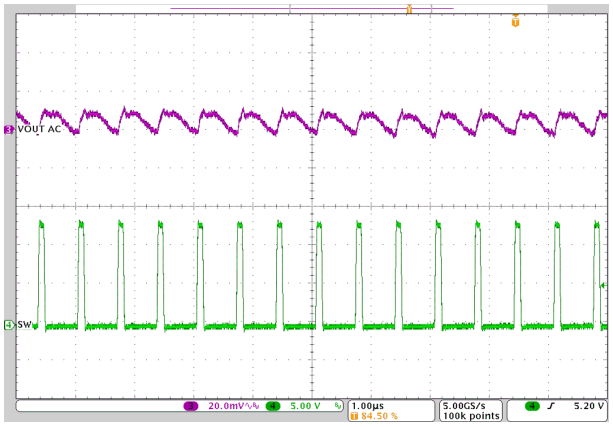


Figure 3-15. U1 Output Ripple – No Load

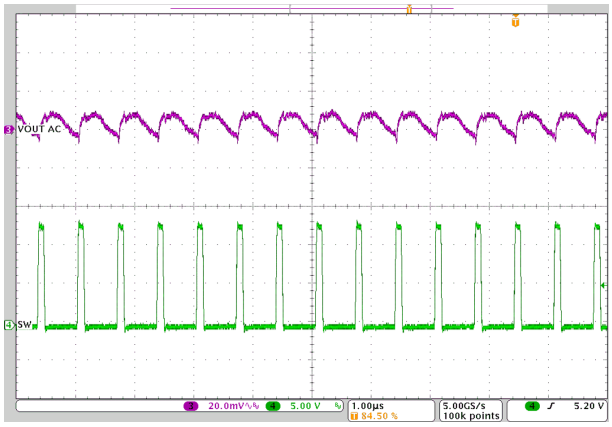


Figure 3-16. U1 Output Ripple – 3-A Load

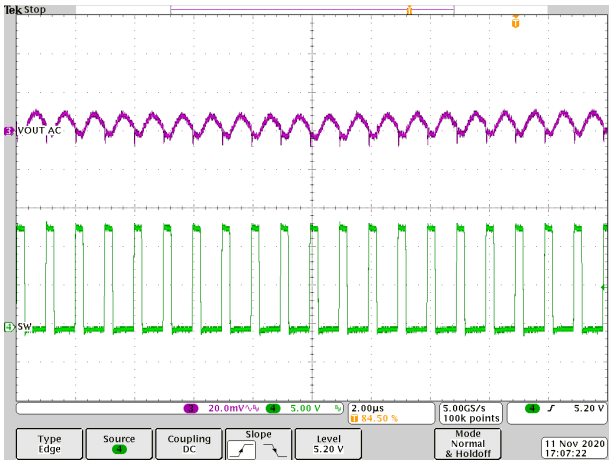


Figure 3-17. U2 Output Ripple – No Load

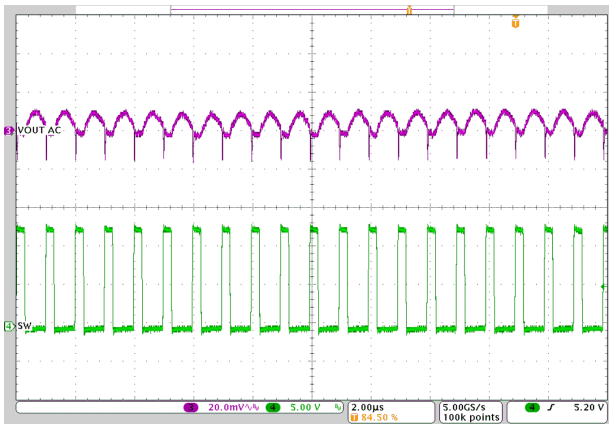


Figure 3-18. U2 Output Ripple – 3-A Load

3.6 Input Voltage Ripple

Figure 3-19 through Figure 3-22 show the TPS543320EVM input voltage ripple. The load currents are no load and 3 A. V_{IN} = 12 V. The ripple voltage is measured across C1 for U1 and measured across C13 for U2.

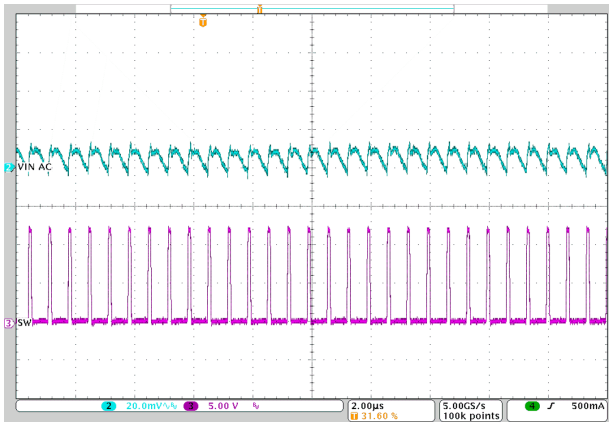


Figure 3-19. U1 Input Ripple – No Load

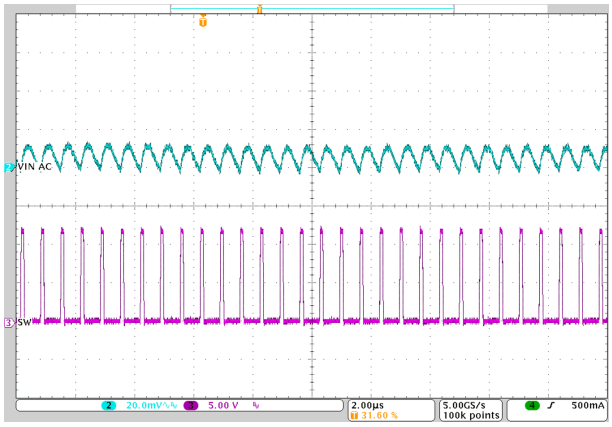


Figure 3-20. U1 Input Ripple – 3-A Load

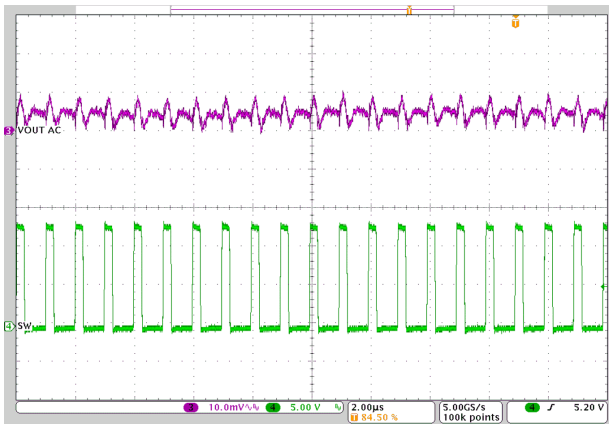


Figure 3-21. U2 Input Ripple – No Load

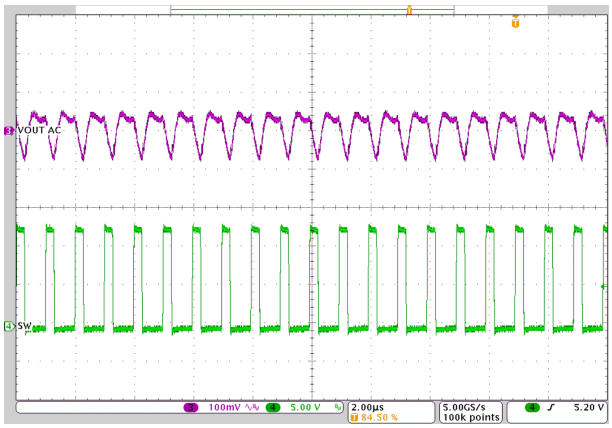


Figure 3-22. U2 Input Ripple – 3-A Load

3.7 Synchronizing to a Clock

Figure 3-23 shows U1 and U2 synchronized to an external clock of 1.25 MHz at the SYNC test point. To synchronize to the clock at the SYNC test point, place a shunt on the ENSYNC_U1 or ENSYNC_U2 jumper or jumpers to enable the output of the buffers.

Figure 3-24 shows the transitions to and from synchronizing to an external clock with 3-A load. 16 pulses with a frequency of 1-MHz were sent to the SYNC testpoint on the EVM. In this waveform, after ten pulses, the TPS543320 begins synchronizing to the clock. After the clock goes away, the TPS543320 switches at 70% of the internal clock frequency for four pulses then transitions back to the normal internal clock frequency. There is only a small variation in the output voltage during these transitions.

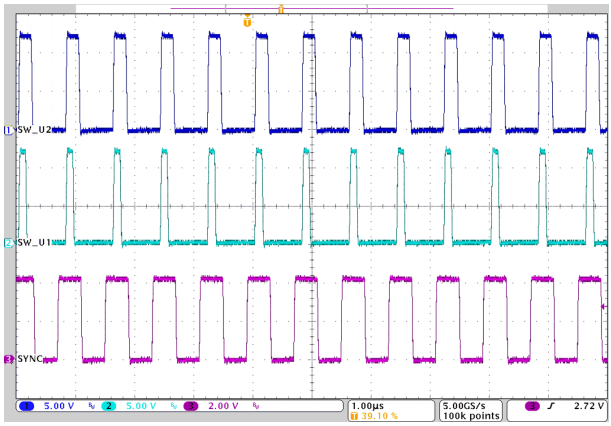


Figure 3-23. U1 and U2 Synchronized to a Clock

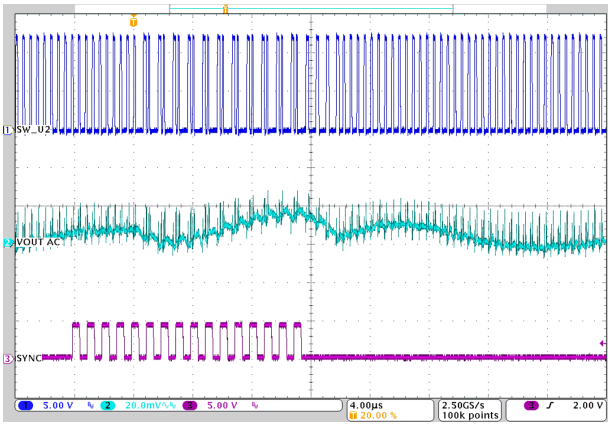


Figure 3-24. U2 Clock Synchronization Transitions

3.8 Start-up and Shutdown with EN

Figure 3-25 and Figure 3-26 show the start-up and shutdown waveforms for U2 with EN. In Figure 3-25, the input voltage is initially applied and the output is inhibited by pulling EN to GND using an external function generator. When the EN voltage is increased above the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value. In Figure 3-26, the external function generator pulls EN to ground and the TPS543320 shuts down.

Figure 3-27 shows the BP5 internal LDO start-up relative to the EN pin.

A shunt on the ENOFF_U1 jumper or RDIV_VIN can be used to test the EN start-up of U1 and U2, respectively. When the shunt is removed from ENOFF_U1, EN is released and the start-up sequence begins for U1. When the shunt is placed on RDIV_VIN, EN is pulled to the input voltage through the resistor divider and the start-up sequence begins for U2.

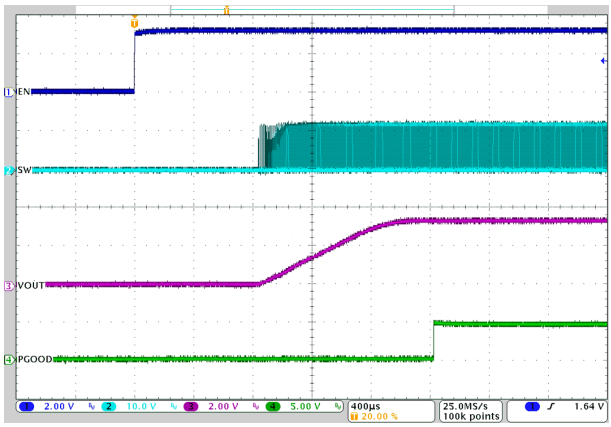


Figure 3-25. U2 Start-up with EN – No Load

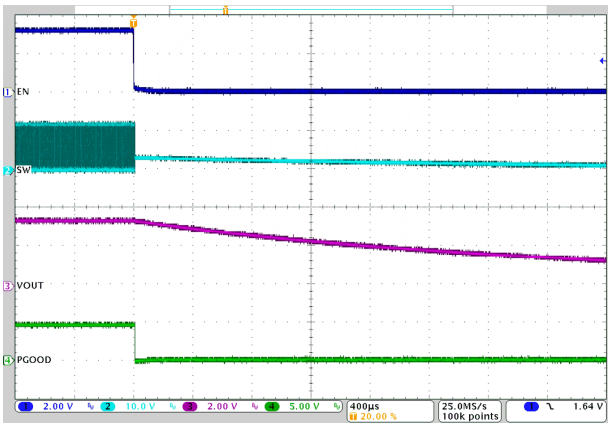


Figure 3-26. U2 Shutdown with EN – No Load

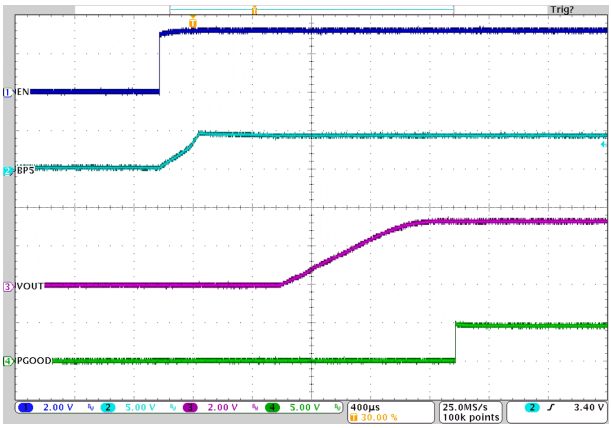


Figure 3-27. U2 Startup with EN – No Load and Measuring BP5

3.9 Start-up and Shutdown with VIN

Figure 3-28 and Figure 3-29 show the start-up and shutdown waveforms for U2 with VIN. In Figure 3-28, the VIN voltage ramps up and output voltage ramps up after the input and EN pin voltages reach their respective UVLO threshold. In Figure 3-29, the VIN voltage ramps down and the TPS543320 shuts down when the input or EN pin voltage reach their respective UVLO threshold. The rate at which VIN ramps down changes as soon as the TPS543320 is disabled because it is no longer loading the input supply.

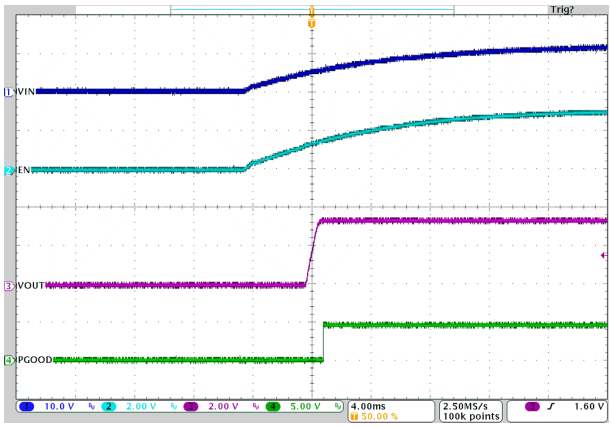


Figure 3-28. U2 Start-up with VIN – 1.5-A Load

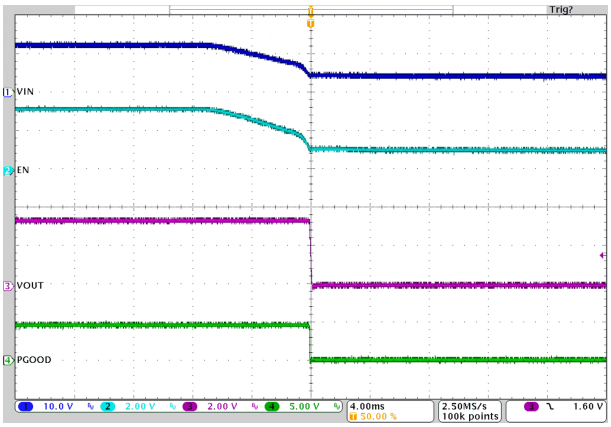


Figure 3-29. U2 Shutdown with VIN – 1.5-A Load

3.10 Hiccup Current Limit

Figure 3-30 through Figure 3-31 show the TPS543320 hiccup current limit feature. These waveforms are measured using U2. Figure 3-30 shows the response to an overload in the current limit settings, while Figure 3-31 shows the response to a hard short on the output.

Figure 3-31 shows the TPS543320 entering hiccup with an overload on the output. The TPS543320 tries to restart after the Hiccup wait time period but the overload was still present on the output. In the next restart attempt, the overload has been removed so the TPS543320 starts up normally.

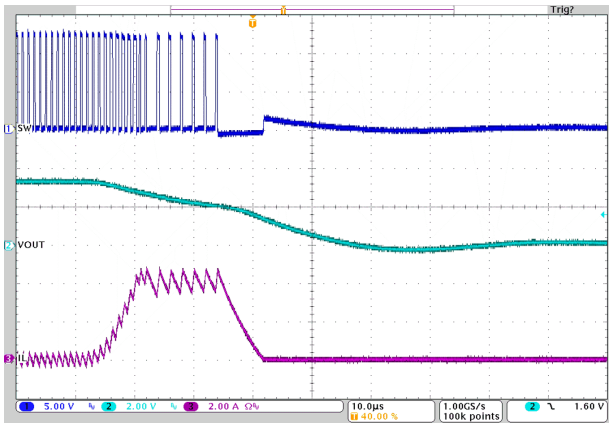


Figure 3-30. U2 Output Overcurrent Protection – Overload

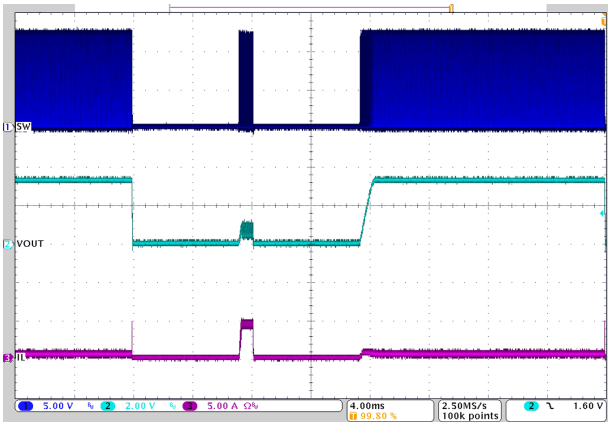


Figure 3-31. U2 OCP Hiccup and Recover

3.11 Overvoltage Protection

Figure 3-32 and Figure 3-33 show the overvoltage protection behavior of U2. This is tested by applying a step to the FB pin with a function generator through the VO_ADJ test point. The VO_ADJ test point is initially equal to the reference voltage of 0.5 V and is stepped up to 3.3 V. The TPS543320 attempts to restart immediately after the OVP fault is cleared. It does not wait for the hiccup time period.

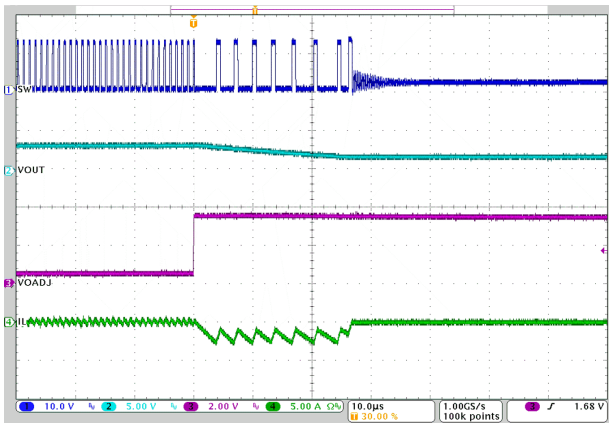


Figure 3-32. U2 Overvoltage Protection

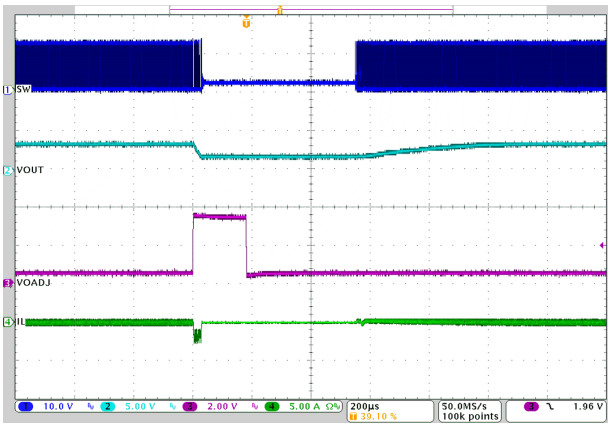


Figure 3-33. U2 OVP and Recover

3.12 Thermal Performance

Figure 3-34 through Figure 3-37 show the temperature rise of the TPS543320 ICs at full 3-A load. Figure 3-34 and Figure 3-35 have only one TPS543320 on and loaded. Figure 3-36 and Figure 3-37 have both TPS543320s loaded. A minimum of a 10 minute soak time was used before taking each measurement.

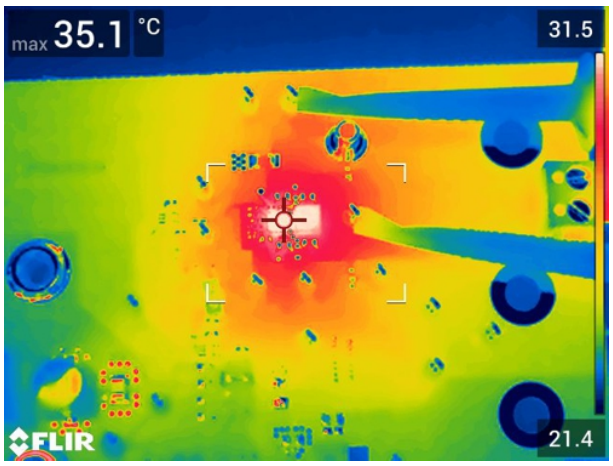


Figure 3-34. U1 Thermal Performance – 3-A Load and U2 off

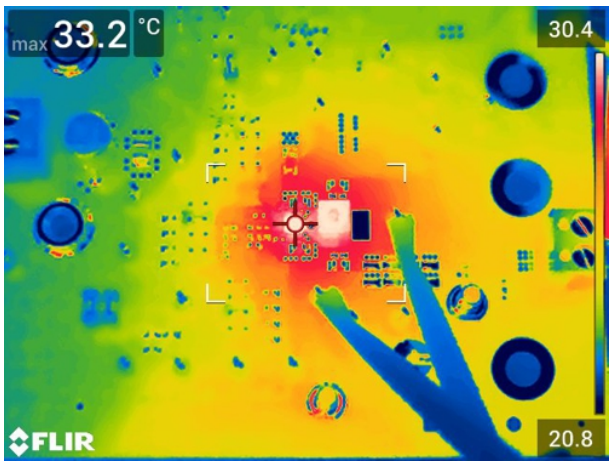


Figure 3-35. U2 Thermal Performance – 3-A Load and U1 off

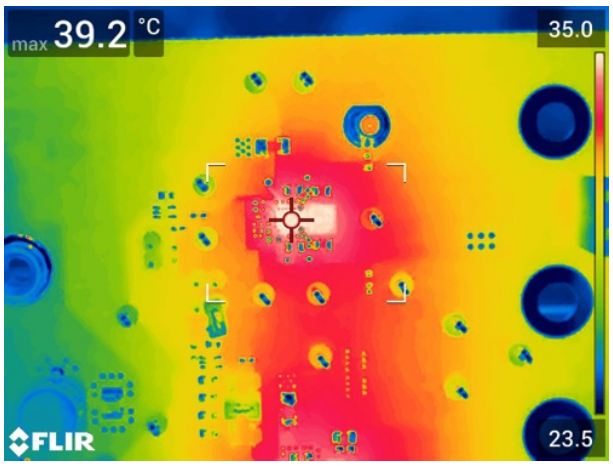


Figure 3-36. U1 Thermal Performance – Both 3-A Load

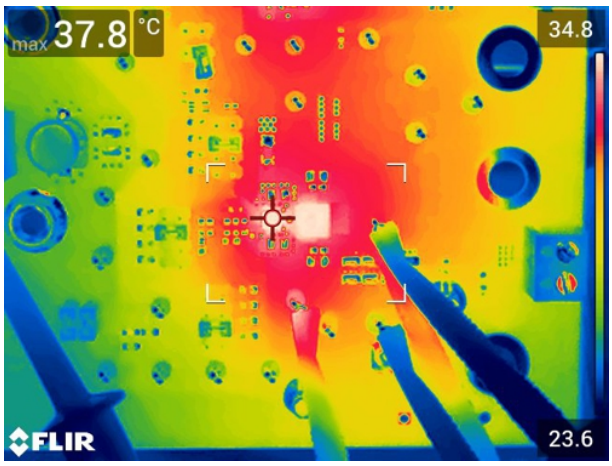


Figure 3-37. U2 Thermal Performance – Both 3-A Load

4 Board Layout

This section provides a description of the TPS543320EVM board layout and layer illustrations.

4.1 Layout

The board layout for the TPS543320EVM is shown in Figure 4-1 through Figure 4-6. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper. The small size U1 circuit takes up an area of only approximately 100 mm^2 as shown on the silkscreen.

All of the required components for the TPS543320 are placed on the top layer. The input decoupling capacitors, BP5 capacitor, and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. An additional input bulk capacitor is used near the input terminal to limit the noise entering the converter from the supply used to power the board. Critical analog circuits such as the voltage set point divider, EN resistor, MODE resistor, and FSEL resistor are kept close to the IC and terminated to the quiet analog ground (AGND) island on the top layer.

The top layer contains the main power traces for VIN, VOUT, and SW. The top layer power traces are connected to the planes on other layers of the board with multiple vias placed around the board. There are multiple vias near the PGND pins of the IC to help maximize the thermal performance. Each TPS543320 circuit has its own dedicated ground are for quiet analog ground that is connected to the main power ground plane at a single point. This single point connection is done using vias to the internal ground planes. Lastly the voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} area on the top layer.

The mid layer 1 is a large ground plane with as few traces as possible to minimize cuts in the ground plane. It is especially important to minimize cuts in the ground plane near the IC to help with minimize noise and maximize thermal performance.

The mid layer 2 contains a VIN copper area to connect both TPS543320 circuits to the input terminals. There is also a VIN copper area beneath each IC to connect its VIN pins together with a low impedance connection. This layer also has the trace to connect the FB divider to the output. Lastly, the remaining area of this layer is filled in with PGND.

The bottom layer is primarily used for another ground plane. This layer also has an additional VOUT copper area for the U2 circuit. Lastly, the load transient circuit is placed on this side of the EVM.

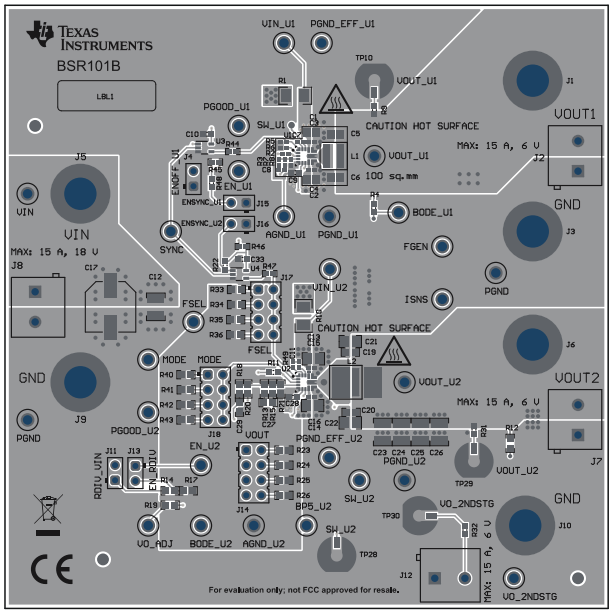


Figure 4-1. Top-Side Composite View

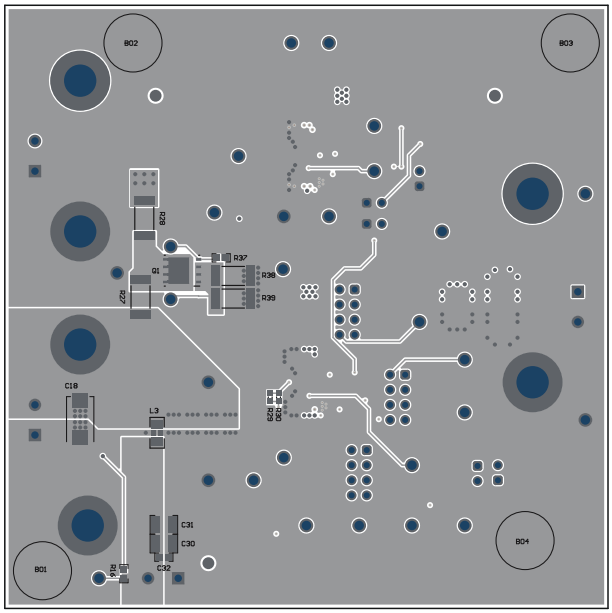


Figure 4-2. Bottom-Side Composite View (Viewed From Bottom)

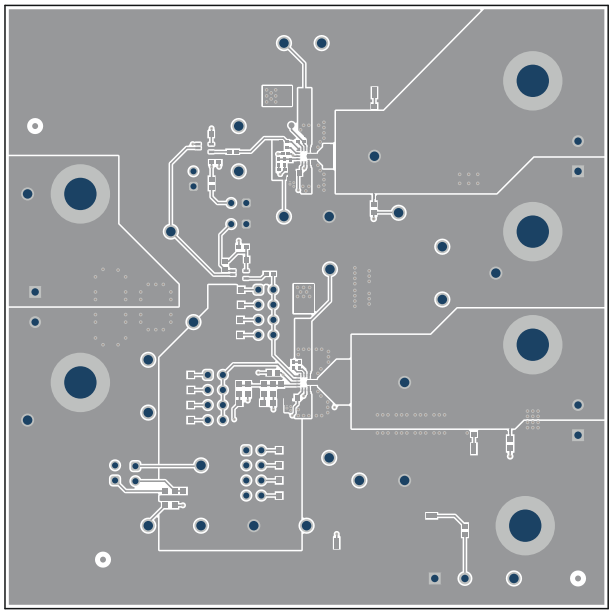


Figure 4-3. Top Layer Layout

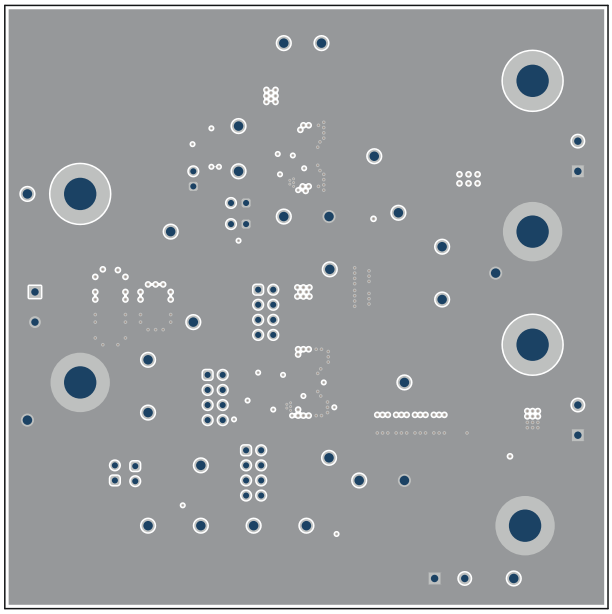


Figure 4-4. Mid Layer 1 Layout

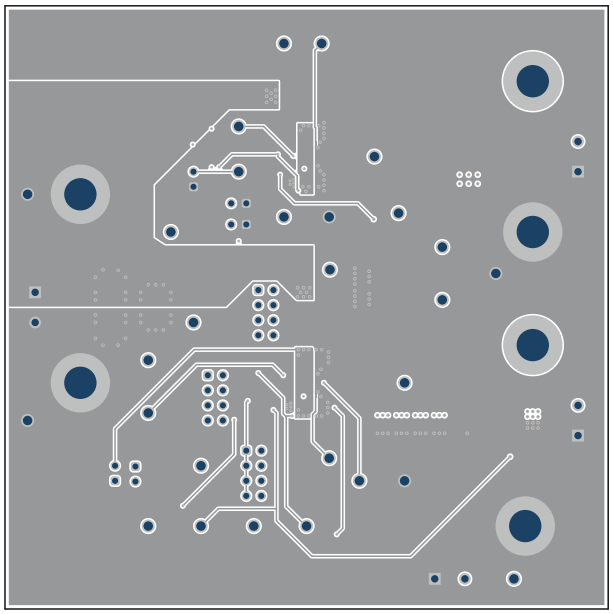


Figure 4-5. Mid Layer 2 Layout

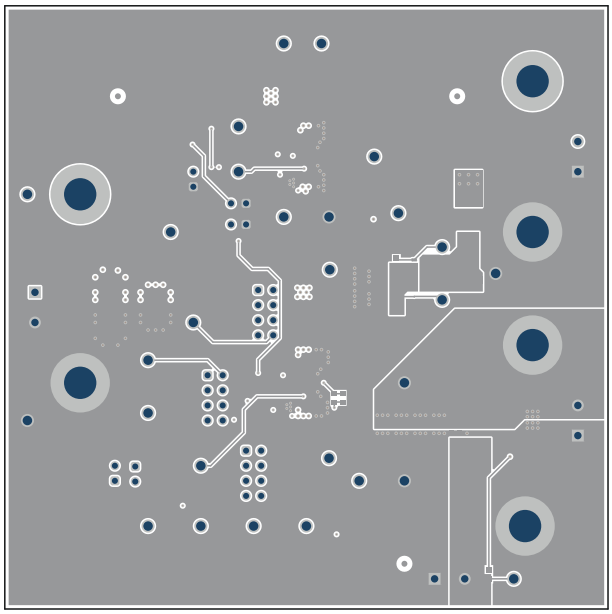


Figure 4-6. Bottom Layer Layout

5 Schematic and Bill of Materials

This section presents the TPS543320EVM schematic and bill of materials.

5.1 Schematic

Figure 5-1 is the schematic for U1. Figure 5-2 is the schematic for U2.

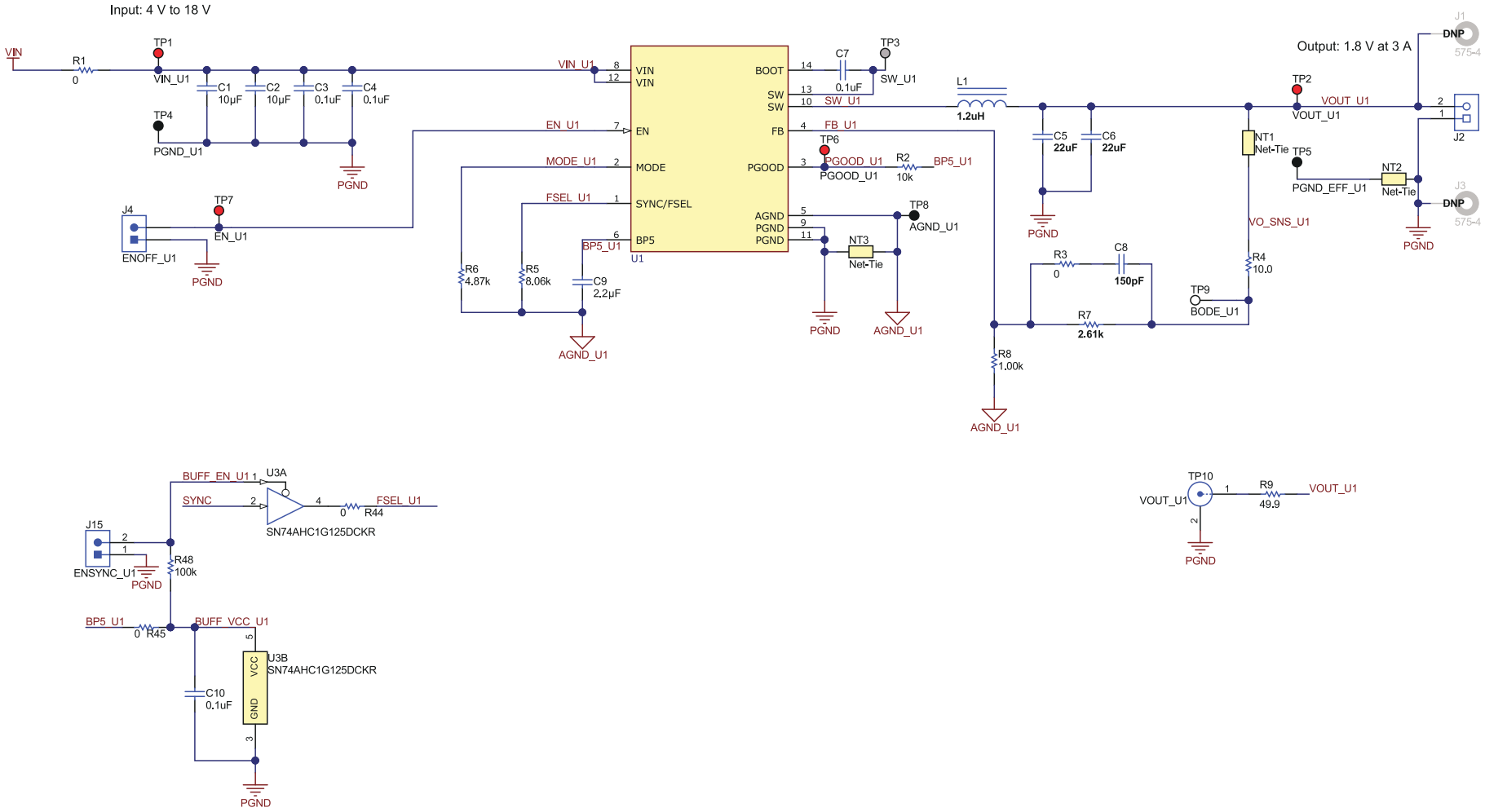


Figure 5-1. U1 Schematic

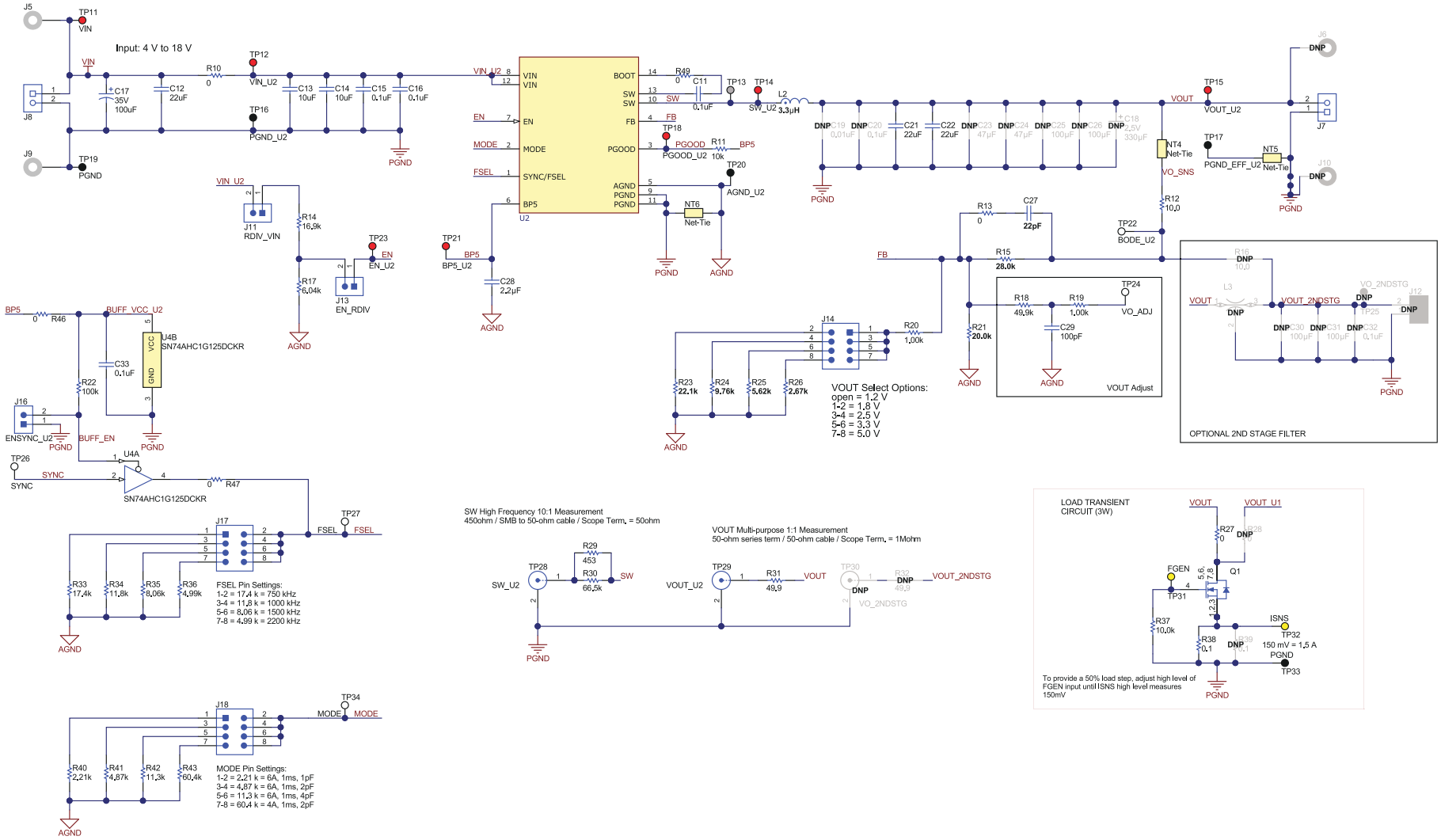


Figure 5-2. U2 Schematic

5.2 Bill of Materials

Table 5-1 presents the bill of materials for the TPS543320EVM.

Table 5-1. TPS543320EVM Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB1	1		Printed Circuit Board		BSR101	Any
BO1, BO2, BO3, BO4	4		Bumpon, Hemisphere, 0.375 X 0.235, Black	Black Bumpon	SJ61A2	3M
C1, C2, C13, C14	4	10 µF	CAP, CERM, 10 uF, 25 V, ±10%, X7S, 0805	0805	GRM21BC71E106KE11L	MuRata
C3, C4, C7, C11, C15, C16	6	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0402	0402	C1005X7R1H104K050BB	TDK
C5, C6, C21, C22	4	22 µF	CAP, CERM, 22 µF, 10 V, ±20%, X7S, 0805	0805	C2012X7S1A226M125AC	TDK
C8	1	150 pF	CAP, CERM, 150 pF, 50 V, ±5%, C0G/NP0, 0402	0402	GRM1555C1H151JA01D	MuRata
C9, C28	2	2.2 µF	CAP, CERM, 2.2 µF, 10 V, ±10%, X7R, 0603	0603	C1608X7R1A225K080AC	TDK
C10, C33	2	0.1 µF	CAP, CERM, 0.1 µF, 25 V, ±5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C12	1	22 µF	CAP, CERM, 22 µF, 25 V, ±10%, X7R, 1210	1210	GRM32ER71E226KE15L	MuRata
C17	1	100 µF	CAP, AL, 100 µF, 35 V, ±20%, 0.16 Ω, AEC-Q200 Grade 2, SMD	SMT Radial F	EEE-FK1V101P	Panasonic
C27	1	22 pF	CAP, CERM, 22 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H220JA01D	MuRata
C29	1	100 pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, 0603	0603	C0603C101J5GACTU	Kemet
J2, J7, J8	3		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J4, J11, J13, J15, J16	5		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54 mm, 2x1, TH	TSW-102-08-G-S	Samtec
J5, J9	2		Standard Banana Jack, Uninsulated, 5.5 mm	Keystone_575-4	575-4	Keystone
J14, J17, J18	3		Header, 2.54 mm, 4x2, Gold, TH	Header, 2.54 mm, 4x2, TH	TSW-104-08-L-D	Samtec
L1	1	1.2 µH	Inductor, Shielded, Composite, 1.2 µH, 8.7 A, 0.0104 Ω, AEC-Q200 Grade 1, SMD	4x4mm	XEL4030-122MEB	Coilcraft
L2	1	3.3 µH	Shielded Power Inductor, 3.3 µH, ±20%, 7.8 A, 14.6 mO max	SMT_IND_5MM48_5MM28	XEL5050-332MEB	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
Q1	1	30 V	MOSFET, N-CH, 30 V, 25 A, DQJ0008A (VSONP-8)	DQJ0008A	CSD17579Q5A	Texas Instruments
R1, R10	2	0	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8GEY0R00V	Panasonic
R2	1	10 k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GEJ103X	Panasonic
R3	1	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R4, R12	2	10.0	RES, 10.0, 1%, 0.1 W, 0603	0603	RC0603FR-0710RL	Yageo
R5	1	8.06 k	RES, 8.06 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04028K06FKED	Vishay-Dale
R6	1	4.87 k	RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K87FKED	Vishay-Dale
R7	1	2.61 k	RES, 2.61 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K61FKED	Vishay-Dale
R8	1	1.00 k	RES, 1.00 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K00FKED	Vishay-Dale
R9, R31	2	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo
R11	1	10 k	RES, 10 k, 5%, 0.1 W, 0603	0603	RC0603JR-0710KL	Yageo
R13	1	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R14	1	16.9 k	RES, 16.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0716K9L	Yageo
R15	1	28.0 k	RES, 28.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0728KL	Yageo
R17	1	6.04 k	RES, 6.04 k, 1%, 0.1 W, 0603	0603	RC0603FR-076K04L	Yageo
R18	1	49.9 k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0749K9L	Yageo
R19, R20	2	1.00 k	RES, 1.00 k, 1%, 0.1 W, 0603	0603	RC0603FR-071KL	Yageo
R21	1	20.0 k	RES, 20.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0720KL	Yageo

Table 5-1. TPS543320EVM Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R22, R48	2	100 k	RES, 100 k, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEAC	Vishay-Dale
R23	1	22.1 k	RES, 22.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0722K1L	Yageo
R24	1	9.76 k	RES, 9.76 k, 1%, 0.1 W, 0603	0603	RC0603FR-079K76L	Yageo
R25	1	5.62 k	RES, 5.62 k, 1%, 0.1 W, 0603	0603	RC0603FR-075K62L	Yageo
R26	1	2.67 k	RES, 2.67 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K67L	Yageo
R27	1	0	RES, 0, 5%, 1 W, AEC-Q200 Grade 0, 2512	2512	CRCW25120000Z0EG	Vishay-Dale
R29	1	453	RES, 453, 1%, 0.1 W, 0603	0603	RC0603FR-07453RL	Yageo
R30	1	66.5 k	RES, 66.5 k, 1%, 0.1 W, 0603	0603	RC0603FR-0766K5L	Yageo
R33	1	17.4 k	RES, 17.4 k, 1%, 0.1 W, 0603	0603	RC0603FR-0717K4L	Yageo
R34	1	11.8 k	RES, 11.8 k, 1%, 0.1 W, 0603	0603	RC0603FR-0711K8L	Yageo
R35	1	8.06 k	RES, 8.06 k, 1%, 0.1 W, 0603	0603	RC0603FR-078K06L	Yageo
R36	1	4.99 k	RES, 4.99 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K99L	Yageo
R37	1	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic
R38	1	0.1	RES, 0.1, 1%, 3 W, 2512	2512	CRA2512-FZ-R100ELF	Bourns
R40	1	2.21 k	RES, 2.21 k, 1%, 0.1 W, 0603	0603	RC0603FR-072K21L	Yageo
R41	1	4.87 k	RES, 4.87 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K87L	Yageo
R42	1	11.3 k	RES, 11.3 k, 1%, 0.1 W, 0603	0603	RC0603FR-0711K3L	Yageo
R43	1	60.4 k	RES, 60.4 k, 1%, 0.1 W, 0603	0603	RC0603FR-0760K4L	Yageo
R44, R45, R46, R47, R49	5	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8	8	1x2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP6, TP7, TP11, TP12, TP14, TP15, TP18, TP21, TP23	11		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP4, TP5, TP8, TP16, TP17, TP19, TP20, TP33	8		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
TP9, TP22, TP24, TP26, TP27, TP34	6		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone
TP10, TP28, TP29	3		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
TP31, TP32	2		Test Point, Multipurpose, Yellow, TH	Yellow Multipurpose Testpoint	5014	Keystone
U1, U2	2		4-V to 18-V Input, 6-A Synchronous SWIFT Step-Down Converter	VQFN-HR14	TPS543320RPYR	Texas Instruments
U3, U4	2		Single Bus Buffer Gate with 3-State Output, DCK0005A, LARGE T&R	DCK0005A	SN74AHC1G125DCKR	Texas Instruments
C18	0	330 µF	CAP, Aluminum Polymer, 330 µF, 2.5 V, ±20%, 0.006 Ω, 7343-20, SMD	7343-20	EEFSX0E331XE	Panasonic
C19	0	0.01 µF	CAP, CERM, 0.01 µF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H103JA01D	MuRata
C20, C32	0	0.1 µF	CAP, CERM, 0.1 µF, 25 V, ±5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
C23, C24	0	47 µF	CAP, CERM, 47 µF, 10 V, ±20%, X7R, 1210	1210	LMK325B7476MM-PR	Taiyo Yuden
C25, C26, C30, C31	0	100 µF	CAP, CERM, 100 µF, 6.3 V, ±20%, X7S, 1210	1210	GRM32EC70J107ME15L	MuRata
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J1, J3, J6, J10	0		Standard Banana Jack, Uninsulated, 5.5 mm	Keystone_575-4	575-4	Keystone
J12	0		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
L3	0	27 µF	FILTER LC HIGH FREQ 27 µF 1206	3.2x1.6 mm	NFM31PC276B0J3L	MuRata
R16	0	10.0	RES, 10.0, 1%, 0.1 W, 0603	0603	RC0603FR-0710RL	Yageo
R28	0	0	RES, 0, 5%, 1 W, AEC-Q200 Grade 0, 2512	2512	CRCW25120000Z0EG	Vishay-Dale
R32	0	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo
R39	0	0.1	RES, 0.1, 1%, 3 W, 2512	2512	CRA2512-FZ-R100ELF	Bourns

Table 5-1. TPS543320EVM Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
TP25	0		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP30	0		Connector, Receptacle, 50 Ω, TH	SMB Connector	SMBR004D00	JAE Electronics

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (May 2021)	Page
• Updated user's guide title	3

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265