User's Guide

TPS7H3301EVM-CVAL (HREL022)

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1 Introduction

The TPS7H3301EVM-CVAL evaluation board, HREL022 is designed to evaluate the performance and characteristics of TI's Rad Hard DDR/DDR2/DDR3/DDR3L/DDR4 termination regulator, the TPS7H3301-SP.

Figure 1-1 and Figure 1-2 illustrate the EVM board.

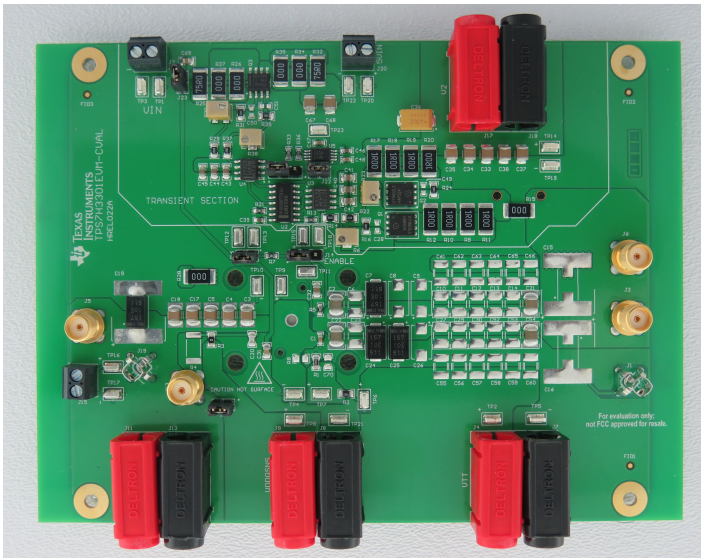


Figure 1-1. TPS7H3301EVM Board (Top View)

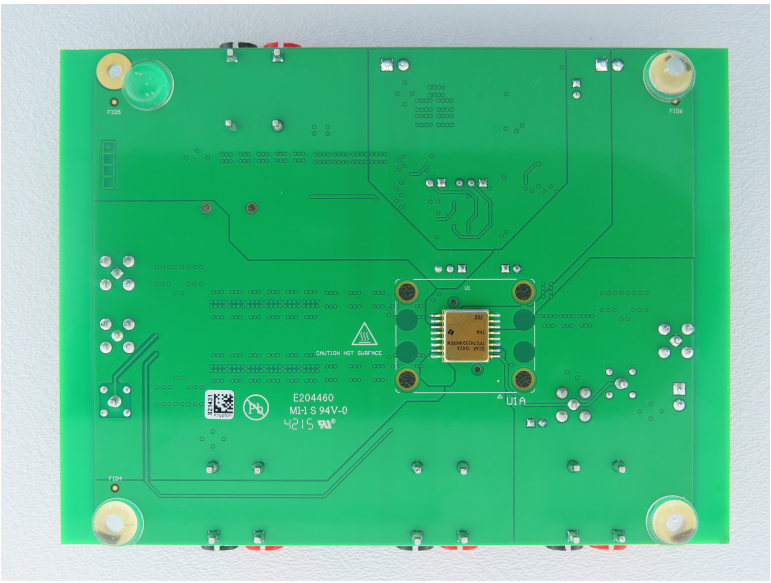


Figure 1-2. TPS7H3301EVM Board (Bottom View)

1.1 Background

The TPS7H3301EVM-CVAL is a full featured EVM designed to facilitate prototyping and testing of the TPS7H3301-SP radiation hardened 3 A DDR termination regulator.

2 Description

The TPS7H3301-SP is a TID and SEE radiation hardened double data rate (DDR) 3-A termination regulator with built-in VTTREF buffer. The regulator is specifically designed to provide a complete, compact, low-noise solution for space DDR termination applications such as single board computers, solid state recorders, and payload processing.

The TPS7H3301-SP supports DDR VTT termination applications using DDR, DDR2, DDR3, DDR4. The fast transient response of the TPS7H3301-SP VTT regulator allows for a very stable supply during read/write conditions. During transients, the fast tracking feature of the VTTREF supply minimizes any voltage offset between VTT/Vo and VTTREF. To enable simple power sequencing, both an enable input and a power-good output (PGOOD) have been integrated into the TPS7H3301-SP. The PGOOD output is open-drain so it can be tied to multiple open-drain outputs to monitor when all supplies have come into regulation. The enable signal can also be used to discharge VTT/Vo during suspend to RAM (S3) power down mode.

2.1 Related Information

- TPS7H3301-SP data sheet (SLVSCJ5)

2.2 Typical Applications

The EVM is used in the following applications:

- Radiation-tolerant DDR power applications
- Memory termination regulator for DDR, DDR2, DDR3, DDR4

2.3 Features

This EVM has the following features:

- Input Voltage: Supports 2.5-V rail and 3.3-V rail
- V_{LDOIN}, V_{DDQ} voltage range: 0.9 V–3.5 V
- Built-in transient load switches (with both sinking and sourcing capability) to emulate the sink/source transient behavior which helps to evaluate the dynamic performance. For ease of use, both load step and transient timing can be modified by on-board resistors. The EVM has four parallel 1 ohm resistors connected for transient load for both the VTT/V_O to GND, and VTT/V_O to V2 to accommodate both sourcing and sinking evaluation.

  CAUTION

  The default EVM configuration using the built-in transient test circuit supports testing the DDR3 node with maximum rated load of ±3 A. To evaluate DDR, DDR2 or lower currents for DDR3, DDR3L, and DDR4 the total resistance of resistors R9-R12, and R17-R20 will need to be increased to not exceed device maximum ratings.

- Jumper J14 (pins 1 and 2) for device enable.
- Convenient test points for probing PGOOD, CLK_IN, and loop response testing.
- 4-layer PCB with flexibility to use test socket as well as solder down IC.

2.4 Performance Specification Summary

Table 2-1 lists the EVM performance specifications.

Table 2-1. Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input voltage range, (V_{VIN})		2.37	3.3	3.5	V
VDDQ voltage range (V_{VDDQ})		1.2		2.5	
VLDOIN voltage range (V_{VLDOIN})		0.9		3.5	
VTT/V_O Termination Voltage					
DDR	VTT/V_O		1.25		
	VTTREF		1.25		
DDR2	VTT/V_O		0.9		
	VTTREF		0.9		
DDR3	VTT/V_O		0.75		
	VTTREF		0.75		
DDR4	VTT/V_O		0.6		
	VTTREF		0.6		
VTT/V_O termination voltage tolerance to VTTREF		–34		34	mV
Termination current (I_{VTT})		–3		3	A
VTTREF voltage tolerance		–15		15	mV
Reference current (I_{VTTREF})		–10		10	mA
Sink current limit (I_{VTT})		3.5		5.5	A
Source current limit (I_{VTT})		3.25		8	

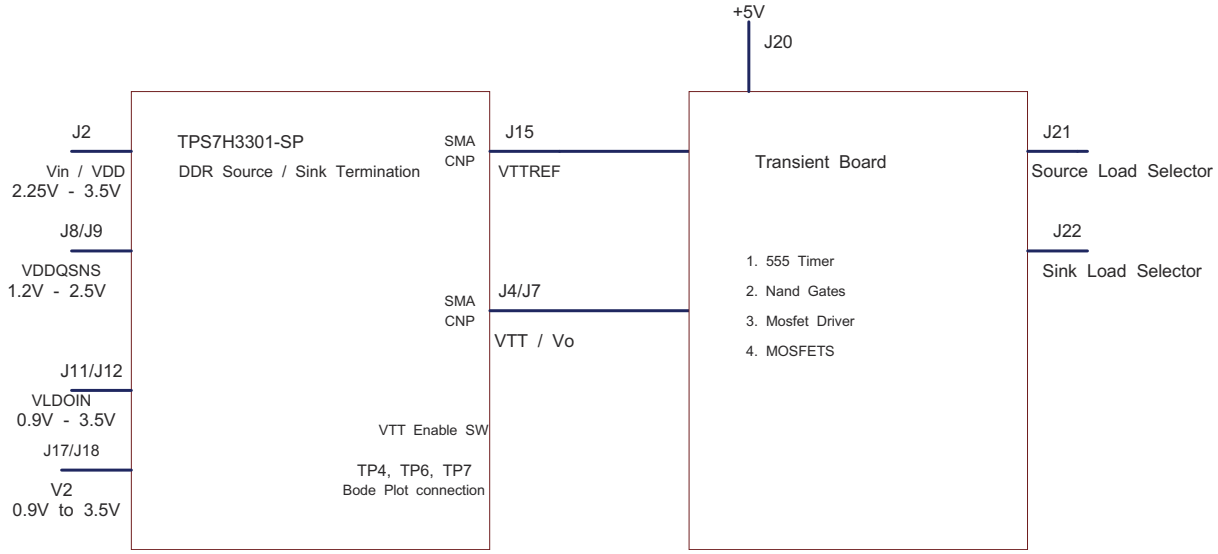


Figure 2-1. EVM Block Diagram

3 Test Setup

3.1 Equipment

3.1.1 Power Supplies

Power supply #1 (PS#1): a power supply capable of supplying up to 3.5 V at 6 A is required for VLODIN.

Power supply #2 (PS#2): a power supply capable of supplying up to 3.5 V at 100 mA is required for VIN.

Power supply #3 (PS#3): a power supply capable of supplying up to 5 V at 100 mA is required to power transient board.

3.1.2 Load #1

Electronic load, that is, Chroma 63640-80-80 module along with 63600-2 DC electronic load Mainframe or Decade Resistor Box.

Keithley 2460 Hi Current Digital Source meter TE P/N 22734-1 or equivalent (Qty 2).

3.2 EVM Connectors and Test Points

Table 3-1 lists the EVM connectors and test points.

Table 3-1. Connectors and Test Points

Reference Designator	Function
J1	Cold nose probe connected to VTT, used to monitor output voltage via scope
J2	Input voltage (pin 1) and ground (GND; pin 2) terminal block. VIN range is from 2.375 V to 3.5 V
J3	SMA connected to VTT
J4	VTT (external load can be applied here)
J5	VLDOIN SMA connection
J6	SMA connected to VTT
J7	Ground (GND) connection of VTT (external load GND)
J8	Ground (GND)
J9	VDDQSNS voltage range 1.2 V – 2.5 V
J10	Jumper to connect VDDQSNS to VLDOIN
J11	VLDOIN
J12	Ground (GND) for VLDOIN
J13	SMA VTTREF
J14	Enable jumper (pins 1 and 2) to enable the device. Jumper pins 2 and 3 to disable.
J15	VTTREF output
J16	Jumper (pins 1 and 2) connects EN (enable) to Vin
J17	V2 voltage for DDR sink – transient test
J18	Ground (GND)
J19	VTTREF cold nose probe connection
J20	Input voltage (pin 1) and ground (GND; pin 2) terminal block. Power for transient board , VIN should be 5.0 V nominal , VIN range is from 4.9 V to 5.1 V.
J21	Source load selector: Jumper (pins 1 and 2), part of transient board
J22	Sink load selector: Jumper (pins 1 and 2) part of transient board
J23	Connection for VTTREF transient test
TP1	Test point for the input voltage node (Vin/Vdd)
TP2	VTT/V_O
TP3	Ground (GND)
TP4	Ground (GND)
TP5	Ground (GND)
TP6	Injection point for bode plot measurements connect injection signal across TP6 and TP7 for bode plot measurements

Table 3-1. Connectors and Test Points (continued)

Reference Designator	Function
TP7	Injection point for bode plot measurements connect injection signal across TP6 and TP7 for bode plot measurements
TP8	Test point connected to VDDQSNS
TP9	Test point connected to VLDOIN
TP10	Test point connected to VLDOIN Ground (GND)
TP11	Power Good
TP12	Test point Vin
TP13	Test point Vin
TP14	Test point V2
TP15	Test point enable
TP16	Test point VTTREF
TP17	Test point ground (GND)
TP18	Test point ground (GND)
TP19	Test point ground (GND)
TP20	Test point 5Vin bias for transient board
TP21	Test point ground (GND)
TP22	Test point ground (GND)
TP23	Test point clock

Table 3-2 displays the input voltage and output current for the TPS7H3301EVM-CVAL.

Table 3-2. Input Voltage and Output Current for TPS7H3301EVM-CVAL

EVM	Input Voltage Range	Output Current Range
TPS7H3301EVM-CVAL	2.375 V ≤ V_{IN} ≤ 3.5V	I_{IN} ≤ 1 A
	0.9 V ≤ VLDOIN ≤ 3.5V	I_{IN} ≤ 6 A
	1.2 V ≤ VDDQSNS ≤ 3.5V	I_{IN} ≤ 1 A
	0.6 V ≤ VTTREF ≤ 1.75V	I_{OUT}≥ - 10 mA ≤ 10 mA
	0.6 V ≤ VTT / V_O ≤ 1.75V	I_{OUT} ≥ -3 A ≤ 3 A

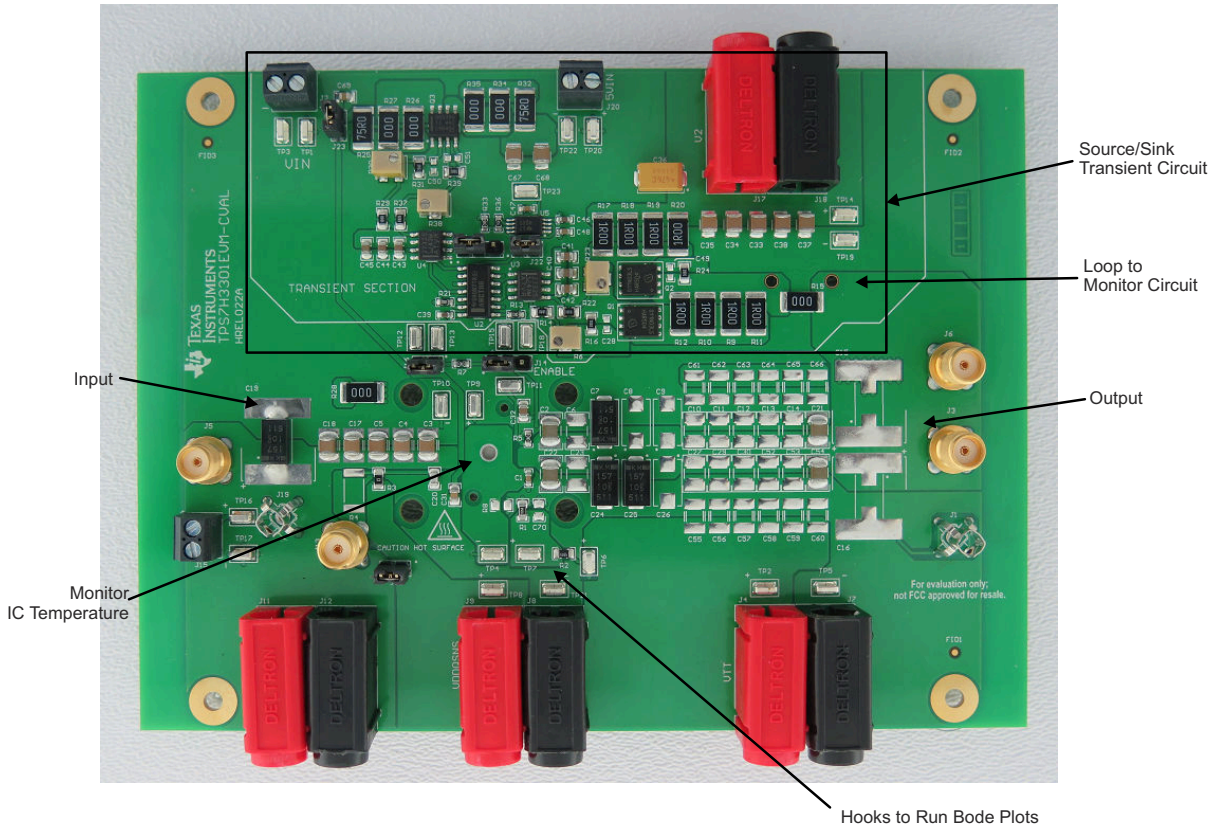


Figure 3-1. TPS7H3301EVM-CVAL Board

3.3 Testing Procedure

Use these steps for testing the EVM with a static external load:

1. Ensure all supplies are off prior to connecting the EVM.
2. Be sure to insure proper polarity of power supply and load connections.
3. Place a jumper on J14 (pins 1 and 2), Enable high.
4. Place a jumper on J10 (pins 1 and 2), connecting VDDQSNS to VLDOIN.
   a. Alternately a separate voltage source can be used for VLDOIN and a separate voltage source of VDDQSNS, thus isolating the two. This isolates the transients introduced on VLDOIN from impacting VDDQSNS. Additionally, it allows for reduced internal power dissipation if VLDOIN is reduced to VTT/V_O + VDO.
5. Set the load to sink desired current up to 3 A.
6. Connect a power supply to J2 - VIN using screw terminals or test points TP1 and TP3. Vin current is less than 100 mA.
7. Connect power supply to J10/J11 - VLDOIN. VLDOIN current can be up to 6 A.
8. Connect VIN voltmeter (+) terminal to TP1 and (–) terminal to TP3 to monitor input voltage.
9. Connect VTT/V_O voltmeter (+) terminal to TP2 and (–) terminal to TP5.
10. Connect the load (+) to J4 and (–) to J7. Connect a current meter in series, if necessary. This will test VTT/V_O sourcing current. Alternatly, connect isolated load (+) from J11 VLDOIN and (-) to J4 to test VTT/V_O sinking.
11. Set the power supply for VLDOIN to 1.8 V.
12. Set the power supply for VIN to 3 V.
13. Enable both VIN and VLDOIN supplies.
14. Connect voltmeter monitoring V_{TTREF} at TP16 (+ve) and TP17 (-ve).
15. The voltmeter monitoring Vo/ VTT should read 0.9 V (see Table 3-3).
16. Turn off the supplies.
17. Move the jumper J14 to the “OFF” side Pin 2-3 shorted.
18. Turn on the supplies.
19. The voltmeter monitoring Vo/VTT should read near zero volts.
20. Connect source meter at J15. Note, VTTREF is active when device is disabled.
21. VTTREF voltage is monitored at TP16 and TP17.
22. Using source meter, load VTTREF J15 (pins 1 and 2) to source 10 mA, monitor and record V_{TTREF} voltage.
23. Using source meter, sink 10 mA and record VTTREF voltage.

Table 3-3 displays the input voltage and output voltage measurement test point. Using the following connection points, monitor VTT and VTTREF regulation overline and overload.

Table 3-3. I/O Voltage Measurement Test Point

EVM	Input / Output Voltage		Test point
TPS7H3301EVM-CVAL	V_{IN}	2.375 V ≤ V_{IN} ≤ 3.5 V	TP1 (+) TP3(–)
	V_{LDOIN}	0.9 V ≤ V_{LDOIN} ≤ 3.5 V	TP9(+) T10(–)
	V_{DDQSNS}	1.2 V ≤ V_{DDQSNS} ≤ 3.5 V	TP8(+) TP10(–)
	V_{TT} / Vo	½ V_{DDQSNS}	TP6(+) TP4(–)
	V_{TTREF}	½ V_{DDQSNS}	TP16(+) TP17(–)

3.3.1 EVM Bode Plot Measurement Setup

The setup for EVM bode plot measurement is as follows:

1. Using a Bode 100 loop analyzer or equivalent equipment.
2. Remove jumper on J10. This isolates VDDQSNS from VLDOIN. To test with VLDOIN tied to single VDDQ along with VDDQSNS, the optional filter will need to be used. See note below.
3. Connect the oscillator output across R2 = 49.9-Ω resistor. Connect the positive connection to TP7 and return to TP6.
4. Connect Channel 2 of the analyzer at TP6 and connect ground to TP4

5. Connect Channel 1 of the analyzer at TP7 and connect ground to TP4.
6. Power EVM with desired conditions for VLDOIN, Vin, VDDQSNS and VTT/V_O load
7. With the EVM loaded to the required load, run bode plot over frequency range from 1 Hz to 5 MHz.

> All of the bode measurements presented, VDDQSNS is provided from an independent supply from VLDOIN. If VDDQSNS and VLDOIN inputs are connected to same supply, then the isolation filter on the EVM should be used to isolate the load effects on VLDOIN from VDDQSNS. The filter can be used by replacing components for R3, and C20.

Figure 3-2 through Figure 3-6 show bode plots for this EVM. All plots generated using default C_{IN} and C_{OUT} capacitances populated on EVM. C_{IN} = 150 µF tantalum // 5 - 10 µF ceramic, C_{OUT} = 3 - 150 µF tantalum // 4 - 4.7 µF ceramic.

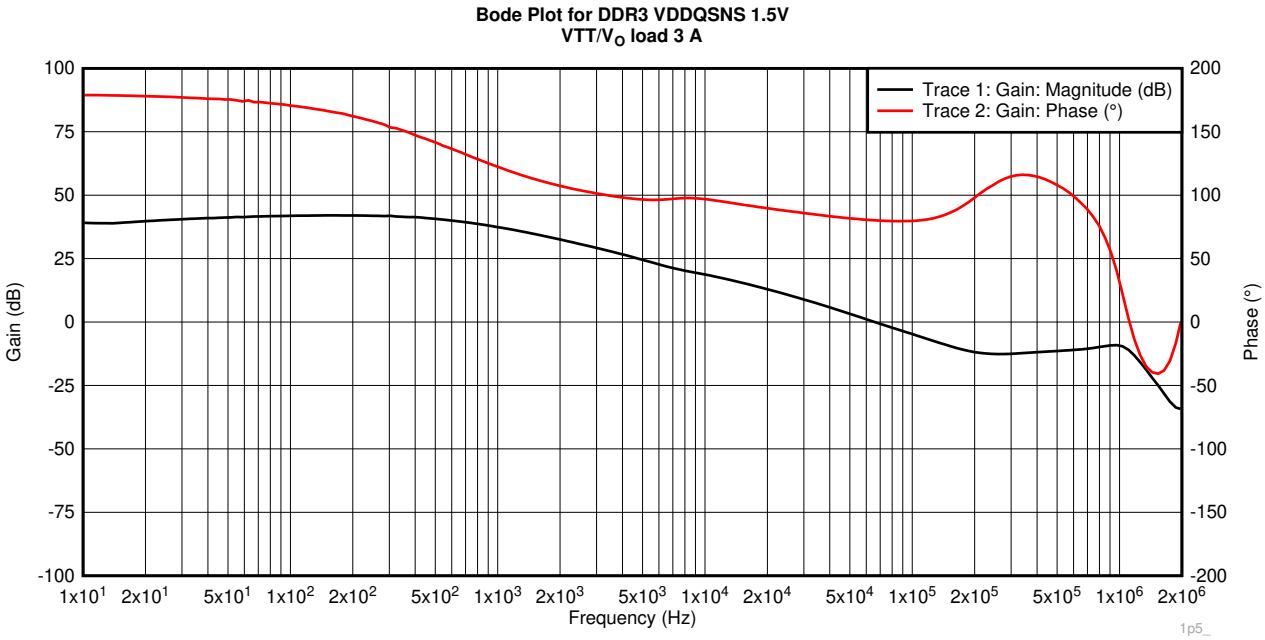


Figure 3-2. DDR3 Bode Plot Iload = 3 A

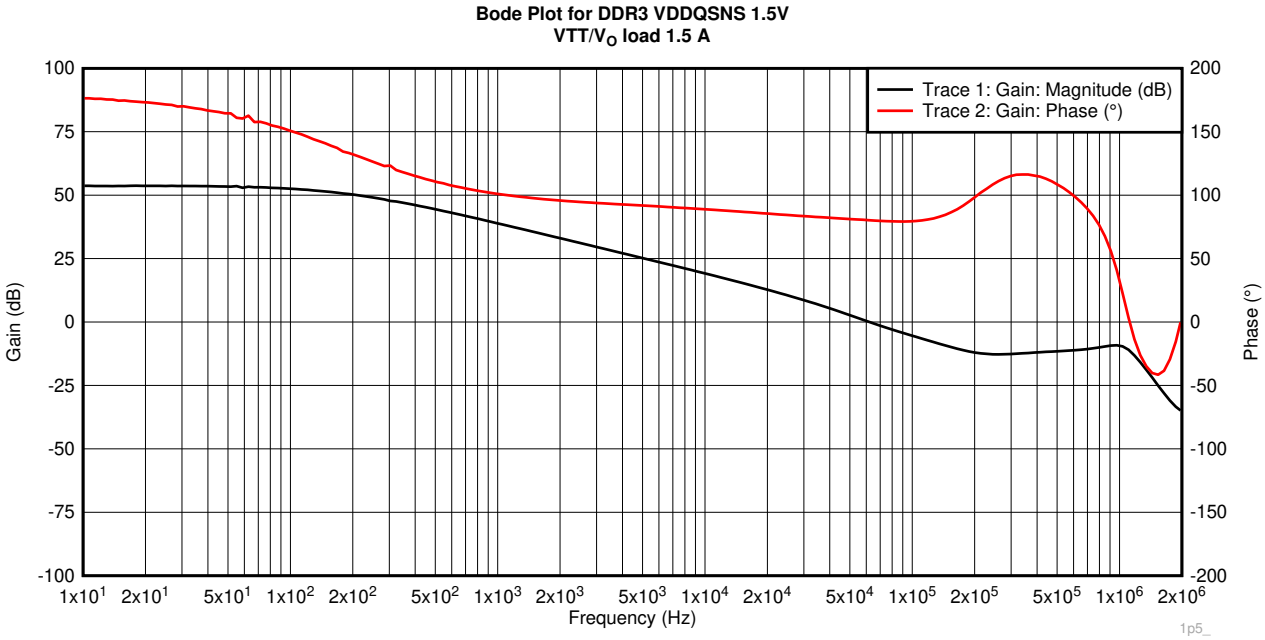


Figure 3-3. DDR3 Bode Plot Iload = 1.5 A

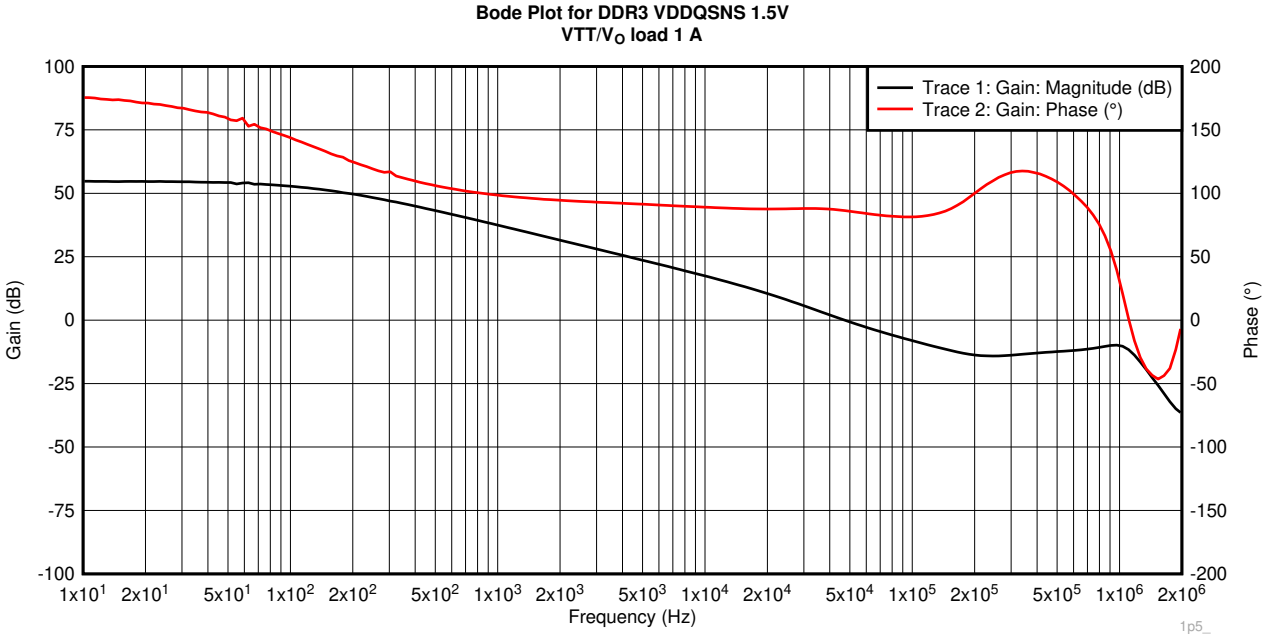


Figure 3-4. DDR3 Bode Plot Iload = 1 A

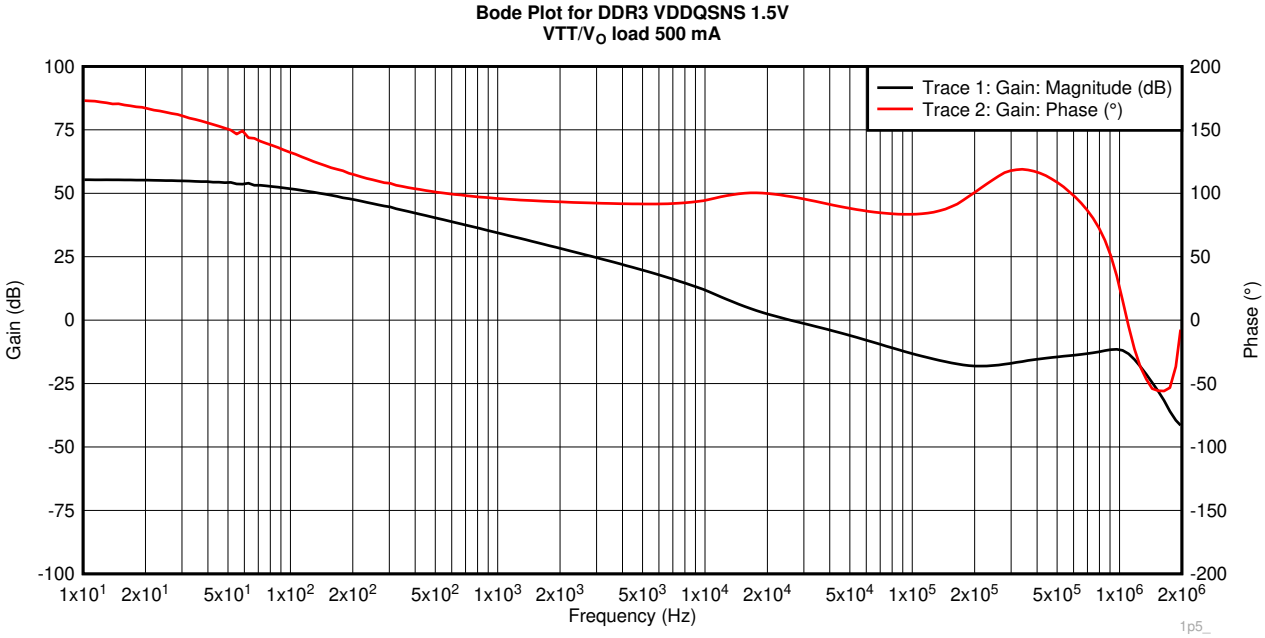


Figure 3-5. DDR3 Bode Plot Iload = 500 mA

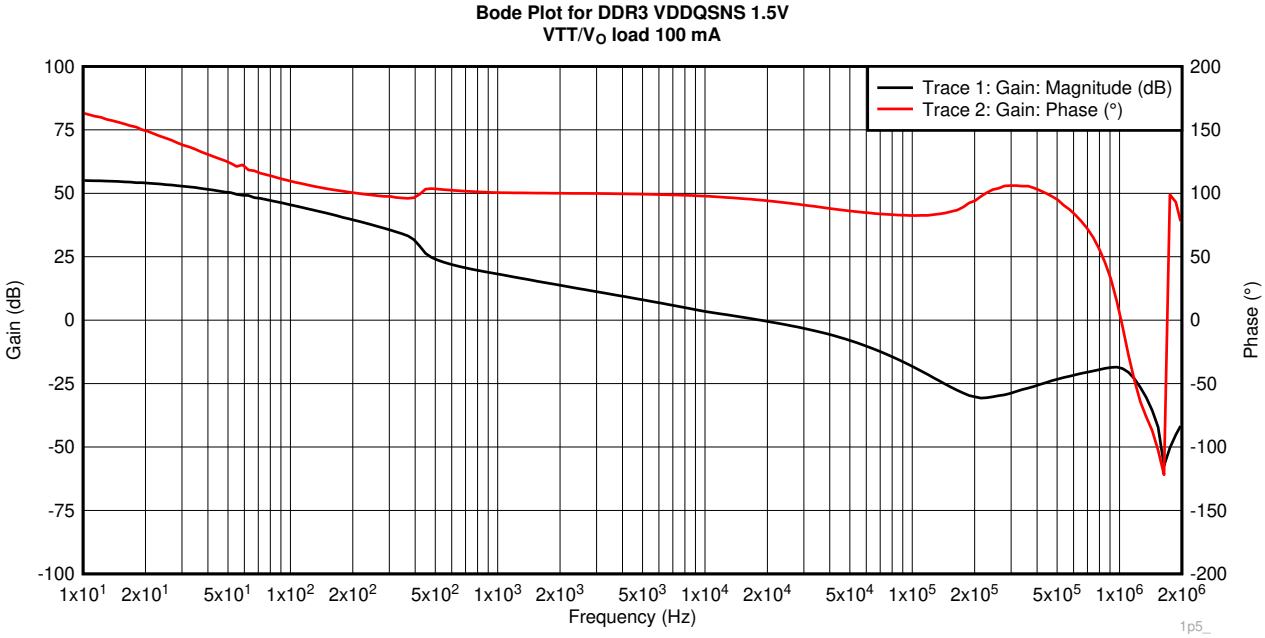


Figure 3-6. DDR3 Bode Plot Iload = 100 mA

It is recommended that VLDOIN and VDDQSNS be isolated from each other, if this is not possible then add an external input filter between VLDOIN and VDDQSNS. Adding an RC filter between VLDOIN and VDDQSNS will result in some loss of dynamic tracking of VTT and VTTREF to be lost.

3.3.2 EVM Transient Test

A transient test setup circuit is incorporated as part of the EVM.

CAUTION

The default EVM configuration using the built-in transient test circuit supports testing the DDR3 node with maximum rated load of ±3 A. To evaluate DDR, DDR2 or lower currents for DDR3, DDR3L, and DDR4 the total resistance of resistors R9-R12, and R17-R20 will need to be increased to not exceed device maximum ratings.

1. Verify if R15 0 Ω resistor is installed. R15 may have been removed during factory test. R15 is required to connect VTT/V_O to the transient load circuit. A wire shunt or 0 Ω 2512 resistor should be installed across R15 pads.
2. Remove any external loads
3. Remove Jumper from J23 isolating VTTREF from transient test circuit.
4. Jumper J21 (pins 1 and 2) source load selector
5. Jumper J22 (pins 1 and 2) sink load selector
6. Remove jumper J10 to isolate VDDQSNS from VLDOIN.
7. Apply 2.5 V to V_{IN}
8. Apply 1.5 V to J11/J12 VLDOIN
9. Apply 1.5 V to J9/J8 VDDQSNS. If testing with VDDQSNS not isolated from VLDOIN, install J10, and only apply to VLDOIN.
10. Monitor VTT/V_O to ensure VTT/V_O voltage is present. VTT/V_O should be approximately 750 mV.
11. Apply 5 V to J20 (pin 1 (+), pin 2 (–)), this provides power to the transient load setup
12. Monitor VTT/Vo at J1 using a scope to see transient results.

Figure 3-7 shows the transient repsonse with VDDQSNS supplied independently from VLDOIN. This isolates the transient effects on VLDOIN supply and unintended disturbances to VDDQSNS. Figure 3-8 shows the effects having VDDQSNS not isolated from VLDOIN. Transient response can be improved with implementation of a filter on VDDQSNS from VLDOIN. The filter can be implemented by replacing components for R3, and C20.

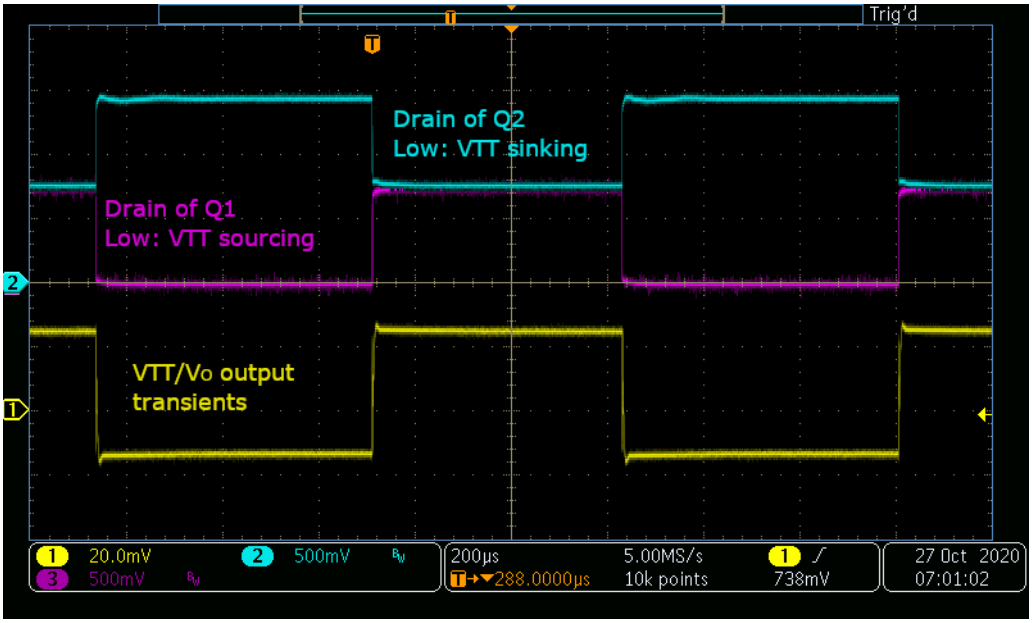
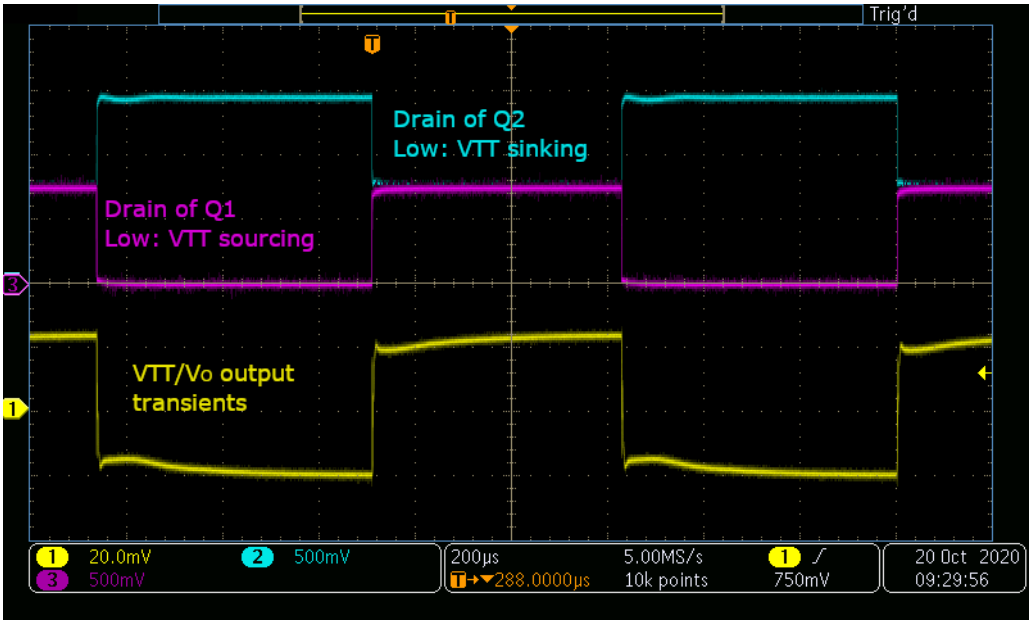


Figure 3-7. DDR3 Transient Response 3 A Source-Sink Load with VDDQSNS isolated from VLDOIN



A. DDR3 V_{TT} = 0.75 V, VLDOIN = 1.5 V, VDDQ = 1.5 V, step load ± 3 A source/sink. C_{IN} = 150 µF tantalum // 5 - 10 µF ceramic, C_{OUT} = 3 - 150 µF tantalum // 4 - 4.7 µF ceramic.

Figure 3-8. DDR3 Transient Response 3 A Source-Sink Load with VDDQSNS not isolated from VLDOIN

4 Board Layout

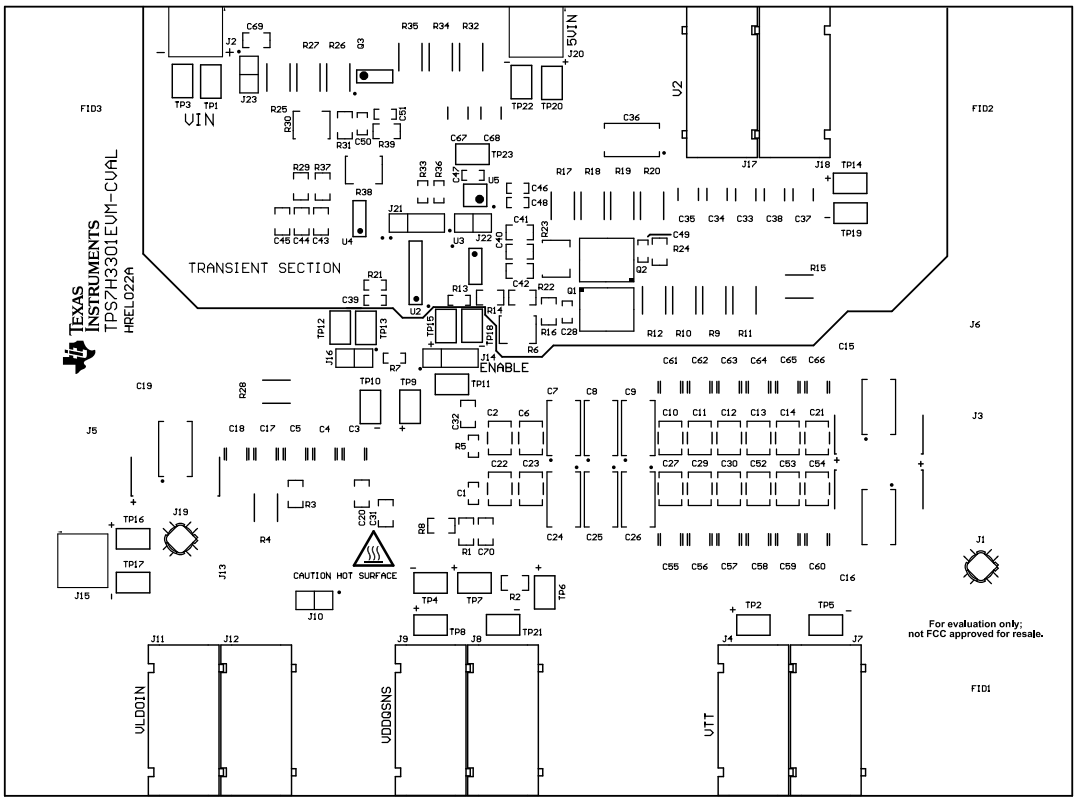


Figure 4-1. Top Overlay

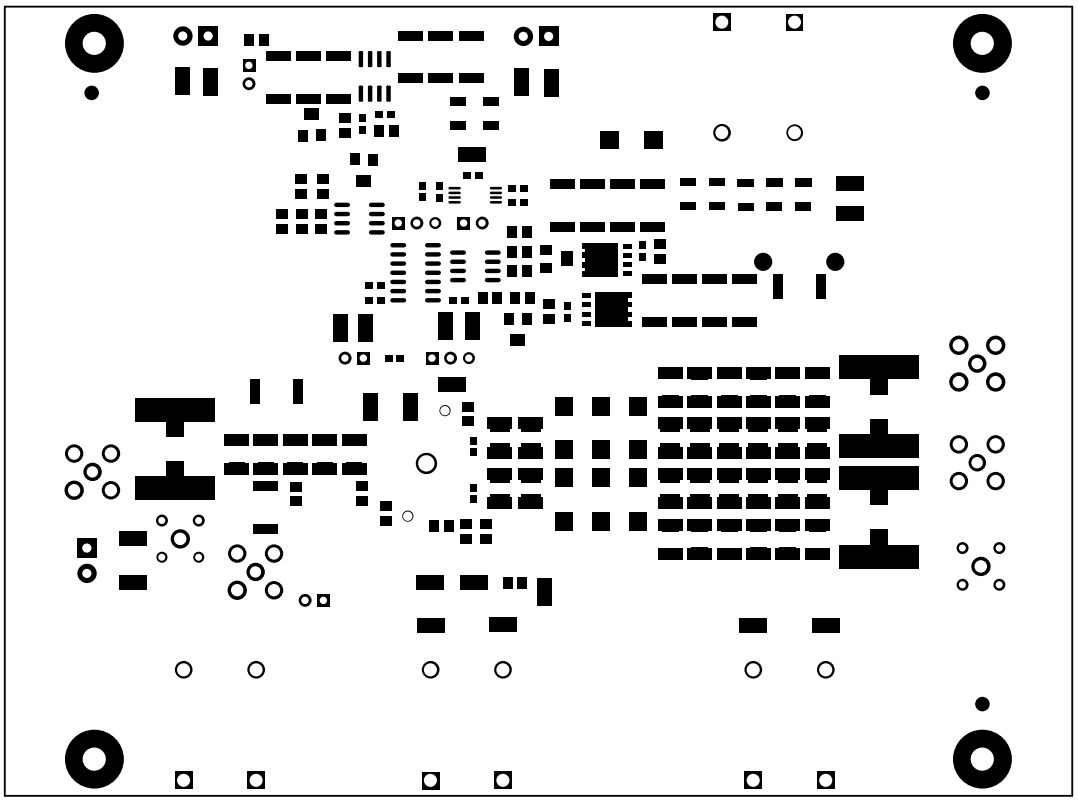


Figure 4-2. Top Solder

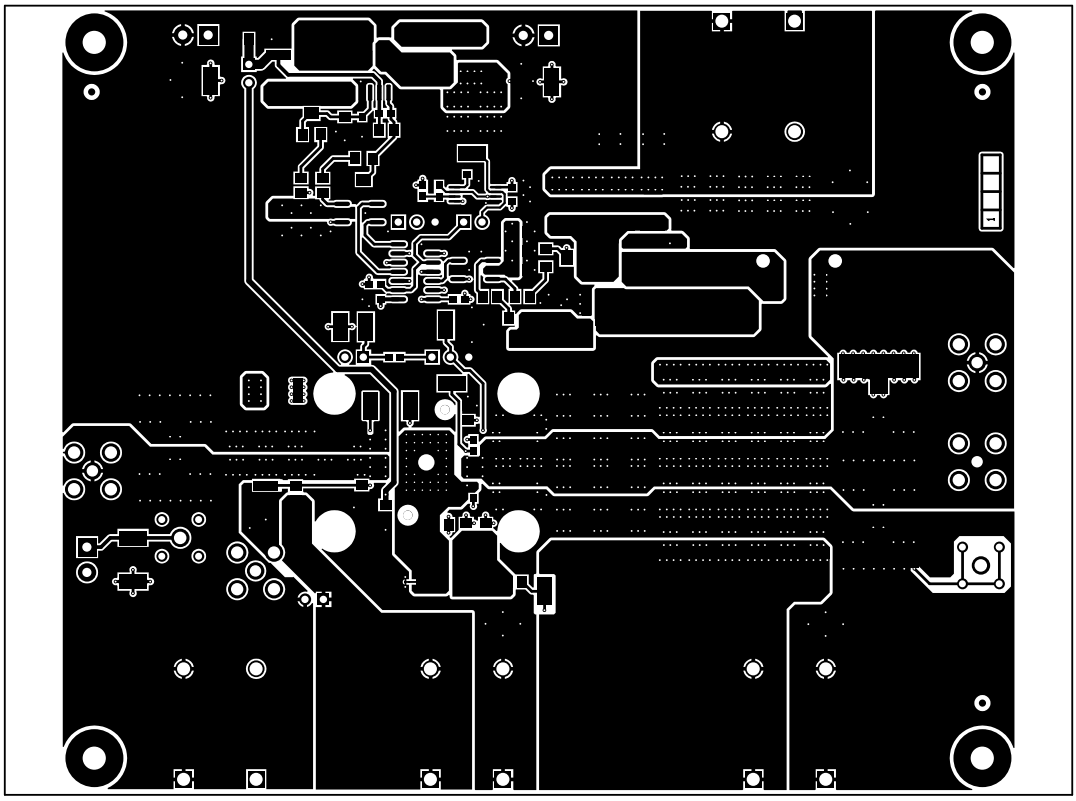


Figure 4-3. Top Layer

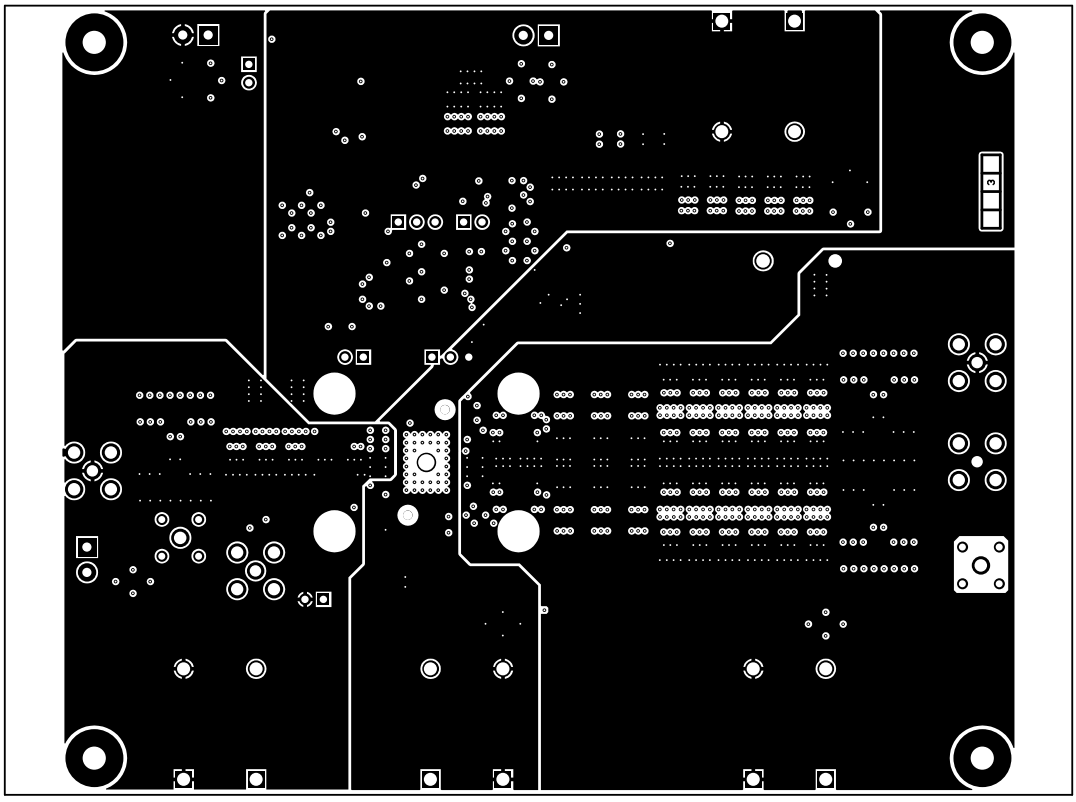


Figure 4-4. Middle Layer Split Power

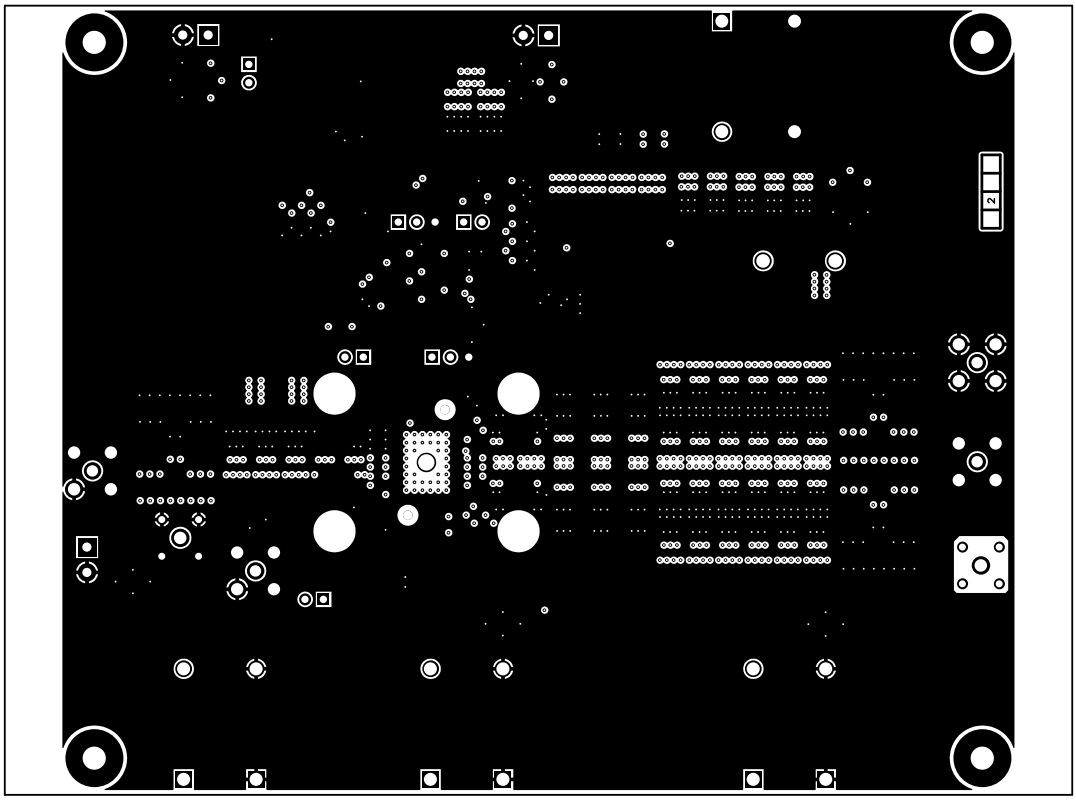


Figure 4-5. Ground Layer

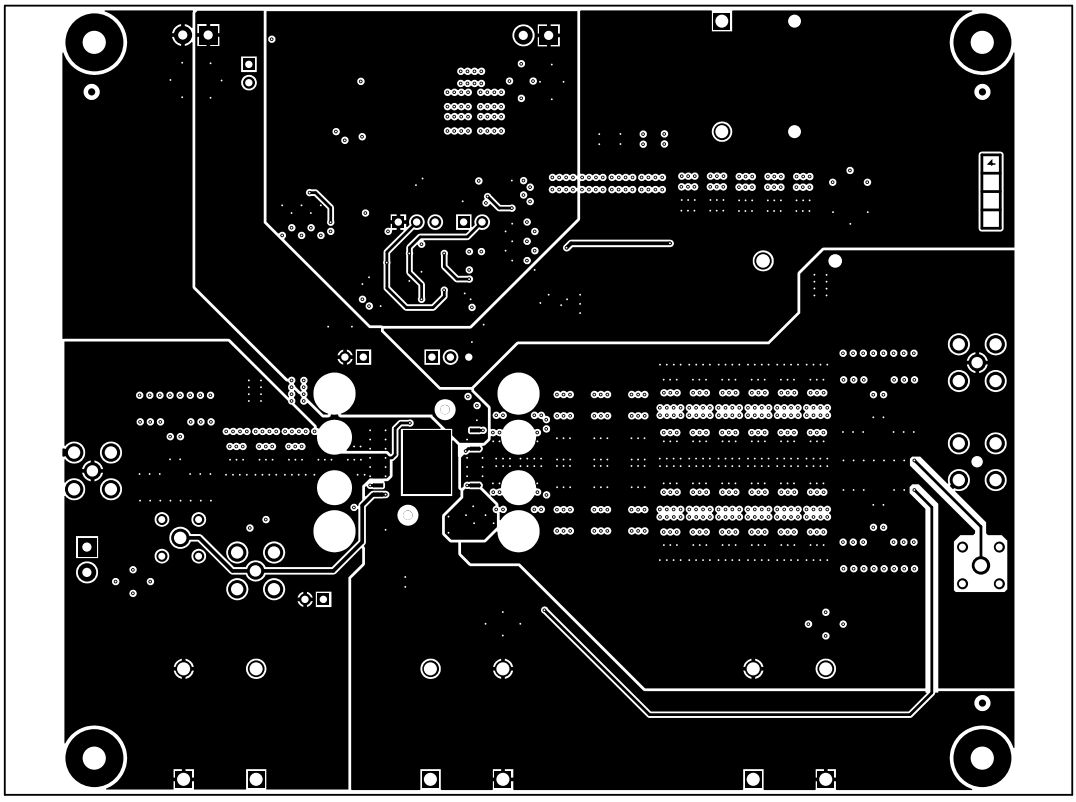


Figure 4-6. Bottom Layer

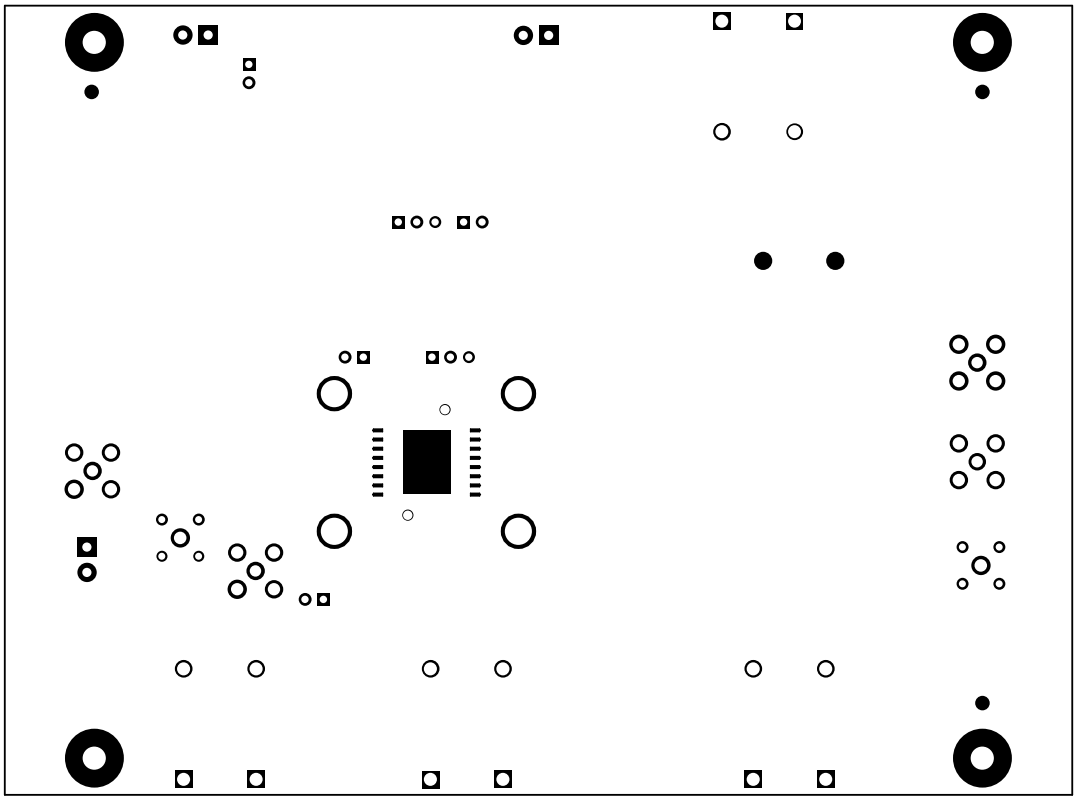


Figure 4-7. Bottom Solder

5 Schematic

Figure 5-1 and Figure 5-2 illustrate the TPS7H3301EVM-CVAL schematics.

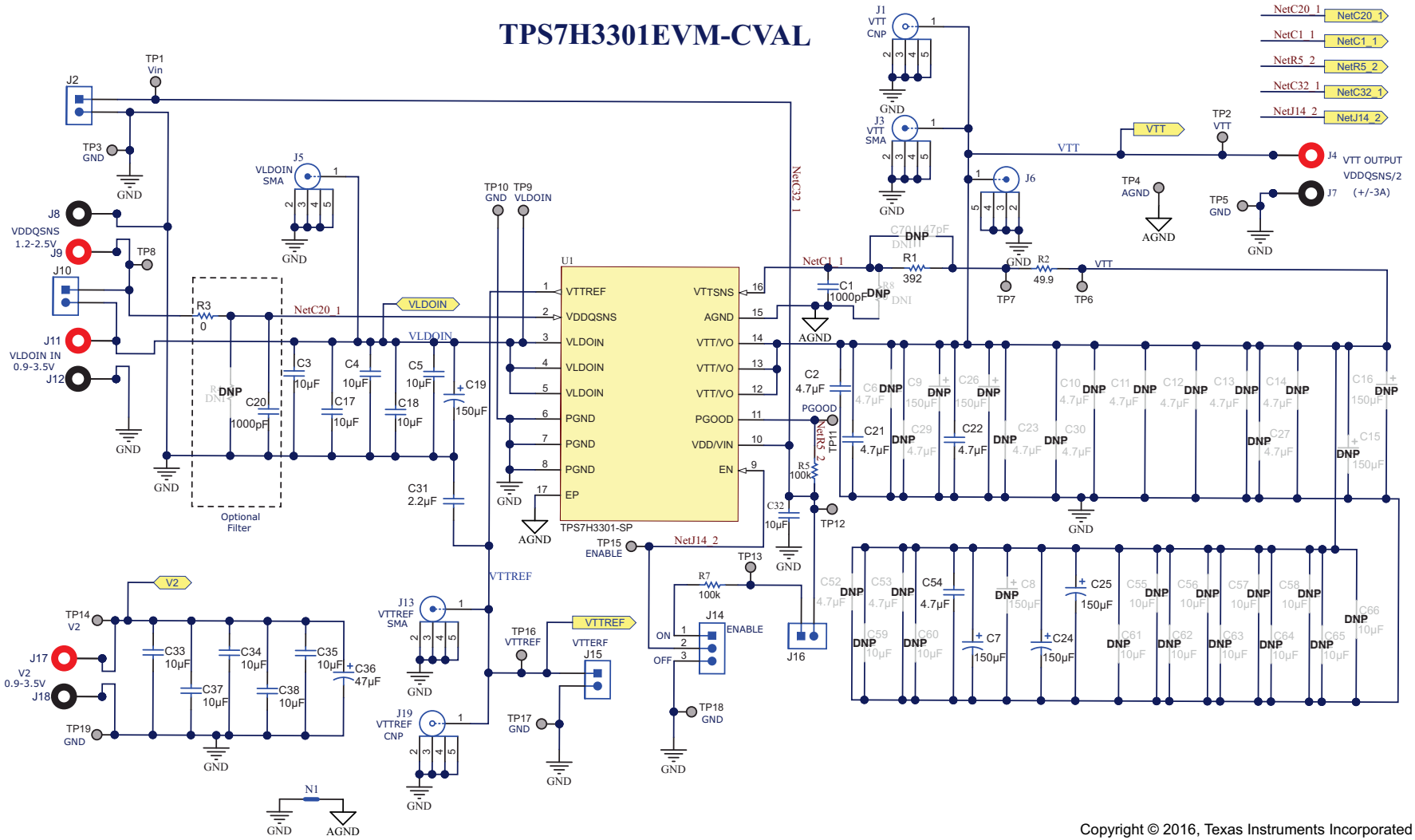


Figure 5-1. EVM Schematic

R1 = 392 Ω , C1 = 1000 pF pole added on the output feedback network.

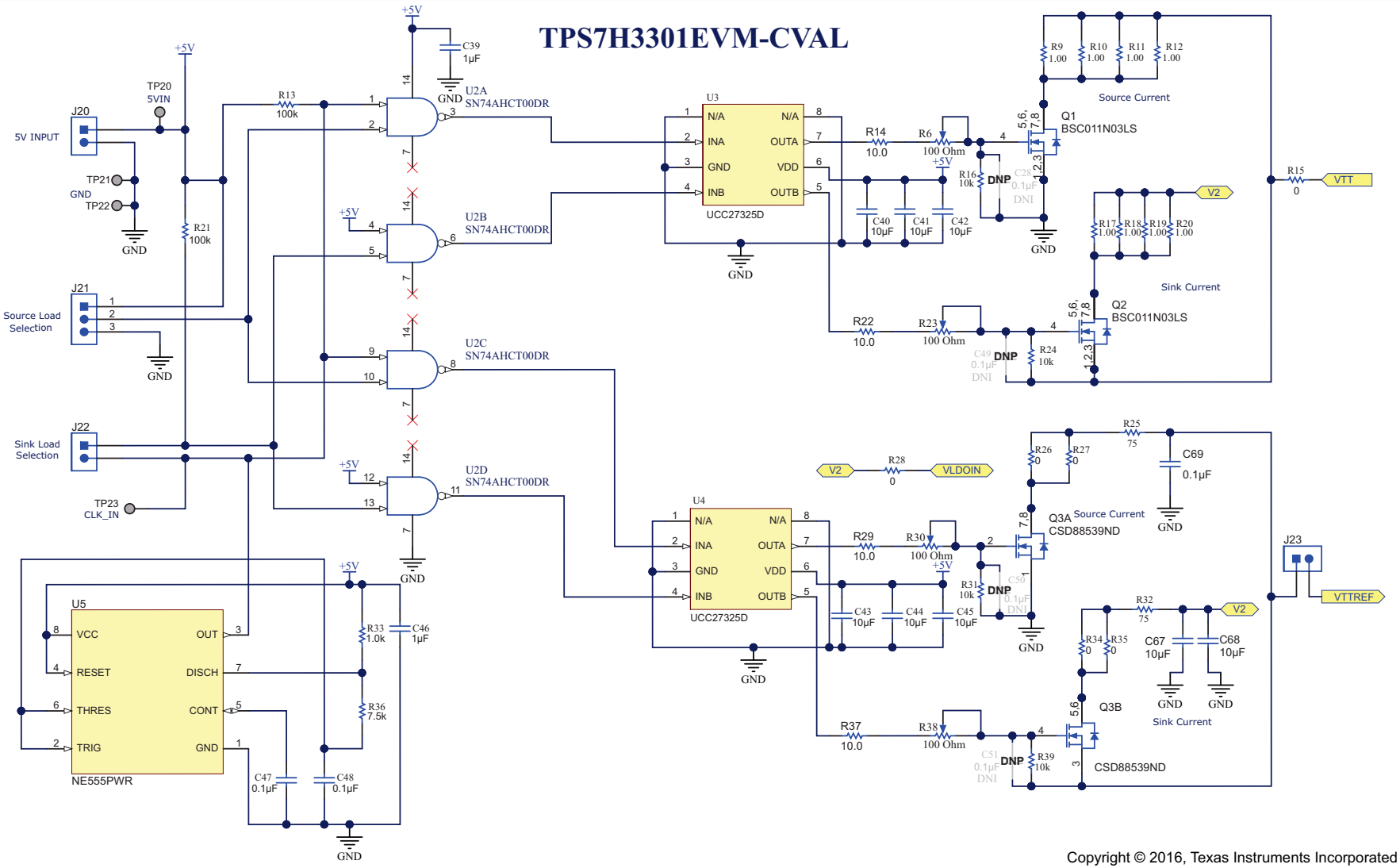


Figure 5-2. EVM Transient Board

6 Bill of Materials

Table 6-1 lists the EVM BOM.

Table 6-1. Bill of Materials

Item	Designator	Description	Manufacturer	Part Number	QTY	Value
1	!PCB1	Printed Circuit Board	Any	HREL022	1	
2	C1	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	Murata	GRM188R71H102KA01D	1	1000pF
3	C2, C21, C22, C54	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X7R, 1210	AVX	1210ZC475KAT2A	4	4.7uF
4	C3, C4, C5, C17, C18, C33, C34, C35, C37, C38, C67, C68	CAP, CERM, 10 µF, 10 V, +/- 10%, X8L, 1210	Kemet	C1210C106K8NACTU	12	10uF
5	C7, C19, C24, C25	CAP, Tantalum Polymer, 150 µF, 10 V, +/- 20%, 0.005 ohm, 7343-31 SMD	Kemet	T530D157M010ATE005	4	150uF
6	C20	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0805	AVX	08055C102KAT2A	1	1000pF
7	C31	CAP, CERM, 2.2 µF, 25 V, +/- 10%, X7R, 0805	AVX	08053C225KAT2A	1	2.2uF
8	C32, C40, C41, C42, C43, C44, C45	CAP, CERM, 10 µF, 10 V, +/- 10%, X7R, 0805	Murata	GRM21BR71A106KE51L	7	10uF
9	C36	CAP, TA, 47 µF, 16 V, +/- 20%, 0.08 ohm, SMD	AVX	TPSD476M016R0080	1	47uF
10	C39, C46	CAP, CERM, 1 µF, 10 V, +/- 10%, X5R, 0603	Murata	GRM188R61A105KA61D	2	1uF
11	C47, C48	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	Kemet	C0603C104K4RACTU	2	0.1uF
12	C69	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0805	AVX	08053C104KAT2A	1	0.1uF
13	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	BampersandF Fastener Supply	NY PMS 440 0025 PH	4	
14	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4	
15	J1, J19	Compact Probe Tip Circuit Board Test Points, TH, 25 per	Tektronix	131-5031-00	2	
16	J2, J15, J20	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS	3	
17	J3, J5, J6, J13	Connector, TH, SMA	Emerson Network Power	142-0701-201	4	
18	J4, J9, J11, J17	Standard Banana Jack, insulated, 10A, red	DEM Manufacturing	571-0500	4	10A
19	J7, J8, J12, J18	Standard Banana Jack, insulated, 10A, black	DEM Manufacturing	571-0100	4	10A
20	J10, J16, J22, J23	Header, 100mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S	4	
21	J14, J21	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	2	
22	Q1, Q2	MOSFET, N-CH, 30 V, 100 A, PG-TDSON-8	Infineon Technologies	BSC011N03LS	2	30V
23	Q3	MOSFET, N-CH, 60 V, 6.3 A, SO-8	Texas Instruments	CSD88539ND	1	60V
24	R1	RES, 392, 1.0%, 0.125 W, 0805	Vishay	CRCW0805392RFKEA	1	392
25	R2	RES, 49.9 ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW080549R9FKEA	1	49.9
26	R3	RES, 0, 5%, 0.125 W, 0805	Rohm	MCR10EZPJ000	1	0
27	R5, R7, R13, R21	RES, 100 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KJNEA	4	100k
28	R6, R23, R30, R38	Trimmer, 100 ohm, 0.25W, SMD	Bourns	3214W-1-101E	4	100 Ohm
29	R9, R10, R11, R12, R17, R18, R19, R20	RES, 1.00, 1%, 1 W, 2512	Vishay-Dale	CRCW25121R00FKEG	8	1.00
30	R14, R22, R29, R37	RES, 10.0, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080510R0FKEA	4	10.0
31	R15, R26, R27, R28, R34, R35	RES, 0 ohm, 5%, 1W, 2512	Vishay-Dale	CRCW25120000Z0EG	6	0

Table 6-1. Bill of Materials (continued)

Item	Designator	Description	Manufacturer	Part Number	QTY	Value
32	R16, R24, R31, R39	RES, 10 k, 5%, 0.125 W, 0805	Vishay-Dale	CRCW080510K0JNEA	4	10k
33	R25, R32	RES, 75, 5%, 1 W, 2512	Vishay-Dale	CRCW251275R0JNEG	2	75
34	R33	RES, 1.0 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00JNEA	1	1.0k
35	R36	RES, 7.5 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06037K50JNEA	1	7.5k
36	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G	6	1x2
37	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23	Test Point, Miniature, SMT	Keystone	5019	23	
38	U1	Sink / Source DDR Termination Regulator, HKR0016_Custom_A	Texas Instruments	TPS7H3301-SP	1	
39	U2	QUADRUPLE 2-INPUT POSITIVE-NAND GATES, D0014A	Texas Instruments	SN74AHCT00DR	1	
40	U3, U4	DUAL 4-A PEAK HIGH SPEED LOW- SIDE POWER MOSFET DRIVERS, D0008A	Texas Instruments	UCC27325D	2	
41	U5	Precision Timers, PW0008A	Texas Instruments	NE555PWR	1	
42	C6, C10, C11, C12, C13, C14, C23, C27, C29, C30, C52, C53	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X7R, 1210	AVX	1210ZC475KAT2A	0	4.7uF
43	C8, C9, C15, C16, C26	CAP, Tantalum Polymer, 150 µF, 10 V, +/- 20%, 0.005 ohm, 7343-31 SMD	Kemet	T530D157M010ATE005	0	150uF
44	C28, C49, C50, C51	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	Kemet	C0603C104K4RACTU	0	0.1uF
45	C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66	CAP, CERM, 10 µF, 10 V, +/- 10%, X8L, 1210	Kemet	C1210C106K8NACTU	0	10uF
46	C70	CAP, CERM, 47 pF, 50 V, +/- 5%, C0G/NP0, 0805	AVX	08055A470JAT2A	0	47pF
47	R4	RES, 0 ohm, 5%, 1W, 2512	Vishay-Dale	CRCW25120000Z0EG	0	0
48	R8	RES, 0 ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW08050000Z0EA	0	0
49	U1A	Socket, TSOP-16, 1.27 mm Pitch	Aries Electronics	A4293-114-24HT	0	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2016) to Revision B (October 2020)	Page
• Added additional description	3
• Added Related Information documenation	3
• Updated DDR features and default current ranges	3
• Updated VTT/V_O termination current	4
• Updated VTT/V_O termination tolerance	4
• Updated power supply minimum requirements	5
• Updated function descriptions in Connector and Test Points table	5
• Updated output current range description for VTTREF and VTT/V_O	5
• Updated testing proceedure	8
• Updated Bode measurement details and plots	8
• Added board layout section	14

Changes from Revision * (December 2015) to Revision A (October 2016)	Page
• Changed EVM Schematic: (1) C31 from 0.1 µF to 2.2 µF (2) DNP format change	18
• Changed EVM Transient board: DNP format change	18
• Changed Bill of Materials: C31 from 0.1 µF to 2.2 µF	20

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