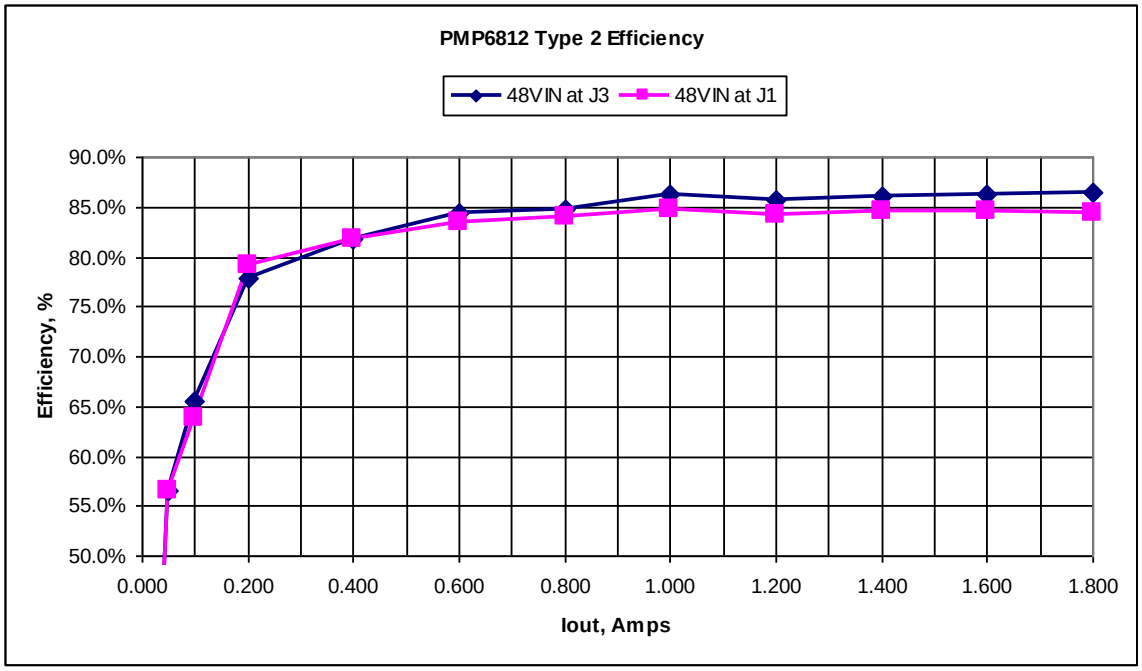
PMP6812 (Type 2) – 12V/1.8A/25W

Efficiency

The efficiency of the converter is shown below:

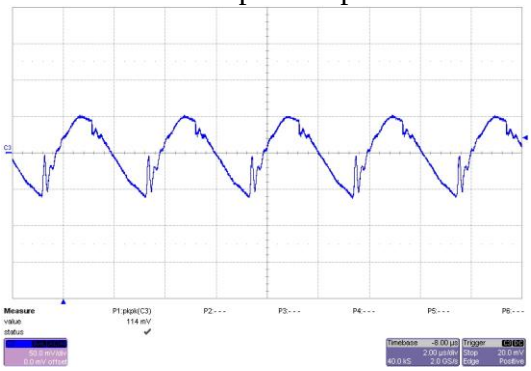
Iout	Vout	J3 Iin	J3 Vin	J3 Eff	J1 Iin	J1 Vin	J1 Eff
0.000	11.96	0.009	48.0	0.0%	0.009	48.0	0.0%
0.050	11.96	0.022	48.0	56.6%	0.022	48.0	56.6%
0.100	11.96	0.038	48.0	65.6%	0.039	48.0	63.9%
0.200	11.96	0.064	48.0	77.9%	0.063	48.0	79.1%
0.400	11.96	0.122	48.0	81.7%	0.122	48.0	81.7%
0.600	11.96	0.177	48.0	84.5%	0.179	48.0	83.5%
0.800	11.96	0.235	48.0	84.8%	0.237	48.0	84.1%
1.000	11.96	0.289	48.0	86.2%	0.294	48.0	84.8%
1.200	11.96	0.349	48.0	85.7%	0.355	48.0	84.2%
1.400	11.96	0.405	48.0	86.1%	0.412	48.0	84.7%
1.600	11.96	0.462	48.0	86.3%	0.471	48.0	84.6%
1.800	11.96	0.519	48.0	86.4%	0.531	48.0	84.5%



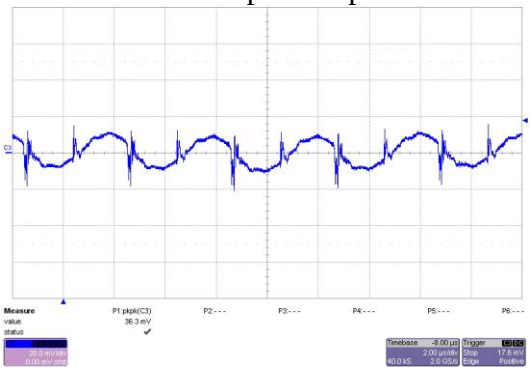
Ripple and Noise

Ripple measurements taken with a 48VIN at J1, 900mA load, and 20MHz BWL.

12V Ripple (C21), 50mV/div, 2us/div
Measured 114mV peak to peak:

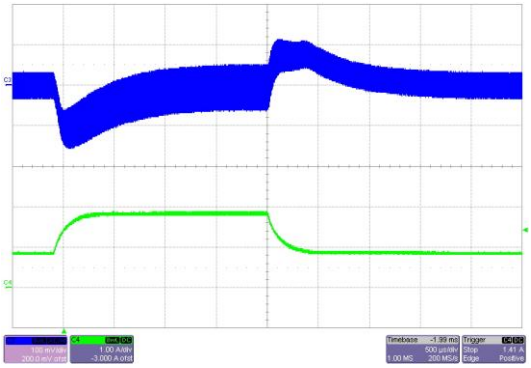


Input Ripple (C10), 20mV/div, 2us/div
Measured 36.3mV peak to peak:



Dynamic Loading

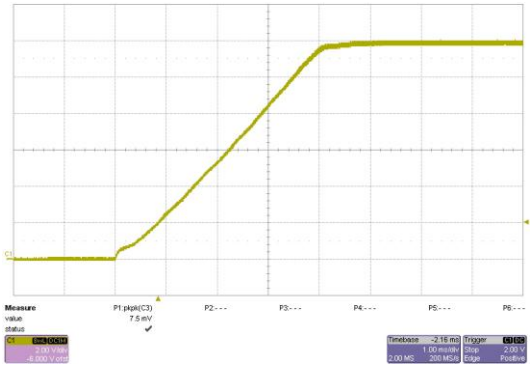
Load Step, 48VIN at J1 100mV/div, 1A/div, 500usec/div
900mA to 1.8A load step
Measured -156mV undershoot and +113mV overshoot:

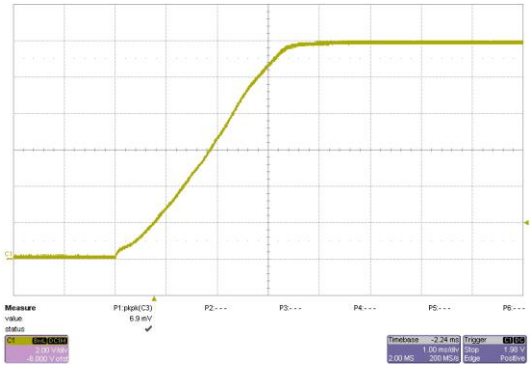


Turn On Response

48VIN, 1.8A Load, 2V/div, 1msec/div:

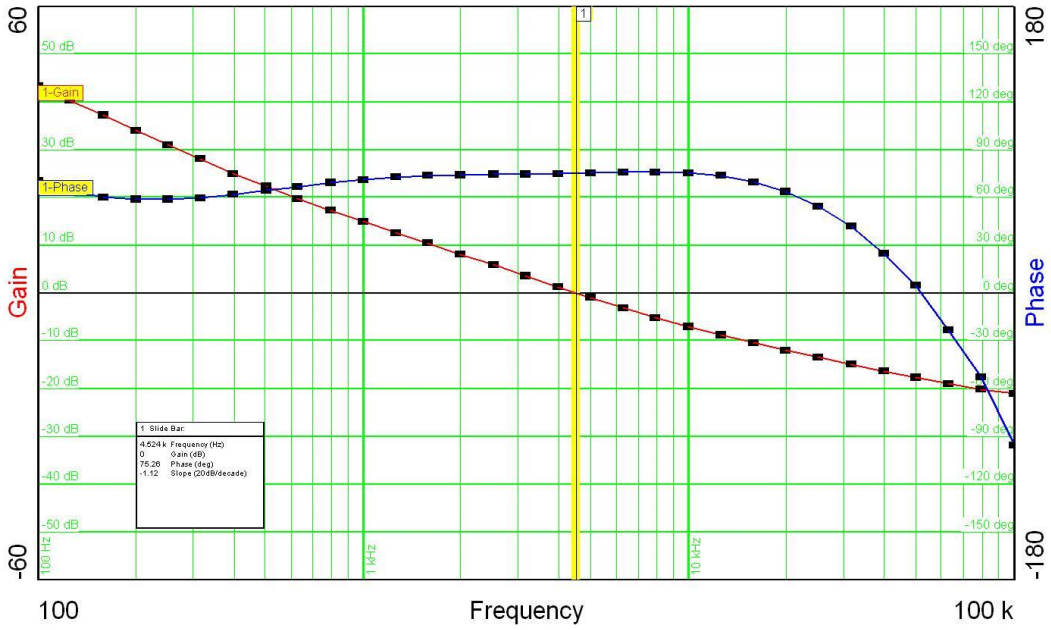
48VIN, 0A Load, 2V/div, 1msec.div:



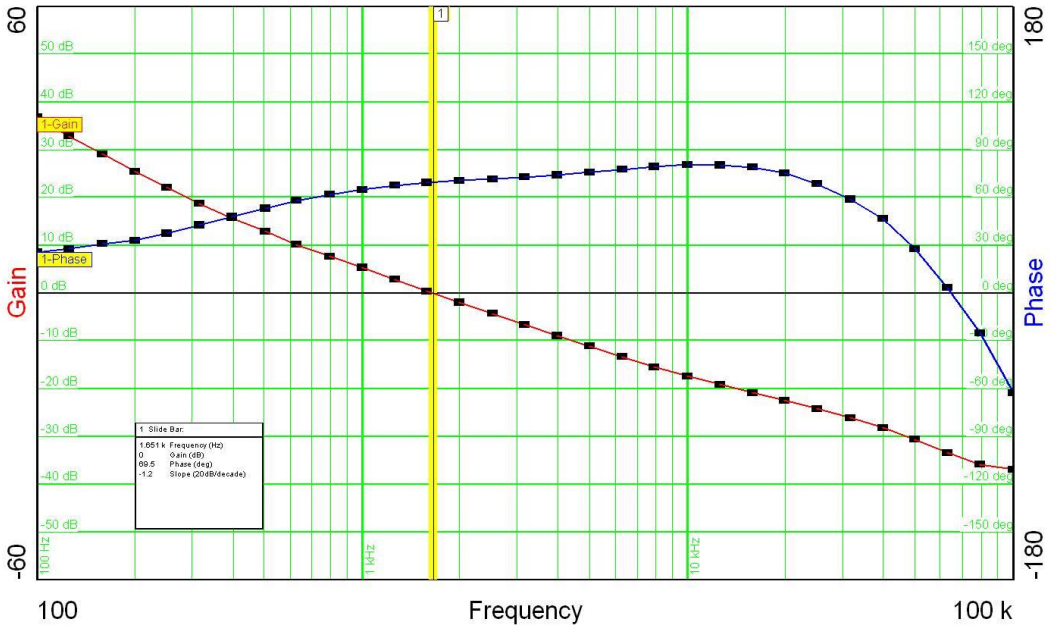


Stability (Loop Gain)

The figure below is the loop gain of the converter with a 48V input and 1.8A load. The bandwidth is 4.5 KHz, the phase margin is 75 degrees, and the gain margin is 18 dB.



The figure below is the loop gain of the converter with a 48V input and 180mA load. The bandwidth is 1.6 KHz, the phase margin is 69 degrees, and the gain margin is 34 dB.



Thermal Analysis:

48V input and 1.8A load:

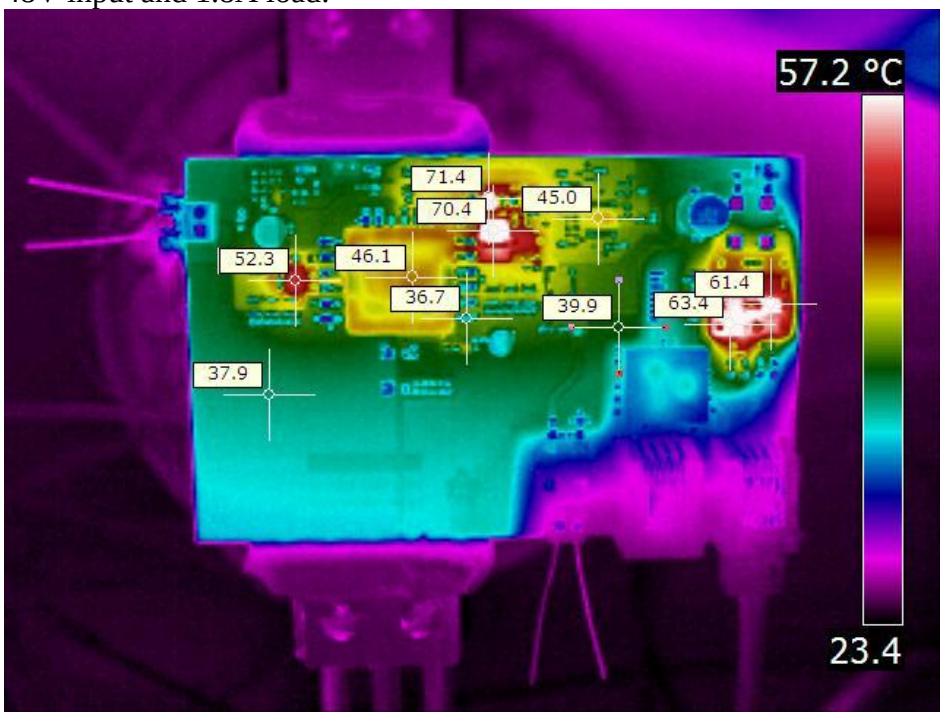
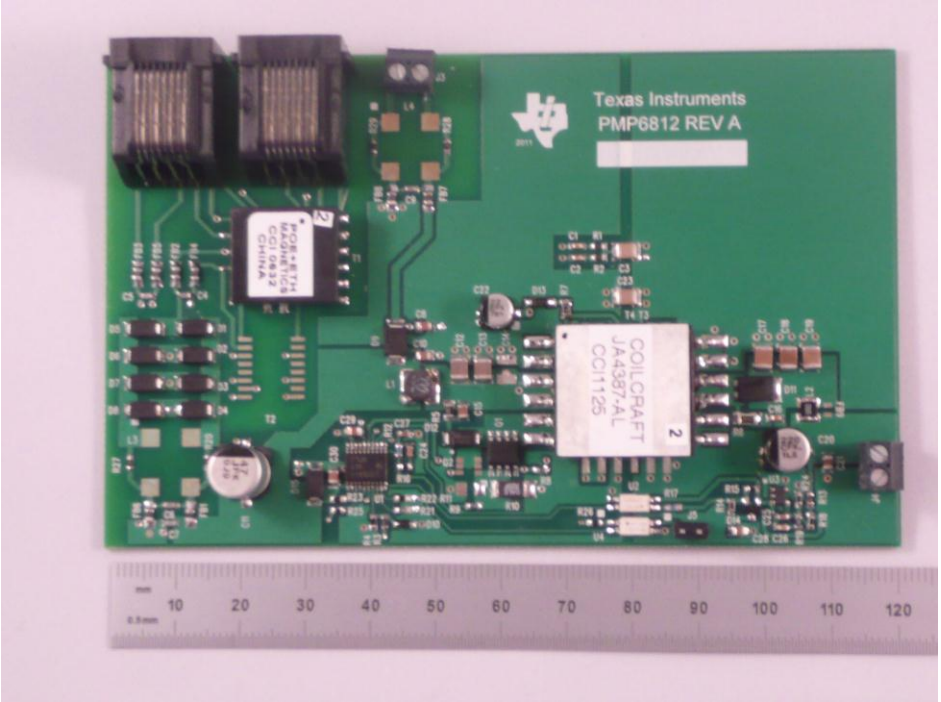


Photo:



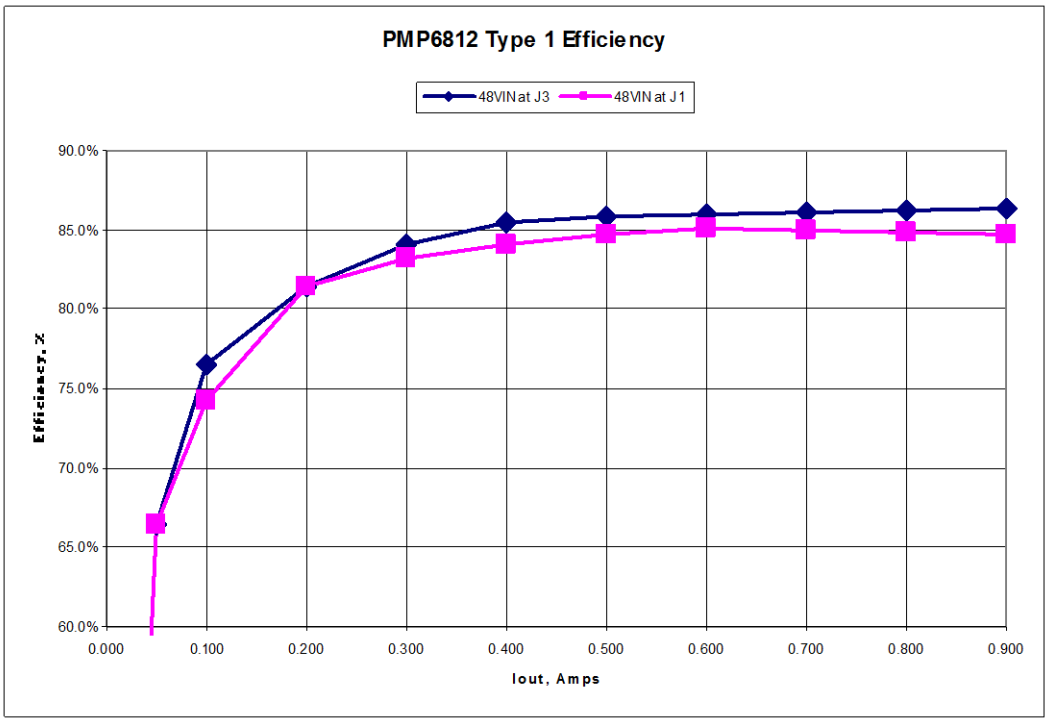
Note: Board Photos are of the PMP6812.2 Rev A board.

PMP6812 (Type 1) – 12V/0.9A/13W

Efficiency

The efficiency of the converter is shown below:

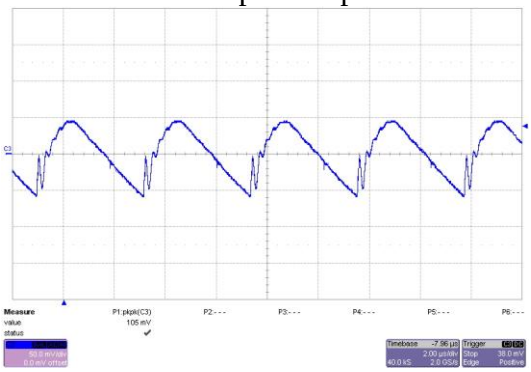
Iout	Vout	J3 Iin	J3 Vin	J3 Eff	J1 Iin	J1 Vin	J1 Eff
0.000	12.11	0.005	48.0	0.0%	0.005	48.0	0.0%
0.050	12.11	0.019	48.0	66.4%	0.019	48.0	66.4%
0.100	12.11	0.033	48.0	76.5%	0.034	48.0	74.2%
0.200	12.11	0.062	48.0	81.4%	0.062	48.0	81.4%
0.300	12.11	0.090	48.0	84.1%	0.091	48.0	83.2%
0.400	12.11	0.118	48.0	85.5%	0.120	48.0	84.1%
0.500	12.11	0.147	48.0	85.8%	0.149	48.0	84.7%
0.600	12.11	0.176	48.0	86.0%	0.178	48.0	85.0%
0.700	12.11	0.205	48.0	86.1%	0.208	48.0	84.9%
0.800	12.11	0.234	48.0	86.3%	0.238	48.0	84.8%
0.900	12.11	0.263	48.0	86.3%	0.268	48.0	84.7%



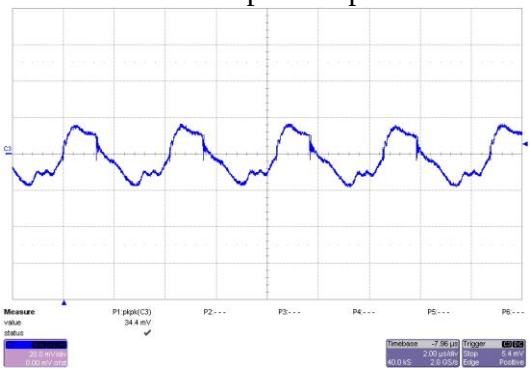
Ripple and Noise

Ripple measurements taken with a 48VIN at J1, 900mA load, and 20MHz BWL.

12V Ripple (C21), 50mV/div, 2us/div
Measured 105mV peak to peak:

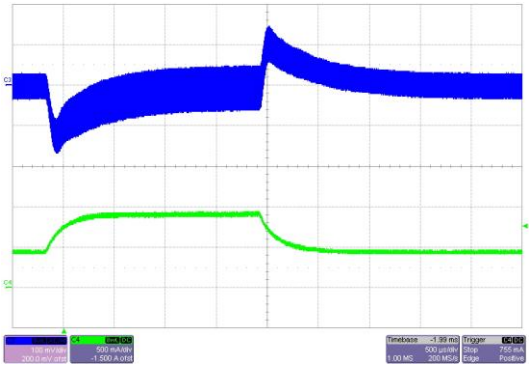


Input Ripple (C10), 20mV/div, 2us/div
Measured 34.4mV peak to peak:



Dynamic Loading

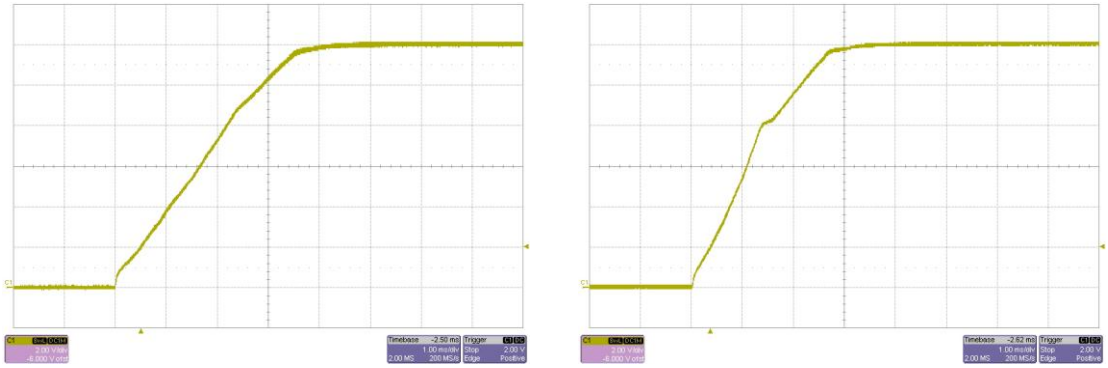
Load Step, 48VIN at J1 100mV/div, 500mA/div, 500usec/div
450mA to 900mA load step
Measured -167mV undershoot and +146mV overshoot:



Turn On Response

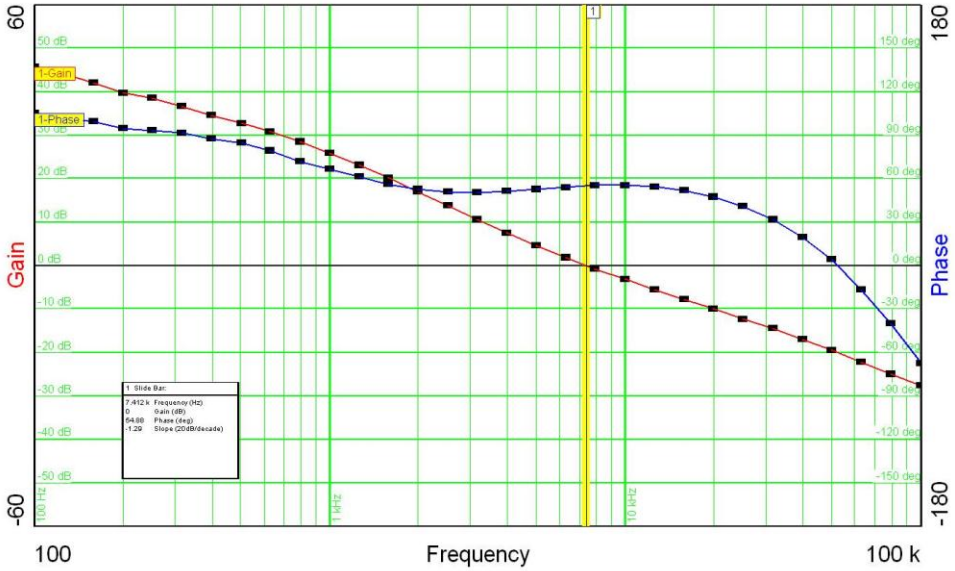
48VIN, 900mA Load, 2V/div, 1msec/div:

48VIN, 0A Load, 2V/div, 1msec.div:

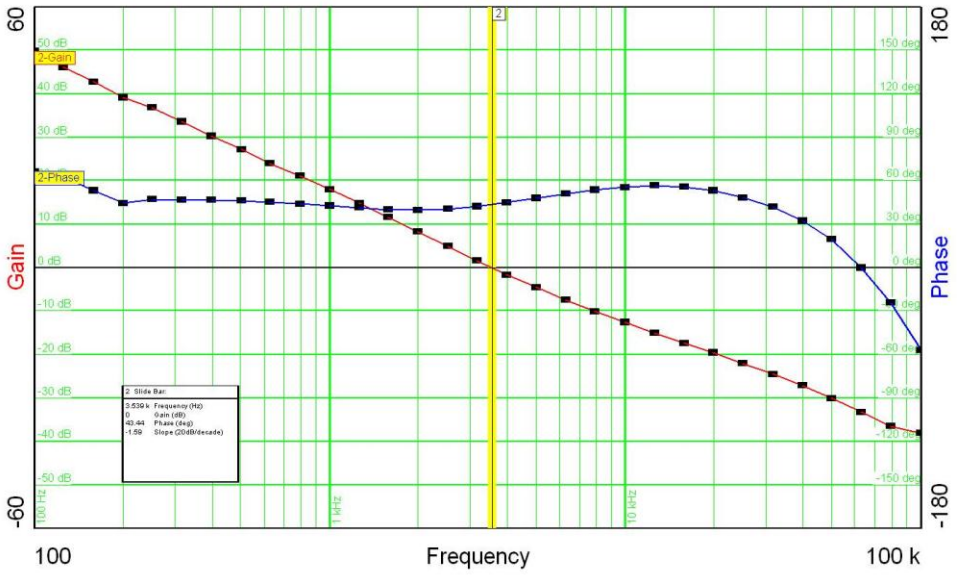


Stability (Loop Gain)

The figure below is the loop gain of the converter with a 48V input and 900mA load. The bandwidth is 7.4 KHz, the phase margin is 55 degrees, and the gain margin is 20 dB.



The figure below is the loop gain of the converter with a 48V input and 90mA load. The bandwidth is 3.5 KHz, the phase margin is 43 degrees, and the gain margin is 33 dB.



Thermal Analysis:

48V input and 900mA load:

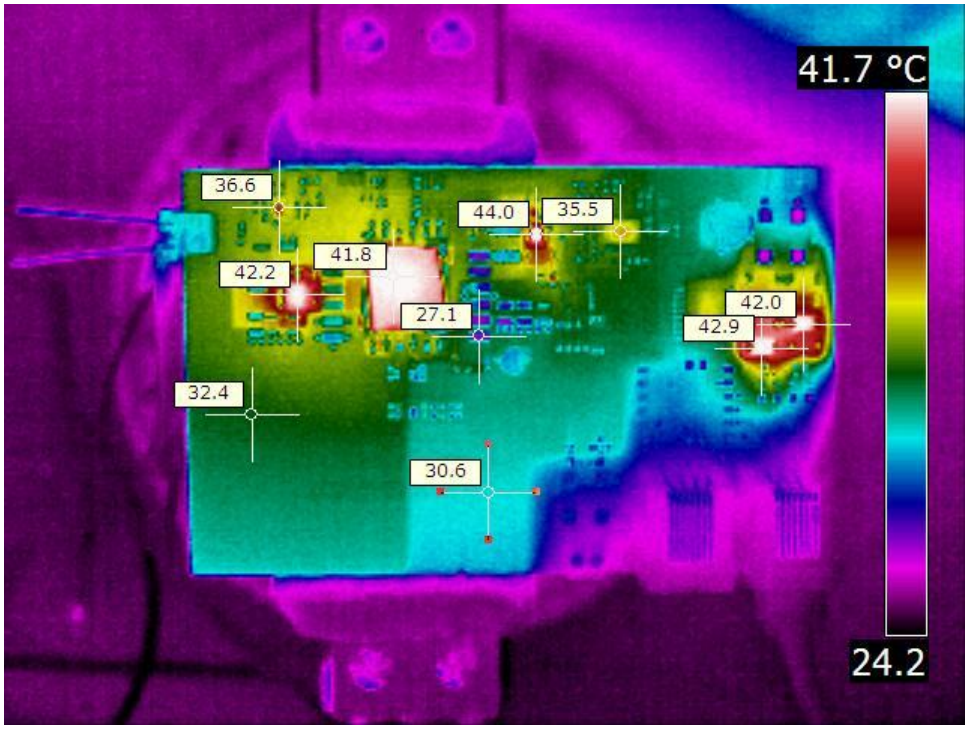
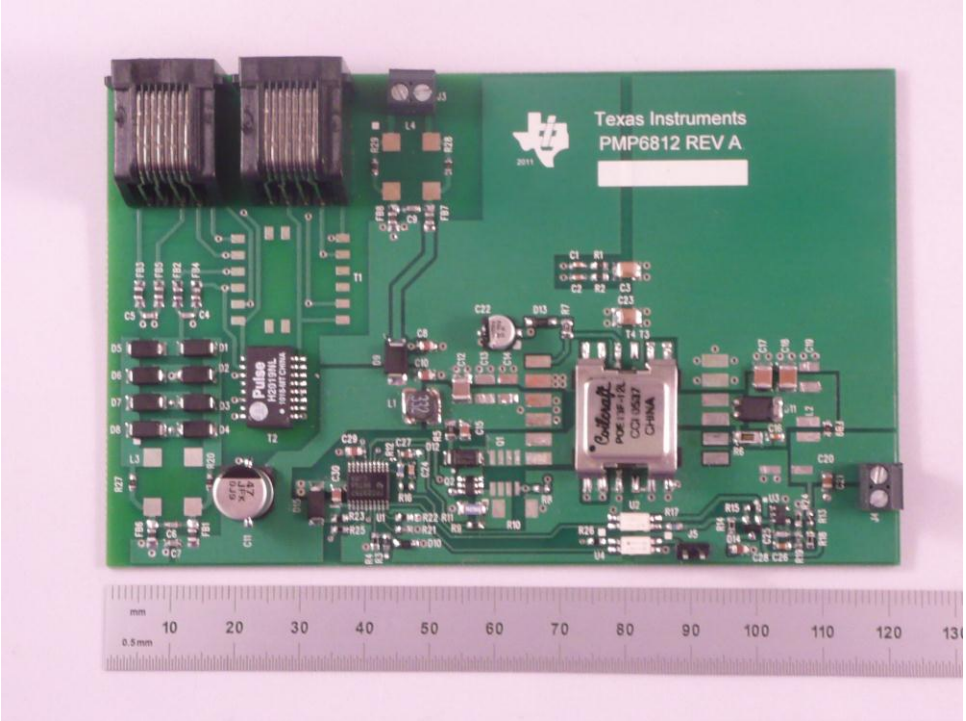


Photo:



Note: Board Photos are of the PMP6812.1 Rev A board.

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