TPS75003EVM User's Guide

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1 Introduction

The Texas Instruments TPS75003EVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS75003 multi-channel power IC. This device has two buck controllers and a low dropout linear regulator. The device will operate at input voltages between 2.2 V and 6.5 V. The buck controllers can provide output voltages between 1.22 V and the input voltage and output currents up to 3 A. This EVM is specifically designed and optimized to operate from a 5 V input with output currents up to 2 A for V_{OUT1} = 1.2 V typical and V_{OUT2} = 3.3 V typical. In addition, the EVM is jumper configurable so that each output can be independently enabled or the outputs can be sequenced in the following order: V_{OUT3}, V_{OUT2} then V_{OUT1}.

2 Performance Specification Summary

Table 1 provides a summary of the TPS75003EVM performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Typical Performance Specification Summary

		CONDITION	VOLTAGE RANGE (V)			CURRENT RANGE (mA)		
			MIN	TYP	MAX	MIN	TYP	MAX
V_{OUT1}	Buck Controller	V_I = 5 V	1.18	1.22	1.26	0		2000
V_{OUT2}	Buck Controller	V_I = 5 V	3.15	3.30	3.43	0		2000
V_{OUT3}	Linear Regulator	V_I = 5 V	2.41	2.50	2.65	0		300

3 Modifications

Passive components with 603 or larger footprints were used to allow for user customization. Additionally, a second soft start capacitor was added for buck controller but not populated to allow the soft start timing to be easily modified.

Input capacitor C1 was included to minimize inductive droop due to long leads from a bench power supply. A capacitor of similar size may or may not be needed in a real application depending on the proximity to the input power supply.

If all of the output voltages are equal to or greater than the minimum 1.4V threshold for EN1 and EN2, then the outputs can be sequenced in any order by simply modifying the V_{OUTx} to ENx connections. If one of the buck output voltages is between 1.2V and 1.4V, then only EN3 with its minimum 1.1V threshold can be enabled by this output voltage. For example, if V_{OUT1} = 1.2V, V_{OUT2} = 3.3V and V_{OUT3} = 2.5V, the following additional sequencing options are available by modifying the EVM's V_{OUTx} to ENx connections: V_{OUT1} = 1.2V, V_{OUT3} = 2.5V then V_{OUT2} = 3.3V or V_{OUT2} = 3.3V, V_{OUT3} = 2.5V then V_{OUT1} = 1.2V. An external SVS, like the TPS3808, monitoring the 1.2V to 1.4V rail and with its RESET output tied to ENx can be used to provide the remaining sequencing options.

3.1 Input/Output Connector Descriptions

This chapter describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS75003EVM.

J1 – **VIN**— This is the positive connection to the input power supply. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission.

J2 – **GND**— This is the return connection for the input power supply.

J3 – **VOUT1**— This is the positive connection for the V_{OUT1} output. Connect this pin to the positive input of the V_{OUT1} load.

J4 – **GND**— This is the negative connection for the V_{OUT1} output. Connect this pin to the negative input of the V_{OUT1} load.

J5 – **VOUT2**— This is the positive connection for the V_{OUT2} output. Connect this pin to the positive input of the V_{OUT2} load.

J6 – **GND**— This is the negative connection for the V_{OUT2} output. Connect this pin to the negative input of the V_{OUT2} load.

J7 – **VOUT3**— This is the positive connection for the V_{OUT3} output. Connect this pin to the positive input of the V_{OUT3} load.

J8 – **GND**— This is the negative connection for the V_{OUT3} output. Connect this pin to the negative input of the V_{OUT3} load.

JP1 – **EN VO1**— This jumper enables and disables V_{OUT1}. With the jumper removed (DEFAULT), EN1 is pulled low by an external pulldown resistor and V_{OUT1} is disabled. With the jumper tied to V_{IN}, EN1 is pulled high to V_{IN} and V_{OUT1} is enabled. With the jumper tied to AFTER VO2, EN1 is tied to V_{OUT2} so that V_{OUT1} will not be enabled until after V_{OUT2} is enabled.

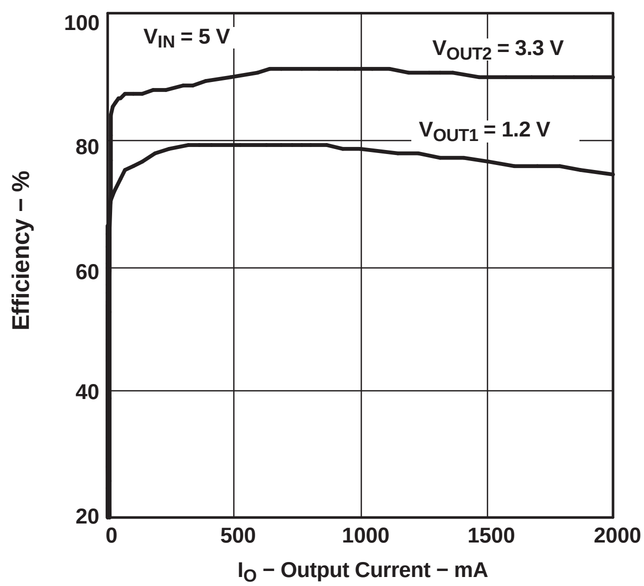
JP2 – **EN VO2**— This jumper enables and disables V_{OUT2}. With the jumper removed (DEFAULT), EN2 is pulled low by an external pulldown resistor and V_{OUT2} is disabled. With the jumper installed, EN2 is pulled high to V_{IN} and V_{OUT2} is enabled. With the jumper tied to AFTER VO3, EN3 is tied to V_{OUT3} so that V_{OUT2} will not be enabled until after V_{OUT3} is enabled.

JP3 – **EN VO3** — This jumper enables and disables V_{OUT3}. With the jumper removed (DEFAULT), EN3 is pulled low by an external pulldown resistor and V_{OUT3} is disabled. With the jumper tied to V_{IN}, EN3 is pulled high to V_{IN} and V_{OUT3} is enabled.

3.2 Setup

Connect an input supply between J1 and J2. The voltage range on this supply should stay between 2.2 V and 6.5 V. Connect a load not to exceed 2 A for the buck controllers between J3 and J4 for V_{OUT1} and between J5 and J6 for V_{OUT2}. Connect a load not to exceed 300 mA for the linear regulator between J7 and J8. Configure the JP1, JP2 and JP3 enabling jumpers to the desired setting. To prevent noise pickup from distorting voltage measurements of any of the three output voltages, keep the loop created by the voltage probe tip and its ground connection as small as possible and as far away as possible from the inductors on the board.

3.3 Test Results



A Efficiency may be improved or degraded by using different FETs and/or inductors.

Figure 1. Efficiency With V_{IN} = 5 V, V_{OUT1} = 1.2 V, V_{OUT2} = 3.3 V

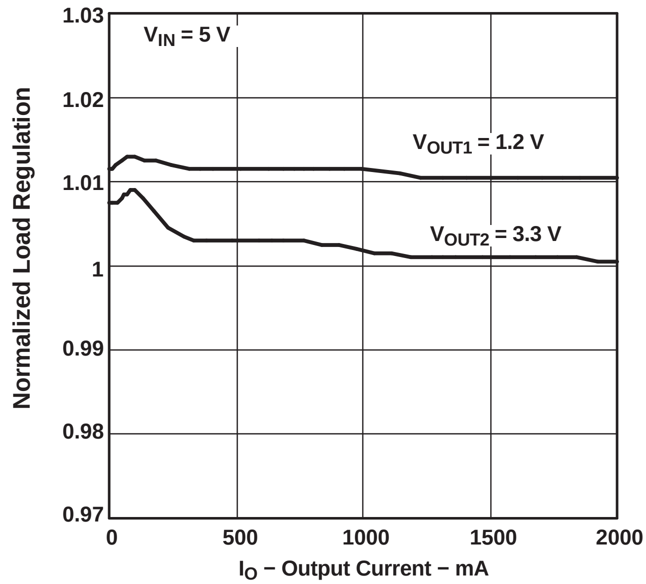


Figure 2. Normalized Load Regulation With V_{IN} = 5 V, V_{OUT1} = 1.2 V, V_{OUT2} = 3.3 V

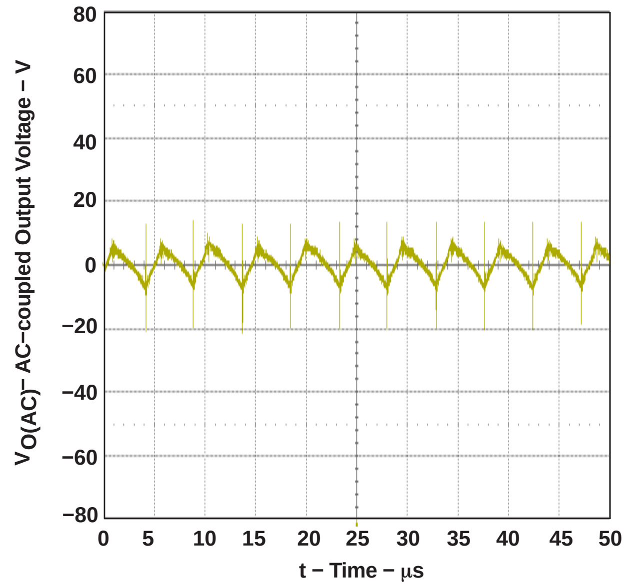


Figure 3. Output Ripple when V_{IN} = 5 V, V_{OUT1} = 1.2 V, I_{OUT1} = 2 A

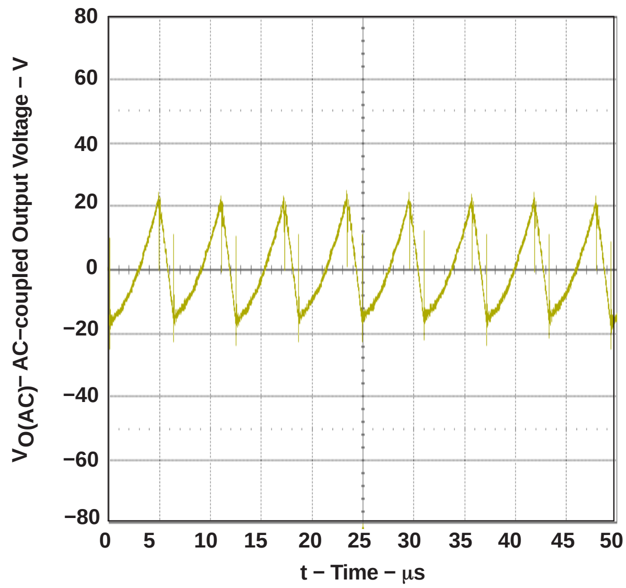


Figure 4. Output Ripple When V_{IN} = 5 V, V_{OUT2} = 3.3 V, I_{OUT2} = 2 A

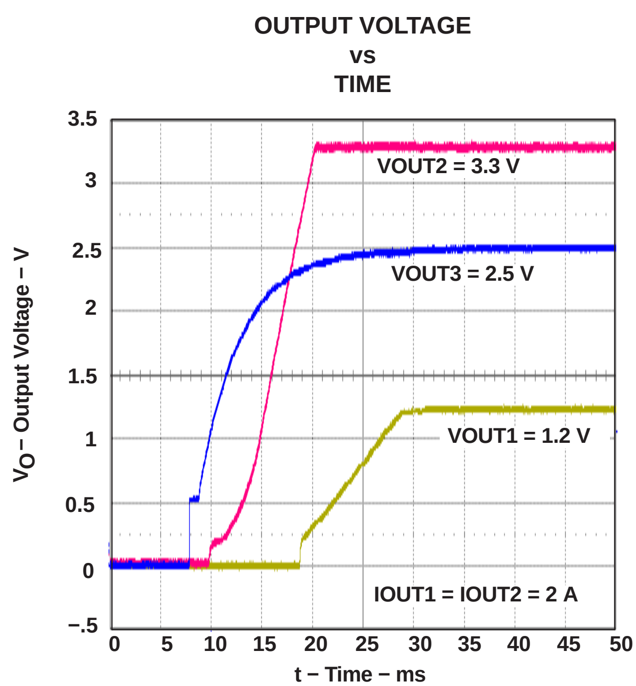


Figure 5. Soft Start With V_{IN} = 5.0 V

4 Board Layout

Board layout is critical for all switch mode power supplies. The following figures show each of the four layers of the TPS75003EVM PWB. The nodes with high switching frequencies and currents are short and are isolated from the noise sensitive feedback circuitry. Careful attention has been given to the routing of high frequency current loops. The sense resistors for the current limit and soft start should be placed between the INx and ISx pins as close to the IC as possible. Refer to the TPS75003 data sheet (literature number SBVS052) for additional layout guidelines.

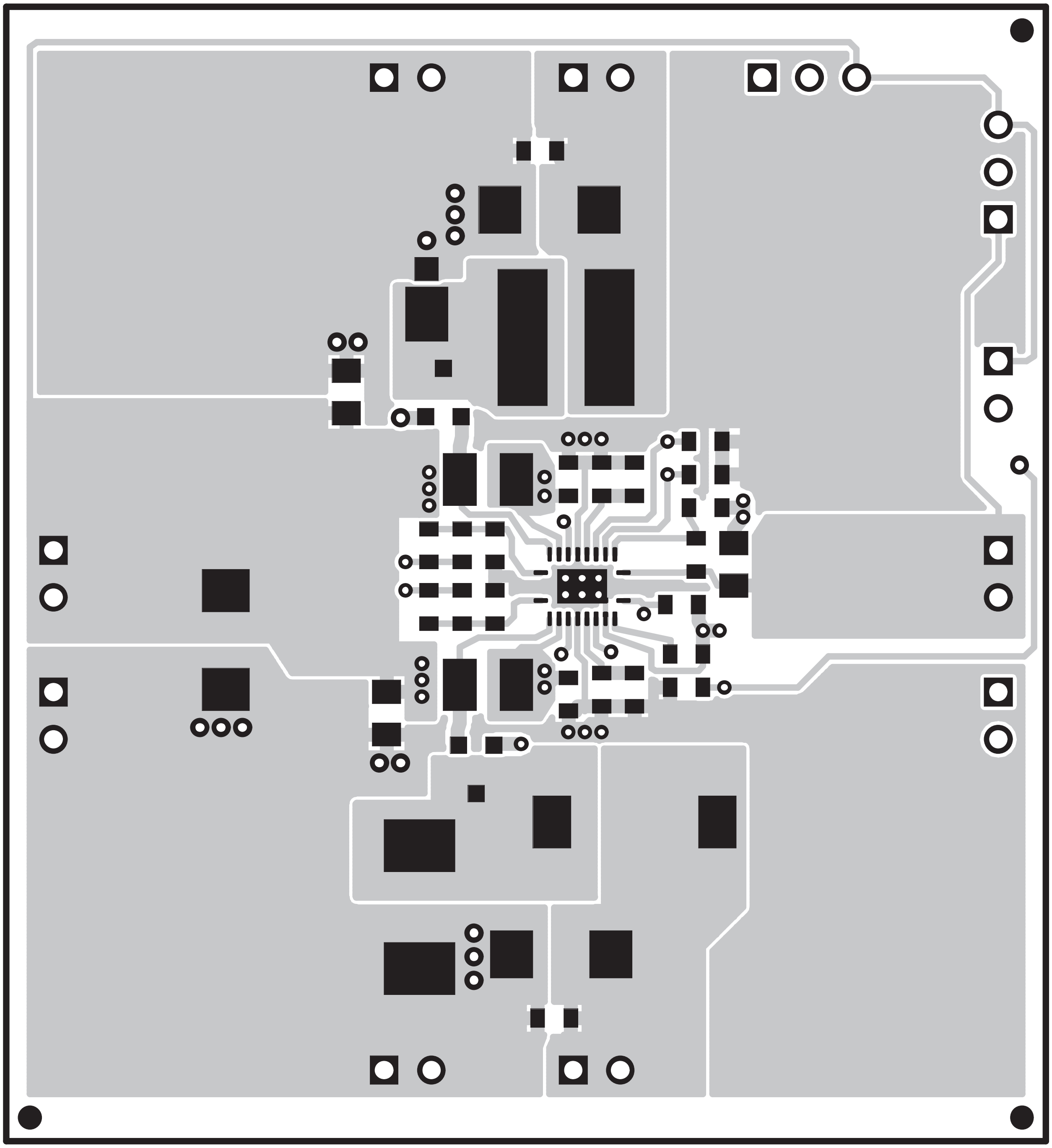


Figure 6. Top Layer

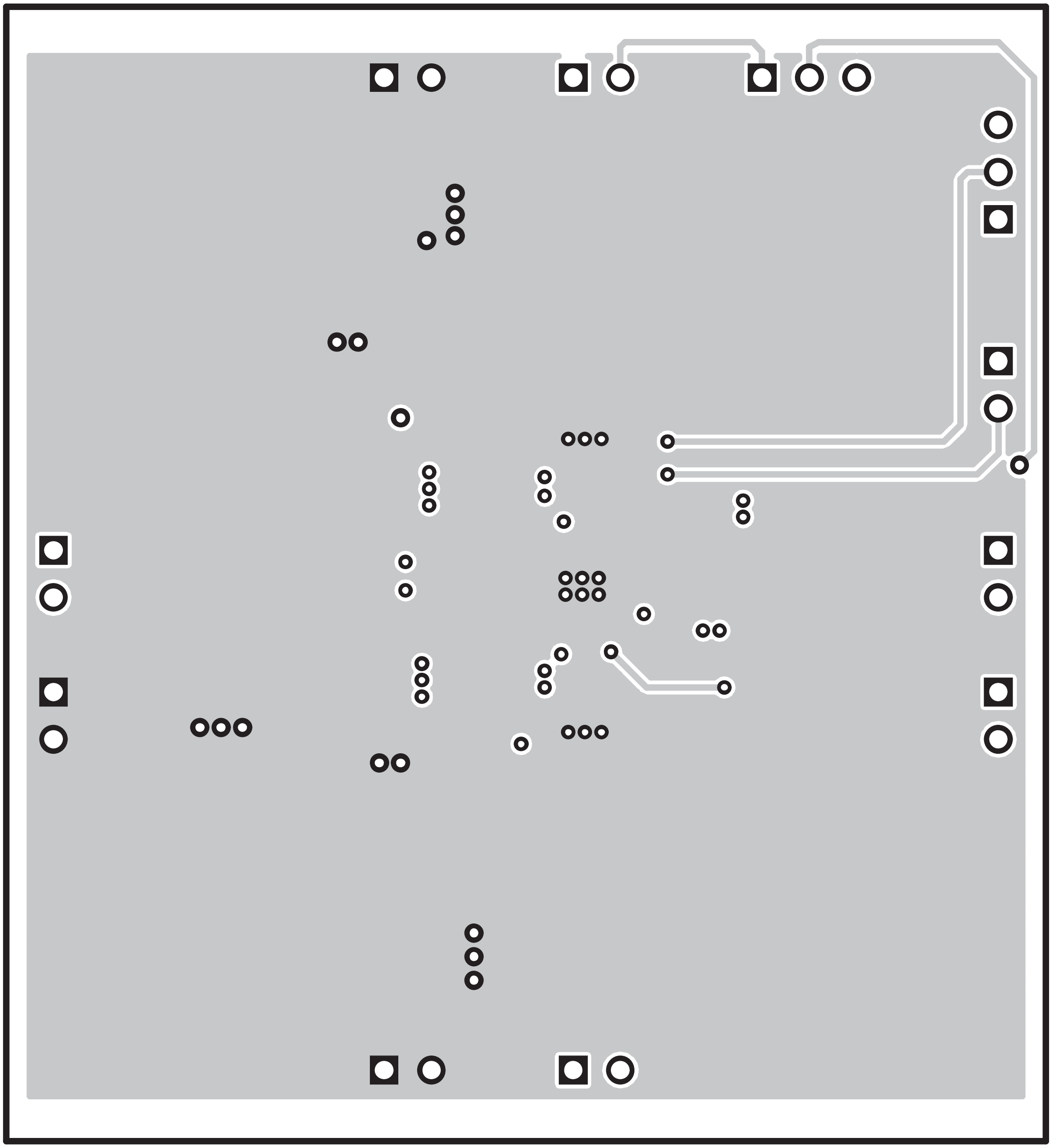


Figure 7. Bottom Layer

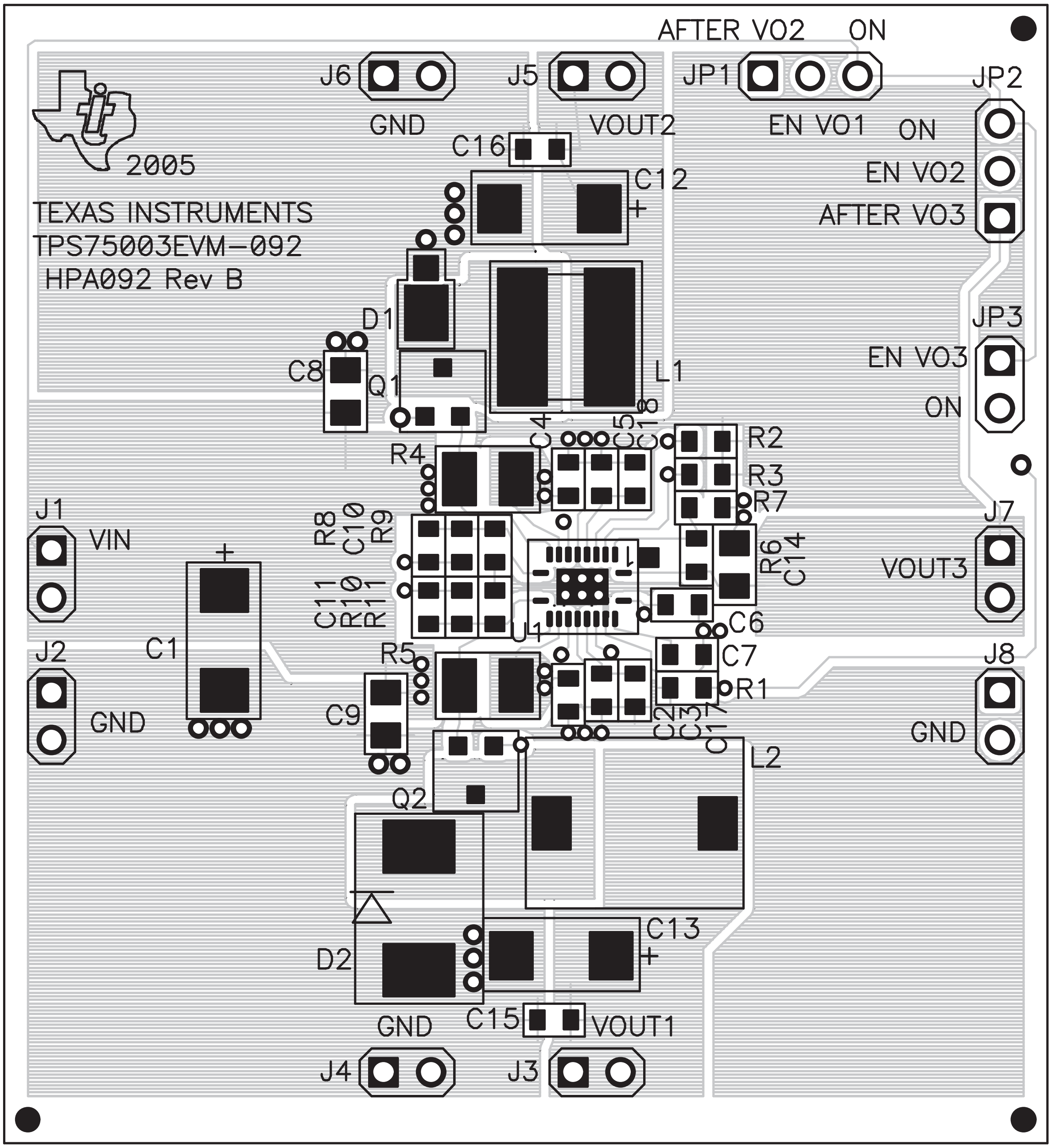


Figure 8. Top Assembly

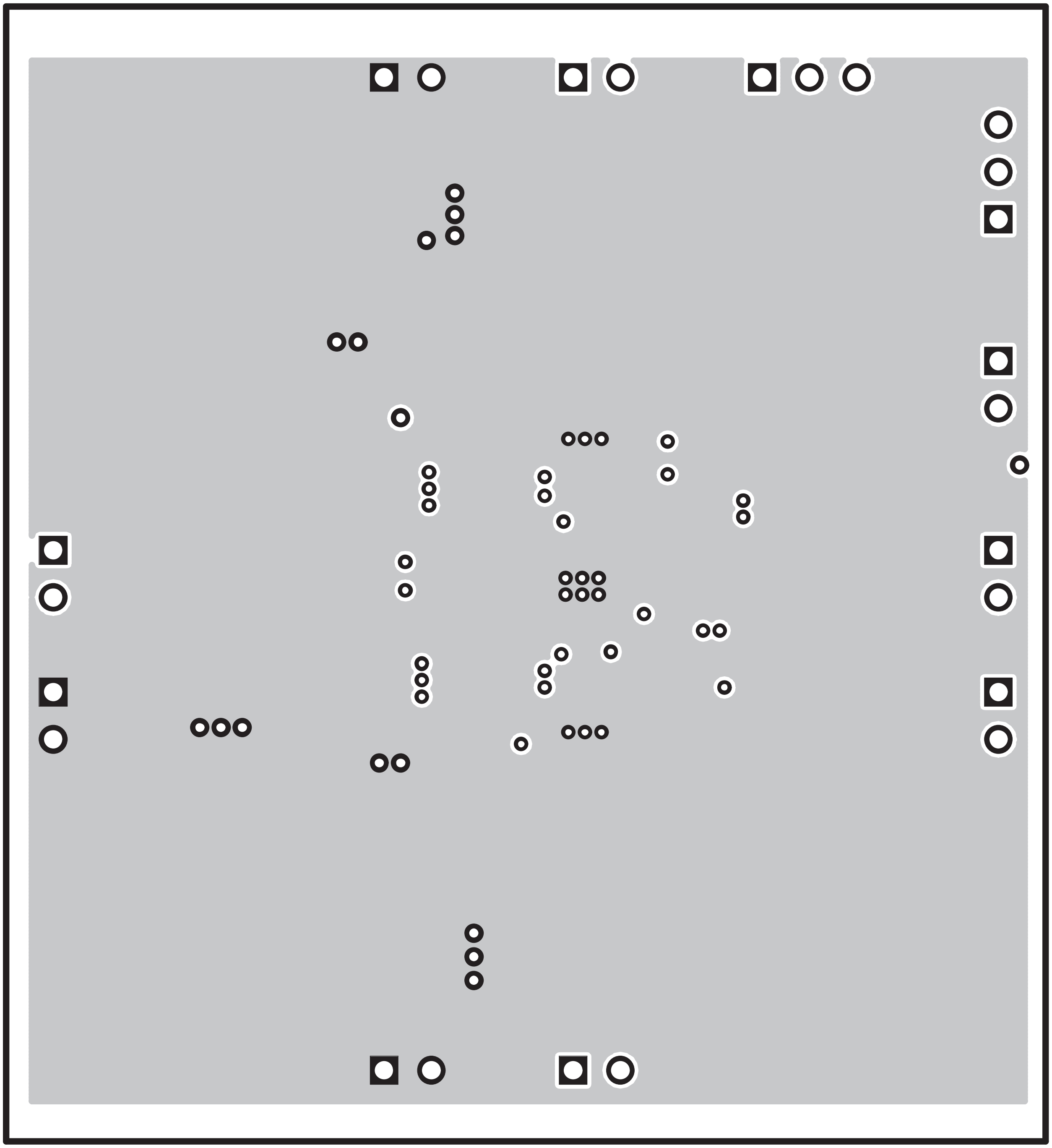


Figure 9. Layer 2

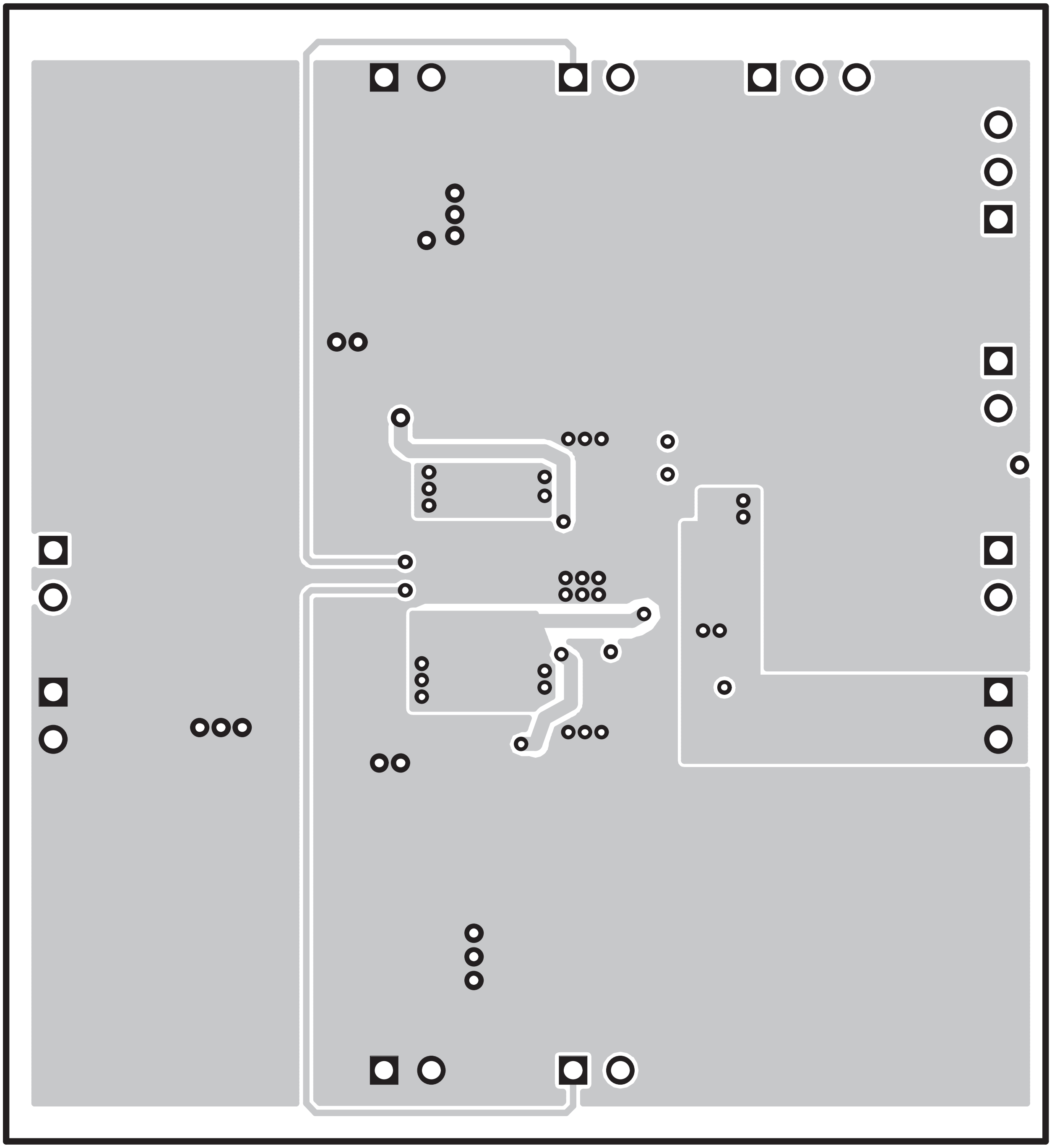


Figure 10. Layer 3

5 Schematic

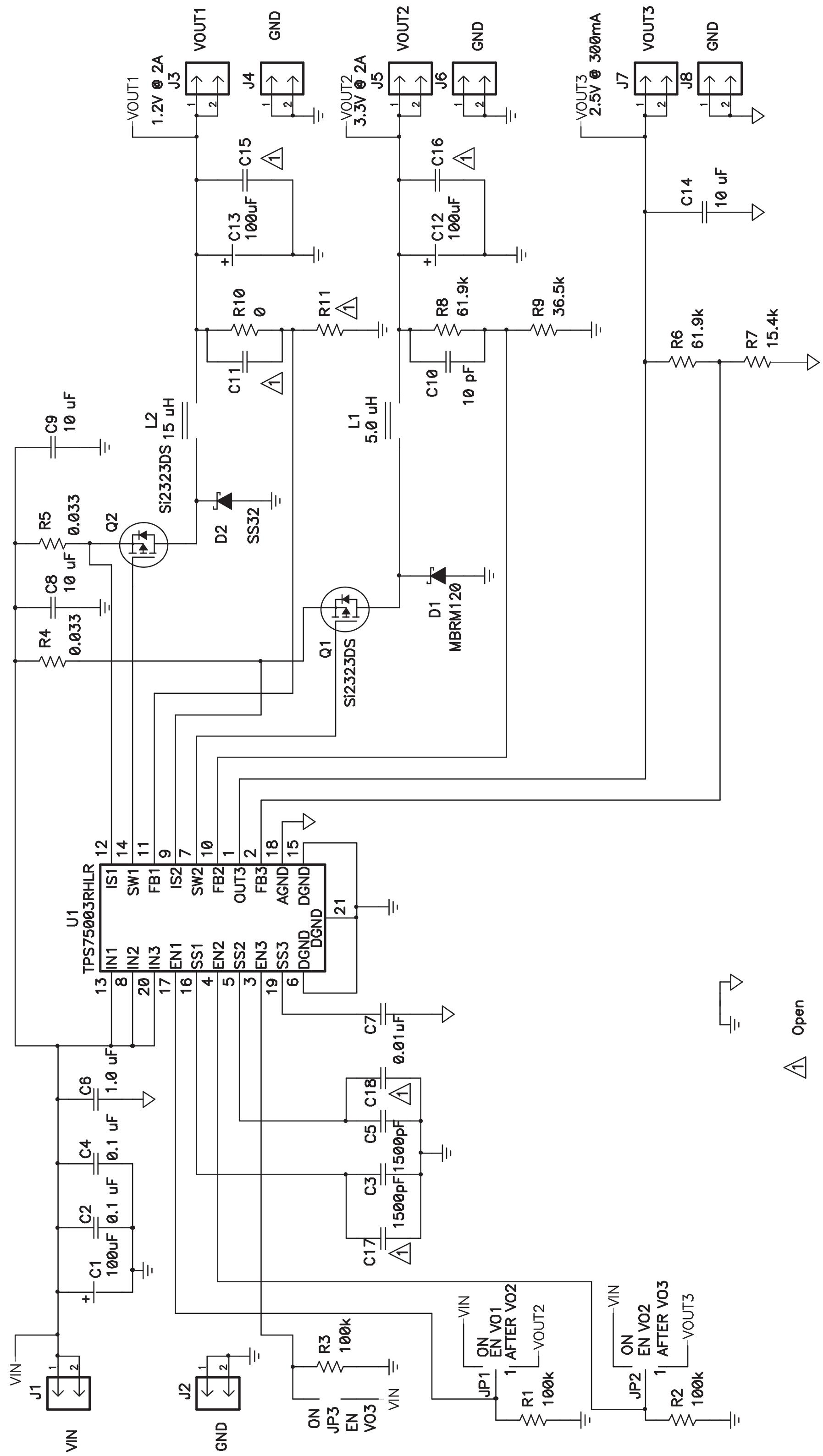


Figure 11. TPS75003EVM Schematic

6 Bill of Materials

Table 2. TPS75003EVM Bill of Materials

COUNT	Ref Des	DESCRIPTION	SIZE	MFR	PART NUMBER
3	C1, C12, C13	Capacitor, POSCAP, 100-μF, 6.3-V, 45-mΩ, 20%	6032 (C)	Sanyo	6TPB100MC
1	C10	Capacitor, Ceramic, 10-pF, 50-V, C0G, 5%	603	TDK	C1608C0G1H100D
0	C11, C15–C18	Capacitor, Ceramic, xx-μF, xx-V	603		
2	C2, C4	Capacitor, Ceramic, 0.1-μF, 16-V, X7R, 10%	603	TDK	C1608X7R1C104K
2	C3, C5	Capacitor, Ceramic, 1500-pF, 50-V, X7R, 10%	603	TDK	C1608X7R1H152K
1	C6	Capacitor, Ceramic, 1.0-μF, 6.3-V, X5R, 10%	603	TDK	C1608X5R0J105K
1	C7	Capacitor, Ceramic, 0.01-μF, 50-V, X7R, 10%	603	TDK	C1608X7R1H103K
3	C8, C9, C14	Capacitor, Ceramic, 10-μF, 10-V, X5R, 20%	805	TDK	C2012X5R1A106MT
1	D1	Diode, Schottky, 1A, 20 V	457-04	On Semi	MBRM120
1	D2	Diode, Schottky, 3.0-A, 20 V	SMC	Vishay	SS32
8	J1–J8	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.100 × 2	Sullins	PTC36SAAN
1	JP2	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.100 × 2	Sullins	PTC36SAAN
2	JP1, JP3	Header, 3-pin, 100 mil spacing, (36-pin strip)	0.100 × 3	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 5.0-μH, 2.9-A, 24-mΩ	0.264 sq	Sumida	CDRH6D38-5R0
1	L2	Inductor, SMT, 15-μH, 2.6-A, 53-mΩ	0.327 × 0.327	Sumida	CDRH8D43-150
2	Q1, Q2	MOSFET, P-ch, 20-V, 4.7-A, 39-mΩ	SOT23	Vishay	Si2323DS
3	R1–R3	Resistor, chip, 100 kΩ, 1/16 W, 1%	603	Std	Std
1	R10	Resistor, chip, 0-Ω, 1/16 W, 5%	603	Std	Std
0	R11	Resistor, chip, xx-Ω, 1/16 W, 1%	603		
2	R4, R5	Resistor, chip, 0.033-Ω,1/4 W, 1%	1210	Std	Std
2	R6, R8	Resistor, chip, 61.9 kΩ, 1/16 W, 1%	603	Std	Std
1	R7	Resistor, chip, 15.4 kΩ, 1/16 W, 1%	603	Std	Std
1	R9	Resistor, chip, 36.5 kΩ, 1/16 W, 1%	603	Std	Std
1	U1	IC, Triple Channel DC/DC Converter	QFN-20	TI	TPS75003RHLR
1	—	PCB, 2.4 In × 2.2 In × 0.062 In		Any	HPA092
3	—	Shunt, 100-mil, black	0.100	3M	929950-00

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.2 V to 6.5 V and the output voltage range of 1 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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