Application Note

Power Supply Design for Semidrive X9SP (X9HP Compatible) Using LP8752-Q1 and LP8756-Q1

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ABSTRACT

This document details the design considerations of a power design for the Semidrive X9SP automotive SoC (system-on-chip) power rails using the LP87521-Q1, LP87562-Q1, and LP87563-Q1 power management ICs (PMICs).

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Additional bucks TPS62811-Q1 and TPS628501-Q1 as well as LDOs TPS74501-Q1 and TLV76733-Q1 are used to power other discrete rails not covered by PMICs. This power design assumes an input voltage of 5V (±5%). If the system input voltage is higher, for example a car battery, a buck converter as a pre-regulator needs to be used to generate a supply voltage of 5V. LM25149-Q1 can be used as a pre-regulator when powered directly from car battery. An additional smart diode controller such as LM74700-Q1 can be used to control external MOSFETS and provide power path ON or OFF control and overvoltage protection.

The LP87562-Q1 has four buck converters configured to work as single 3-phase converter and a separate single phase converter. LP87563-Q1 has four buck converters configured to work as single 2-phase converter and two separate single phase converters. LP87563-Q1 has four buck converters configured to work as single 4-phase converter. These devices are OTP programmable, meaning default register values are set in TI production line to desired values and is also possible to control registers through I2C after power-up. Contact TI sales for samples with specific OTP settings.

TPS62811-Q1 is a discrete buck converter with up to 6V input voltage and output voltage ranging from 0.6V to 5.5V. TPS62811-Q1 has maximum output current of 1A and this product family has also other pin-to-pin compatible options ranging from 1A to 6A current capability. 1A buck converter TPS628501-Q1 also has the pin-to-pin compatible devices covering 1A to 3A output current range. This makes it easy to change the part to a different version depending on the use case requirements. This power design is an example how Semidrive X9SP required rails can be powered with TI PMICs. Sequencing is handled through programmable startup/ shutdown delays of the PMICs and GPIOs.

This power supply design is also compatible with Semidrive X9HP. Since the power rating of AP rails in X9HP and X9SP are similar, pin-to-pin devices can be used and replaced to lessen design effort in meeting the requirements. Details of the compatibility and options for implementation is discussed later in the document.

This power design is possible to customize and optimize based on the actual use case regarding current requirements, used peripherals, and so forth. I^2C control allows diagnostic and control of the PMICs.

For error handling and control this design also has PGOOD output, Interrupt output, and Reset output for the SoC.

2 Design Parameters

Table 2-1 shows the power rails, load requirements, and startup or shutdown sequencing requirements and Section 8 shows typical measurement data.

Table 2-1. Design Parameters

VOLTAGE (V)	RAIL NAME	MAX LOAD (mA)	SOURCE	STARTUP DELAY (trigger)	SHUTDOWN DELAY (trigger)
0.6	VDDQLP_DRAM	500	AP_TPS628501	0ms (EN_TPS628501 high)	0ms (EN_TPS628501 low)
0.8	VDDIO_RTC0V8	5	RTC_LDO2	0ms (EN_RTC_LDO2 high)	0ms (EN_RTC_LDO2 low)
0.85	VDD_SAF_0V85	1000	SAF_BUCK1	0ms (SAF_BUCK1 = SYS_PWR_ON high)	10ms (SAF_BUCK1 = SYS_PWR_ON low)
	VDD_AP_0V85	10000	LP87562_B0-B2	0ms (LP87562_EN1 = SYS_CTRL0 high)	3ms (LP87562_EN1 = SYS_CTRL0 low)
	VDD_MIPI_0V85 VDD_PCIE_0V85 VDD_USB VDDD_USB	450	LP87562_B0-B2	0ms (LP87562_EN1 = SYS_CTRL0 high)	3ms (LP87562_EN1 = SYS_CTRL0 low)
	VDD_DRAM_0V85	2000	LP87562_B3	0ms (LP87562_EN1 = SYS_CTRL0 high)	3ms (LP87562_EN1 = SYS_CTRL0 low)
	VDD_CPU_0V85	10000	LP87521_B0-B3	0ms (LP87521_EN1 = SYS_CTRL1 high)	3ms (LP87521_EN1 = SYS_CTRL1 low)
	VDD_GPU_0V85	8000	LP87563_B0-B1	2ms (LP87563_EN1 = SYS_CTRL1 high)	1ms (LP87521_EN1 = SYS_CTRL1 low)
1.1	VDDQ_DRAM_1V1	2000	LP87563_B2	1ms (LP87563_EN1 = SYS_CTRL1 high)	1ms (LP87521_EN1 = SYS_CTRL1 low)
1.8	VDD_RTC_1V8	300	RTC_LDO1	0ms (EN_RTC_LDO1 high)	0ms (EN_RTC_LDO1 low)
	VDD_SAF_1V8	<500	SAF_LDO1	0ms (EN_SAF_LDO1 high)	0ms (EN_SAF_LDO1 low)
	VDDA_1V8 VDDA_MIPI_1V8	1300	LP87563_B3	1ms (LP87563_EN1 = SYS_CTRL1 high)	2ms (LP87563_EN1 = SYS_CTRL1 low)
	VDD_LP4_1V8	200	AP_TPS745	0ms (EN_AP_TPS745 high)	0ms (EN_AP_TPS745 low)
3.3	VDD_SAF_3V3	<500	SAF_LDO2	0ms (EN_SAF_LDO2 high)	0ms (EN_SAF_LDO2 low)
	VDDH_3V3 VDDIO_3V3	750	AP_TLV767	0ms (EN_AP_TLV767 high)	0ms (EN_AP_TLV767 low)
Signal	RTC_RESET	-	PG_RTC_LDO2	-	-
	SAFETY_RESET	-	PG_SAF_LDO1	-	-
	AP_RESET	-	PG_AP_TPS628501	-	-

3 Power Design

Figure 3-1 and Figure 3-2 show the example power tree of LP87562-Q1, LP87563-Q1, LP87521-Q1 and other discrete buck converters and LDOs powering the X9SP power rails. LM25149-Q1 is used as a pre-regulator to generate 5V input voltage for the PMICs and discrete buck converters and LDOs. LP87562-Q1, LP87563-Q1, LP87521-Q have the output voltages, sequencing etc. pre-programmed to the OTP memory. Please contact TI sales for details on the OTP settings.

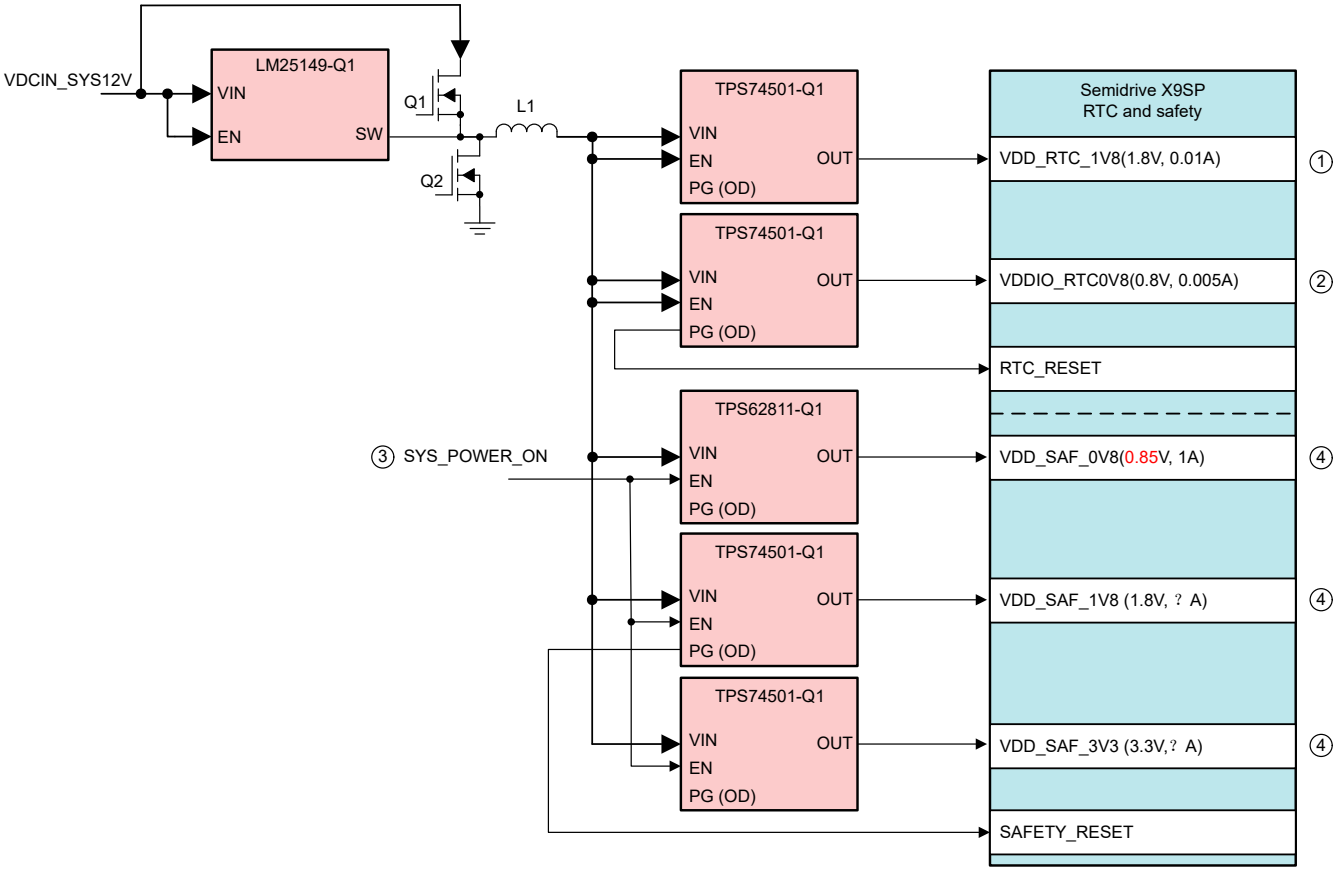
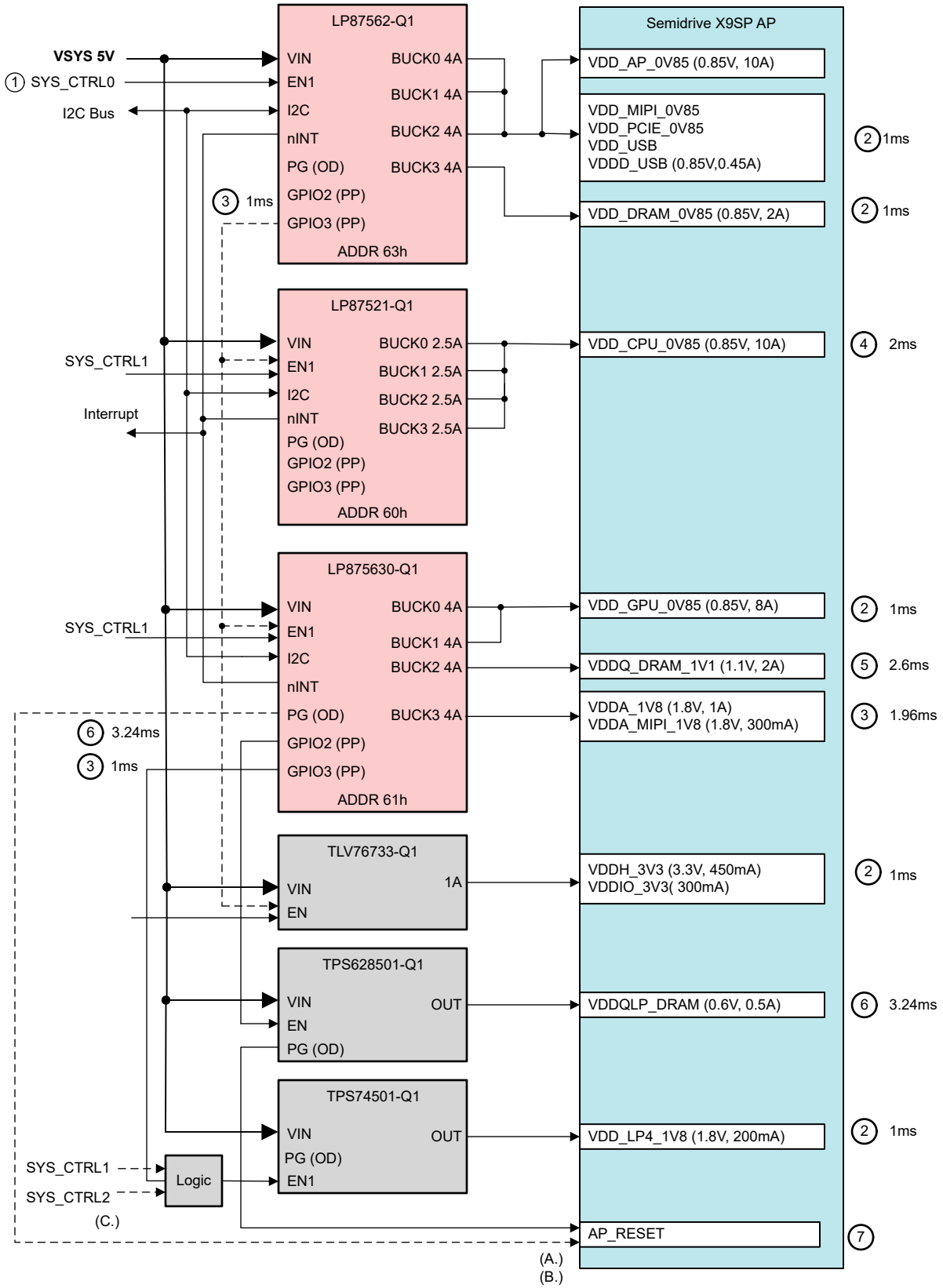


Figure 3-1. Semidrive X9SP RTC and Safety Power Tree

The main features include the following:

- 5V supplied from pre-regulator
- After the RTC devices are powered, the LDO TPS74501-Q1 PGOOD for VDDIO_RTC0V8 can set the signal RTC_RESET to high.
- MCU (in this case Semidrive X9SP) can set SYS_PWR_ON high to initiate startup sequence for safety rails.
- When the powering up for safety rails is complete, the LDO TPS74501-Q1 PGOOD for VDD_SAF_1V8 can set the signal SAFETY_RESET to high.
- Both RTC_RESET and SAFETY_RESET are open-drain.



A. LP87563 device reserves the PG pin reserved when VDDQLP_DRAM is absent.
B. Numbering denotes startup sequence.
C. For the purpose of STR.

Figure 3-2. Semidrive X9SP AP Power Tree

The main features include:

- 5V supplied from pre-regulator
- After the devices are powered, the microcontroller can control the EN signals of LP87521-Q1, LP87562-Q1 and LP87563-Q1 using system control signals SYS_CTRL0 and SYS_CTRL1.
- Startup delays are controlled internally in the LP87521-Q1, LP87562-Q1 and LP87563-Q1 logic and discrete LDO/buck regulators are controlled with LP87562-Q1 and LP87563-Q1 GPIO3. Section 3 has more details about the startup/shutdown sequence.
- I2C can be used to read status registers and reset interrupts. Because interrupt lines are connected together, both PMIC fault registers need to be read or cleared in case of interrupt goes low.
- All PMIC devices have dedicated I2C address so the devices can share the same I2C bus.
- TPS628501-Q1 PGOOD signals act as nRESET signal for the SoC (AP_RESET). Note the PGOOD functionality is disabled in the PMIC configuration, although it can be enabled through I2C bus.

4 Sequencing

4.1 Startup

Figure 4-1 shows startup timing of the power rails (RTC, safety, and AP) and corresponding signals.

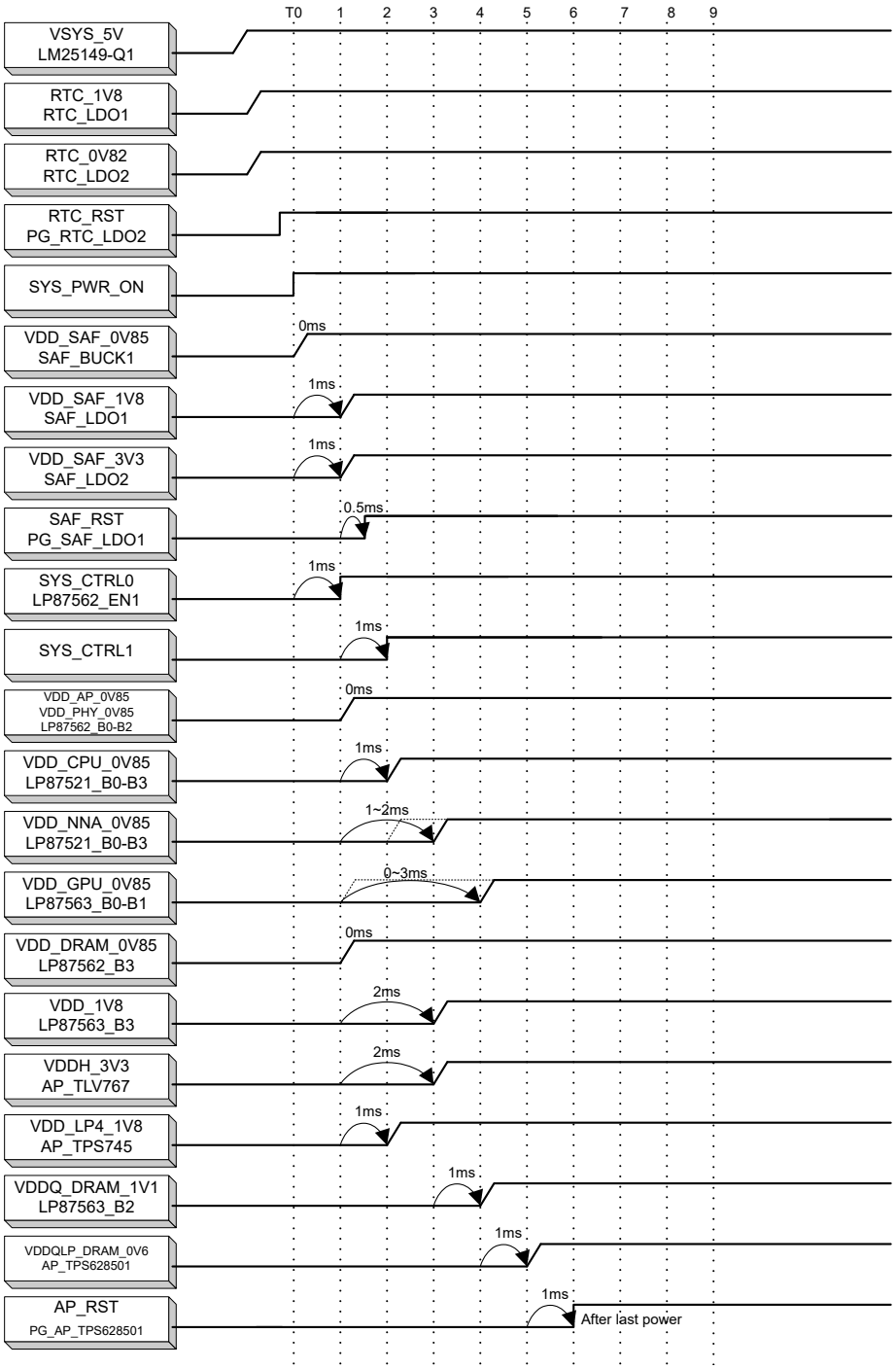


Figure 4-1. Semidrive X9SP Power Startup Timing Diagram

4.2 Shutdown

Figure 4-2 shows shutdown timing of the power rails (RTC, safety, and AP), and corresponding signals.

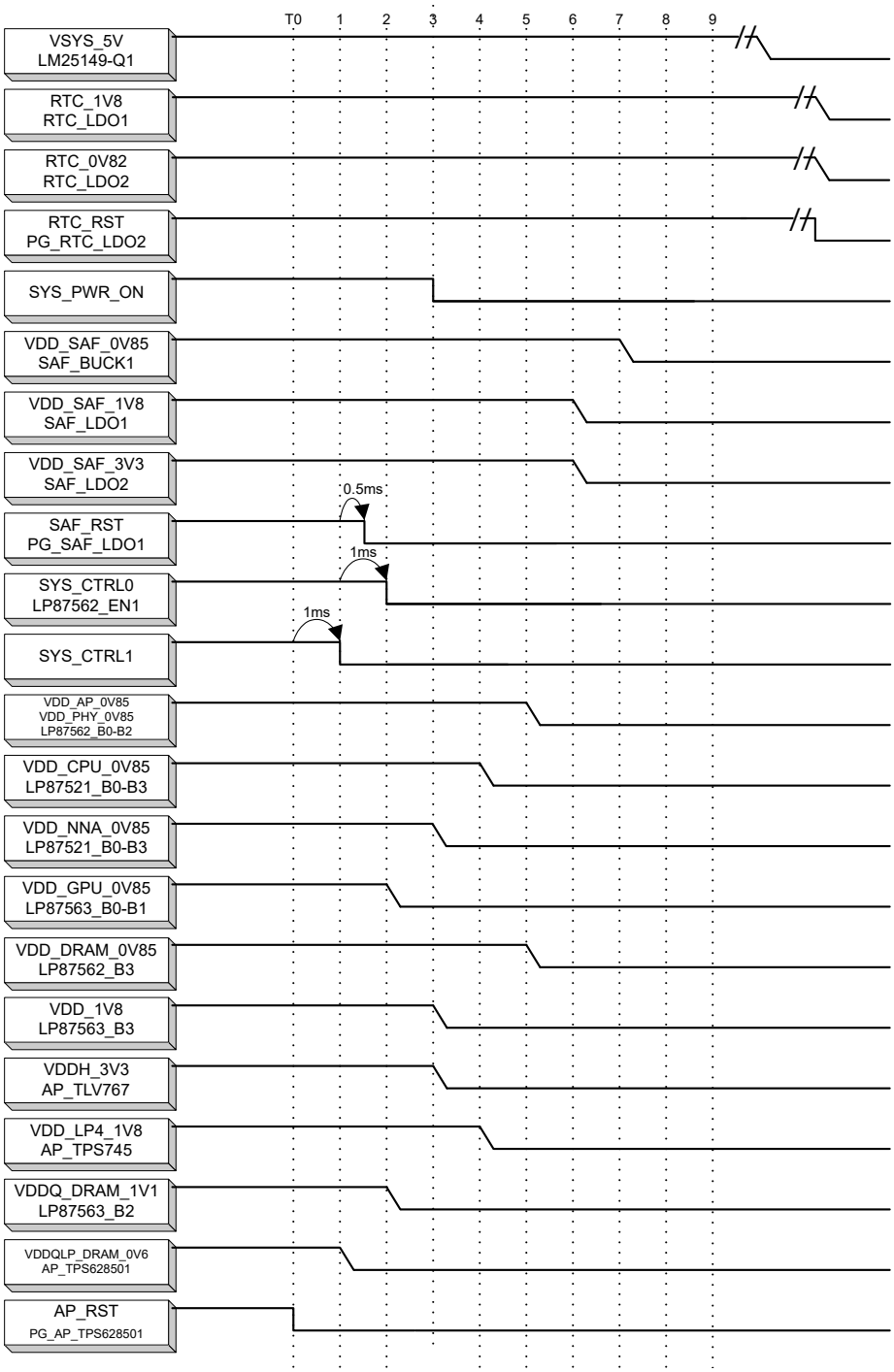


Figure 4-2. Semidrive X9SP Power Shutdown Timing Diagram

5 Schematic

Figure 5-1 through Figure 5-9 show the Semidrive X9SP power tree schematic with critical components. For guidance on layout, please refer to the data sheet application section and EVM user guide for the particular device.

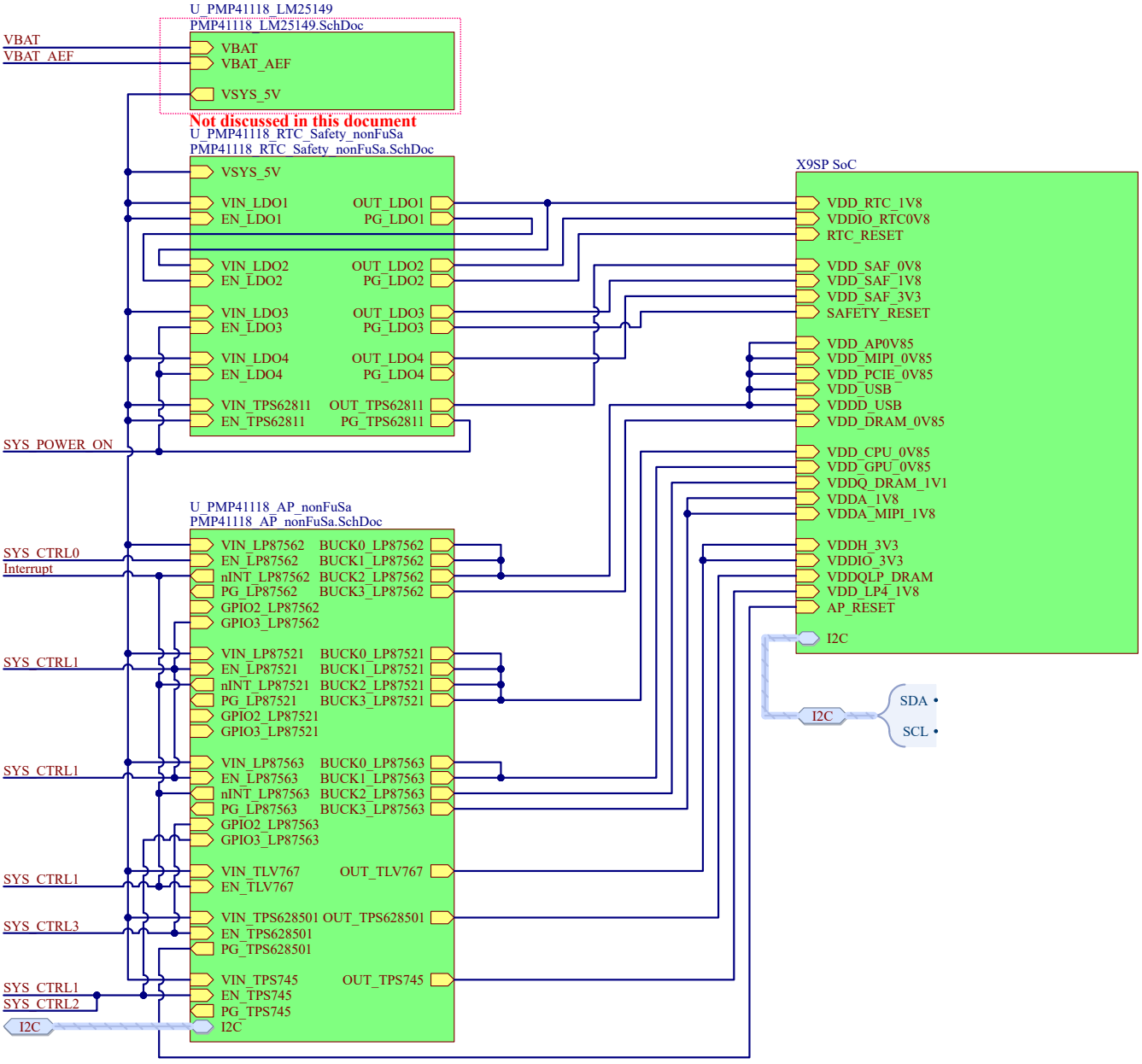


Figure 5-1. X9SP Power Tree Top Level Schematic

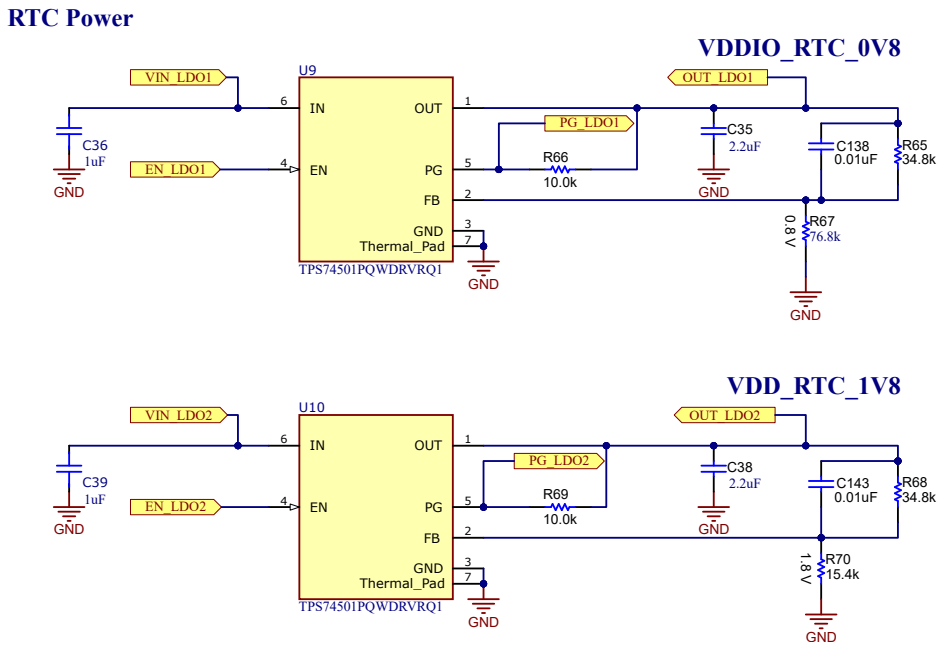


Figure 5-2. RTC Power Schematics (TPS74501-Q1)

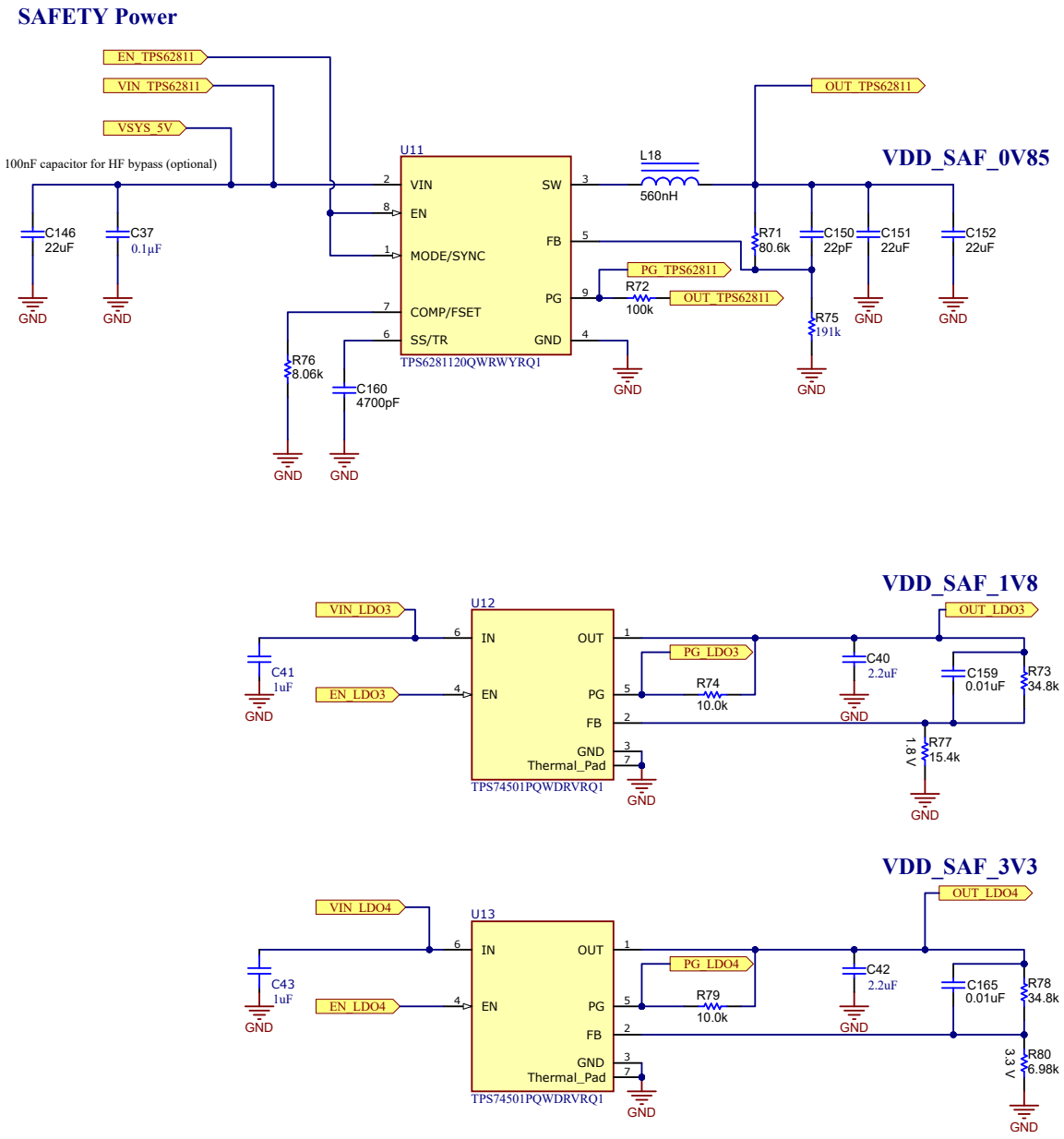


Figure 5-3. Safety Power Schematics (TPS62811-Q1 and TPS74501-Q1)

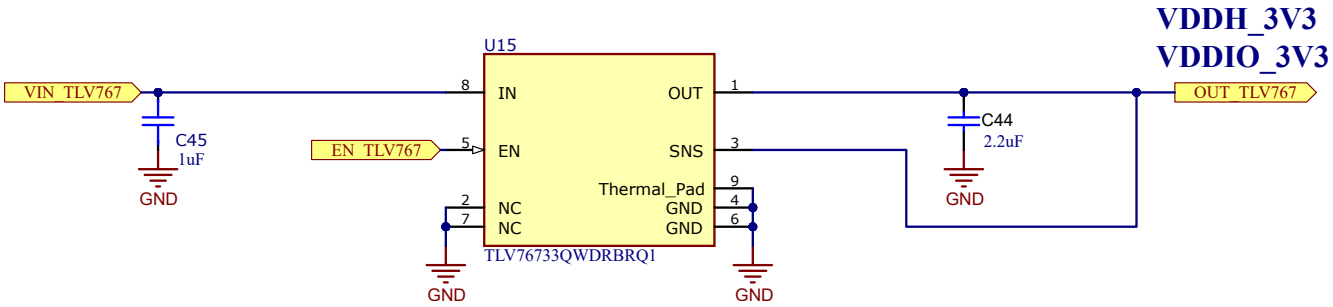


Figure 5-4. AP Power Schematics (TLV76733-Q1)

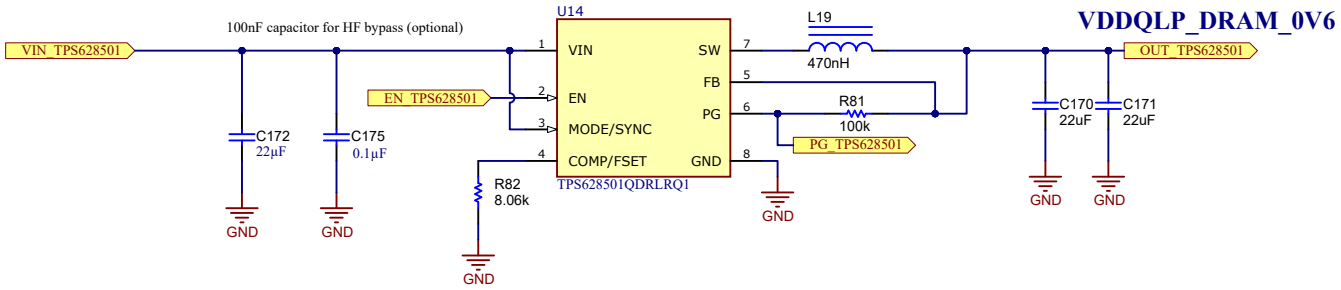


Figure 5-5. AP Power Schematics (TPS628501-Q1)

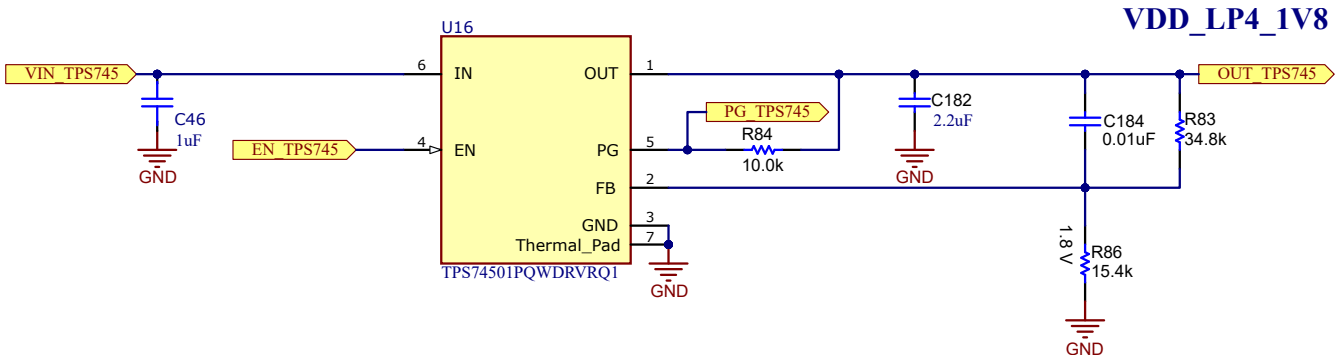


Figure 5-6. AP Power Schematics (TPS74501-Q1)

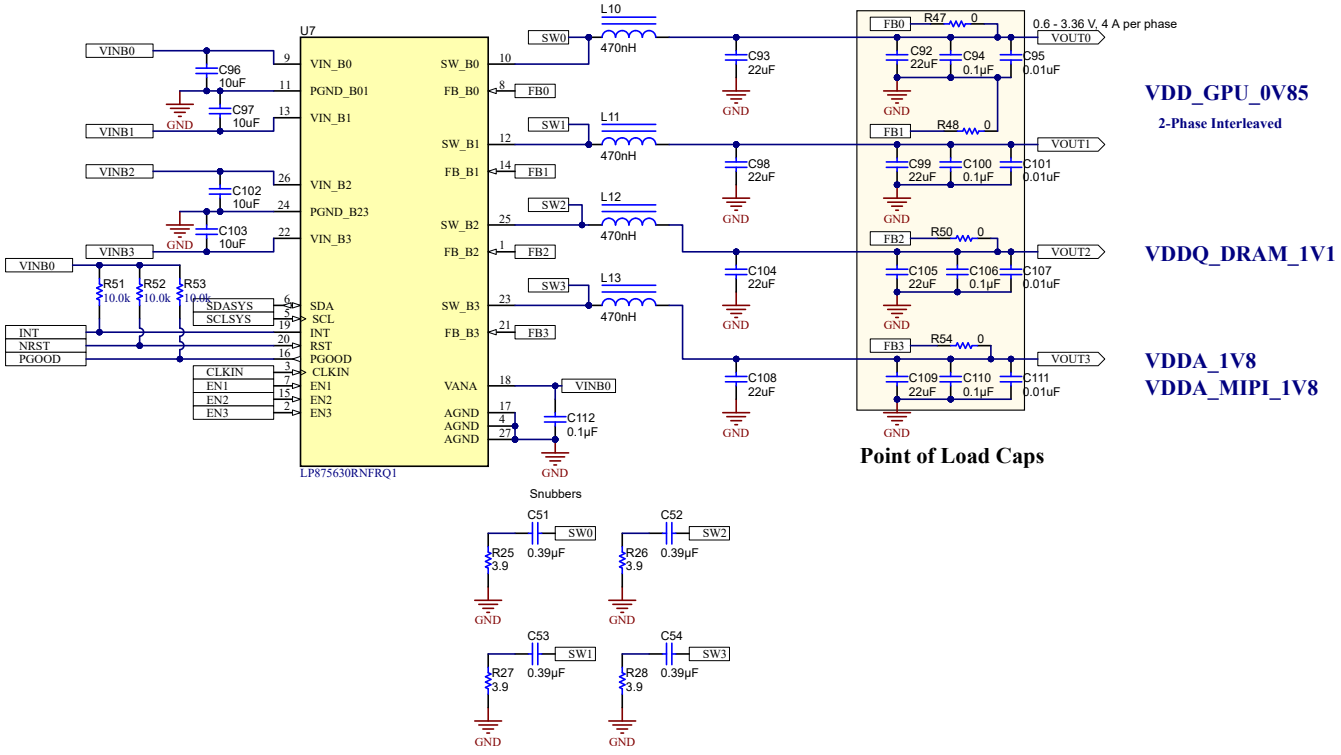


Figure 5-7. AP Power Schematics (LP87563-Q1)

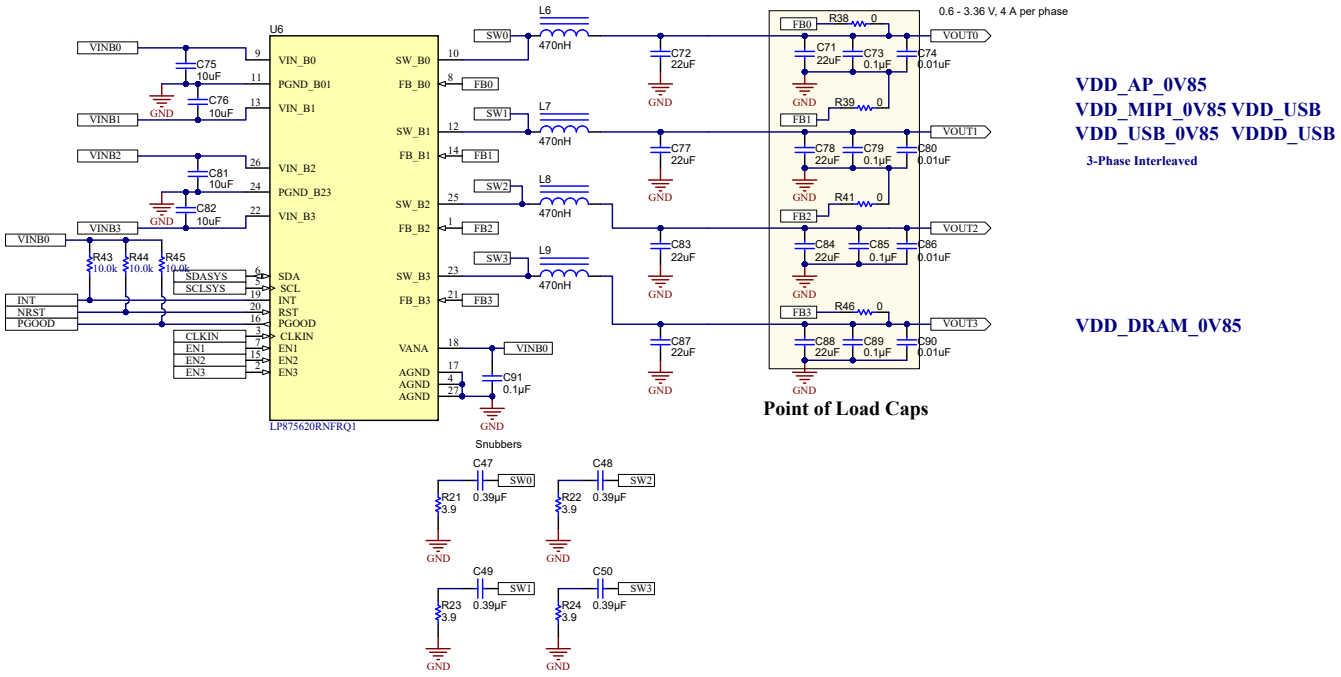


Figure 5-8. AP Power Schematics (LP87562-Q1)

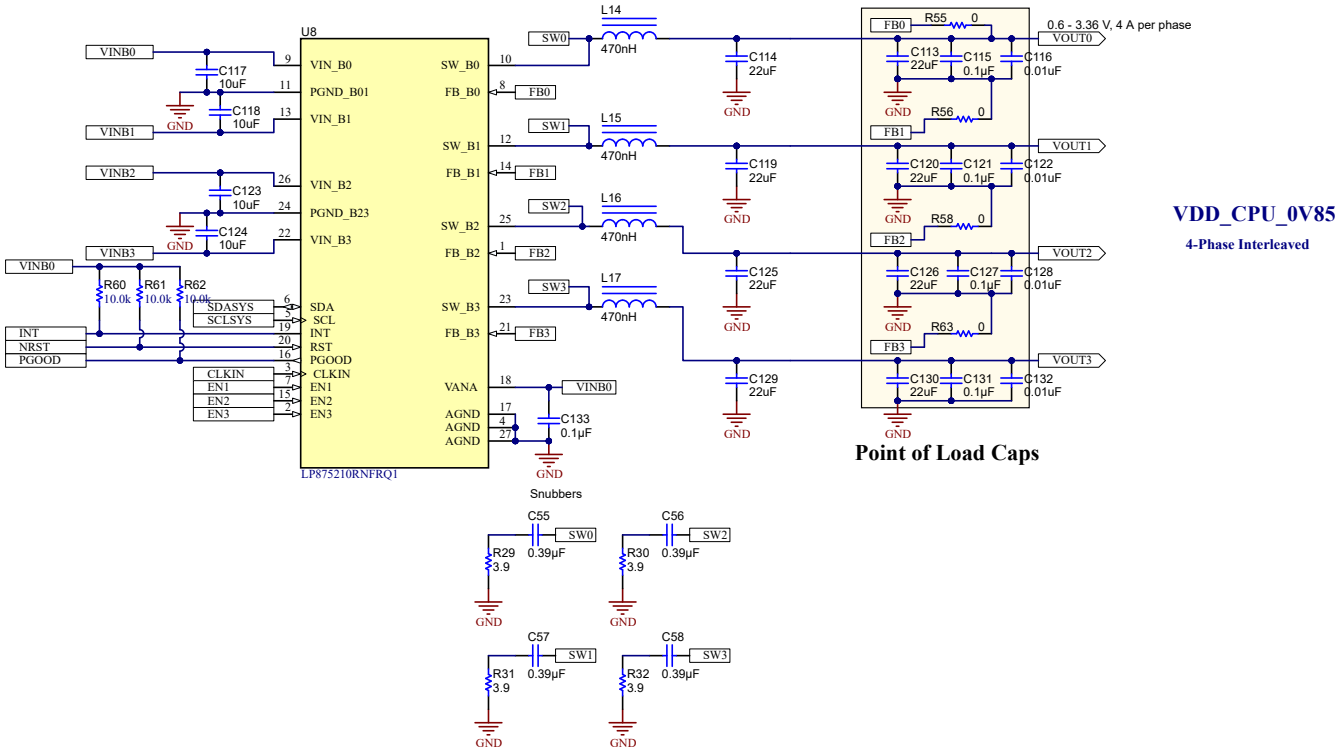


Figure 5-9. AP Power Schematics (LP87521-Q1)

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[1] Snubber is required for LP875x-Q1 since V_{in} = 5V is greater than 4V.

6 Compatibility with X9HP

This power supply design can be compatible with Semidrive X9HP, where pin-to-pin devices can be used to lessen re-design effort.

RTC and safety power supply for both MCUs are the same, so same power tree can be reused in powering X9HP.

There are some differences in powering the AP rails for X9HP and X9SP. Table 6-1 summarizes the differences in power requirement of X9HP and X9HP.

Table 6-1. Power Requirement Differences of X9HP and X9SP

Rail Names	Power Requirement in X9HP	Power Requirement in X9SP
VDD_AP + VDD_PHY(VDD_MIPI, VDD_PCIE, VDD_USB, VDDD_USB)	0.8V, 8A(combined with VDD_AP and VDD_PHY)	0.85V, 10A+0.45A
VDD_DRAM	0.8V, 8A(combined with VDD_AP and VDD_PHY)	0.85V, 2A
VDD_GPU	0.85V, 5A	0.85V, 8A
VDDQ_DRAM	1.1V, 1.75A	1.1V, 2A
VDDA, VDDA_MIPI	1.8V, 1A+50mA	1.8V, 1A+300mA
VDD_CPU	0.8V, 6A	0.85V, 10A
VDDH	3.3V, 450mA	3.3V, 450mA Combined with VDDIO_3V3, 3.3V, 300mA

Figure 6-1 shows AP power tree with LP87565V-Q1, LP875230C-Q1, TLV76733-Q1, TPS6281120-Q1, and TPS74518-Q1 devices powering the X9HP rails. Note that the PMICs for VDD_AP, VDD_DRAM and VDD_CPU are not pin-to-pin replaceable (two PMICs (LP87562-Q1 and LP87521-Q1) are used for these three rails in powering X9SP, while only one PMIC (LP87565V-Q1) is used for X9HP).

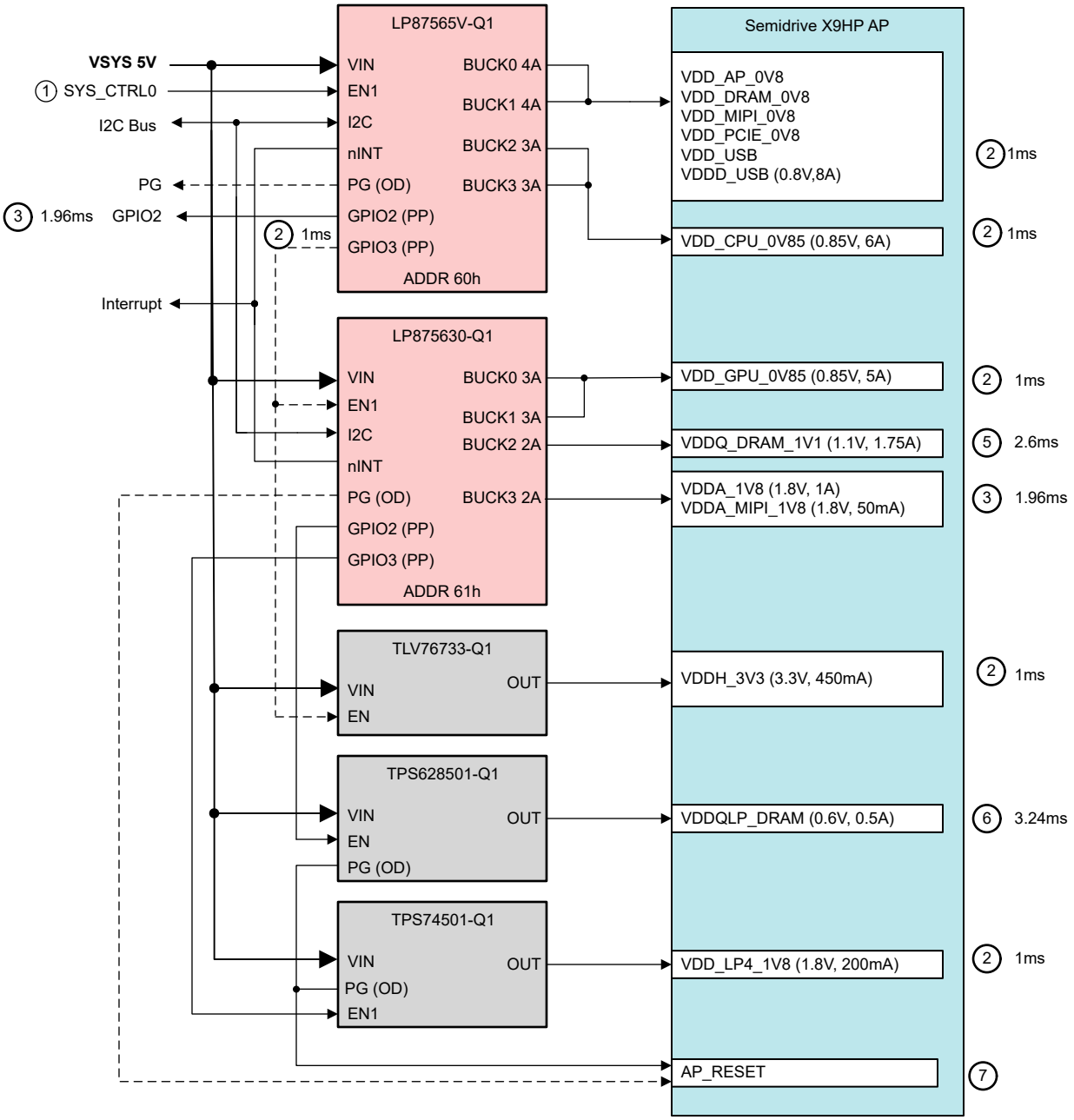

Figure 6-1. Semidrive X9HP AP Power Tree

Since other rails are still pin-to-pin interchangeable, Table 6-2 shows the pin-to-pin options for rail VDD_GPU, VDDQ_DRAM, VDDA_1V8, VDDA_MIPI, VDDH_3V3 (and VDDIO_3V3), VDDQLP_DRAM and VDD_LP4.

Table 6-2. Pin-to-Pin Options

Rail Names	Allocated Device for X9HP	Allocated Device for X9SP
VDD_GPU, VDDQ_DRAM, VDDA_1V8, VDDA_MIPI_1V8	LP875230C-Q1	LP87563-Q1
VDDH_3V3 (and VDDIO_3V3)	TLV76733-Q1	TLV76733-Q1
VDDQLP_DRAM	TPS628501-Q1	TPS628501-Q1
VDD_LP4_1V8	TPS74518-Q1	TPS74501-Q1 (substitution is optional)

There are three options when re-selecting the devices for achieving the compatibility between X9HP and X9SP.

1. **Substituting PMICs:** As discussed previously, use LP87562TRNFRQ1 and LP87521SRNFRQ1 for X9SP to substitute LP87565VRNFRQ1 for X9HP in powering VDD_AP, VDD_DRAM and VDD_CPU.
2. **Substitute PMICs with discrete bucks:** End users can power VDD_AP, VDD_DRAM and VDD_CPU with discrete pin-to-pin bucks for simple upgrade compatibility. See Table 6-3 for an example substitution.

Table 6-3. Examples of Substitution

Rail Names	Allocated Device for X9HP	Allocated Device for X9SP
VDD_AP	TPS62870-Q1 (rated at 6A; 6A needed)	TPS62872-Q1 (rated at 12A; 10.45A needed)
VDD_DRAM	TPS62811-Q1 (rated at 1A; 1A needed)	TPS62812-Q1 (rated at 2A; 2A needed)
VDD_CPU	TPS62870-Q1 (rated at 6A; 6A needed)	TPS62872-Q1 (rated at 12A; 10A needed)

3. **Substitute all rails with discrete bucks/LDOs:** End users can further replace the LP8752/63-Q1 PMIC (originally for VDD_GPU, VDDQ_DRAM, VDDA_1V8 and VDDA_MIPI_1V8) with discrete pin-to-pin bucks, as an extension of previous discussions. See Table 6-4 for an example substitution.

Table 6-4. Examples of Substitution

Rail Names	Allocated Device for X9HP	Allocated Device for X9SP
VDD_GPU	TPS62870-Q1 (rated at 6A; 5A needed)	TPS62871-Q1 (rated at 9A; 8A needed)
VDDQ_DRAM	TPS62812-Q1 (rated at 2A; 1.75A needed)	TPS62811-Q1 (rated at 1A; 0.75A needed)
VDDA_1V8 VDDA_MIPI_1V8	TPS62812-Q1 (rated at 2A; 1.05A needed)	TPS62812-Q1 (rated at 2A; 1.3A needed)

7 Software Drivers

This design supports control through I2C bus. Linux drivers for the LP875x are available in public git repository. These can be used to help integrate the LP875x control to system software:

- https://github.com/torvalds/linux/blob/master/drivers/mfd/lp87565.c
- https://github.com/torvalds/linux/blob/master/drivers/regulator/lp87565-regulator.c
- https://github.com/torvalds/linux/blob/master/drivers/gpio/gpio-lp87565.c

Note: Every header file is in the include folder starting from the root directory. Once in the include folder, the user can navigate to the relevant header file. For example, the LP87565.h file: Torvalds/Linux/include/linux/mfd/lp87565.h.

8 Recommended External Components

Assuming 1mm keep-out around each component, and multiplying by component count.

Table 8-1. Bill of Materials

COUNT	VENDOR	PART NUMBER	SYSTEM COMPONENT	W (mm)	L (mm)	H (mm)	UNIT AREA	TOTAL BOARD AREA
3	TI	LP875x-Q1	Configurable 4-phase Buck	4	4.5	0.9	27.5	82.5
12	Murata	DFE252012PD-R47M	LP875x Inductor 0.47µH, Imax 4.0A, Rdc typ 21mOhm	2.5	2	1.2	10.5	126
12	Murata	GCM21BR71A106KE22	LP875x SMPS Input Capacitor 10µF, 10V, 10%	2	1.25	1.25	6.75	81
24	Murata	GCM21BD70J226ME35	LP875x SMPS Output Capacitor 22µF, 10V, 10%	2	1.25	1.25	6.75	162
3	Murata	GCM155R71C104KA55D	LP875x Input Capacitor 0.1µF, 16V, 10%	1	0.5	0.5	3	9
5	TI	TPS74501-Q1	Low Dropout Regulator (adjustable)	2	2	0.8	9	45
5	Murata	GCM188R71C105KA64D	Input Capacitor 1µF	1	0.5	0.5	3	15
15			Output voltage set/PG resistor	1	0.5	0.5	3	45
5	Murata	GRT155C71A225KE13	Output Capacitor 2.2µF	1	0.5	0.5	3	15
1	TI	TPS628501-Q1	Buck Converter	3	2	0.8	12	12
1	Murata	DFE252012PD-R47M	Inductor 0.47µH, Imax 4.0A, Rdc typ 21mOhm	2.5	2	1.2	10.5	10.5
1	Murata	GCM21BD70J226ME35	Input Capacitor 22µF, 10V, 10%	2	1.25	1.25	6.75	6.75
2	Murata	GCM21BD70J226ME35	Output Capacitor 22µF, 10V, 10%	2	1.25	1.25	6.75	13.5
2			Frequency set/PG resistor	1	0.5	0.5	3	6
1	TI	TPS6281120-Q1	Buck Converter	3	2	0.8	12	12
1	Murata	DFE252012PD-R47M	Inductor 0.47µH, Imax 4.0A, Rdc typ 21mOhm	2.5	2	1.2	10.5	10.5
1	Murata	GCM21BD70J226ME35	Input Capacitor 22µF, 10V, 10%	2	1.25	1.25	6.75	6.75
2	Murata	GCM21BD70J226ME35	Output Capacitor 22µF, 10V, 10%	2	1.25	1.25	6.75	13.5
1	Murata	GRT155R71H472KE01	CSS capacitors	1	0.5	0.5	3	3
4			Config resistor	1	0.5	0.5	3	12
1	Murata	GCM21BR71A106KE22	Output Capacitor 10µF, 10V, 10%	2	1.25	1.25	6.75	6.75
1	TI	TLV76733-Q1	Low Dropout Regulator	3	3	1	16	16
1	Murata	GCM188R71C105KA64D	Input Capacitor 1µF	1	0.5	0.5	3	3

Table 8-1. Bill of Materials (continued)

COUNT	VENDOR	PART NUMBER	SYSTEM COMPONENT	W (mm)	L (mm)	H (mm)	UNIT AREA	TOTAL BOARD AREA
1	Murata	GCM188R71C105KA64D	Input Capacitor 1µF	1	0.5	0.5	3	3
TOTAL								715.75mm^2
Routing area calculated with 0.3 routing factor								306.75mm^2
Total estimated area								1022.5mm^2

9 Summary

With this presented design with the LP87563-Q1, LP87562-Q1 and LP87521-Q1 PMICs + discrete LDOs and Bucks, there is a possibility to meet power requirements for Semidrive X9SP application processor while maintaining good efficiency. The power supply design for Semidirve X9HP is compatible with this system design and the AP power supply are pin-to-pin interchangeable. Sequencing is handled in PMICs and only one EN signal is needed from the controller. The design is compact due to minimum number of external components. I2C control allows diagnostic and PMIC control if needed.

10 References

1. Texas Instruments, *LP8756x-Q1 16A Buck Converter With Integrated Switches*, data sheet.
2. Texas Instruments, *LP87562T-Q1 Technical Reference Manual*.
3. Texas Instruments, *LP875630-Q1 Technical Reference Manual*.
4. Texas Instruments, *LP8752x-Q1 10-A Buck Converter With Integrated Switches*, data sheet.
5. Texas Instruments, *LP87521S-Q1 Technical Reference Manual*.
6. Texas Instruments, *LP87565V-Q1 Technical Reference Manual*.
7. Texas Instruments, *TLV767-Q1 1-A, 16-V Linear Voltage Regulator*, data sheet.
8. Texas Instruments, *TPS6287x-Q1 2.7-V to 6-V Input, 6-A, 9-A, 12-A, 15-A, Stackable, Synchronous Step Down Converters with Fast Transient Response*, data sheet.
9. Texas Instruments, *TPS745-Q1 500-mA LDO With Power-Good in Small Wettable Flank WSON Packages* data sheet.
10. Texas Instruments, *TPS628501-Q1 2.7V-to 6V 1-A adjustable-frequency step-down converter in SOT-583 package*, data sheet.
11. Texas Instruments, *TPS6281x-Q1 2.75-V to 6-V Adjustable-Frequency Step-Down Converter*, data sheet.

11 Revision History

Changes from Revision * (July 2024) to Revision A (December 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

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