Application Report

TPS5516x-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS5516x-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

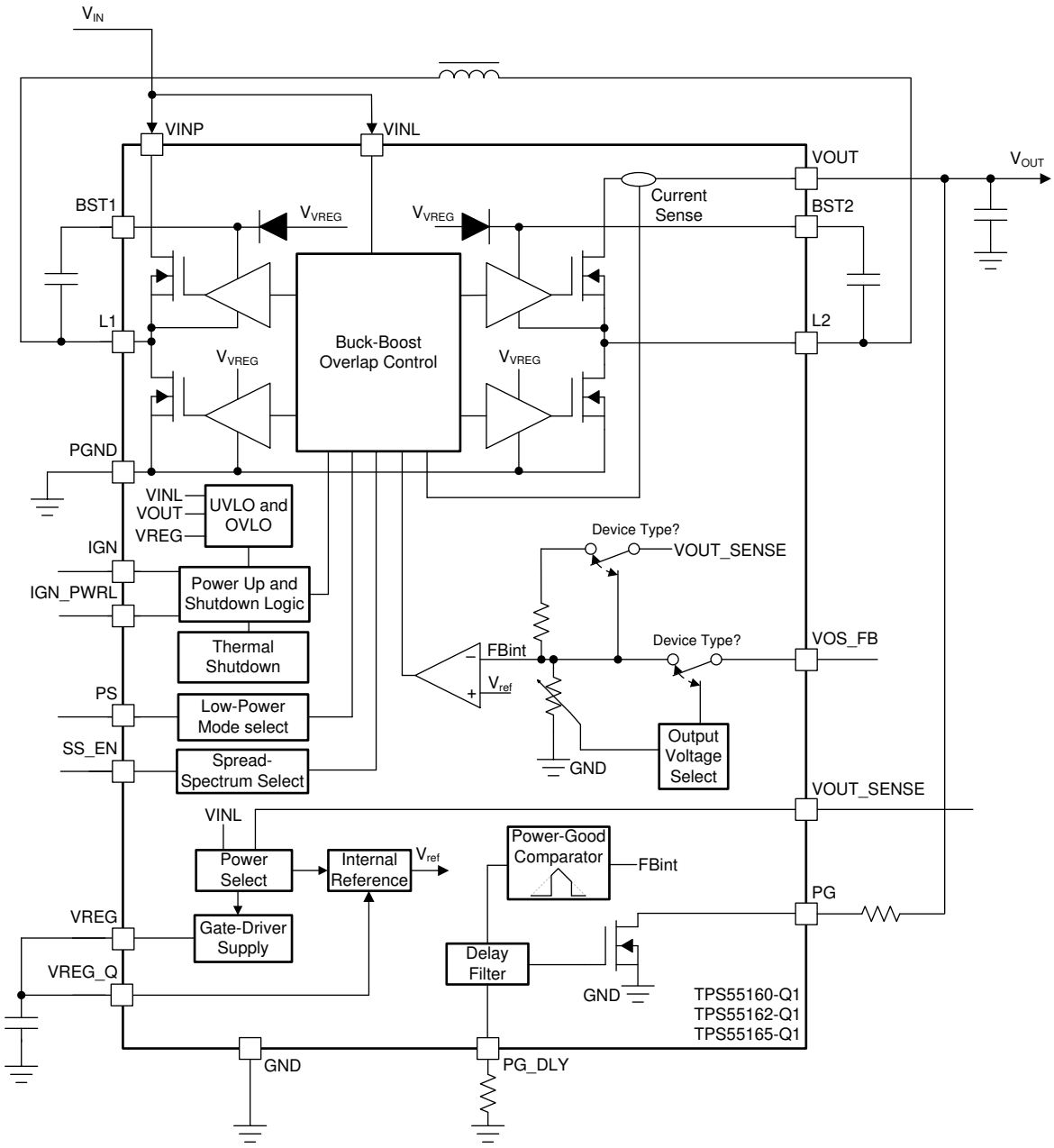

Figure 1-1. Functional Block Diagram

TPS5516x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS5516x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	22
Die FIT Rate	9
Package FIT Rate	13

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1200 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed =<50V supply	60 FIT	70 °C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS5516x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT no output (HiZ)	25%
VOUT out of specification high	20%
VOUT out of specification low	20%
VOUT functional, out for specification timing	30%
PG false trip, fails to trip	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS5516x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS5516x-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS5516x-Q1 data sheet.

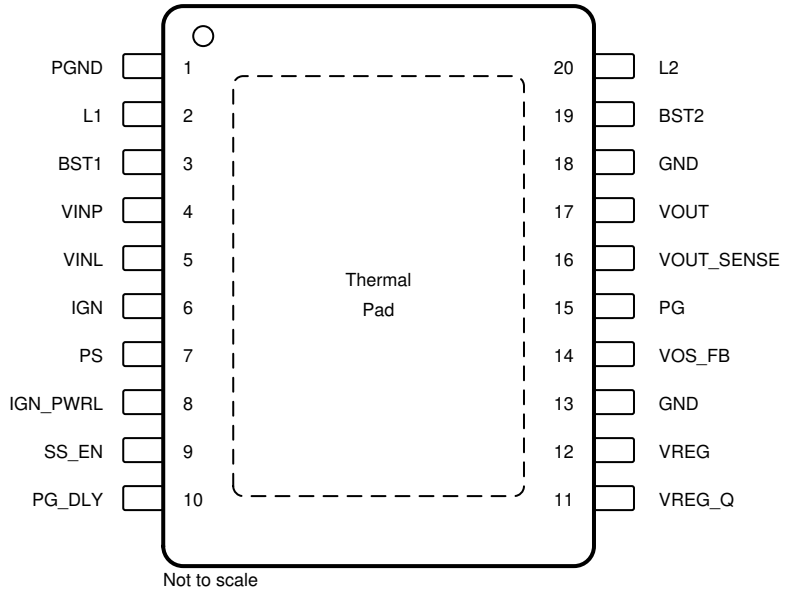

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the '*Recommended Operating Conditions*' and the '*Absolute Maximum Ratings*' found in the TPS5516x-Q1 data sheet.
- Configuration as shown in the '*Application and Implementation*' found in the TPS5516x-Q1 data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	No effect.	D
L1	2	Possible device damage.	A
BST1	3	No output voltage.	B
VINP	4	No output voltage. Power supply is short.	B
VINL	5	No output voltage. Power supply is short.	B
IGN	6	No output voltage.	B
PS	7	Loss of low-power mode functionality.	C
IGN_PWRL	8	Loss of IGN power-latch functionality.	C
SS_EN	9	Loss of spread-spectrum functionality.	C
PG_DLY	10	The PG delay time is fixed 2 ms.	C
VREG_Q	11	No output voltage.	B
VREG	12	No output voltage.	B
GND	13	No effect.	D
VOS_FB	14	For TPS55160-Q1 and TPS55162-Q1, OVP.	B
		For TPS55165-Q1, Vout = 5 V.	C
PG	15	Loss of PG functionality.	C
VOUT_SENSE	16	No output voltage because of OCP protection.	B
VOUT	17	No output voltage because of OCP protection.	B
GND	18	No effect.	D
BST2	19	No output voltage.	B
L2	20	No output voltage.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	No output voltage.	B
L1	2	No output voltage.	B
BST1	3	No output voltage.	B
VINP	4	No output voltage.	B
VINL	5	No output voltage.	B
IGN	6	No output voltage.	B
PS	7	The IC works in the normal mode condition. But it can't enter into the low-power mode.	C
IGN_PWRL	8	Correct output voltage. Loss of IGN power-latch functionality.	C
SS_EN	9	Correct output voltage. Loss of spread-spectrum functionality.	C
PG_DLY	10	Correct output voltage. But it can't configure power-good delay time.	C
VREG_Q	11	No output voltage.	B
VREG	12	No output voltage.	B
GND	13	No output voltage.	B
VOS_FB	14	For TPS55160-Q1 and TPS55162-Q1, OVP.	B
		For TPS55165-Q1, Vout = 5 V.	C
PG	15	Correct output voltage. Loss of power good functionality.	C
VOUT_SENSE	16	No output voltage.	B
VOUT	17	No output voltage.	B
GND	18	No output voltage.	B
BST2	19	No output voltage.	B
L2	20	No output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	L1	IC damaged. No output.	A
L1	2	BST1	No output voltage.	B
BST1	3	VINP	Possible device damage.	A
VINP	4	VINL	Higher output voltage ripple if power decouple capacitor is put far away from VINP.	C
VINL	5	IGN	Device can't be disabled by IGN pin.	C
IGN	6	PS	Output voltage oscillates. The IC works in the low power mode.	B
PS	7	IGN_PWRL	IC damaged if PS is set to higher than 5.5 V.	A
IGN_PWRL	8	SS_EN	IGN power-latch, spread-specturm function can't be controlled independenly.	C
SS_EN	9	PG_DLY	Spread-specturm, PG delay function can't be controlled independenly.	C
VREG_Q	11	VREG	Output voltage ripple higher(circuit unstable). But the device is good.	C
VREG	12	GND	No output voltage.	B
GND	13	VOS_FB	For TPS55160-Q1 and TPS55162-Q1, OVP.	B
			For TPS55165-Q1, Vout = 5 V.	C
VOS_FB	14	PG	For TPS55160-Q1 and TPS55162-Q1, OVP.	B
			For TPS55165-Q1, no effect.	D
PG	15	VOUT_SENSE	Possible damage to device.	A
VOUT_SENSE	16	VOUT	Output voltage ripple higher(circuit unstable).	C
VOUT	17	GND	No output because of OCP protection.	B
GND	18	BST2	No output voltage.	B
BST2	19	L2	No output voltage.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	Possible damage to this pin due to large current.	A
L1	2	Vout follows Vin change (Vo ≈ Vin - 0.7 V). Possible device damage.	A
BST1	3	No output voltage. Possible device damage.	A
VINP	4	The IC works normally.	D
VINL	5	The IC works normally.	D
IGN	6	Device can't be disabled by IGN pin.	C
PS	7	The IC works in the low power mode, can't draw > 50 mA load current.	C
IGN_PWRL	8	IGN_PWRL pin damaged when the supply voltage is higher than 5.5 V, then no output.	A
SS_EN	9	SS_EN pin may damaged when the supply voltage is higher than 5.5 V.	A
PG_DLY	10	The PG_DLY pin may damaged when the supply voltage is higher than 5.5 V.	A
VREG_Q	11	VREG_Q pin damaged when the supply voltage is higher than 5.5 V..	A
VREG	12	VREG pin damaged when the supply voltage is higher than 5.5 V.	A
GND	13	Possible damage to this pin due to large current.	A
VOS_FB	14	No output voltage. Possible device damage.	A
PG	15	PG pin damaged when supply volatge is higher than 15 V.	A
VOUT_SENSE	16	When Vin > 20 V, Vout pin and VOUT_SENSE pin may be damaged.	A
VOUT	17	When Vin > 20 V, Vout pin and VOUT_SENSE pin may be damaged.	A
GND	18	Possible damage to this pin due to large current.	A
BST2	19	No output voltage. BST2 pin may damaged when the supply voltage is higher than 5.5 V.	A
L2	20	Possible damage to device when the supply voltage is higher than 20V.	A

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