Application Report

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FET Configurations for the bq76200 High-Side N-Channel FET Driver

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ABSTRACT

The bq76200 is a low-power, high-side, N-Channel MOSFET driver that can be utilized in a variety of FET configurations to assist the user's battery protection system from faults such as a cell's undervoltage and overvoltage or a short circuit. The following material is aimed to portray various applications of the bq76200 with several different configurations of FETs, pack voltages, and cell counts that will represent the driver's functionality under each setup. These configurations were chosen to portray the optimal functionality of the part as well as to define the parameters of applicability in order to present examples where a setup may need debugging.

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1 Introduction

The bq76200 high-side FET driver can be used in battery protection systems in order to provide switching between normal operating modes and fault conditions. Faults such as a cell's undervoltage and overvoltage and short circuit were simulated across the following set of FET and pack voltage configurations in order to portray the switching times of the CHG and DSG signals, which when becoming high, allow the battery access to charging and discharging, respectfully.

2 Test Configurations Table

Table 1 contains the test configurations data.

Table 1. Test Configurations

Name of Setup	Companion Devices	Pack Configurations	CHG FETs	DSG FETs	FET Arrangement
940 - 1x FETs	bq76940 + bq78350	48 V, 36 V	1x	1x	Series
940 - 2x FETs	bq76940 + bq78350	48 V, 36 V	2x	2x	Series
940 - 4x FETs	bq76940 + bq78350	48 V, 36 V	4x	4x	Series

Table 1. Test Configurations (continued)

Name of Setup	Companion Devices	Pack Configurations	CHG FETs	DSG FETs	FET Arrangement
940 - 8x FETs	bq76940 + bq78350	48 V, 36 V	8x	8x	Series
940 - 12x FETs	bq76940 + bq78350	48 V, 36 V	12x	12x	Series
940 - 4:8x FETs	bq76940 + bq78350	48 V, 36 V	4x	8x	Parallel
940 - 4:12x FETs	bq76940 + bq78350	48 V, 36 V	4x	12x	Parallel
940 - Parallel FETs	bq76940 + bq78350	48 V, 36 V	4x	4x	Parallel
930 - 1x FETs	bq76930 + bq78350	36 V, 24 V	1x	1x	Series
930 - 8x FETs	bq76930 + bq78350	36 V, 24 V	8x	8x	Series
930 - 4:8x FETs	bq76930 + bq78350	36 V, 24 V	4x	8x	Parallel
930 - Parallel FETs	bq76930 + bq78350	36 V, 24 V	4x	4x	Parallel
920 - 1x FETs	bq76920 + bq78350	14.4 V, 18 V	1x	1x	Series
920 - 8x FETs	bq76920 + bq78350	14.4 V, 18 V	8x	8x	Series
920 - 4:8x FETs	bq76920 + bq78350	14.4 V, 18 V	4x	8x	Parallel
920 - Parallel FETs	bq76920 + bq78350	14.4 V, 18 V	4x	4x	Parallel
940 - Pre*discharge*	bq76940 + bq78350	48 V	8x	8x	Series
920 - Pre*discharge*	bq76920 + bq78350	18 V	8x	8x	Series
940 - Max Cells	bq76940 + bq78350	63 V ("54 V")	8x	8x	Series
920 - Min Cells	bq76920 + bq78350	10.8 V	2x	2x	Series

- bq76930 and bq76940 Evaluation Module User's Guide (SLVU925)
- bq76920 EVM User's Guide (SLVU924)
- bq78350 Technical Reference Manual (SLUUAN7)

NOTE: The pack voltages were chosen so that the cells would perform at a nominal voltage of approximately 3.6 V and the corresponding FETs were chosen to best represent an ideal application.

- CSD19536KCS N-channel MOSFETs used for tests:
  – Approximately 9.24 nF C_L, Vds: 100 V, Current: 150 A

NOTE: Several of the tests were performed using the IRFB3207ZPBF FETs which produced similar results.

3 Main Test Setup

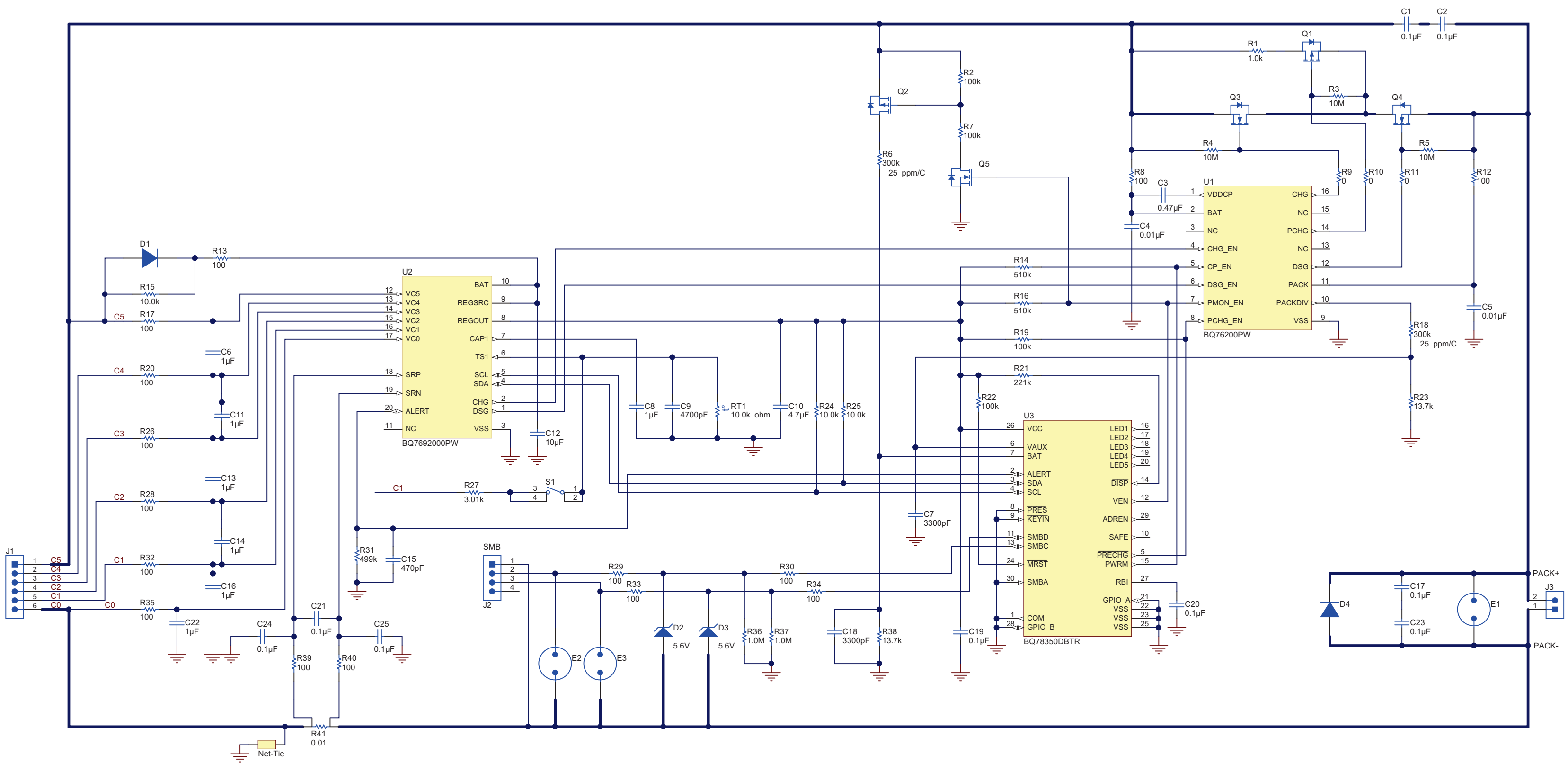


Figure 1. Main Test Setup Schematic

4 Test Data

The following set of data represents the functionality of the bq76200 under various FET configurations and PACK voltages when driving FETs after an undervoltage, overvoltage or short circuit. Due to the increasing voltage difference/AFE among tests only slightly delaying FET switching times, each table of FET configurations will be represented by one set of data that provides a reference for the others.

4.1 1xCFET/1xDFET

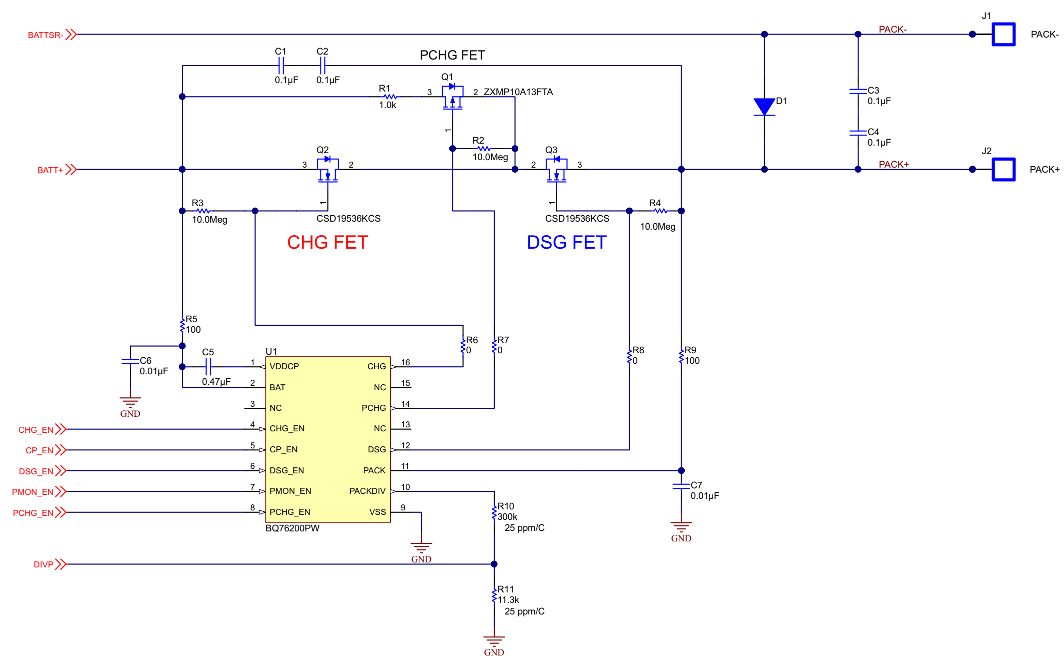
FET Arrangement: 1 charge FET (1xCFET), 1 discharge FET (1xDFET) in series

Table 2. 1xFET Configurations

AFE	# CHG FETs	# DSG FETs	PACK Voltage	# of Cells	FET Arrangement	VDDCP Capacitance
bq76920	1x	1x	14.4 V, 18 V	4, 5	Series	0.47 µF
bq76930			24 V, 36 V	6, 10		
bq76940			36 V, 48 V	10, 13		

4.1.1 Series Configuration

The CHG and DSG FETs are commonly arranged in series in order to support the PCHG feature and to reduce modifications to their design. In this arrangement the FETs will share a common charge path to PACK+ and the user will not need to add extra discharge capacitors for the one path. The following schematic details an ideal setup and construction when utilizing the series FET configuration.



BATTSR- represents BATT- with the sense resistor relative to the AFE used in the application.

Figure 2. CHG and DSG FETs Arranged in Series

Test: 36 V, 1xFETs, 10 cells, Undervoltage of a cell with a load of 1 A

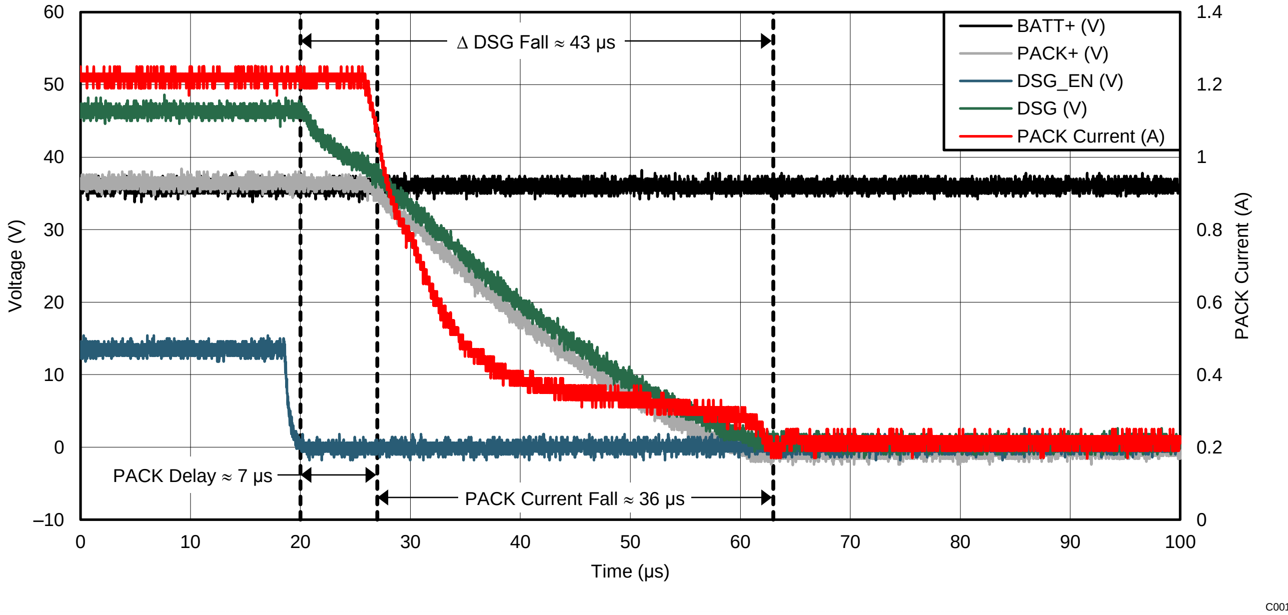


Figure 3. 1xDFET DSG Turn-Off After UV

Test: 36 V, 1xFETs, 10 cells, Overvoltage of a cell when charging at 21 V (4.2 V per cell)

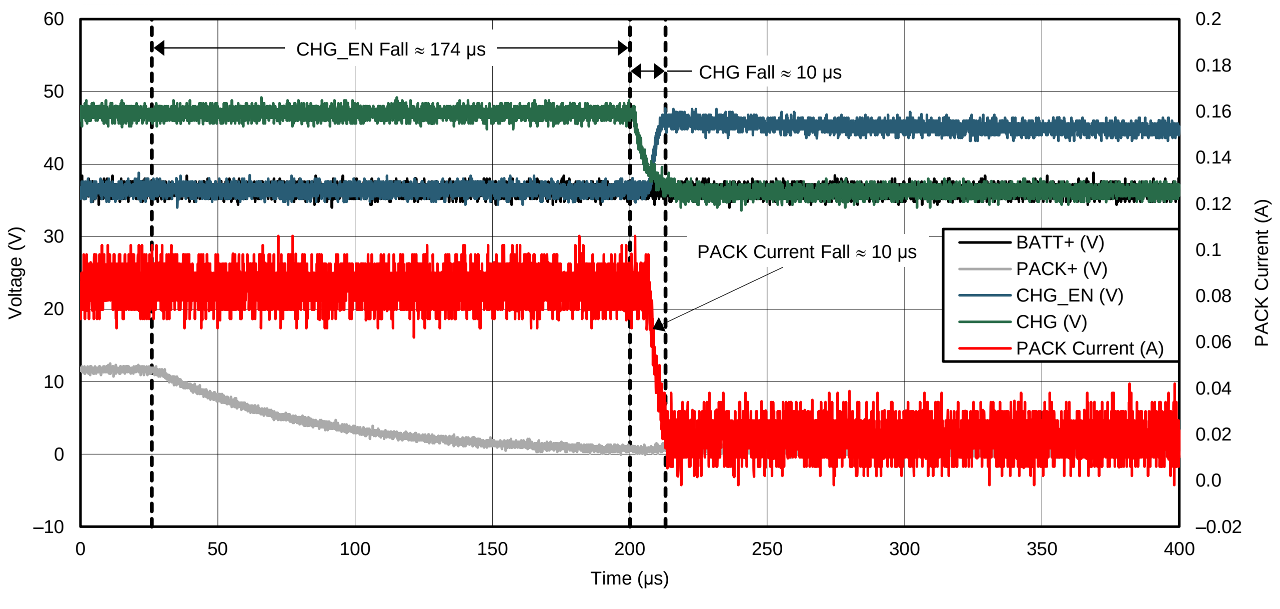


Figure 4. 1xCFET CHG Turn-Off After OV

Test: Short circuit

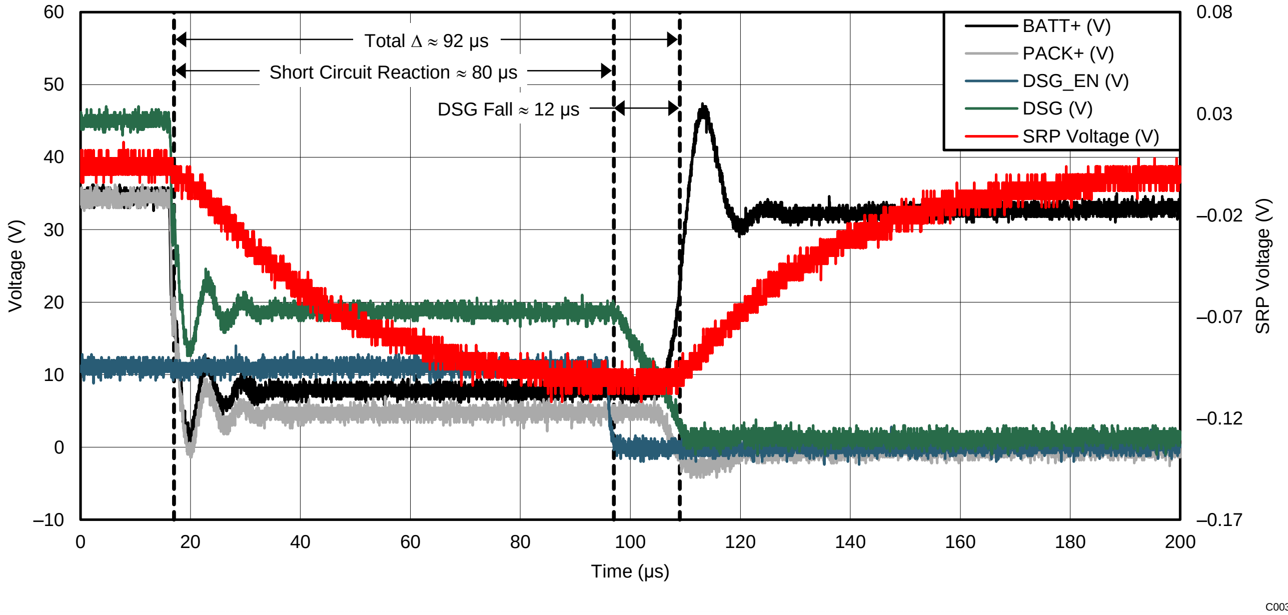


Figure 5. 1x DFET DSG Fall After SC

When using a minimal number of FETs (1–2) under increased battery pack voltages, that is, 48 V, and a short circuit occurs, the CSD19536KCS FETs Cgd capacitance requires an increase of approximately 220 pF in order to provide feedback to keep the gate on as it switches. Otherwise, the FET will jump on and off without being able to recover which eventually results in recovery or shorting of the FET depending on the amount of FETs used and their respective Cgd capacitance. Figure 7 shows the same configuration with 1xFET until it shorts and after the Cgd capacitance was increased, Figure 8 shows the elimination of the gate oscillation without sacrificing switching times.

However, when performing the same tests using the IRFB3207ZPBF FETs, the issue did not occur due to its lower input capacitance of about 6920 pF at 50 V compared to the CSD19536KCS 12000 pF at 50 V. Refer to your FET manufacturer's data sheet to determine ideal use.

The following schematic displays the Cgd capacitance addition.

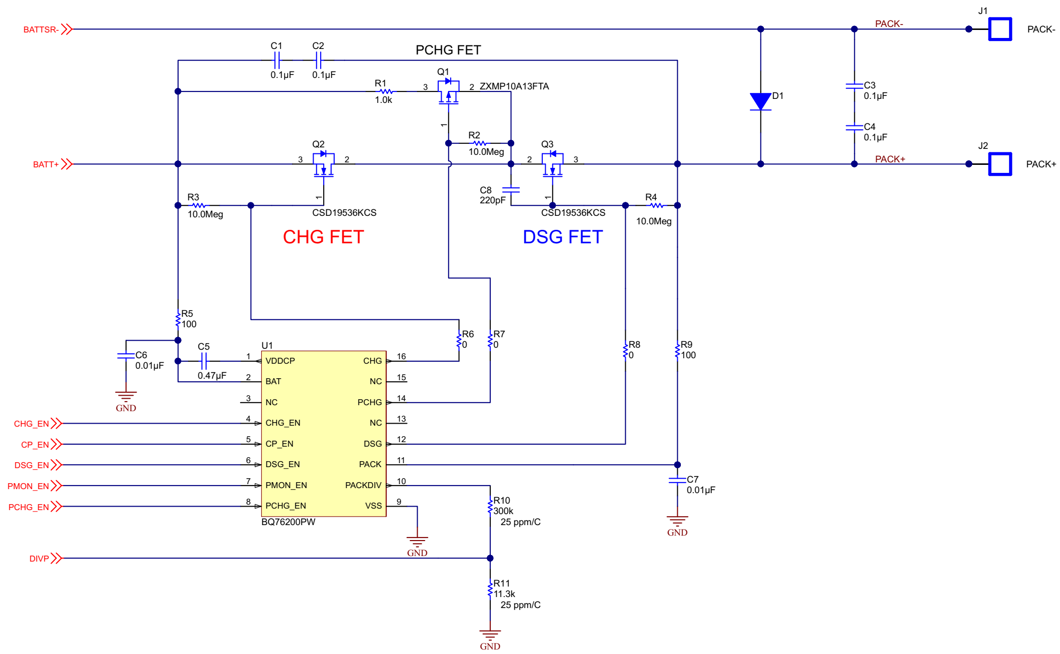


Figure 6. DSG FET With Added Cgd

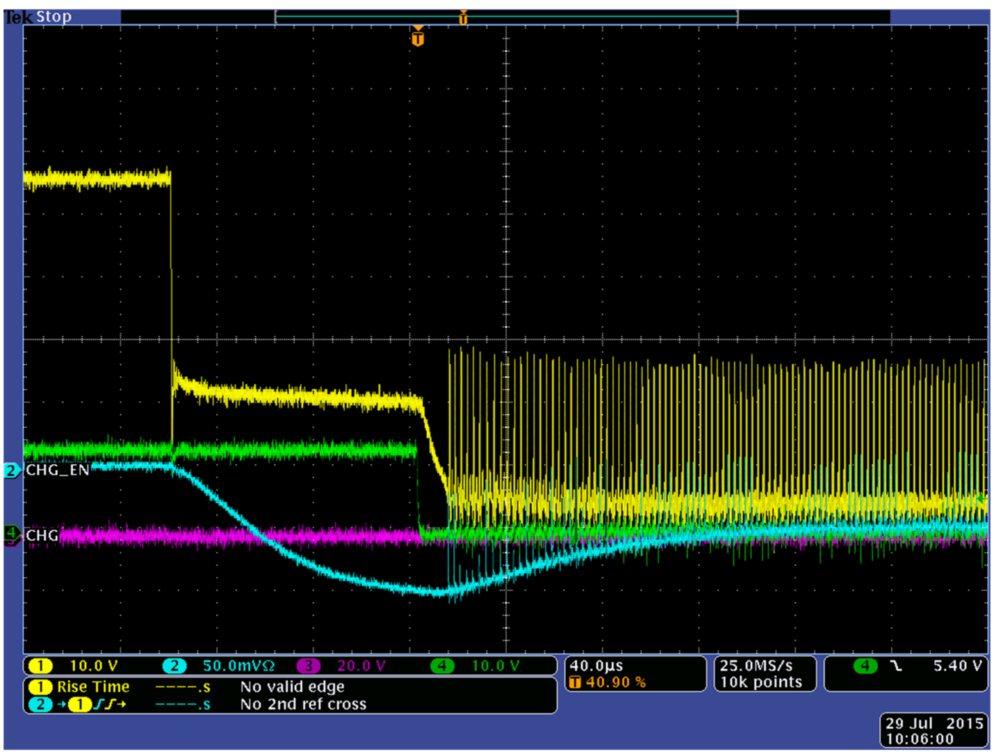


Figure 7. DSG Fall After SC Without Added Cgd

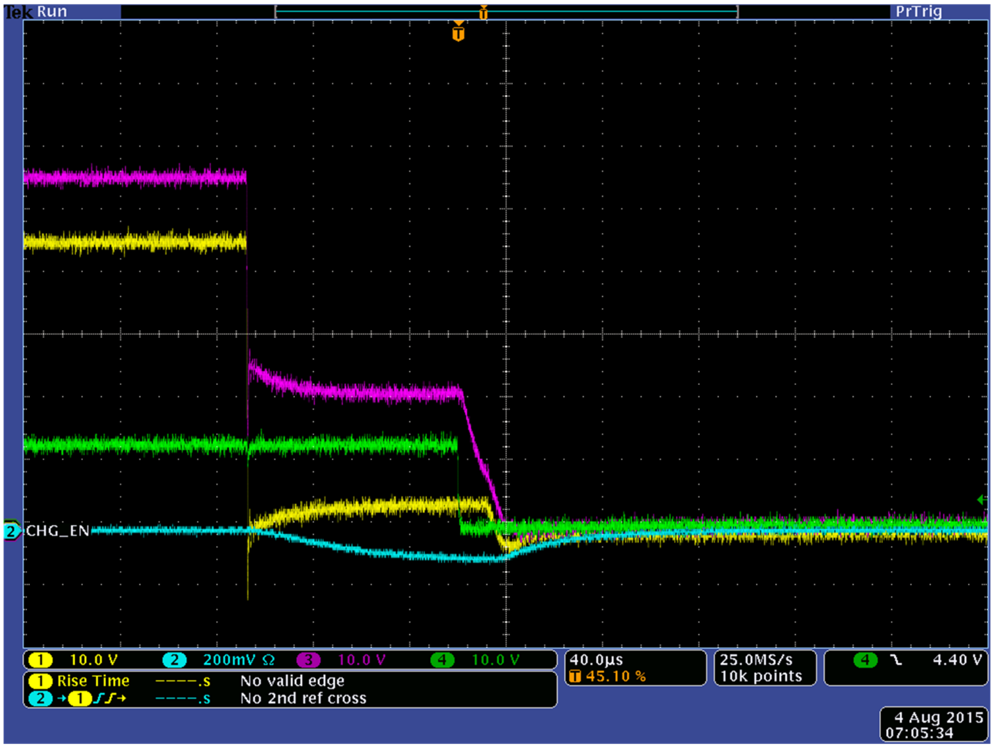


Figure 8. DSG Fall After SC With Added Cgd

4.2 2xCFET/2xDFET

FET Arrangement: 2 charge FETs (2xCFET), 2 discharge FETs (2xDFET) in series.

Table 3. 2xFET Configurations

AFE	# CHG FETs	# DSG FETs	PACK Voltage	# of Cells	FET Arrangement	VDDCP Capacitance
bq76920	2x	2x	10.8 V,14.4 V, 18 V	3, 4, 5	Series	1 µF
bq76930			24 V,36 V	6,10		
bq76940			36 V, 48 V	10, 13		

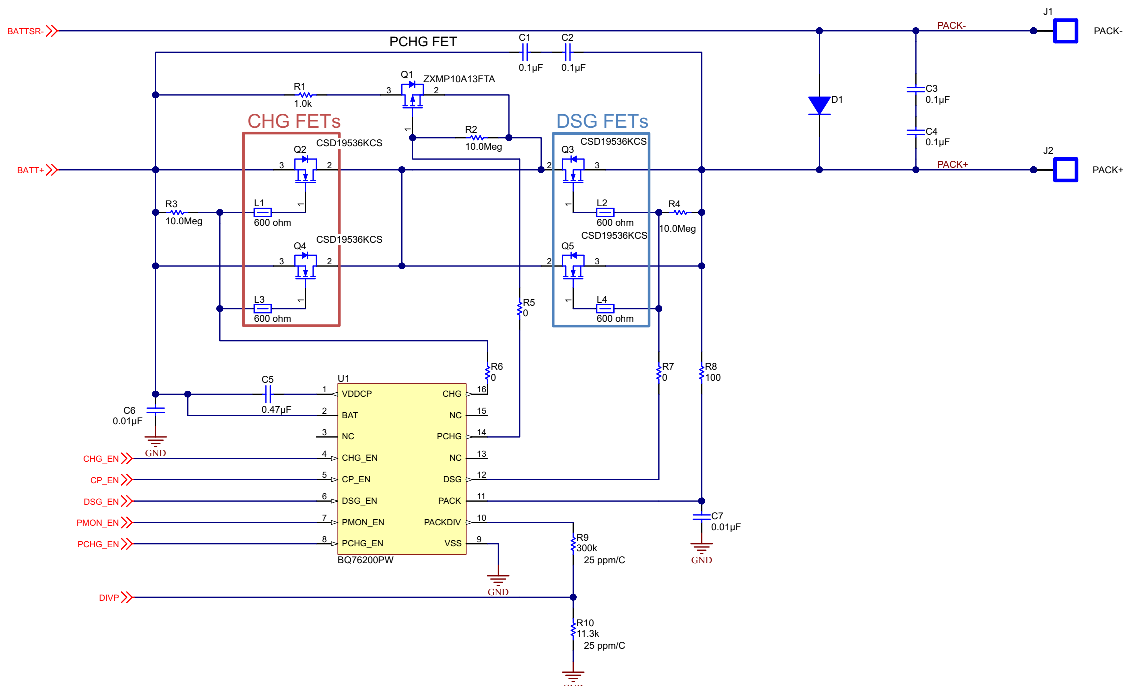


Figure 9. 2xCFET/2xDFET Schematic

NOTE: For configurations with multiple CHG or DSG FETs in parallel, 600-Ω ferrite beads were placed each FET gate in order to prevent parasitic oscillations.

Test: 10.8 V, 2xFETs, 3 cell, Undervoltage with a 2-A load.

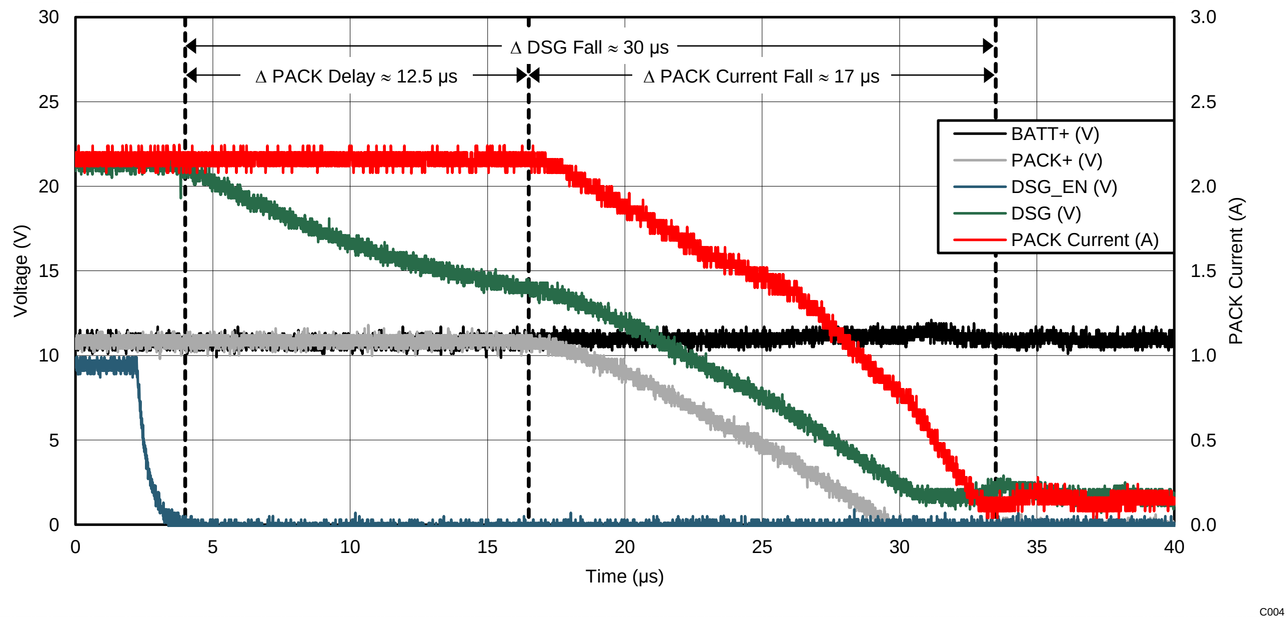


Figure 10. 2xDFET DSG Fall After Undervoltage of a Cell

Test: 10.8 V, 3 cell, Overvoltage of a cell when charging at 12.6 V (4.2 V a cell)

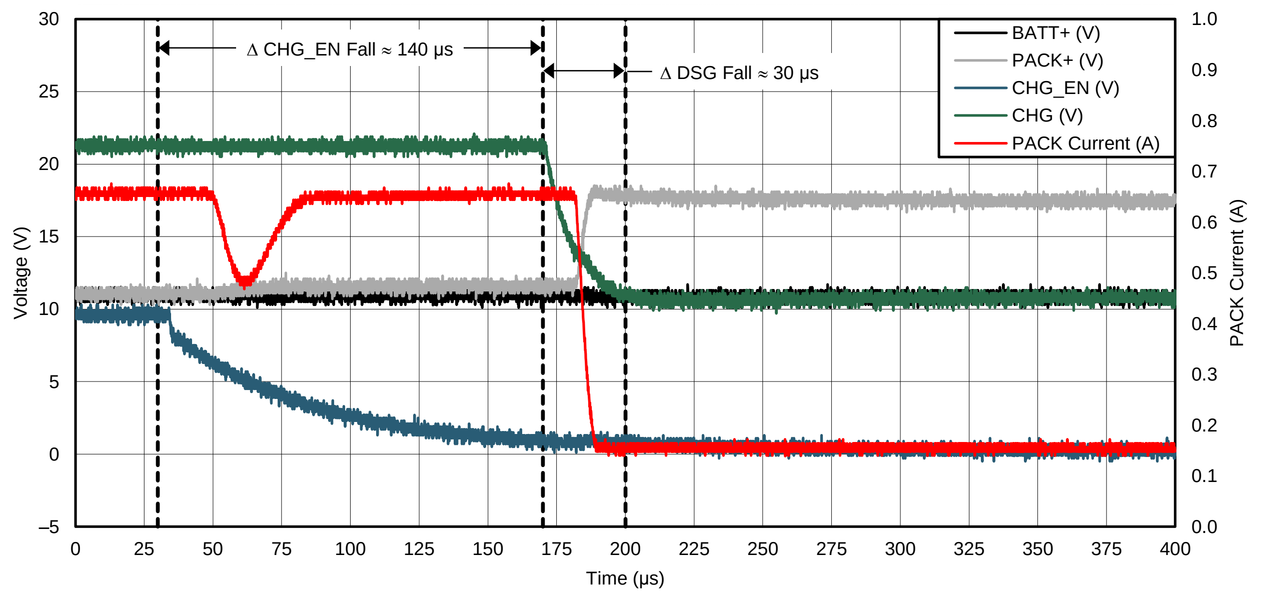


Figure 11. 2xCFET CHG Fall After Overvoltage of a Cell

Test: 10.8 V, 2xFETs, 3 cell, short circuit

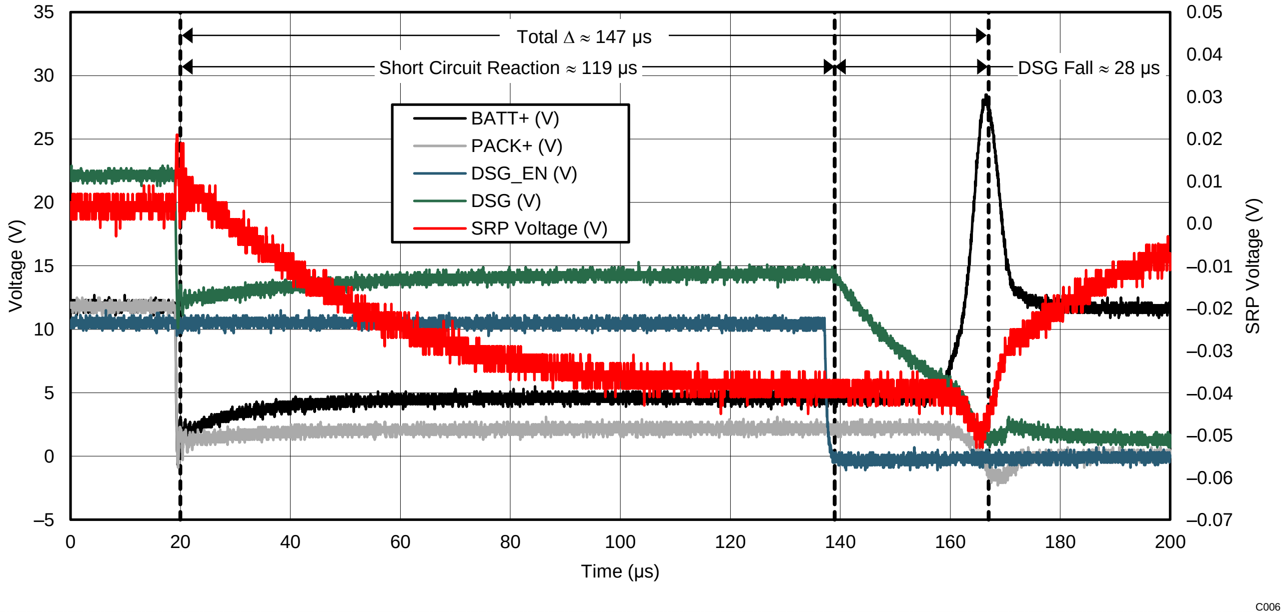


Figure 12. 2xDFET DSG Fall After Short Circuit Occurs

4.3 4xCFET/4xDFET

FET Arrangement: 4 charge FETs (4xCFET), 4 discharge FETs (4xDFET)

Table 4. 4xFET Configurations

AFE	# CHG FETs	# DSG FETs	PACK Voltage	# of Cells	FET Arrangement	VDDCP Capacitance
bq76920	4x	4x	14.4 V, 18 V	4, 5	Parallel	2.2 µF
bq76930			24 V,36 V	6,10	Parallel	
bq76940			36 V, 48 V	10, 13	Series	

NOTE: When using multiple CHG or DSG FETs in parallel with one another, refer to the VDDCP Capacitance Reference table in order to implement a VDDCP capacitance size necessary for the user's application.

Parallel Configuration

The user may want to configure the CHG and DSG FETs in a parallel configuration in order to support separate charge paths for CHG and DSG. However, this creates a CHG PACK+ path separate from the PACK+ path for the DSG FETs that can manage the voltage level by the PACKDIV feature so the initial intention of the PCHG FET would only be useful for PDSG. Though, these separate CHG and DSG paths do allow the user to support applications with a differing number of CHG and DSG FETs. The following schematic details an ideal setup and construction when utilizing the parallel FET configuration.

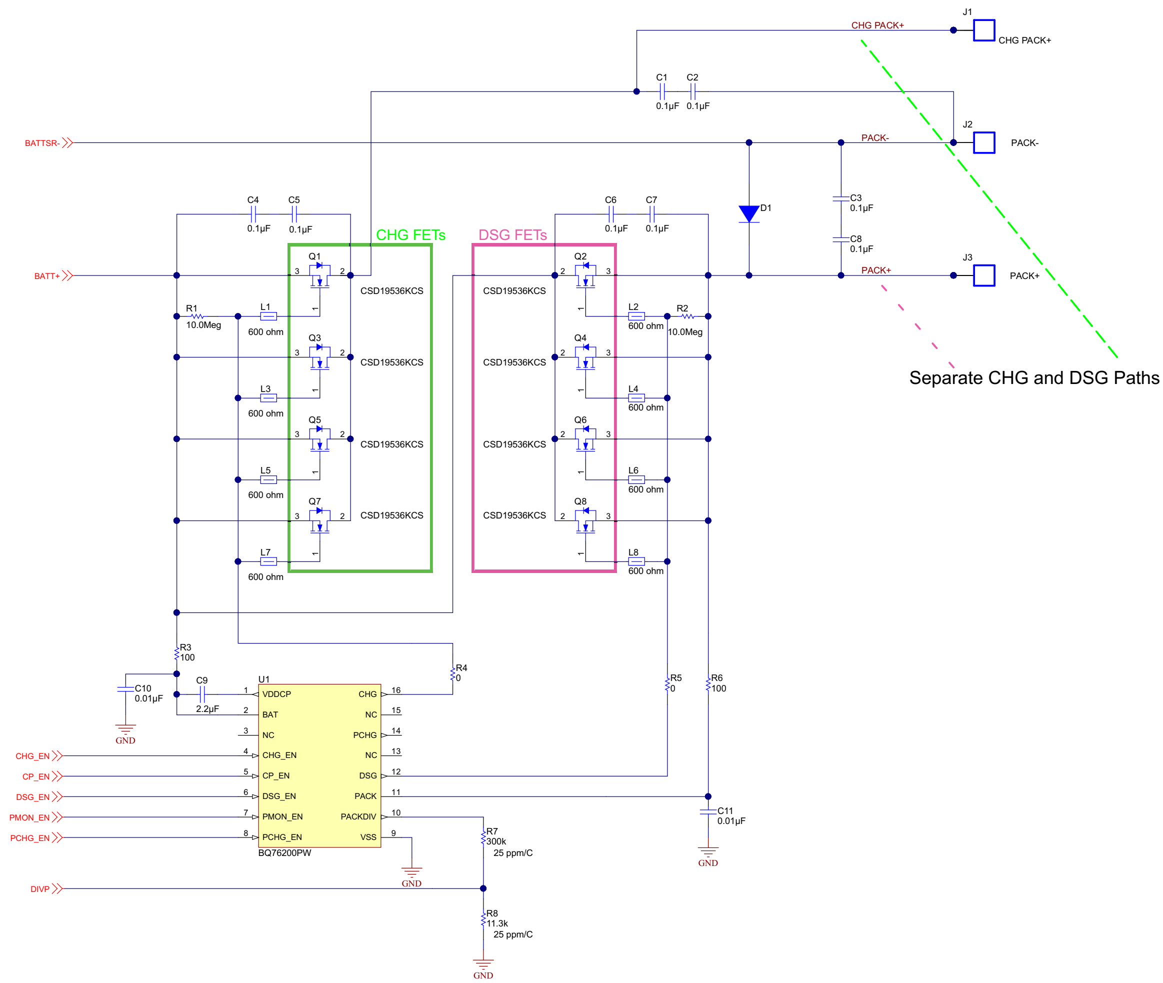


Figure 13. 4xCFETs and 4xDFETs in Parallel

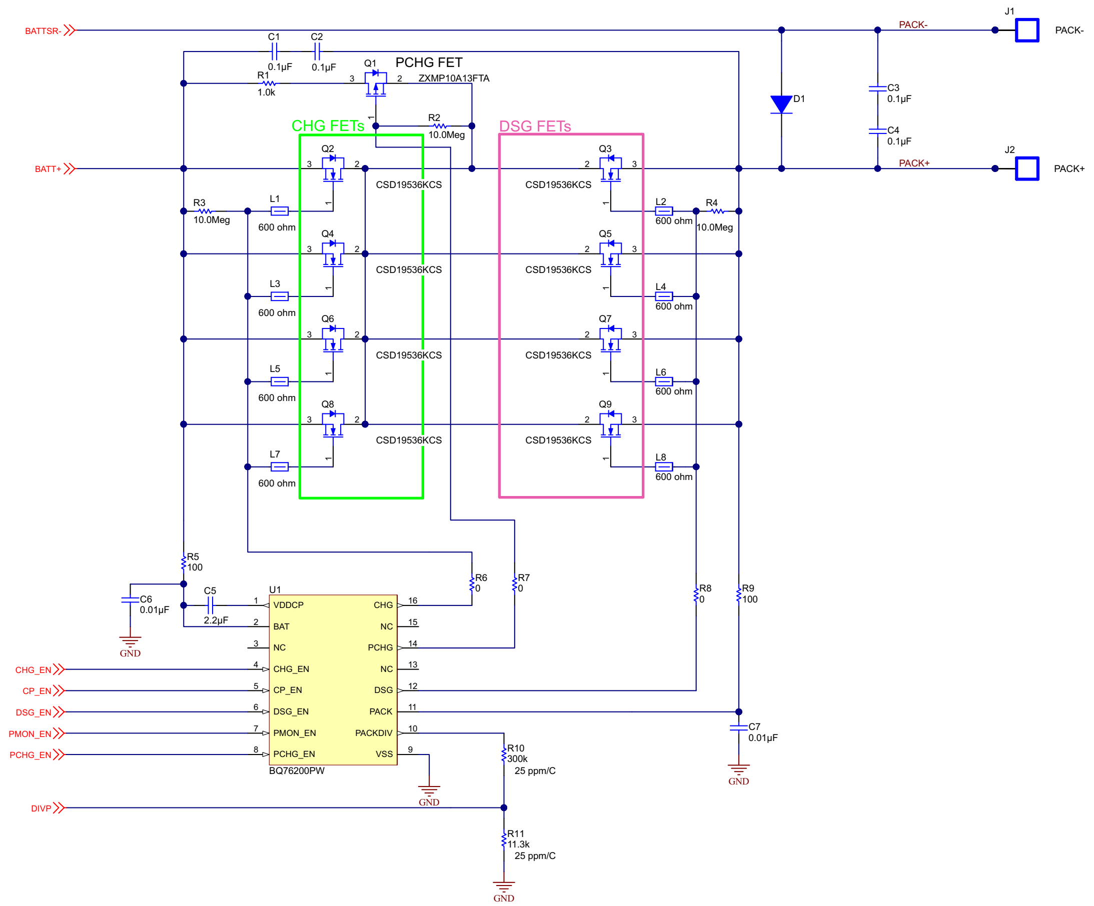


Figure 14. 4xCFETs and 4xDFETs in Series

Test: 36 V, 4xFETs, 10 cells, Undervoltage of a cell with a load of approximately 4 A.

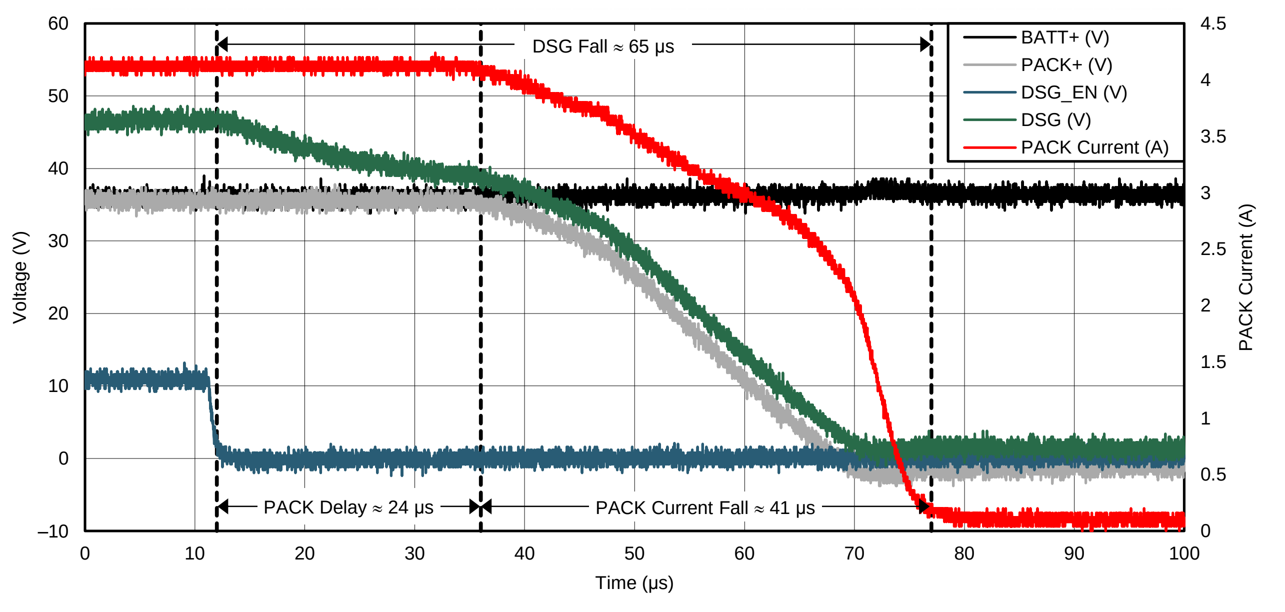


Figure 15. 4xDFET DSG Turn-Off After UV

Test: 36 V, 4xFETs, 10 cell, Overvoltage of a cell when charging at 42 V (4.2 V per cell)

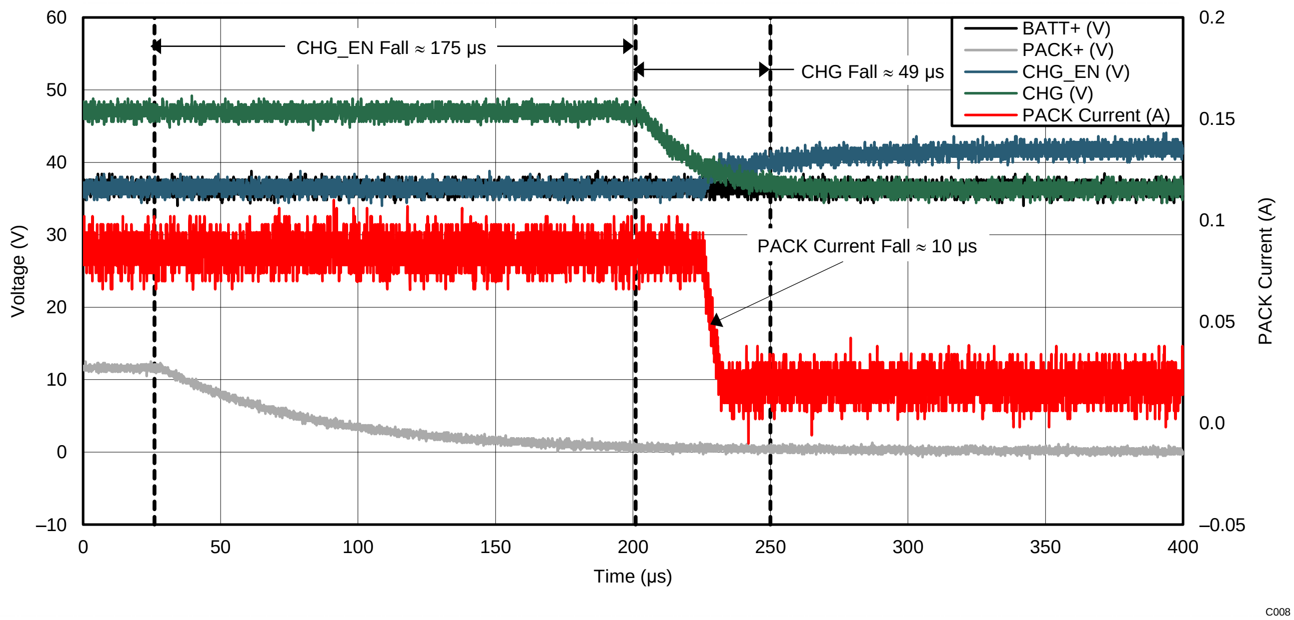


Figure 16. 4xCFET CHG Turn-Off After OV

Test: 36 V, 4xFETs, 10 cell, Short circuit

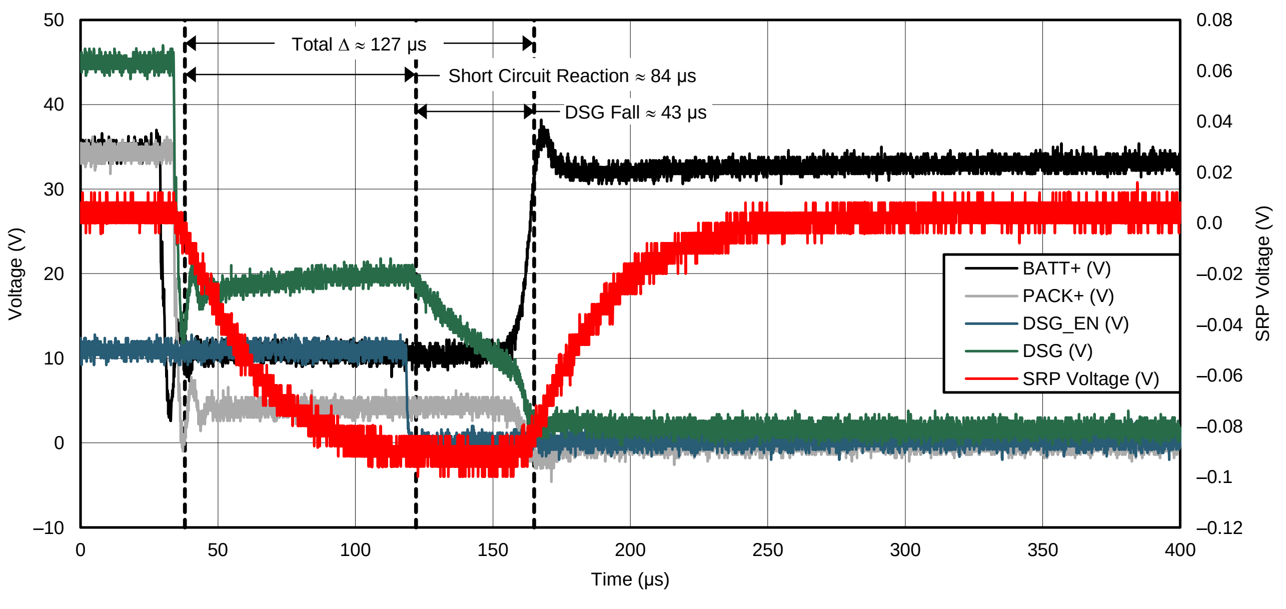


Figure 17. 4xDFET DSG Turn-Off After SC

4.4 4xCFET/8xDFET

FET Arrangement: 4 charge FETs (4xCFET), 8 discharge FETs (8xDFET) in parallel.

Table 5. 4x8xFET Configurations

AFE	# CHG FETs	# DSG FETs	PACK Voltage	# of Cells	FET Arrangement	VDDCP Capacitance
bq76920	4x	8x	14.4 V, 18 V	4, 5	Parallel	2.2 µF
bq76930			24 V,36 V	6,10		
bq76940			36 V, 48 V	10, 13		

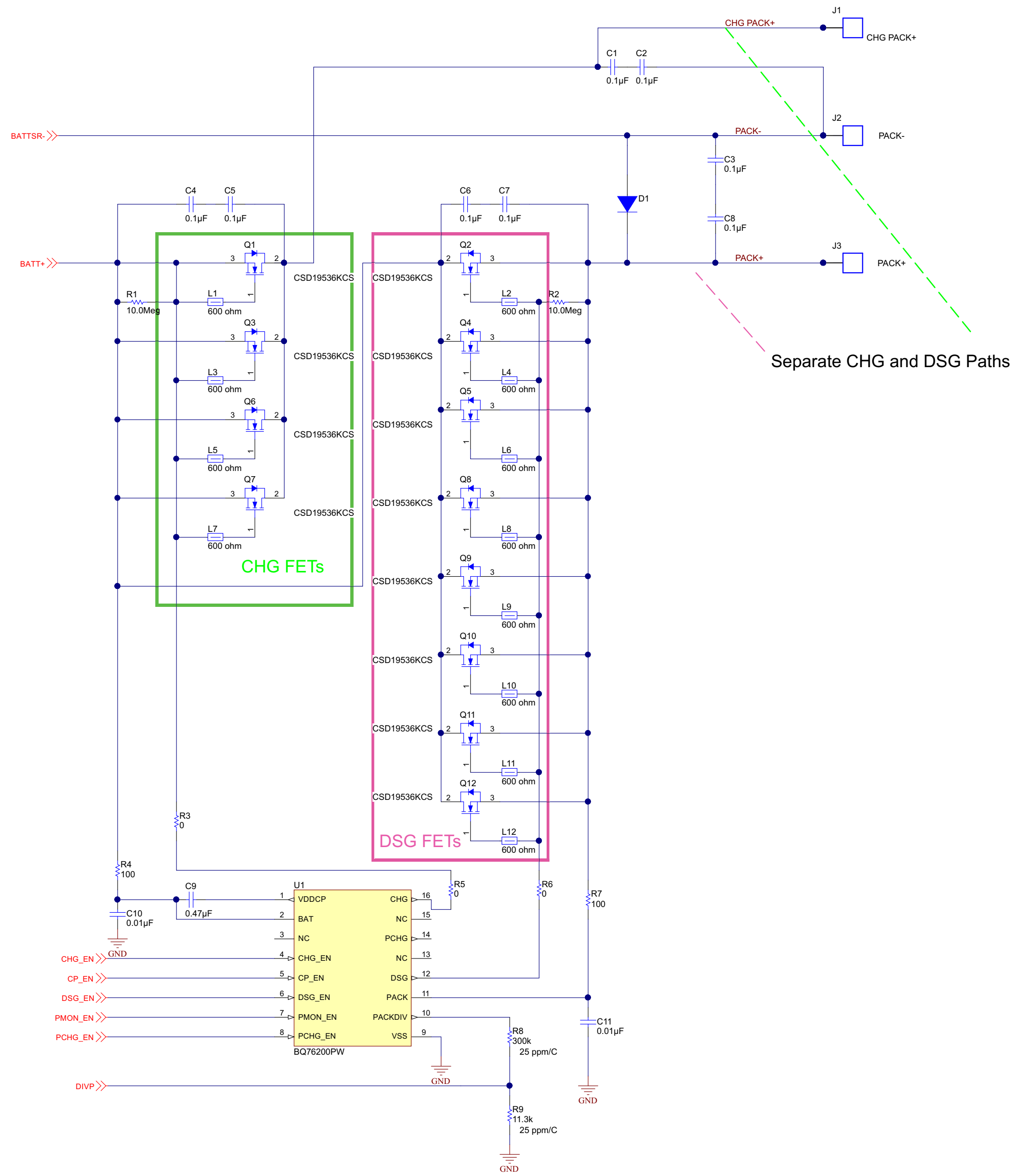


Figure 18. 4xCFETs and 8xDFETs in Parallel

4.5 4xCFET/12xDFET

FET Arrangement: 4 charge FETs (4xCFET), 12 discharge FETs (12xDFET) in parallel.

Table 6. 4x12xFET Configurations

AFE	# CHG FETs	# DSG FETs	PACK Voltage	# of Cells	FET Arrangement	VDDCP Capacitance
bq76940	4x	12x	36 V, 48 V	10, 13	Parallel	4.7 µF

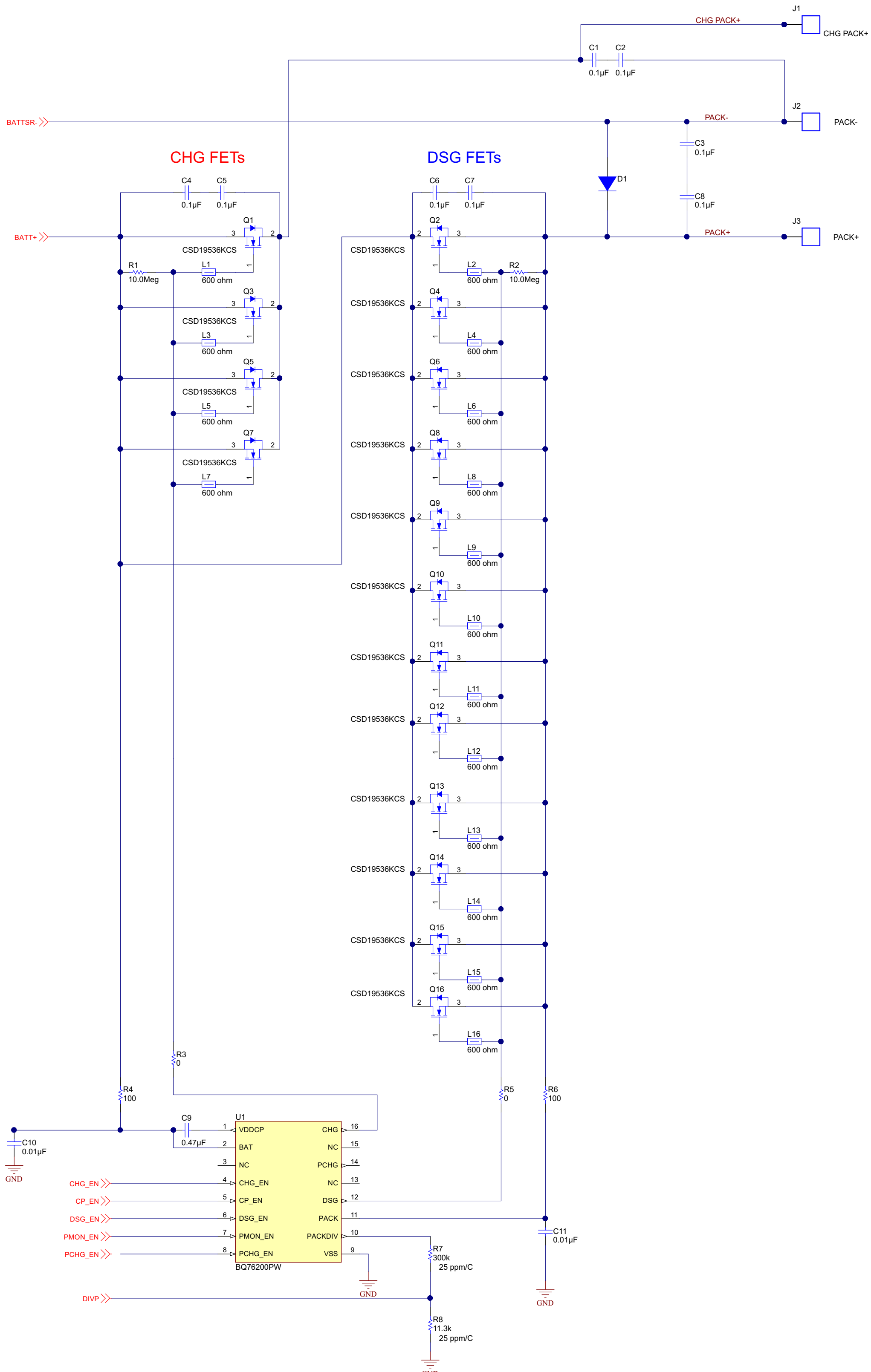


Figure 19. 4xCFETs and 12xDFETs in Parallel

NOTE: The 4x8x and 4x12x parallel configurations show no substantial differences from the series test for the same number of FETs. This is expected as the parallel configuration simply allows differing CHG and DSG FET numbers. The following references to other figures display the functionality of these configurations.

4x8x UV test, refer to Figure 21
4x8x OV test, refer to Figure 16
4x8x SC test, refer to Figure 25
4x12x UV test, refer to Figure 32
4x12x OV test, refer to Figure 16
4x12x SC test, refer to Figure 34

4.6 8xCFET/8xDFET

FET Arrangement: 8 charge FETs (8xCFET), 8 discharge FETs (8xDFET) in series.

Table 7. 8xFET Configurations

AFE	# CHG FETs	# DSG FETs	PACK Voltage	# of Cells	FET Arrangement	VDDCP Capacitance
bq76920	8x	8x	14.4 V, 18 V	4, 5	Series	4.7 µF
bq76930			24 V,36 V	6,10	Series	
bq76940			36 V, 48 V, 54 V	10, 13, 15	Series	
bq76940			48 V	13	Pre-Discharge	
bq76920			18 V	5	Pre-Discharge	

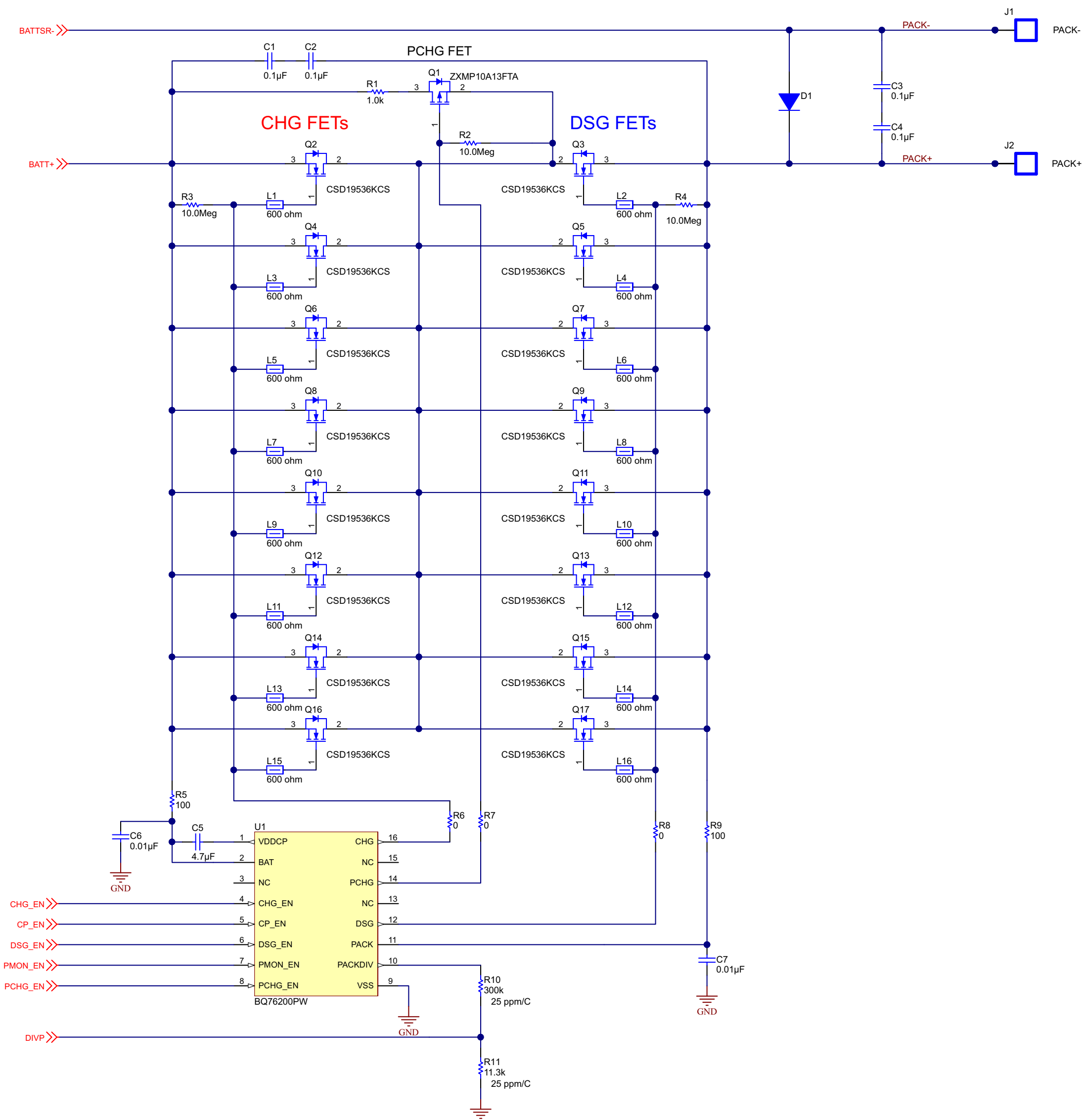


Figure 20. 8xCFET/8xDFET Schematic

Test: 48 V, 8xFETs, 13 cells, Undervoltage of a cell with a load of approximately 8 A

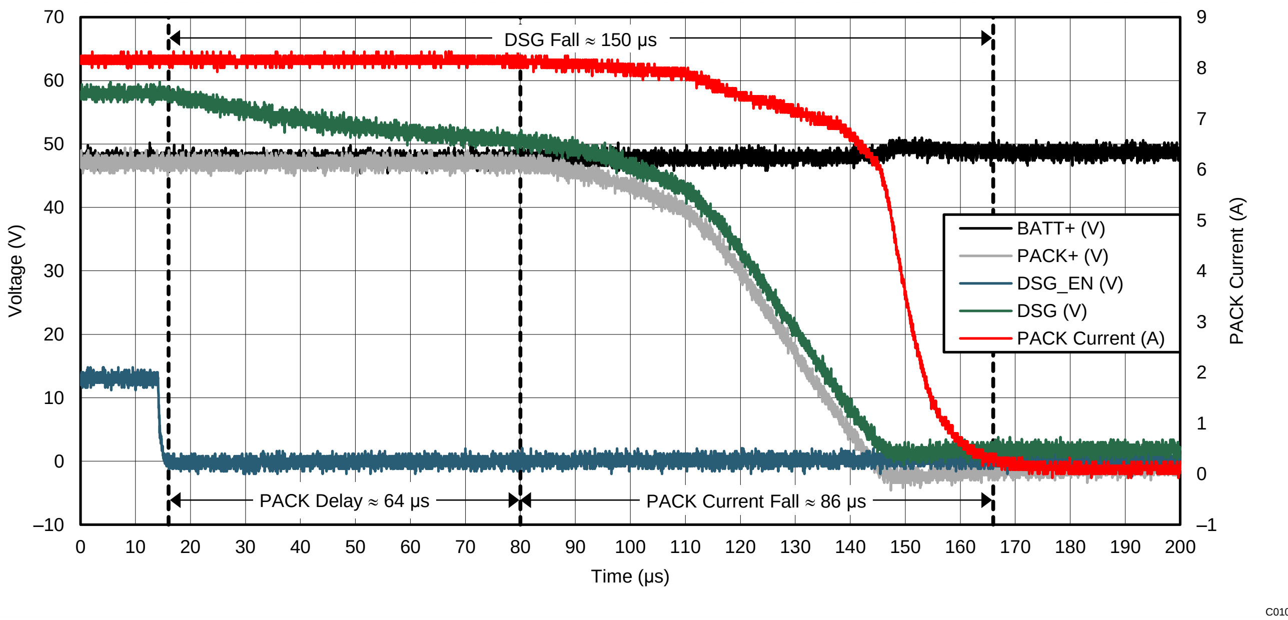


Figure 21. 8xDFET DSG Turn-Off After UV

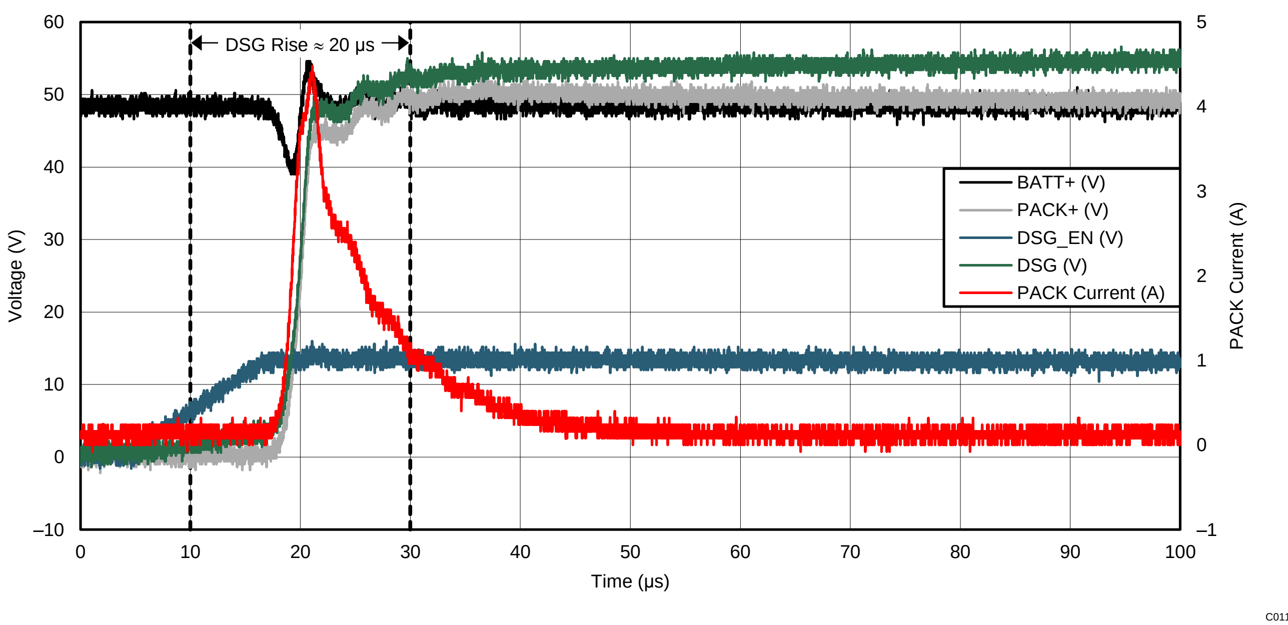


Figure 22. 8xDFET DSG Turn-On After UV Recovery

NOTE: The longer delays in the PACK current recovery from an undervoltage or overvoltage is a result of an instrument response time of the Kikusui PLZ1004W Electronic Load. PACK eventually rises approximately5ms later in this setup, and will rise quickly as expected when referenced through a resistor.

Test: 48 V, 8xFETs, 10 cell, Overvoltage of a cell when charging at 54.6 V (4.2 V per cell)

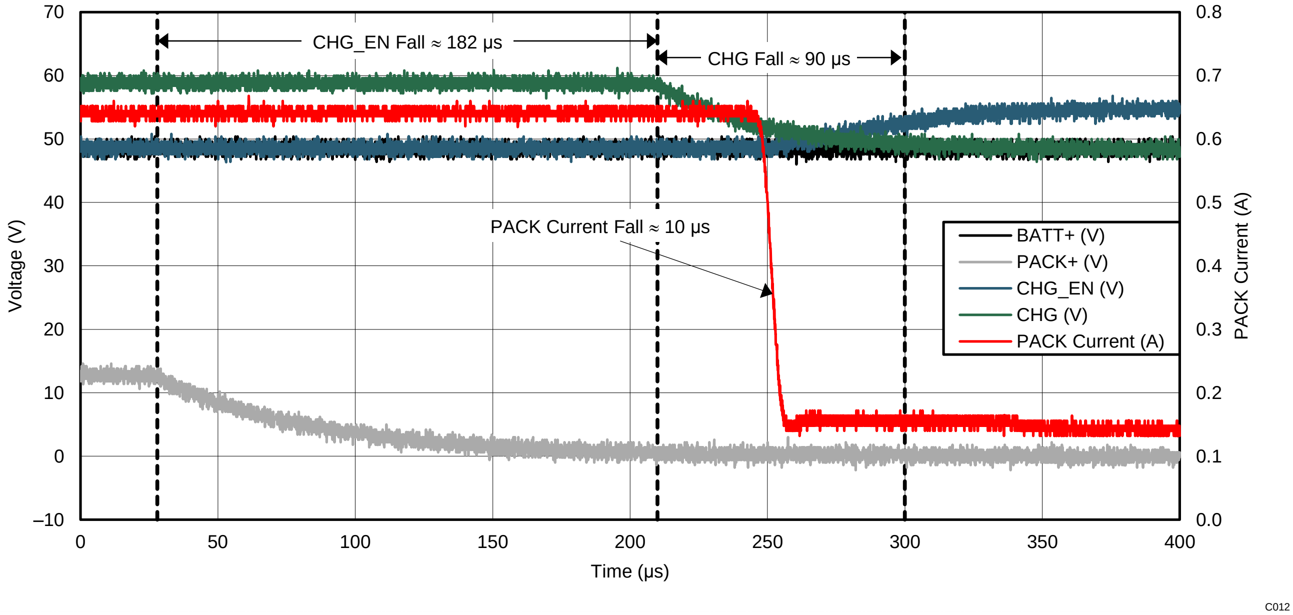


Figure 23. 8xCFET CHG Turn-Off After OV

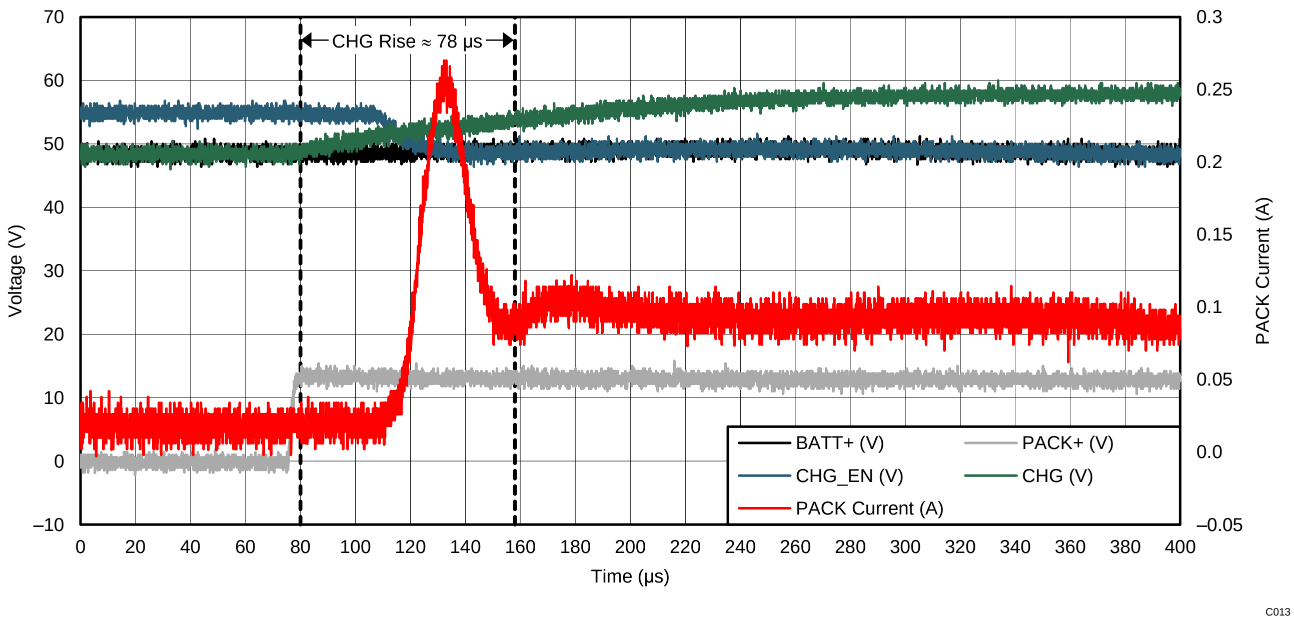


Figure 24. 8xCFET CHG Turn-On After OV Recovery

Test: 48 V, 8xFETs, 13 cell, Short circuit

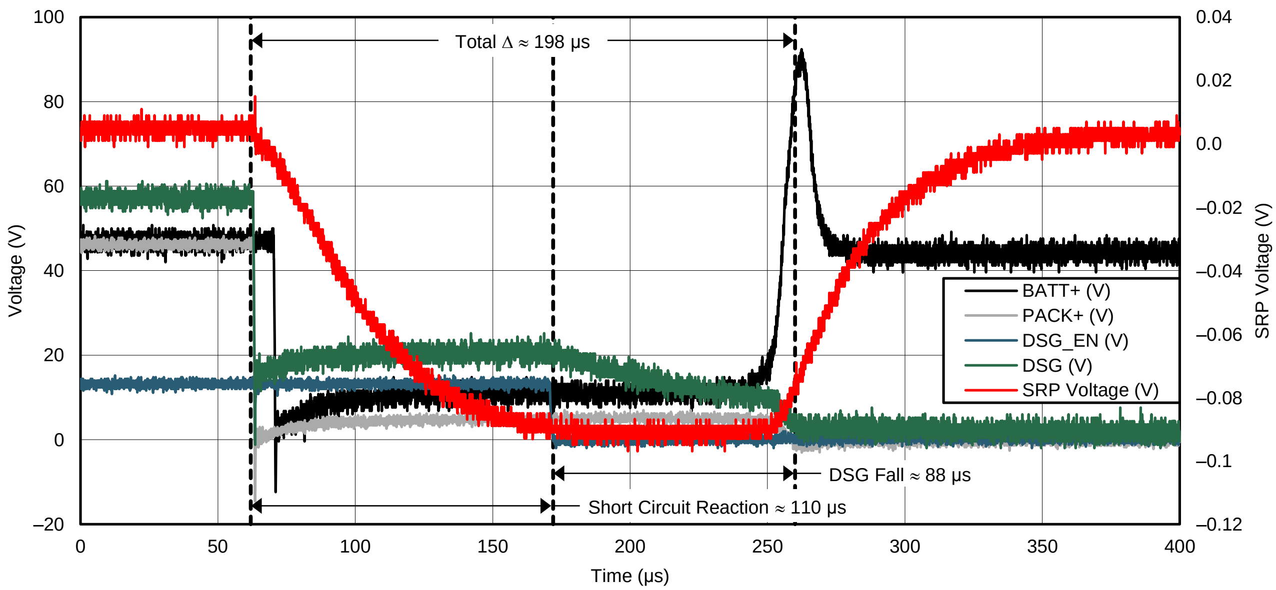


Figure 25. 8xDFET DSG Turn-Off After SC

NOTE: The following tests are displayed to show the differences between the switching times across consistent FET amounts, but a changed PACK voltage. The change is fairly minimal as opposed to increasing FETs which has a much more profound delay.

Test: 54 V, 8xFETs, 15 cells, Undervoltage of a cell with a load of approximately 8A

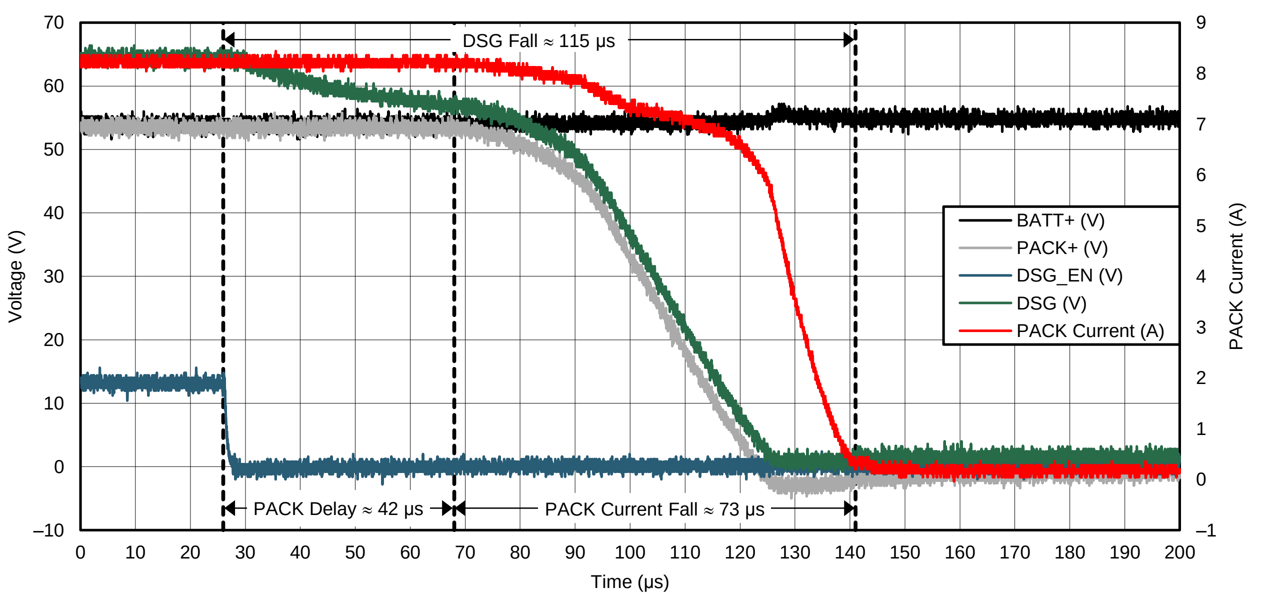


Figure 26. 8xDFET DSG Turn-Off After UV

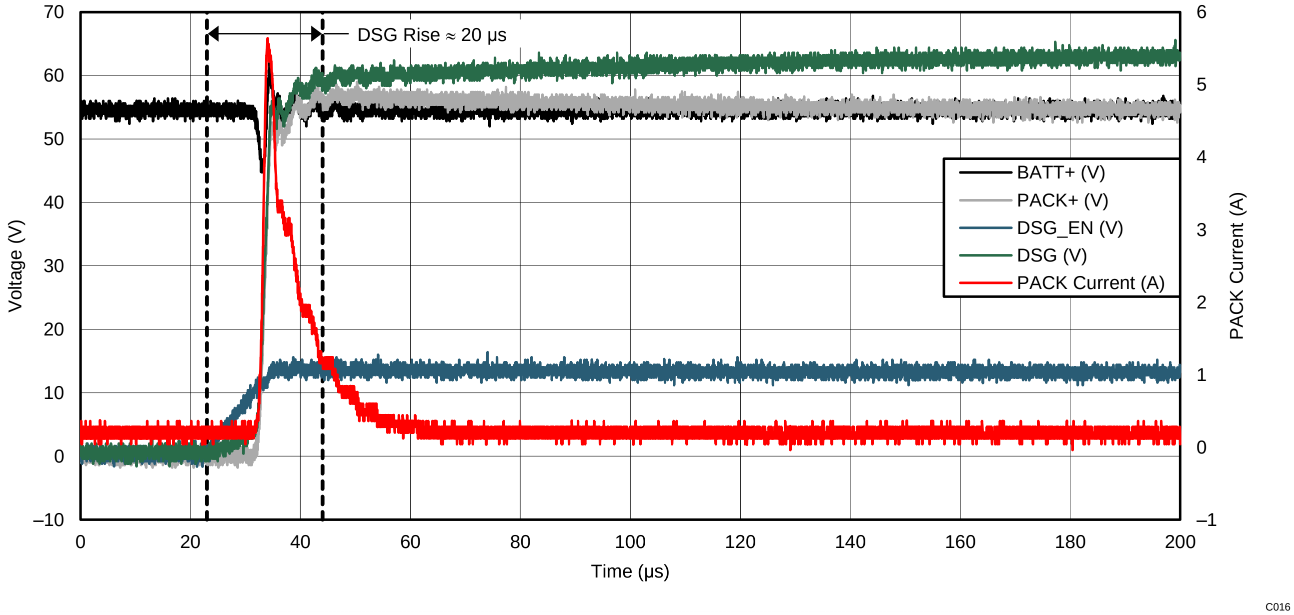


Figure 27. 8xDFET DSG Turn-On After UV Recovery

Test: 54 V, 8xFETs, 15 cell, Overvoltage of a cell when charging at 63 V (4.2 V per cell)

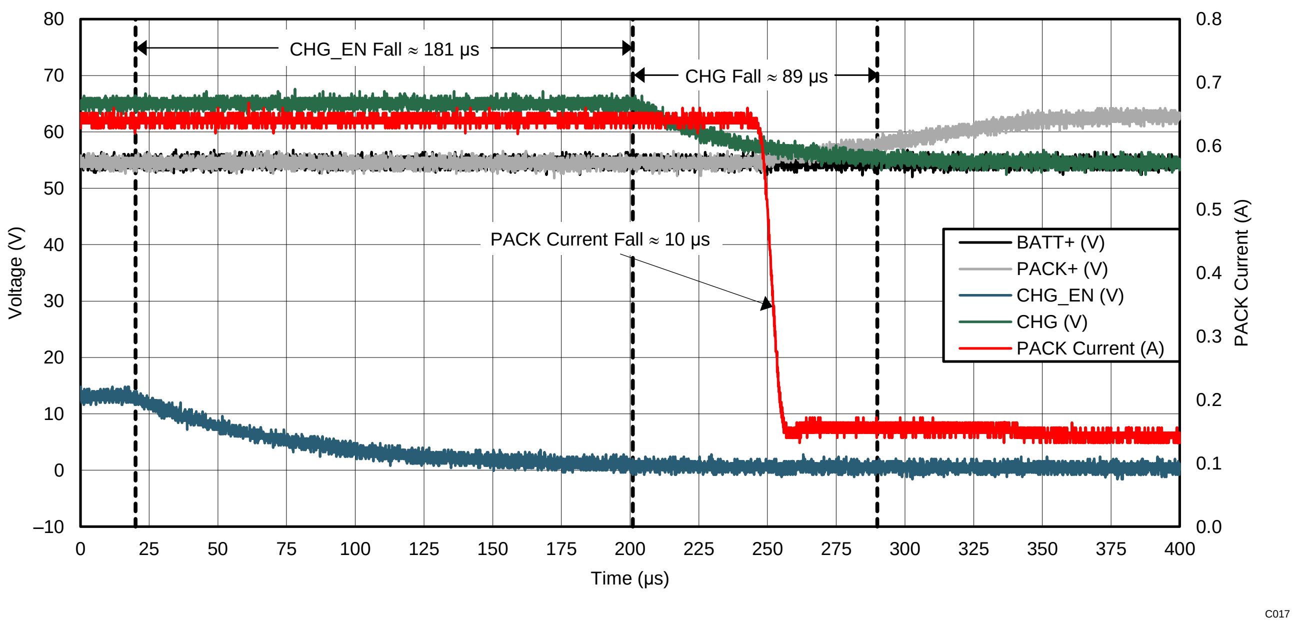


Figure 28. 8xCFET CHG Turn-Off After OV

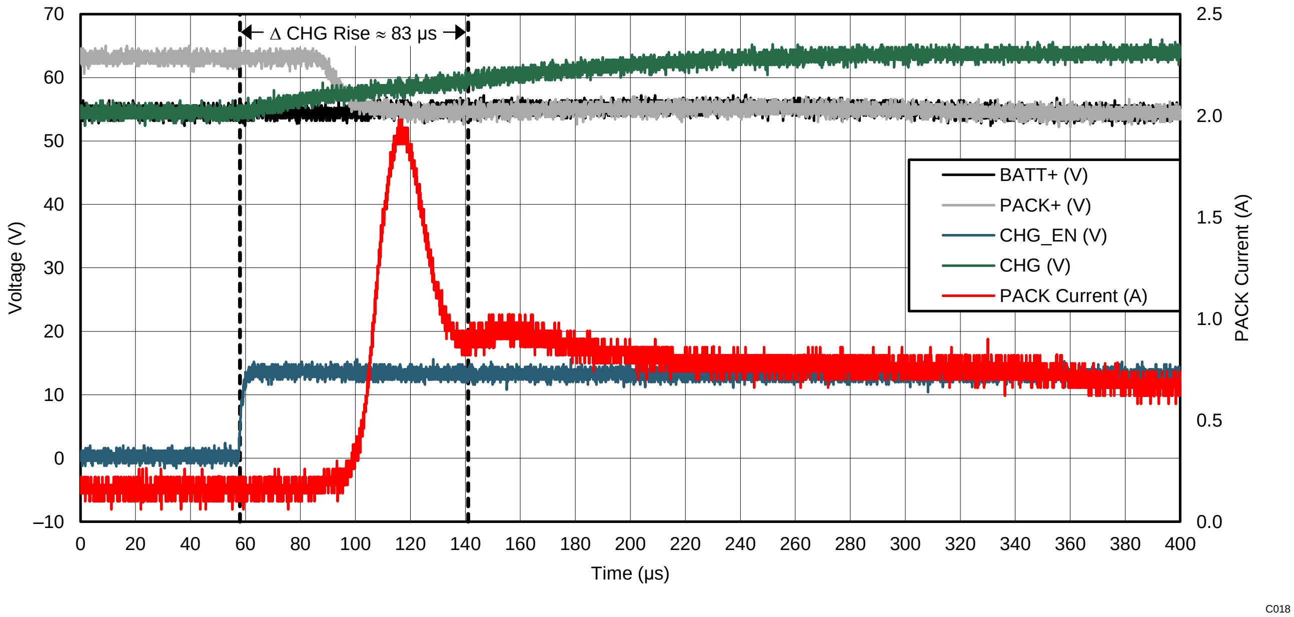


Figure 29. 8xCFET CHG Turn-On After OV Recovery

Test: 54 V, 8xFETs, 15 cell, Short circuit

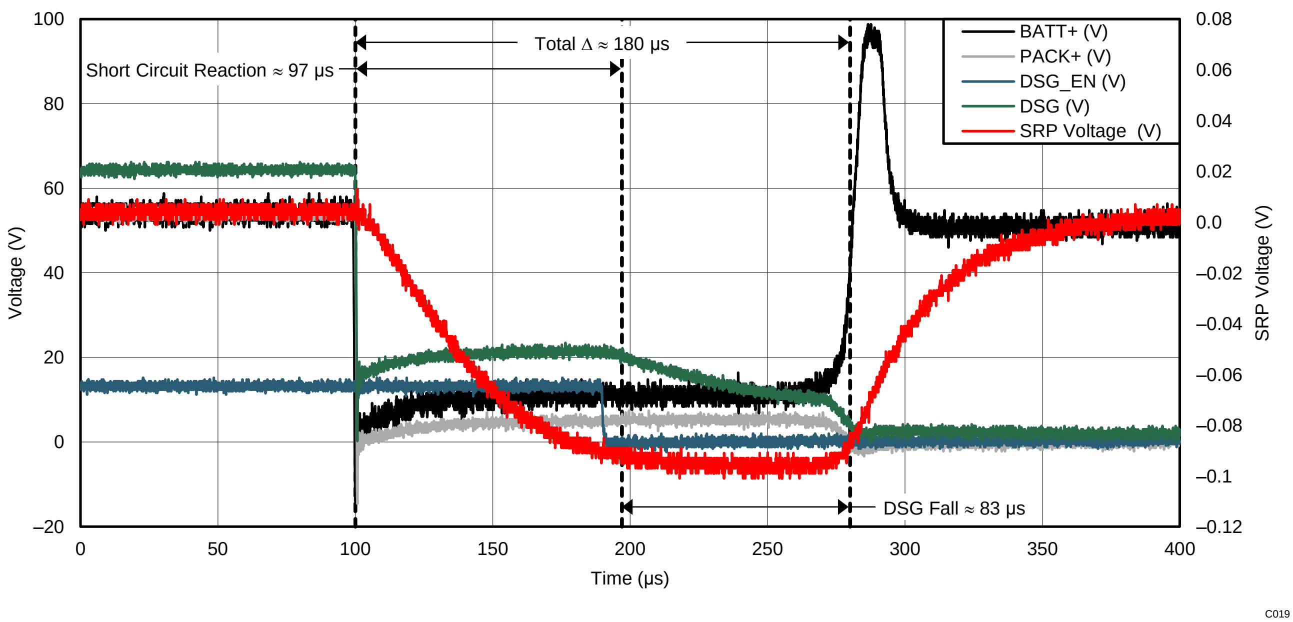


Figure 30. 8xDFET DSG Turn-Off After SC

4.7 12xCFET/12xDFET

FET Arrangement: 12 charge FETs (12xCFET), 12 discharge FETs (12xDFET) in series.

Table 8. 12xFET Configurations

AFE	# CHG FETs	# DSG FETs	PACK Voltage	# of Cells	FET Arrangement	VDDCP Capacitance
bq76940	12x	12x	36 V, 48 V	10, 13	Series	4.7 µF

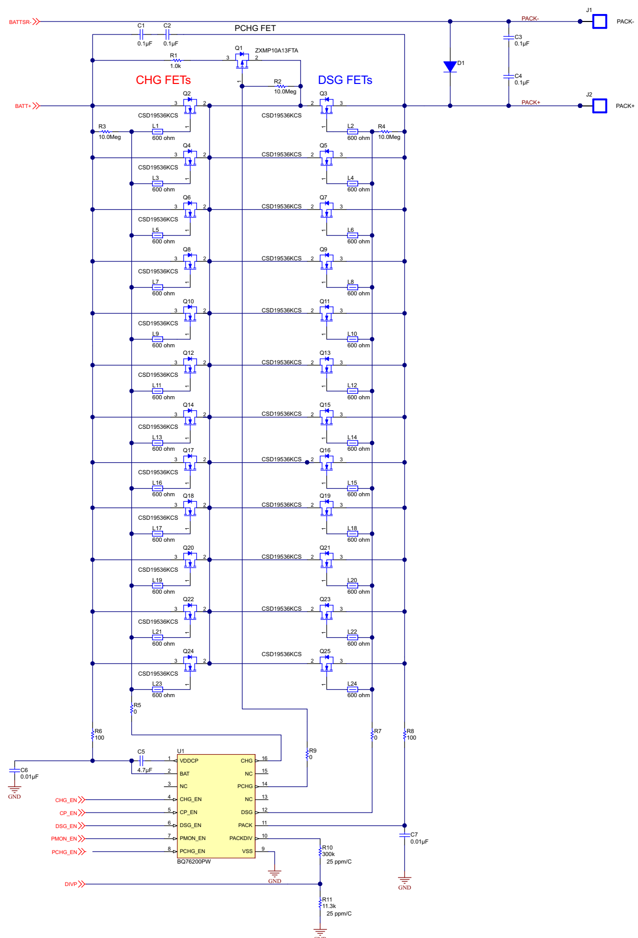


Figure 31. 12xCFET/12xDFET Schematic

Test: 48 V, 12xFETs, 13 cells, Undervoltage of a cell with a load of approximately 10 A

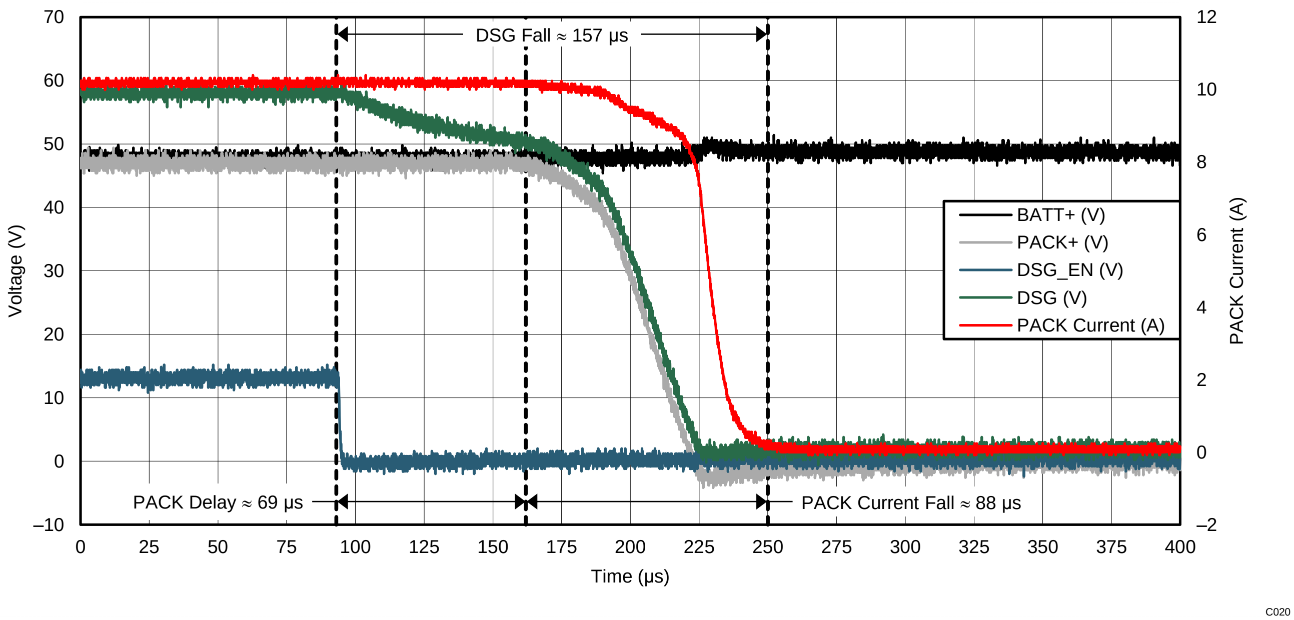


Figure 32. 12xDFET DSG Turn-Off After UV

Test: 48 V, 12xFETs, 13 cell, Overvoltage of a cell when charging at 54.6 V (4.2 V per cell)

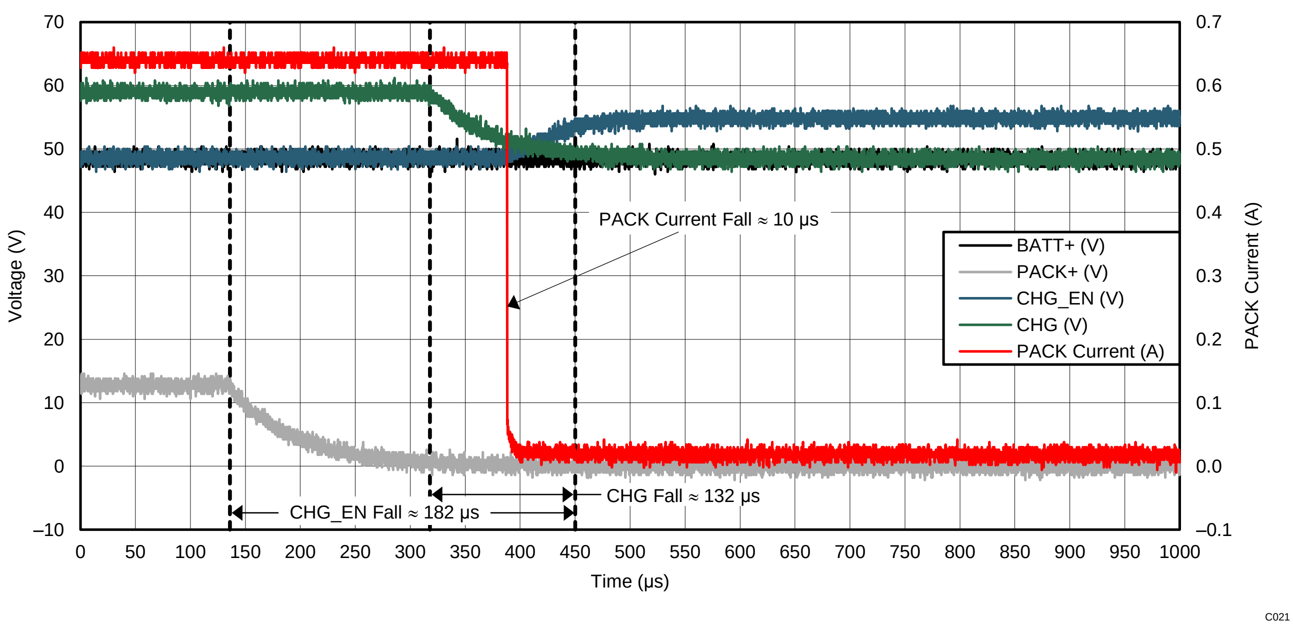


Figure 33. 12xCFET CHG Turn-Off After OV

Test: 48 V, 12xFETs, 13 cell, Short circuit

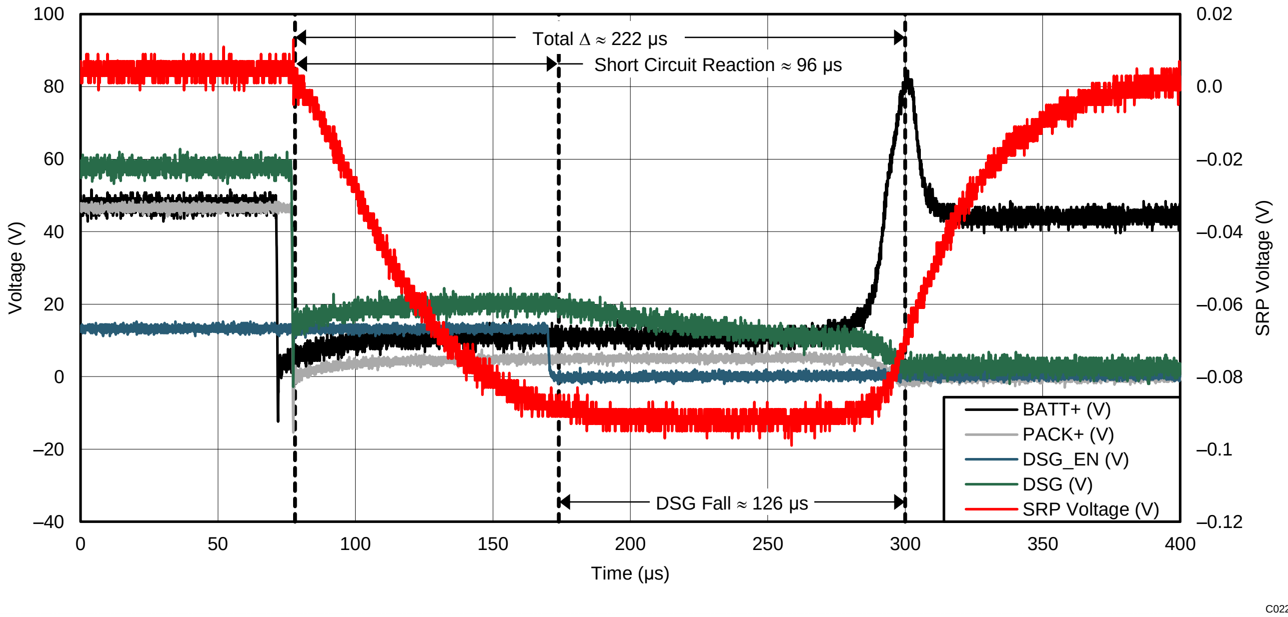


Figure 34. 12xDFET DSG Turn-Off After SC

5 Pre-Discharge

Table 9. Pre-Discharge Configurations

AFE	# CHG FETs	# DSG FETs	PACK Voltage	# of Cells	FET Arrangement	VDDCP Capacitance
bq76940	8x	8x	48 V	13	Series	4.7 µF
bq76920			18 V	5	Series	

When attempting to connect the battery in systems where the load has an extremely high capacitance, the battery may short circuit and attempt to recover, resulting in DSG failing to switch on and PACK spiking to a low voltage which slowly dissipates in the load resistance and repeats the cycle. Figure 37 portrays this behavior when the bq76200 attempts to switch DSG on. After some time, PACK may slowly increase its initial voltage spike to a point where DSG may turn on but that is situationally unreliable.

In order to avoid this problem, consider using a pre-discharge FET in order to slowly push PACK and DSG into their normal operating voltage. The following schematic displays the use of the PDSG FET and how it can be implemented within an 8xDFET configuration in systems where the bq76200 PCHG function is not needed for battery precharge. Figure 39 shows PDSG turn on and the effect it has on resolving the PACK and DSG turn on.

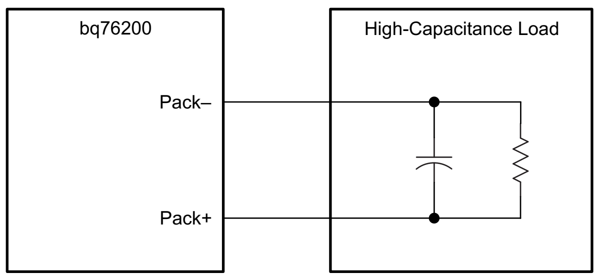


Figure 35. Battery with High Capacitive Load

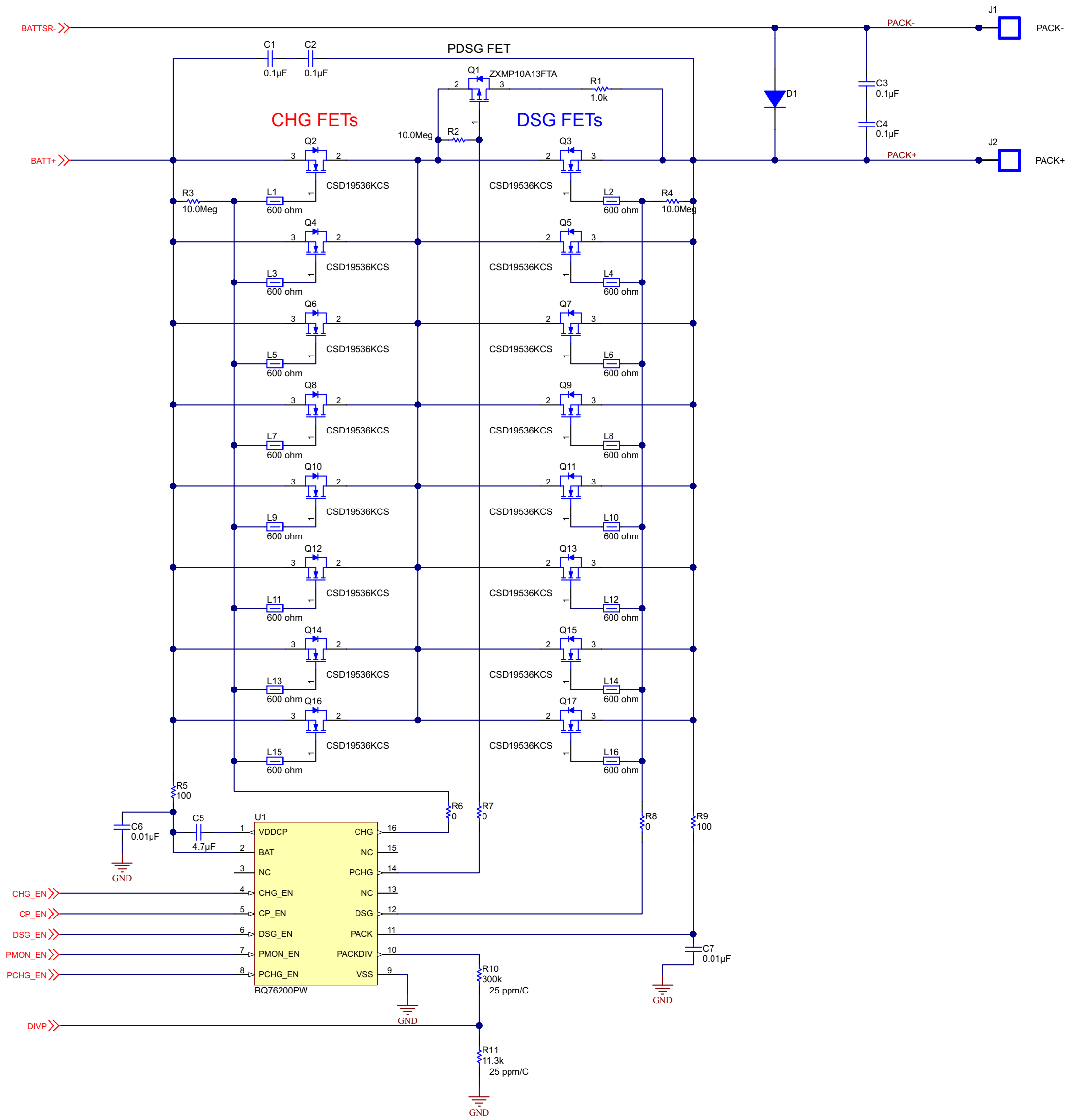


Figure 36. Pre-Discharge Schematic

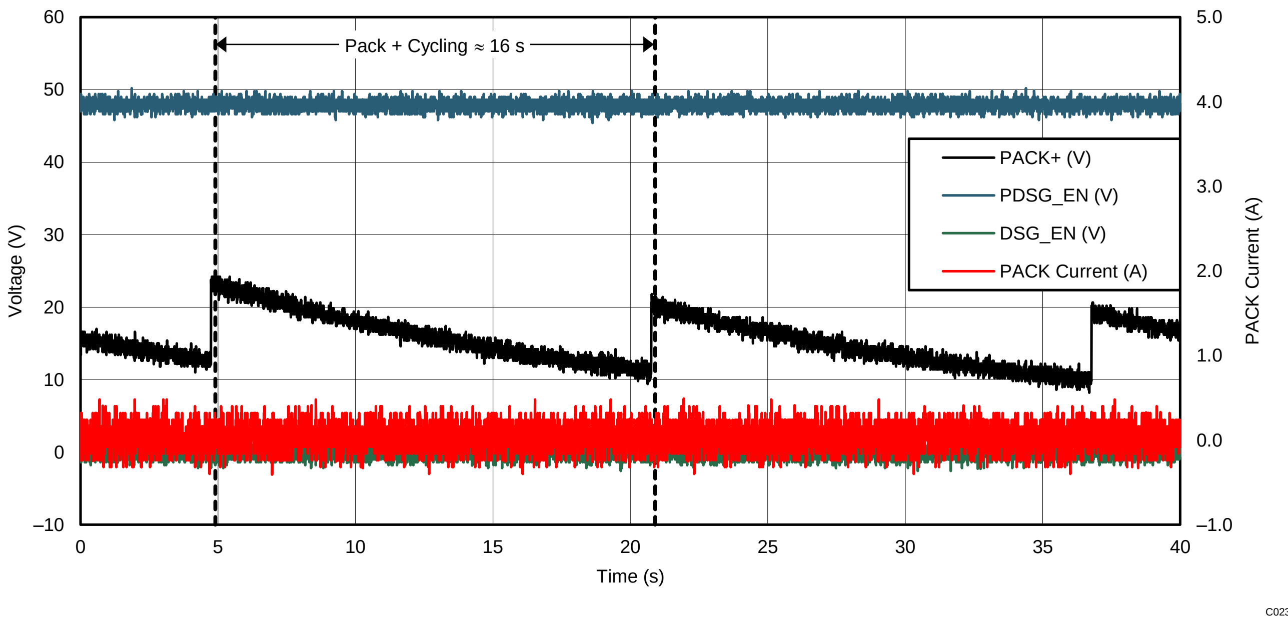


Figure 37. Capacitive Load DSG Spike and Current Spike

NOTE: The oscilloscope could not capture the rapid jump of DSG_EN and pack current which occurs exactly as the PACK begins a new cycle of dissipating. Figure 38 shows the spike zoomed in.

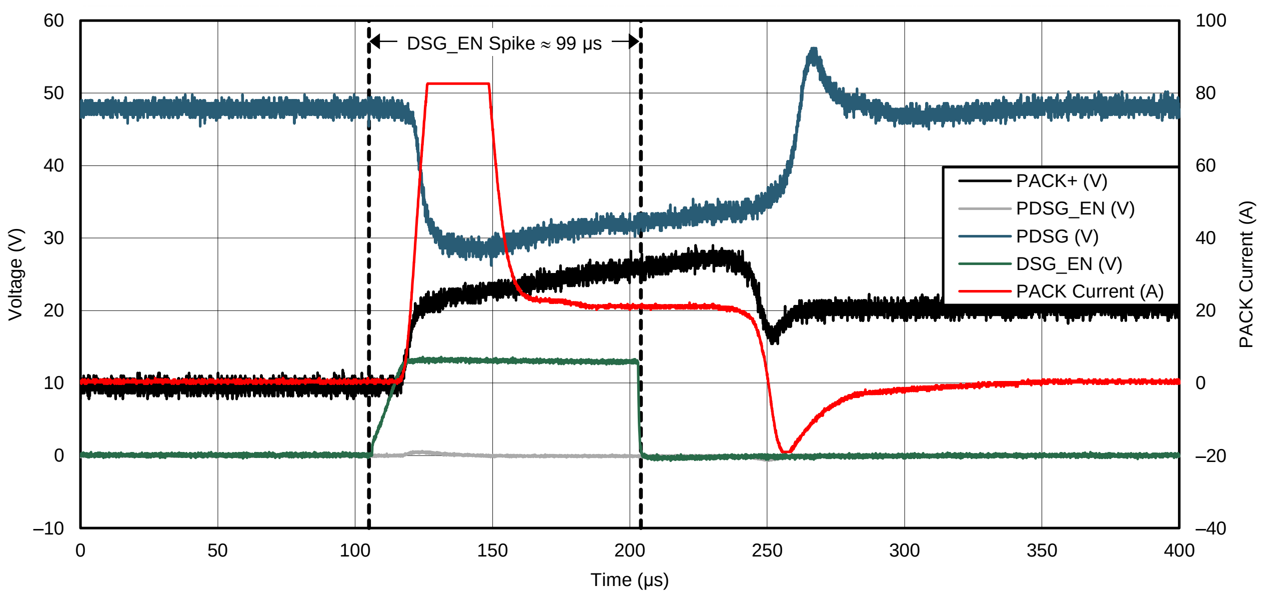
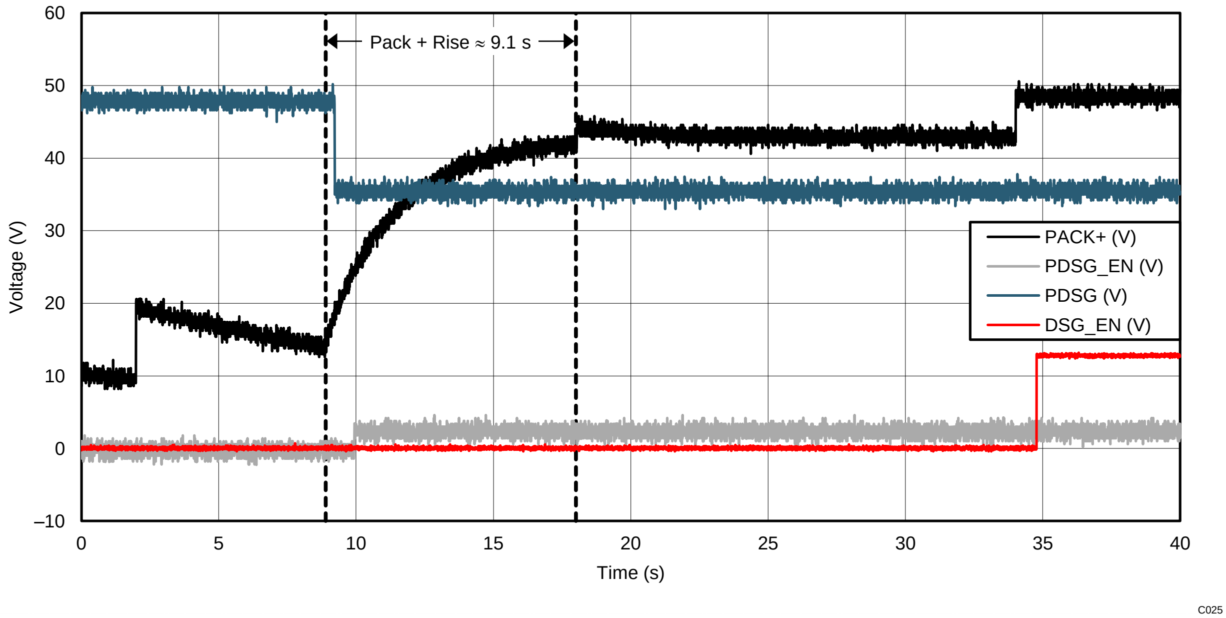


Figure 38. Capacitive Load DSG Spike and Current Spike (Zoomed-In View)



Problem resolved when PDSG _EN is turned on causing the PDSG FET to slowly ramp up PACK+ to turn on DSG

Figure 39. DSG Spike and Current Spike Problem Resolved

Using the pre-discharge feature, program the microcontroller to enable PDSG through the PCHG_EN pin. This is beneficial when using a high-capacitive load that essentially shorts DSG_EN and PACK which then attempt to recover in a cycle.

6 VDDCP Capacitance Reference Table

Due to the rising load capacitance as we increase the total number of FETs, the bq76200 requires an increase in the charge pump capacitor across the VDDCP and BATT terminals. If the capacitor is not increased as FETs are added, at some threshold the FETs will not comply and VDDCP will begin to cycle between slightly on and off states as there is not enough power to switch the FETs. Table 10 represents a reference for certain FET configurations and the recommended VDDCP capacitance size for each total FET amount.

Once more than approximately 4 total FETs are used, the charge pump capacitor must be increased from the base 470 nF capacitor at a ratio of roughly 23.5 charge pump capacitance (C_{VDDCP}) to total FET input capacitance (C_L). These tests were done with the TI CSD19536KCS FET which carries an input capacitance of about 9.25 nF. Subsequently, C_L was calculated by rounding the individual FET capacitance up to 10 nF to support applications with potentially higher FET capacitances. Note that as the charge pump capacitance increases, the longer the charge pump turn on time.

Table 10. VDDCP Capacitance Reference

Total # of DSG and CHG FETs	C_L (nF) (Total FET Capacitance)	C_{VDDCP} (nF) (Theoretical Minimum Charge Pump Capacitance)	C_{VDDCP} (nF) (Actual Used Capacitance)
2	20	470	470
4	40	940	1000
8	80	1880	2200
12	120	2820	2200
16	160	3760	4700
24	240	5640	4700

NOTE: The VDDCP capacitance fault may not occur in every application with more than approximately 4 FETs, for example, tests were successfully completed using the 470 nF with 4xFETs and using the 1000 nF with 8xFETs. Other capacitances used in the test did not meet the theoretical minimum. However, it may not work consistently, and therefore it is more reliable to follow the theoretical minimum value in Table 10 to guide your VDDCP capacitance selection. The recommended minimum VDDCP capacitor C_{CP} = 470 nF

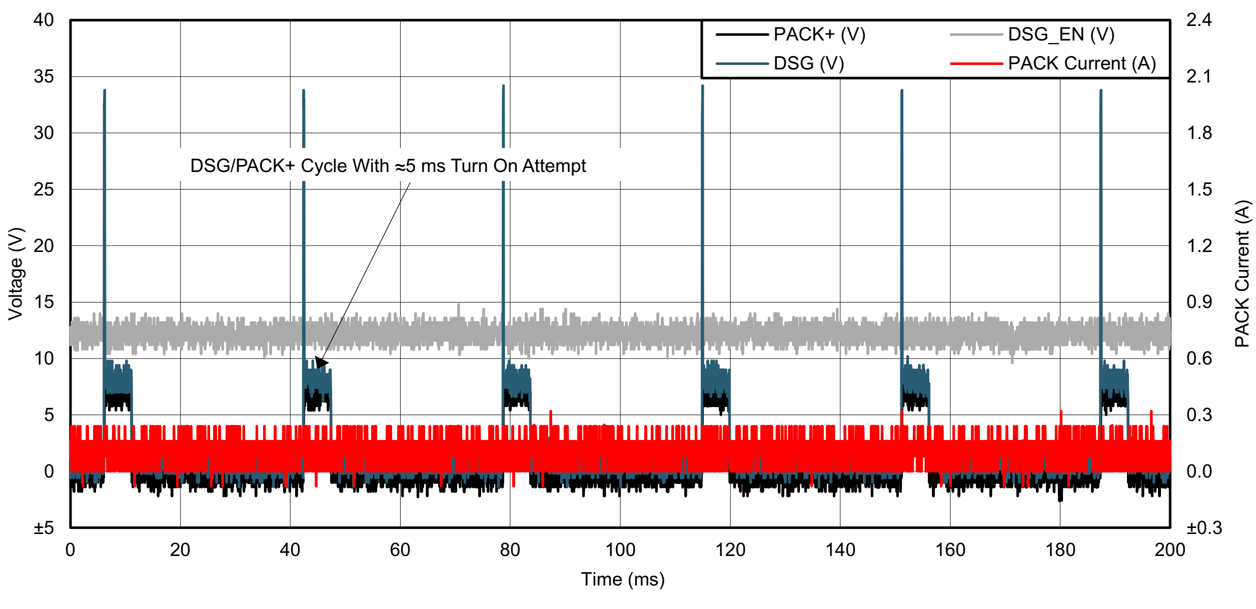


Figure 40. Example DSG Cycling With Inadequate VDDCP Capacitance

7 Data Conclusions

- Testing with the same number of CHG/DSG FETs using a parallel or series configuration produces similar results.
- In multiple FET configurations, it is important to include a ferrite bead/gate resistance at each FET gate.
- As FETs are increased, refer to Table 10 to determine an suitable capacitor.
- FET switching time is significantly delayed as FETs are increased, and less affected as the voltage increases.
- In higher power applications and minimal FET amounts, it may be useful to add Cgd capacitance to the FETs to provide feedback to the gate.
- The CHG FETs seem to recover slower than the DSG FETs.

8 References

1. *bq76200 High Voltage Battery Pack Front-End Charge/Discharge High-Side NFET Driver* (SLUSC16)
2. *bq76200 High Voltage Battery Pack Front-End Charge/Discharge High-Side NFET Driver Evaluation Module User's Guide* (SLVU926)

Revision History

Changes from Original (November 2015) to A Revision **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.